CD4066
Quad Bilateral Switches

Product Specification

Specification Revision History：

Version	Date	Description
2019-06-A1	2019-06	New
2021-07-A2	2021-07	Modify Ordering Information
2021-12-A3	2021-12	Modify Ordering Information

1、General Description

The CD4066 provides four single-pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

The CD4066 is pin compatible with the CD4016 but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.

Features:

- Wide supply voltage range from 3V to 9V
- Fully static operation
- 5V and 9V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40℃ to +85℃
- Packaging information: DIP14/SOP14/TSSOP14

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
CD4066DA14.TB	DIP14	CD4066	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
CD4066SA14.TB	SOP14	CD4066	50 PCS/tube	200 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
CD4066TA14.TB	TSSOP14	CD4066	94 PCS/tube	200 tube/box	18800 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
CD4066SA14.TR	SOP14	CD4066	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 8.7mm×3.9mm Pin spacing: 1.27mm
CD4066TA14.TR	TSSOP14	CD4066	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

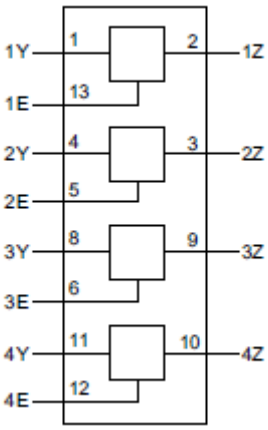


Figure 1. Functional diagram

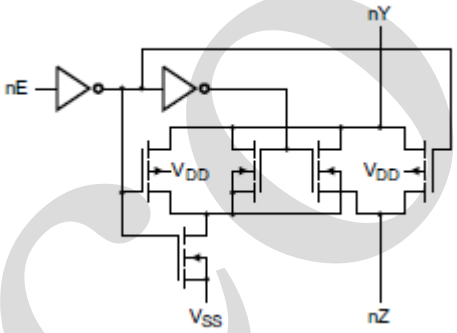
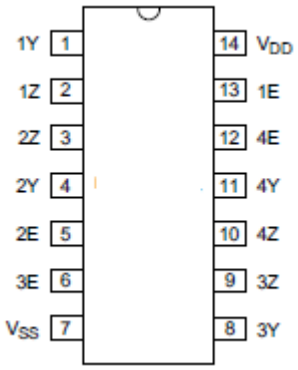


Figure 2. Logic diagram (one switch)

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	1Y	independent input or output
2	1Z	independent input or output
3	2Z	independent input or output
4	2Y	independent input or output
5	2E	enable input (active HIGH)
6	3E	enable input (active HIGH)
7	V_{SS}	ground (0V)
8	3Y	independent input or output
9	3Z	independent input or output
10	4Z	independent input or output
11	4Y	independent input or output
12	4E	enable input (active HIGH)
13	1E	enable input (active HIGH)
14	V_{DD}	supply voltage

2.4、Function Table

Input	Switch
nE	
H	ON
L	OFF

Note: H=HIGH voltage level; L=LOW voltage level.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0.5	+12	V
input voltage	V_I	-		-0.5	V_{DD}+0.5	V
input clamping current	I_{IK}	V_I<0.5V or V_I>V_{DD}+0.5V		-	±10	mA
input/output current	$I_{I/O}$	-		-	±10	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:

[1] For DIP14 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.

[2] For SOP14 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.

[3] For (T)SSOP14 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

(T_{amb}=25℃; R_L=10kΩ; C_L=50pF; nE=V_{DD}; Vis=V_{DD}=5V.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	5	9	V
ambient temperature	T_{amb}	in free air	-40	-	+85	℃
input voltage	V_I	-	0	-	V_{DD}	V
Disable output time （High level→turn off）	t_{PHZ}	nE to nZ or nE to nY	-	80	160	ns
Disable output time （Low level→turn off）	t_{PLZ}	nE to nZ or nE to nY	-	80	160	ns
Enable output time （turn off→high/low level）	t_{PZH}, t_{PZL}	-	-	45	90	ns
input capacitance	C_I	-	-	-	7.5	pF

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		T_{amb}=25℃			Unit
				Min.	Typ.	Max.	
supply current	I_{DD}	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	-	1.0	uA
			V_{DD}=9V	-	-	2.0	uA
HIGH-level input voltage	V_{IH}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	-	V
			V_{DD}=9V, V_O=0.5V or 8V	7.0	-	-	V
LOW-level input voltage	V_{IL}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	-	1.5	V
			V_{DD}=9V, V_O=0.5V or 8V	-	-	3.0	V
input leakage current	I_I	V_I=0V or 9V, V_{DD}=9V		-	-	0.3	uA
ON resistance (rail)	R_{ON}	V_I=0V to V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	350	2500	Ω
			V_{DD}-V_{EE}=9V	-	80	245	Ω
		V_I=0V	V_{DD}-V_{EE}=5V	-	115	340	Ω
			V_{DD}-V_{EE}=9V	-	50	160	Ω
		V_I=V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	120	365	Ω
			V_{DD}-V_{EE}=9V	-	65	200	Ω
ON resistance mismatch between channels	Δ R_{ON}	V_I=0V to V_{DD}-V_{EE}	V_{DD}-V_{EE}=5V	-	25	-	Ω
			V_{DD}-V_{EE}=9V	-	10	-	Ω

Note: On resistance waveform and test circuit see Figure 9 and Figure 10.

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)		T_{amb}=-40℃		T_{amb}=+85℃		Unit
				Min.	Max.	Min.	Max.	
supply current	I_{DD}	V_I=V_{DD} or V_{SS}, I_O=0A	V_{DD}=5V	-	1.0	-	7.5	uA
			V_{DD}=9V	-	2.0	-	15.0	uA
HIGH-level input voltage	V_{IH}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	3.5	-	3.5	-	V
			V_{DD}=9V, V_O=0.5V or 8V	7.0	-	7.0	-	V
LOW-level input voltage	V_{IL}	$\|I_O\|$<1uA	V_{DD}=5V, V_O=0.5V or 4.5V	-	1.5	-	1.5	V
			V_{DD}=9V, V_O=0.5V or 8V	-	3.0	-	3.0	V
input leakage current	I_I	V_I=0V or 9V, V_{DD}=9V		-	-	-	1.0	uA

3.3.3、AC Characteristics 1

(T_{amb}=25℃, V_{EE}=V_{SS}=0V, t_r, t_f≤20ns, C_L=50pF, R_L=10kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
HIGH to LOW propagation delay time	t_{PHL}	nY to nZ; nZ to nY; see Figure 4	V_{DD}=5V	-	10	20	ns
			V_{DD}=9V	-	5	10	ns
LOW to HIGH propagation delay	t_{PLH}	nY to nZ; nZ to nY; see Figure 4	V_{DD}=5V	-	10	20	ns
			V_{DD}=9V	-	5	10	ns
HIGH to OFF-state propagation delay	t_{PHZ}	nE to nY, nZ; see Figure 5	V_{DD}=5V	-	80	160	ns
			V_{DD}=9V	-	65	130	ns
LOW to OFF-state propagation delay	t_{PLZ}	nE to nY, nZ; see Figure 5	V_{DD}=5V	-	80	160	ns
			V_{DD}=9V	-	70	140	ns
OFF-state to HIGH propagation delay	t_{PZH}	nE to nY, nZ; see Figure 5	V_{DD}=5V	-	40	80	ns
			V_{DD}=9V	-	20	40	ns
OFF-state to LOW propagation delay	t_{PZL}	nE to nY, nZ; see Figure 5	V_{DD}=5V	-	45	90	ns
			V_{DD}=9V	-	20	40	ns

3.3.4、AC Characteristics 2

(T_{amb}=25℃, V_{EE}=V_{SS}=0V, V_I=0.5V_{DD} (p-p), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Square wave distortion	d_{sin}	see Figure 6; R_L=10kΩ; C_L=15pF; channel ON; f_i=1kHz	V_{DD}=5V	0.25	-	-	%
			V_{DD}=9V	0.04	-	-	%
any two channel crosstalk	f_{ct}	V_{DD}=9V, see note2		1	-	-	MHz
crosstalk voltage (nE to nY to nZ)	V_{ct}	see Figure 7; R_L=10kΩ; C_L=15pF; $\overline{E}$ or Sn=V_{DD} (square-wave)		50	-	-	mV
OFF frequency	f_{OFF}	V_{DD}=9V, see note3		1	-	-	MHz
conduction frequency	f_{ON}	V_{DD}=5V, see note4		-	-	-	MHz
		V_{DD}=9V, see note4		90	-	-	MHz

Note:

[1] f_i is biased at 0.5V_{DD}; V_I=0.5V_{DD} (p-p).

[2] R_L=1kΩ; 20logVos/Vis=-50dB, see Figure 8.

[3] R_L=1kΩ; C_L=5pF, channel off, 20logVos/Vis=-50dB, see Figure 6.

[4] R_L=1kΩ; C_L=5pF, channel on, 20logVos/Vis=-3dB, see Figure 6.

4、Testing Circuit

4.1、AC Testing Circuit 1

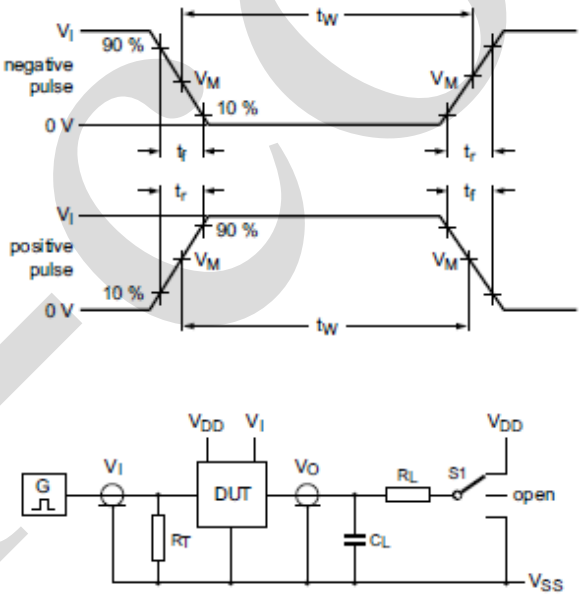


Figure 3. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L=Load resistance.

4.2、AC Testing Waveforms

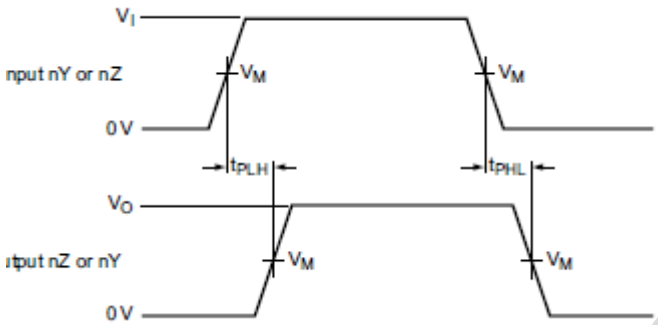


Figure 4. nY or nZ to nZ or nY propagation delays

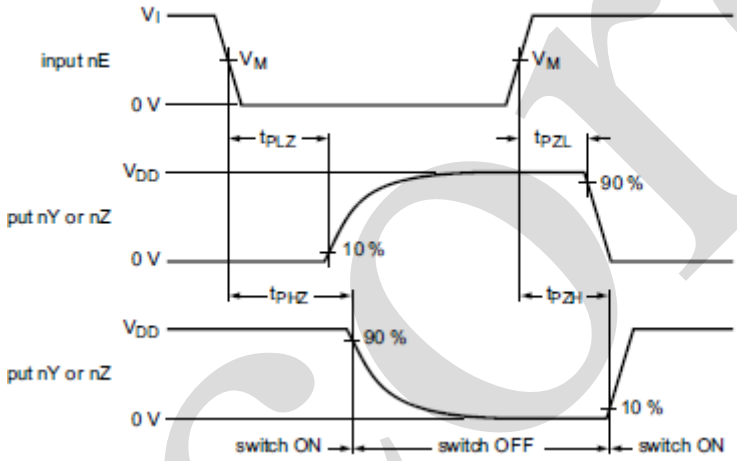


Figure 5. Enable and disable times

4.3、AC Testing Circuit 2

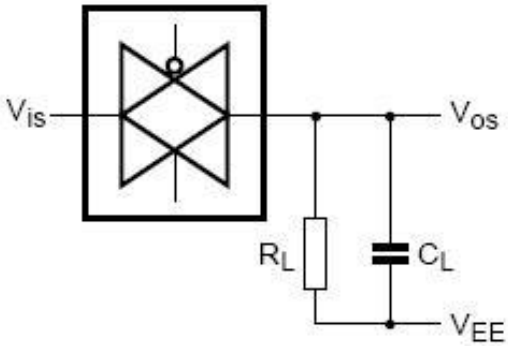


Figure 6. Square wave distortion degree of cut-off frequency and conduction frequency test pattern

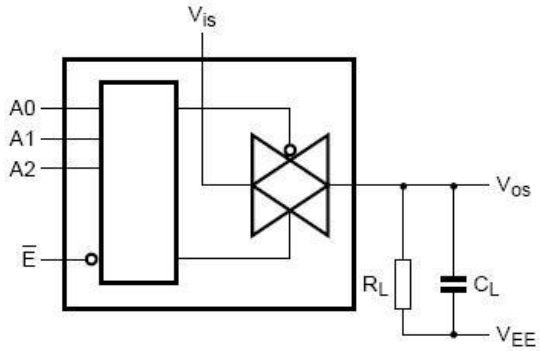


Figure 7. Crosstalk logical input/output test

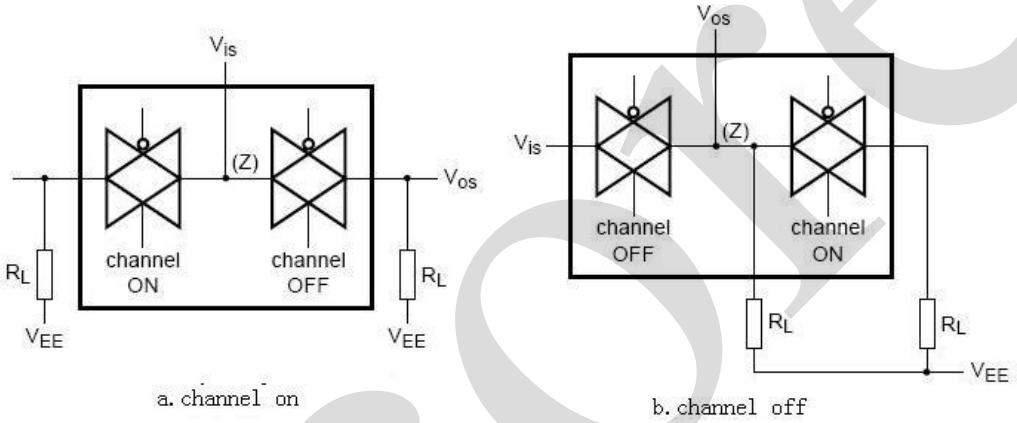
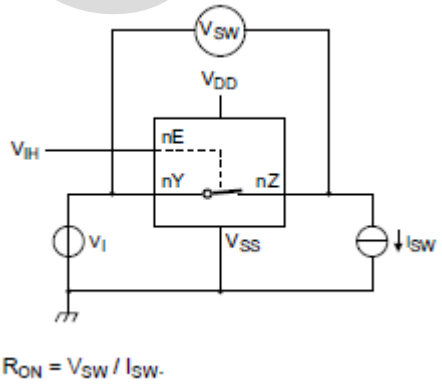


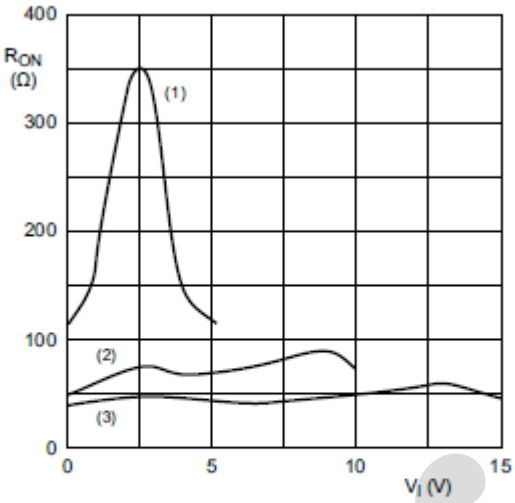
Figure 8. Inter channel Crosstalk

4.4、On Resistance Waveform And Test Circuit



$R_{ON} = V_{SW} / I_{SW}$.

Figure 9. Test circuit for measuring R_{ON}



I_{SW} = 200 µA.
(1) V_{DD} = 5 V
(2) V_{DD} = 10 V
(3) V_{DD} = 15 V

Figure 10. Typical R_{ON} as a function of input voltage

4.5、Measurement Points

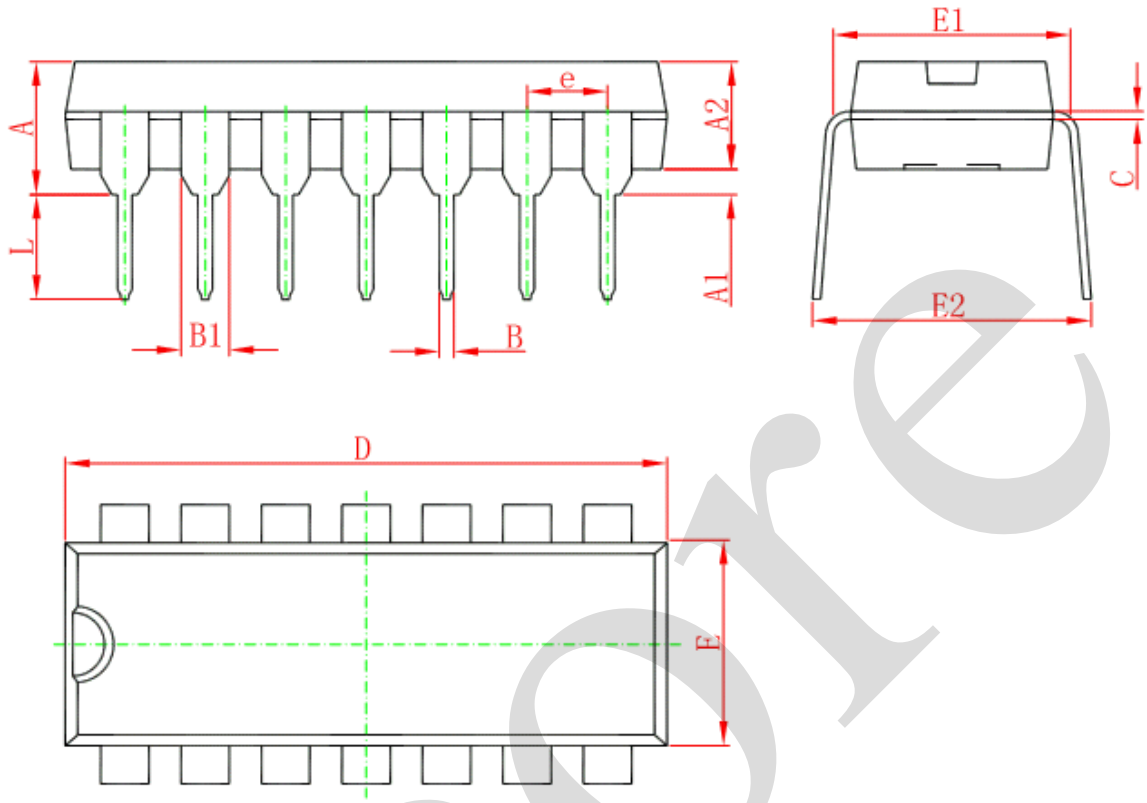
Supply voltage	Input	Output
V_{DD}	V_M	V_M
3V to 9V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

4.6、Test Data

Test	Input		Load		Switch
	V_{is}	t_r, t_f	C_L	R_L	
t_{PHL}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
t_{PLH}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZH}, t_{PHZ}	V_{DD}	20ns	50pF	10kΩ	V_{EE}
t_{PZL}, t_{PLZ}	V_{EE}	20ns	50pF	10kΩ	V_{DD}
others	pulse	20ns	50pF	10kΩ	open

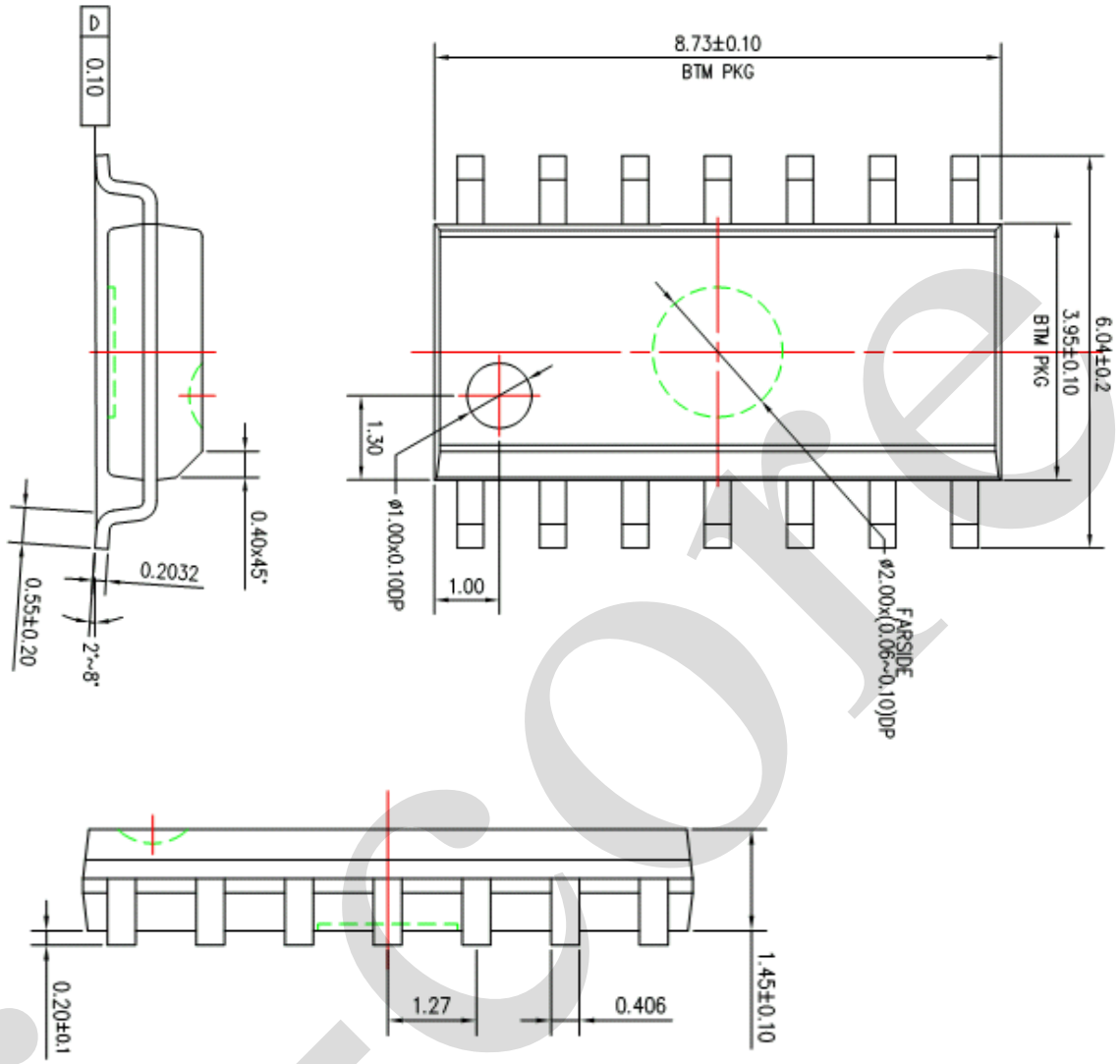
5、Package Information

5.1、DIP14

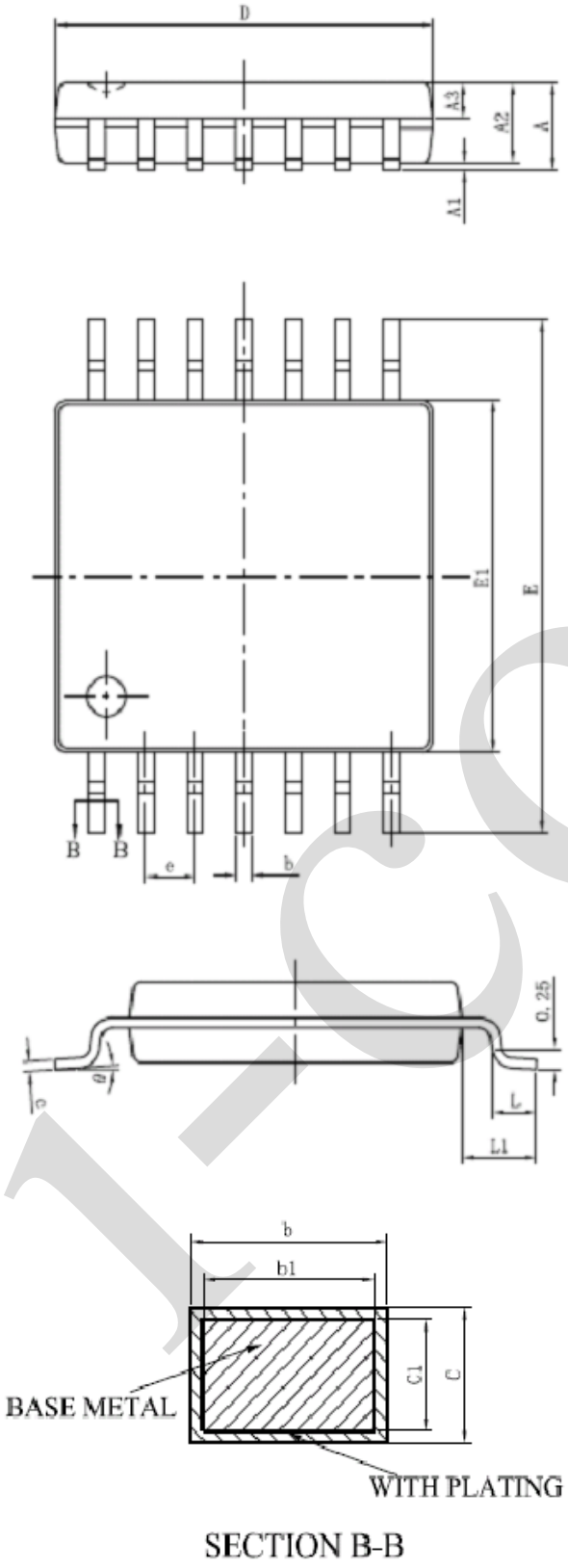


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

5.2、SOP14


0.10
8.73±0.10
BTM PKG
6.04±0.2
3.95±0.10
BTM PKG
1.30
Ø1.00x0.100P
1.00
Ø2.00x(0.06~0.10)DP
FARSIDE
0.40x45°
0.2032
0.55±0.20
2°~8°
0.20±0.1
1.27
0.406
1.45±0.10

5.3、TSSOP14



SECTION B-B

SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.20	0.30
b1	0.19	0.25
c	0.13	0.19
c1	0.12	0.14
D	4.86	5.06
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

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