AiP74HC/HCT573
Octal D-type transparent latch; 3-state

Product Specification

Specification Revision History：

Version	Date	Description
2012-06-A1	2012-06	New
2021-12-A2	2021-12	Modify ordering information
2022-01-A3	2022-01	Modify ambient temperature to -40℃~+105℃ and add electrical characteristics of -40℃~+105℃

1、General Description

The AiP74HC/HCT573 is an 8-bit D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable ($\overline{OE}$) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latches. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Features:

- Input levels:
  For AiP74HC573: CMOS level
  For AiP74HCT573: TTL level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Specified from -40℃ to +105℃
- Packaging information: DIP20/SOP20/TSSOP20

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
AiP74HC573DA20.TB	DIP20	74HC573	18 PCS/tube	40 tube/box	720 PCS/box	Dimensions of plastic enclosure: 26.3mm×6.4mm Pin spacing: 2.54mm
AiP74HCT573DA20.TB	DIP20	74HCT573	18 PCS/tube	40 tube/box	720 PCS/box	Dimensions of plastic enclosure: 26.3mm×6.4mm Pin spacing: 2.54mm
AiP74HC573SA20.TB	SOP20(1)	74HC573	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74HCT573SA20.TB	SOP20(1)	74HCT573	35 PCS/tube	80 tube/box	2800 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74HC573SA20.TB	SOP20(2)	74HC573	36 PCS/tube	80 tube/box	2880 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74HCT573SA20.TB	SOP20(2)	74HCT573	36 PCS/tube	80 tube/box	2880 PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing: 1.27mm
AiP74HC573TA20.TB	TSSOP20	74HC573	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm
AiP74HCT573TA20.TB	TSSOP20	74HCT573	70 PCS/tube	200 tube/box	14000 PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
AiP74HC573SA20.TR	SOP20	74HC573	1000PCS/reel	1000PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74HCT573SA20.TR	SOP20	74HCT573	1000PCS/reel	1000PCS/box	Dimensions of plastic enclosure: 12.8mm×7.5mm Pin spacing:1.27mm
AiP74HC573TA20.TR	TSSOP20	74HC573	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm
AiP74HCT573TA20.TR	TSSOP20	74HCT573	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 6.5mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

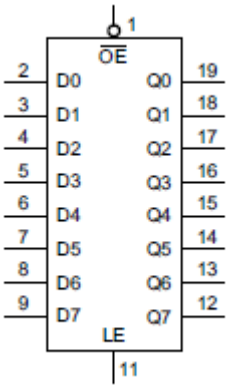


Figure 1. Logic symbol

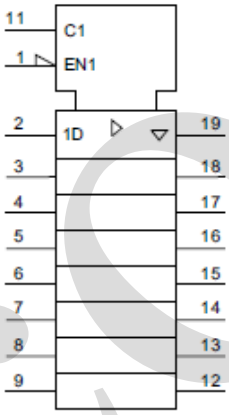


Figure 2. IEC logic symbol

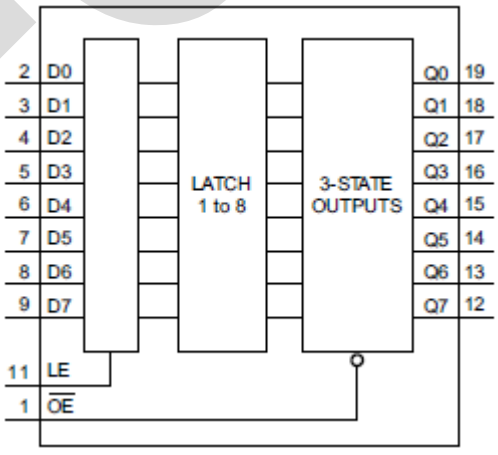


Figure 3. Functional diagram

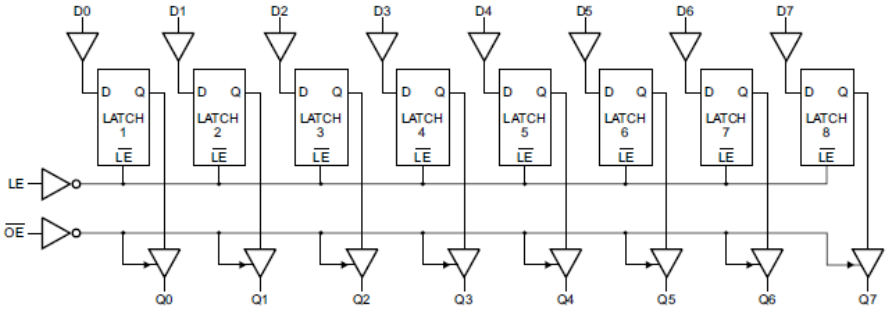
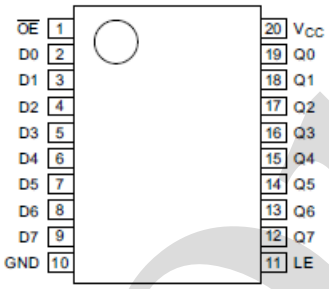


Figure 4. Logic diagram

2.2、Pin Configurations



2.3、Pin Description

Pin No.	Pin Name	Description
1	$\overline{OE}$	3-state output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input
9	D7	data input
10	GND	ground (0V)
11	LE	latch enable input (active HIGH)
12	Q7	3-state latch output
13	Q6	3-state latch output
14	Q5	3-state latch output
15	Q4	3-state latch output
16	Q3	3-state latch output
17	Q2	3-state latch output
18	Q1	3-state latch output
19	Q0	3-state latch output
20	V_{CC}	supply voltage

2.4、Function Table

Operating mode	Control		Input	Internal latches	Output
	$\overline{OE}$	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
			H	H	H
Latch and read register	L	L	l	L	L
			h	H	H
Latch register and disable outputs	H	L	l	L	Z
			h	H	Z

Note: H=HIGH voltage level; L=LOW voltage level; Z=high-impedance OFF-state;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition.

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Max.	Unit
supply voltage	V_{CC}	-		-0.5	+7.0	V
input clamping current	I_{IK}	V_I < -0.5V or V_I > V_{CC}+0.5V		-	±20	mA
output clamping current	I_{OK}	V_O < -0.5V or V_O > V_{CC}+0.5V		-	±20	mA
output current	I_O	V_O= -0.5V to (V_{CC}+0.5V)		-	±35	mA
supply current	I_{CC}	-		-	+70	mA
ground current	I_{GND}	-		-70	-	mA
storage temperature	T_{stg}	-		-65	+150	℃
total power dissipation	P_{tot}	-		-	500	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		℃

Note:
[1] For DIP20 packages: above 70℃ the value of P_{tot} derates linearly with 12mW/K.
[2] For SOP20 packages: above 70℃ the value of P_{tot} derates linearly with 8mW/K.
[3] For (T)SSOP20 packages: above 60℃ the value of P_{tot} derates linearly with 5.5mW/K.

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC573						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	℃
AiP74HCT573						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	Δt/ΔV	V_{CC}=4.5V	-	1.67	139	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	℃

3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC573							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	1.2	-	V
		V_{CC}=4.5V		3.15	2.4	-	V
		V_{CC}=6.0V		4.2	3.2	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	0.8	0.5	V
		V_{CC}=4.5V		-	2.1	1.35	V
		V_{CC}=6.0V		-	2.8	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	2.0	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	4.5	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	6.0	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.98	4.32	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	0	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	0	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	0	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	0.15	0.26	V
			I_O=7.8mA; V_{CC}=6.0V	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±0.1	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±0.5	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	8.0	uA

input capacitance	C_I	-	-	3.5	-	pF
AiP74HCT573						
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V	2.0	1.6	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V	-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=-20uA	4.4	4.5	-	V
		V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=-6.0mA	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=20uA	-	0	0.1	V
		V_I = V_{IH} or V_{IL}; V_{CC}=4.5V; I_O=6.0mA	-	0.16	0.26	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V	-	-	±0.1	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or $V_{IL;}$ V_{CC}=5.5V; V_O=V_{CC} or GND	-	-	±0.5	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V	-	-	8.0	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A; per input pin; Dn inputs	-	35	126	uA
		per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A; per input pin; LE input	-	65	234	uA
		per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A; per input pin; $\overline{OE}$ input	-	125	450	uA
input capacitance	C_I	-	-	3.5	-	pF

3.3.2、DC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
AiP74HC573						
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V	1.5	-	-	V
		V_{CC}=4.5V	3.15	-	-	V
		V_{CC}=6.0V	4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V	-	-	0.5	V
		V_{CC}=4.5V	-	-	1.35	V
		V_{CC}=6.0V	-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-6.0mA; V_{CC}=4.5V	3.84	-	-	V
		V_I = V_{IH} or V_{IL}; I_O=-7.8mA; V_{CC}=6.0V	5.34	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
		V_I = V_{IH} or V_{IL}; I_O=6.0mA; V_{CC}=4.5V	-	-	0.33	V
		V_I = V_{IH} or V_{IL}; I_O=7.8mA; V_{CC}=6.0V	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V	-	-	±1.0	uA
OFF-state	I_{OZ}	V_I=V_{IH} or $V_{IL;}$ V_{CC}=6.0V;	-	-	±5.0	uA

output current		V_O=V_{CC} or GND					
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	80	uA
AiP74HCT573							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-6.0mA	3.84	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=6.0mA	-	-	0.33	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or $V_{IL;}$ V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±5.0	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	80	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	per input pin; Dn inputs	-	-	158	uA
			per input pin; LE input	-	-	293	uA
			per input pin; $\overline{OE}$ input	-	-	563	uA

3.3.3、DC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC573							
HIGH-level input voltage	V_{IH}	V_{CC}=2.0V		1.5	-	-	V
		V_{CC}=4.5V		3.15	-	-	V
		V_{CC}=6.0V		4.2	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=2.0V		-	-	0.5	V
		V_{CC}=4.5V		-	-	1.35	V
		V_{CC}=6.0V		-	-	1.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}	I_O=-20uA; V_{CC}=2.0V	1.9	-	-	V
			I_O=-20uA; V_{CC}=4.5V	4.4	-	-	V
			I_O=-20uA; V_{CC}=6.0V	5.9	-	-	V
			I_O=-6.0mA; V_{CC}=4.5V	3.7	-	-	V
			I_O=-7.8mA; V_{CC}=6.0V	5.2	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}	I_O=20uA; V_{CC}=2.0V	-	-	0.1	V
			I_O=20uA; V_{CC}=4.5V	-	-	0.1	V
			I_O=20uA; V_{CC}=6.0V	-	-	0.1	V
			I_O=6.0mA; V_{CC}=4.5V	-	-	0.4	V
			I_O=7.8mA; V_{CC}=6.0V	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=6.0V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or $V_{IL;}$ V_{CC}=6.0V; V_O=V_{CC} or GND		-	-	±10	uA

supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=6.0V		-	-	160	uA
AiP74HCT573							
HIGH-level input voltage	V_{IH}	V_{CC}=4.5V to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	V_{CC}=4.5V to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=-20uA	4.4	-	-	V
			I_O=-6.0mA	3.7	-	-	V
LOW-level output voltage	V_{OL}	V_I = V_{IH} or V_{IL}; V_{CC}=4.5V	I_O=20uA	-	-	0.1	V
			I_O=6.0mA	-	-	0.4	V
input leakage current	I_I	V_I=V_{CC} or GND; V_{CC}=5.5V		-	-	±1.0	uA
OFF-state output current	I_{OZ}	V_I=V_{IH} or $V_{IL;}$ V_{CC}=5.5V; V_O=V_{CC} or GND		-	-	±10	uA
supply current	I_{CC}	V_I=V_{CC} or GND; I_O=0A; V_{CC}=5.5V		-	-	160	uA
additional supply current	ΔI_{CC}	per input pin; V_I=V_{CC}-2.1V; other inputs at V_{CC} or GND; V_{CC}=4.5V to 5.5V; I_O=0A	per input pin; Dn inputs	-	-	172	uA
			per input pin; LE input	-	-	319	uA
			per input pin; $\overline{OE}$ input	-	-	613	uA

3.3.4、AC Characteristics 1

(T_{amb}=25℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC573							
propagation delay	t_{pd}	Dn to Qn; see Figure 6	V_{CC}=2.0V	-	47	150	ns
			V_{CC}=4.5V	-	17	30	ns
			V_{CC}=5.0V; C_L=15pF	-	14	-	ns
			V_{CC}=6.0V	-	14	26	ns
		LE to Qn; see Figure 7	V_{CC}=2.0V	-	50	150	ns
			V_{CC}=4.5V	-	18	30	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
			V_{CC}=6.0V	-	14	26	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 8	V_{CC}=2.0V	-	44	140	ns
			V_{CC}=4.5V	-	16	28	ns
			V_{CC}=6.0V	-	13	24	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 8	V_{CC}=2.0V	-	55	150	ns
			V_{CC}=4.5V	-	20	30	ns
			V_{CC}=6.0V	-	16	26	ns
transition time	t_t	Qn; see Figure 6	V_{CC}=2.0V	-	14	60	ns
			V_{CC}=4.5V	-	5	12	ns
			V_{CC}=6.0V	-	4	10	ns
pulse width	t_W	LE HIGH; see Figure 7	V_{CC}=2.0V	80	14	-	ns
			V_{CC}=4.5V	16	5	-	ns
			V_{CC}=6.0V	14	4	-	ns
set-up time	t_{su}	Dn to LE;	V_{CC}=2.0V	50	11	-	ns

		see Figure 9	V_{CC}=4.5V	10	4	-	ns
			V_{CC}=6.0V	9	3	-	ns
hold time	t_h	Dn to LE; see Figure 9	V_{CC}=2.0V	5	3	-	ns
			V_{CC}=4.5V	5	1	-	ns
			V_{CC}=6.0V	5	1	-	ns
power dissipation capacitance	C_{PD}	C_L=50pF, f=1MHz; V_I=GND to V_{CC}		-	26	-	pF
AiP74HCT573							
propagation delay	t_{pd}	Dn to Qn; see Figure 6	V_{CC}=4.5V	-	20	35	ns
			V_{CC}=5.0V; C_L=15pF	-	17	-	ns
		LE to Qn; see Figure 7	V_{CC}=4.5V	-	18	35	ns
			V_{CC}=5.0V; C_L=15pF	-	15	-	ns
$\overline{OE}$ to Qn enable time	t_{en}	V_{CC}=4.5V; see Figure 8		-	17	30	ns
$\overline{OE}$ to Qn disable time	t_{dis}	V_{CC}=4.5V; see Figure 8		-	18	30	ns
transition time	t_t	Qn; V_{CC}=4.5V; see Figure 6		-	5	12	ns
pulse width	t_W	LE HIGH; V_{CC}=4.5V; see Figure 7		16	5	-	ns
Dn to LE set-up time	t_{su}	V_{CC}=4.5V; see Figure 9		13	7	-	ns
Dn to LE hold time	t_h	V_{CC}=4.5V; see Figure 9		9	4	-	ns
power dissipation capacitance	C_{PD}	C_L=50pF, f=1MHz; V_I=GND to V_{CC}-1.5V		-	26	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZL} and t_{PZH}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D=C_{PD}\times V_{CC}^2\times f_i\times N+\sum(C_L\times V_{CC}^2\times f_o)$ where:

f_i=input frequency in MHz;

f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

N=number of inputs switching;

$\sum(C_L\times V_{CC}^2\times f_o)$=sum of outputs.

3.3.5、AC Characteristics 2

(T_{amb}=-40℃ to +85℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC573							
propagation delay	t_{pd}	Dn to Qn; see Figure 6	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
		LE to Qn; see Figure 7	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 8	V_{CC}=2.0V	-	-	175	ns
			V_{CC}=4.5V	-	-	35	ns
			V_{CC}=6.0V	-	-	30	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 8	V_{CC}=2.0V	-	-	190	ns
			V_{CC}=4.5V	-	-	38	ns
			V_{CC}=6.0V	-	-	33	ns
transition time	t_t	Qn; see Figure 6	V_{CC}=2.0V	-	-	75	ns
			V_{CC}=4.5V	-	-	15	ns
			V_{CC}=6.0V	-	-	13	ns
pulse width	t_W	LE HIGH; see Figure 7	V_{CC}=2.0V	100	-	-	ns
			V_{CC}=4.5V	20	-	-	ns
			V_{CC}=6.0V	17	-	-	ns
set-up time	t_{su}	Dn to LE; see Figure 9	V_{CC}=2.0V	65	-	-	ns
			V_{CC}=4.5V	13	-	-	ns
			V_{CC}=6.0V	11	-	-	ns
hold time	t_h	Dn to LE; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
AiP74HCT573							
propagation delay	t_{pd}	Dn to Qn; see Figure 6	V_{CC}=4.5V	-	-	44	ns
		LE to Qn; see Figure 7	V_{CC}=4.5V	-	-	44	ns
$\overline{OE}$ to Qn enable time	t_{en}	V_{CC}=4.5V; see Figure 8		-	-	38	ns
$\overline{OE}$ to Qn disable time	t_{dis}	V_{CC}=4.5V; see Figure 8		-	-	38	ns
transition time	t_t	Qn; V_{CC}=4.5V; see Figure 6		-	-	15	ns
pulse width	t_W	LE HIGH; V_{CC}=4.5V; see Figure 7		20	-	-	ns
Dn to LE set-up time	t_{su}	V_{CC}=4.5V; see Figure 9		16	-	-	ns
Dn to LE hold time	t_h	V_{CC}=4.5V; see Figure 9		11	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZL} and t_{PZH}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

3.3.6、AC Characteristics 3

(T_{amb}=-40℃ to +105℃, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AiP74HC573							
propagation delay	t_{pd}	Dn to Qn; see Figure 6	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
		LE to Qn; see Figure 7	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
$\overline{OE}$ to Qn enable time	t_{en}	see Figure 8	V_{CC}=2.0V	-	-	210	ns
			V_{CC}=4.5V	-	-	42	ns
			V_{CC}=6.0V	-	-	36	ns
$\overline{OE}$ to Qn disable time	t_{dis}	see Figure 8	V_{CC}=2.0V	-	-	225	ns
			V_{CC}=4.5V	-	-	45	ns
			V_{CC}=6.0V	-	-	38	ns
transition time	t_t	Qn; see Figure 6	V_{CC}=2.0V	-	-	90	ns
			V_{CC}=4.5V	-	-	18	ns
			V_{CC}=6.0V	-	-	15	ns
pulse width	t_W	LE HIGH; see Figure 7	V_{CC}=2.0V	120	-	-	ns
			V_{CC}=4.5V	24	-	-	ns
			V_{CC}=6.0V	20	-	-	ns
set-up time	t_{su}	Dn to LE; see Figure 9	V_{CC}=2.0V	75	-	-	ns
			V_{CC}=4.5V	15	-	-	ns
			V_{CC}=6.0V	13	-	-	ns
hold time	t_h	Dn to LE; see Figure 9	V_{CC}=2.0V	5	-	-	ns
			V_{CC}=4.5V	5	-	-	ns
			V_{CC}=6.0V	5	-	-	ns
AiP74HCT573							
propagation delay	t_{pd}	Dn to Qn; see Figure 6	V_{CC}=4.5V	-	-	53	ns
		LE to Qn; see Figure 7	V_{CC}=4.5V	-	-	53	ns
$\overline{OE}$ to Qn enable time	t_{en}	V_{CC}=4.5V; see Figure 8		-	-	45	ns
$\overline{OE}$ to Qn disable time	t_{dis}	V_{CC}=4.5V; see Figure 8		-	-	45	ns
transition time	t_t	Qn; V_{CC}=4.5V; see Figure 6		-	-	18	ns
pulse width	t_W	LE HIGH; V_{CC}=4.5V; see Figure 7		24	-	-	ns
Dn to LE set-up time	t_{su}	V_{CC}=4.5V; see Figure 9		20	-	-	ns
Dn to LE hold time	t_h	V_{CC}=4.5V; see Figure 9		15	-	-	ns

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_{en} is the same as t_{PZL} and t_{PZH}.

[3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[4] t_t is the same as t_{THL} and t_{TLH}.

4、Testing Circuit

4.1、AC Testing Circuit

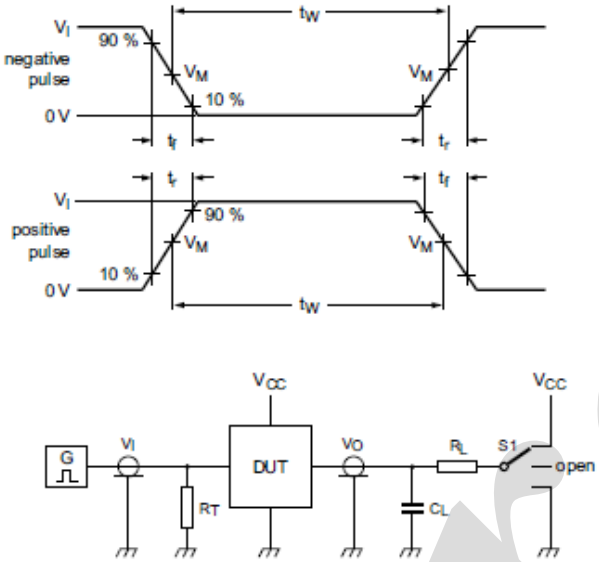


Figure 5. Test circuit for measuring switching times

Definitions for test circuit:

R_L=Load resistance.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1=Test selection switch.

4.2、AC Testing Waveforms

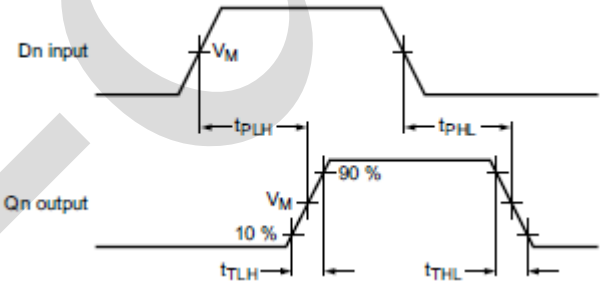


Figure 6. Propagation delay data input (Dn) to output (Qn) and output transition time

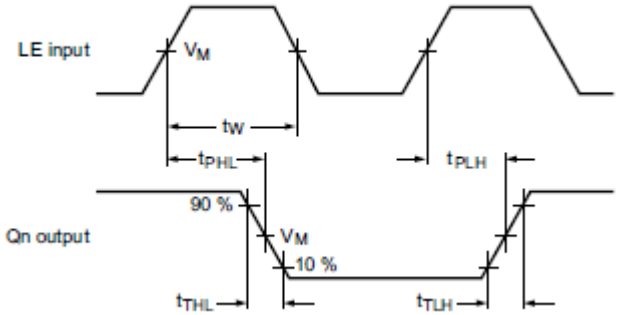


Figure 7. Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and output transition time

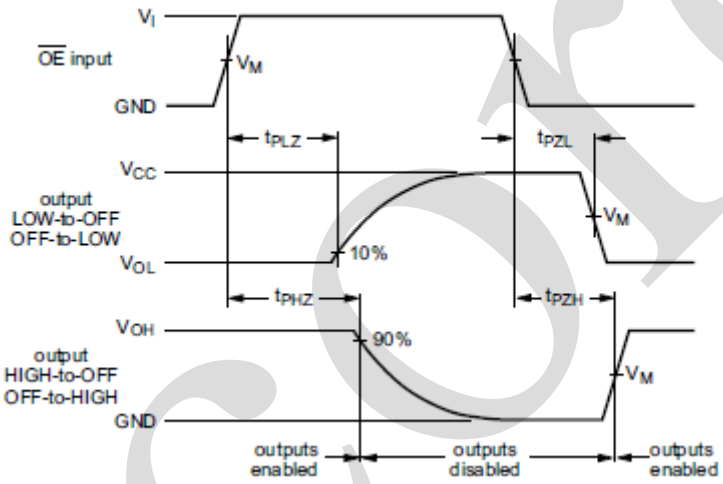


Figure 8. Enable and disable times

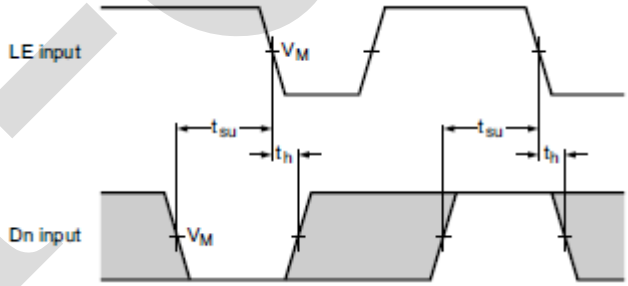


Figure 9. Set-up and hold times for data input (Dn) to latch input (LE)

4.3、Measurement Points

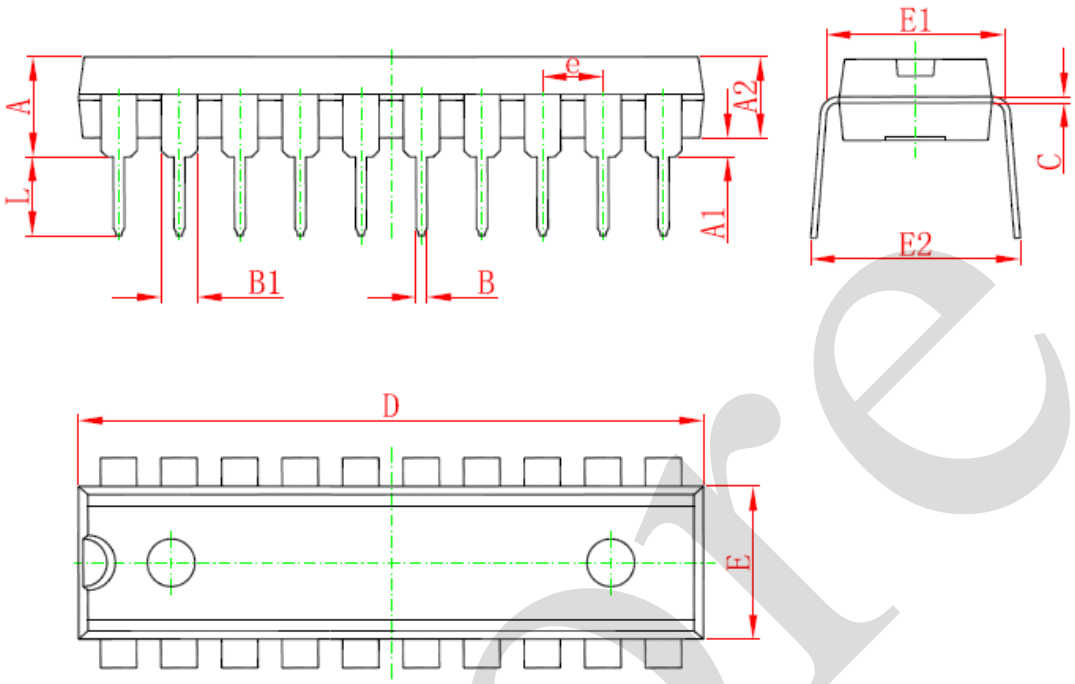
Type	Input	Output
	V_M	V_M
AiP74HC573	$0.5\times V_{CC}$	$0.5\times V_{CC}$
AiP74HCT573	1.3V	1.3V

4.4、Test Data

Type	Input		Load		S1 position		
	V_I	t_r , t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
AiP74HC573	V_{CC}	6ns	15pF, 50pF	1kΩ	open	GND	V_{CC}
AiP74HCT573	3V	6ns	15pF, 50pF	1kΩ	open	GND	V_{CC}

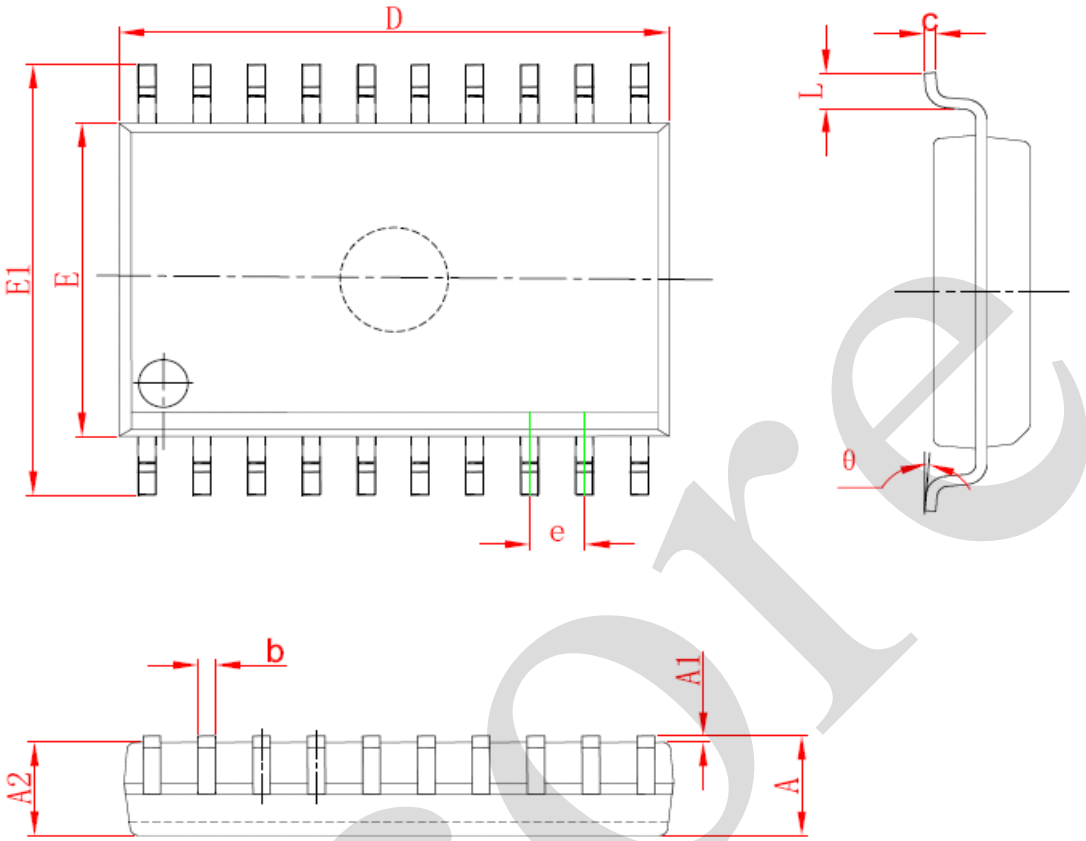
5、Package Information

5.1、DIP20



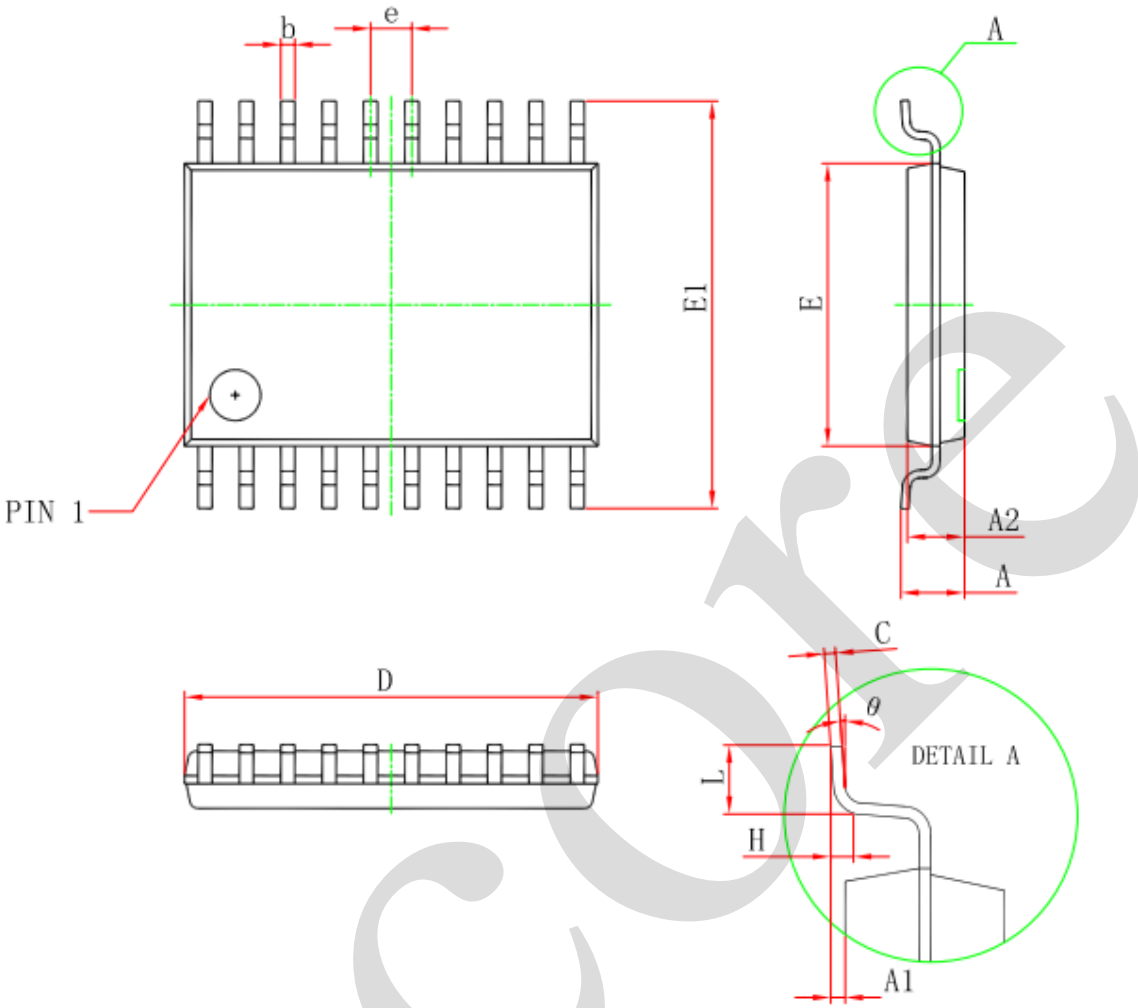
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	25.950	26.550	1.022	1.045
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

5.2、SOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

5.3、TSSOP20



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.