XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32A4A0 Series

32-bit ARM® Cortex® -M4 Microcontroller

Datasheet

Rev1.0 November 2022

Features

ARM Cortex-M4 32bit MCU+FPU, 300DMIPS, 2MB Flash, 516KB SRAM, 2USBs (HS/FS OTG), Ethernet MAC, 2CANs (FD/2.0B), 2SDIOs, DVP, EXMC, 32 Timers, 16HRPWMs, 3ADCs, 4DACs , 4PGAs, 4 CMPs, 10UARTs, 6SPIs, 6I2Cs, 4I2Ss, QSPI, AES, HASH (SHA256/HMAC), FMAC (FIR), MAU

- ARMv7-M architecture 32bit Cortex-M4 CPU, integrated FPU, MPU, DSP supporting SIMD instructions, full instruction tracking unit ETM, and CoreSight standard debug unit. The highest working frequency is 240MHz, reaching the computing performance of 300DMIPS or 825Coremarks
- Built-in memory
  - Maximum 2048KByte dual bank Flash memory
  - Maximum 516KByte SRAM, including 128KByte single-cycle access high-speed RAM
- Power, Clock, Reset Management
  - System Power (Vcc): 1.8-3.6V
  - 6 independent clock sources: External main clock crystal oscillator (4-25MHz), external sub-crystal oscillator (32.768kHz), internal high-speed RC (16/20MHz), internal medium-speed RC (8MHz), internal low-speed RC (32kHz), internal WDT dedicated RC (10kHz)
  - 15 reset sources including power-on reset (POR), low voltage detection reset (PVD1R/PVD2R), port reset (NRST), each reset source has an independent flag bit
- Low power operation
  - Peripherals can be turned off or on independently
  - Three low power modes: Sleep, Stop, Power down mode
  - VBAT independent power supply supports ultra-low power RTC, 128Byte backup register, 4KByte backup SRAM
- Peripheral operation support system significantly reduces CPU processing load
  - 16-channel dual-host DMAC
  - DMAC for USBHS, USBFS, Ethernet MAC
  - 8 Data Computation Units (DCUs)
  - Math co-processing unit (MAU), supports Sin/Sqrt
  - Support 16th order FIR digital filter (FMAC)
  - Support peripheral event mutual trigger (AOS)
- High performance simulation
  - 3 independent 12bit 2.5MSPS ADCs
  - 3 simultaneous sample and hold circuits to achieve simultaneous sampling of 3 channels
  - 4 independent 12bit 15MSPS DACs
  - 4 Programmable Gain Amplifiers (PGA)
  - 4 independent voltage comparators (CMP)
  - 1 On-Chip Temperature Sensor (OTS)
- Timer
  - 8 multi-function 32/16bit PWM Timer (Timer6)
  - 16 50ps high resolution PWM (HRPWM)
  - 3 16-bit motor PWM Timers (Timer4)
  - 12 16bit general-purpose Timer (TimerA)
  - 4 16bit general-purpose Timer (Timer2)
  - 2 16bit basic Timer (Timer0)
  - Real Time Clock Timer (RTC)
  - 2 WDTs, support internal dedicated clock
- Up to 142 GPIOs
  - Up to 134 5V-tolerant IOs
- Maximum 32 communication interfaces
  - 10 USARTs, of which 8 support ISO7816-3 protocol, 2 support LIN bus
  - 6 SPIs
  - 6 I2C, support SMBus protocol
  - 4 I2S, built-in audio PLL
  - 2 SDIO, support SD/MMC/eMMC format
  - 1 QSPI, support 240Mbps high-speed access (XIP)
  - 2 CAN, support CAN2.0B, up to CAN FD
  - 2 USB 2.0, respectively support HS, FS, built-in FS-PHY, support Device/Host
  - 1 10/100M Ethernet MAC, support dedicated DMA, IEEE 1588-2018 PTP, MII/RMII interface
- External Memory Controller EXMC
  - Support for static memory controller
  - Support dynamic memory controller
- Data encryption function
  - AES/HASH (SHA256/HMAC)/TRNG
- Working conditions: -40-105℃
  - AEC-Q100 Grade 2
- Encapsulation form:
  LQFP176 (24×24mm) LQFP100 (14×14mm)

Support Model:

HC32A4A0PITI-LQFP100	HC32A4A0SITI-LQFP176

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1 Overview

The HC32A4A0 series is a high-performance MCU based on ARM® Cortex®-M4 32-bit RISC CPU with a maximum operating frequency of 240MHz. The Cortex-M4 core integrates a floating-point arithmetic unit (FPU) and a DSP to implement single-precision floating-point arithmetic operations, supports all ARM single-precision data processing instructions and data types, and supports the complete DSP instruction set. The kernel integrates the MPU unit and superimposes the DMAC dedicated MPU unit at the same time to ensure the safety of system operation.

The HC32A4A0 series integrates high-speed on-chip memory, including a maximum of 2MB of Flash and a maximum of 512KB of SRAM. Integrated Flash access acceleration unit to achieve single cycle program execution of the CPU on Flash. The polled bus matrix supports multiple bus hosts to access memory and peripherals simultaneously, improving performance. The bus host includes CPU, DMA, USB dedicated DMA, ETHMAC dedicated DMA. In addition to the bus matrix, data transfer between peripherals is supported, and basic arithmetic operations and events are triggered each other, which can significantly reduce the transaction processing load of the CPU.

The HC32A4A0 series integrates rich peripheral functions. Including 3 independent 12bit 2.5MSPS ADC, 4 gain adjustable PGA, 4 12-bit 15MSPS DAC, 4 high-speed voltage comparator (CMP), 8 multi-function PWM Timer (Timer6) ,support 16 complementary PWM Output, 16 high-precision PWM (HRPWM) extend the resolution of Timer6 PWM signal, 3 motor PWM Timer (Timer4) support 18 complementary PWM outputs, 12 16bit general Timer (TimerA) support 6 3-phase quadrature Code input and 48 independent PWM outputs for Duty, 22 serial communication interfaces (I2C/UART/SPI), 1 QSPI interface, 2 CAN, 4 I2S support audio PLL, 2 SDIO, 1 ETHMAC, USBFS Controller and USBHS Controller with built-in USBFS PHY, 1 external expansion bus controller, including NFC controller, SMC controller and DMC controller, 1 digital video interface DVP, 1 math operation unit (MAU) and 4 filtering Mathematics Accelerator (FMAC).

HC32A4A0 series supports wide voltage range (1.8-3.6V), wide temperature range (-40-105℃) and various low power consumption modes. Supports fast wake-up in low power consumption mode, the fastest wake-up to STOP mode is 2us, and the fastest wake-up to Power-down mode is 25us.

Typical application

The HC32A4A0 series provides 100pin and 176pin LQFP packages, which are suitable for automotive electronics, such as T-Box, BMS controller, gateway, car light control and other applications.

1.1 Part naming rules

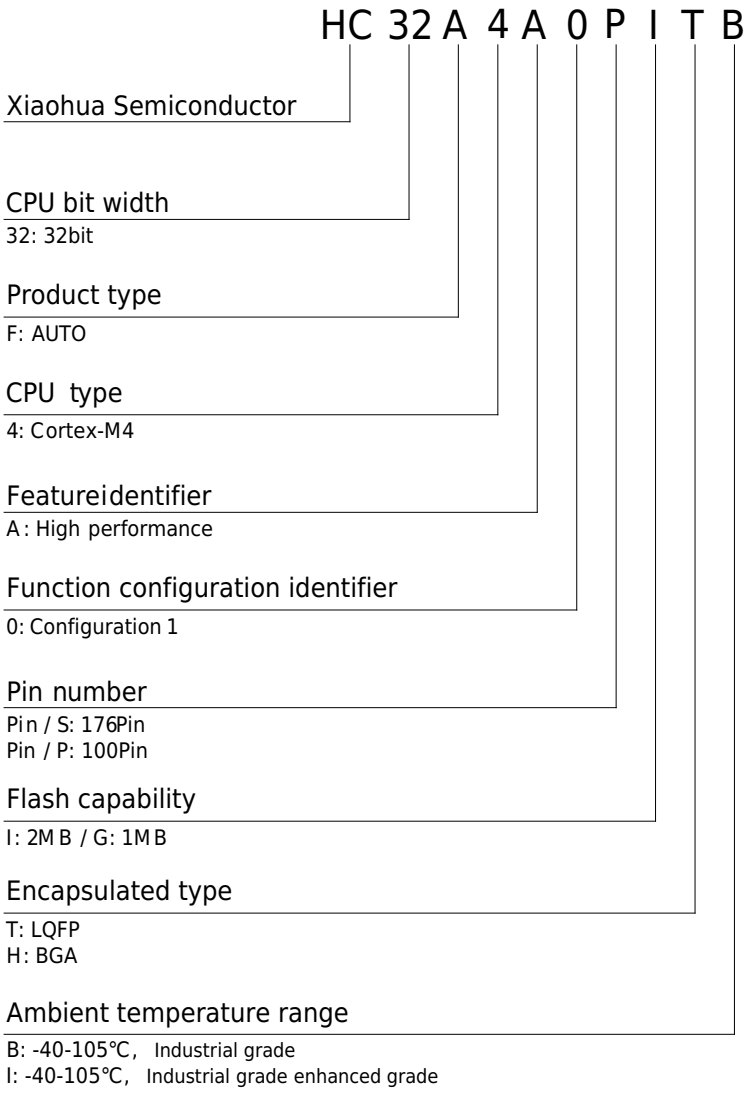


Figure 1-1 Model naming convention

1.2 Part function comparison table

Table 1-1 Model function comparison table

Function		Product	
		HC32A4A0SITI-LQFP176	HC32A4A0PITI-LQFP100
Pin number		176	100
Number of GPIOs		142	83
5V Tolerant GPIO number		138	79
Pin Pitch		LQFP	
Temperature range		-40 ~ 105℃	
Supply voltage range		1.8 ~ 3.6V	
Memory	Flash	2MB	
	OTP	134KByte	
	SRAM	512 + 4KB	
DMA		2unit * 8ch	
External port interrupt		EIRQ*16vec	
Communication Interfaces (In parentheses is the minimum number of IO required for each ch)	UART	10ch (1)	
	SPI	6ch (3)	
	I2C	6ch (2)	
	I2S	4ch (3)	
	CAN2.0B	2ch (2)	
	CAN FD (CAN_2)	1ch (2)	
	QSPI	1ch (3)	
	SDIO	2ch (3)	
	ETHMAC	1ch (10)	
	USBHS	1ch (2)	
	USB-FS	1ch (2)	
Timers	Timer0	2unit	
	Timer2	4unit	
	TimerA	12unit	
	Timer4	3unit	
	Timer6	8unit	
	HRPWM	16unit	
	WDT	1ch	
	SWDT	1ch	
	RTC	1ch	
Analog	12bit ADC	3unit, 28ch	3unit, 16ch
	SH	3 ch	
	12bitDAC	4ch	

Function		Product	
		HC32A4A0SITI-LQFP176	HC32A4A0PITI-LQFP100
	PGA	4ch	
	CMP	4ch	
	OTS	√	
DVP		√	
DCU		√	
FMAC		√	
MAU		√	
AES256		√	
HASH (SHA256)		√	
TRNG		√	
EXMC		√	
Frequency Monitoring Module (FCM)		√	
Programmable Voltage Detection Function (PVD)		√	
Debug interface		SWD	
		JTAG	

1.3 Functional block diagram

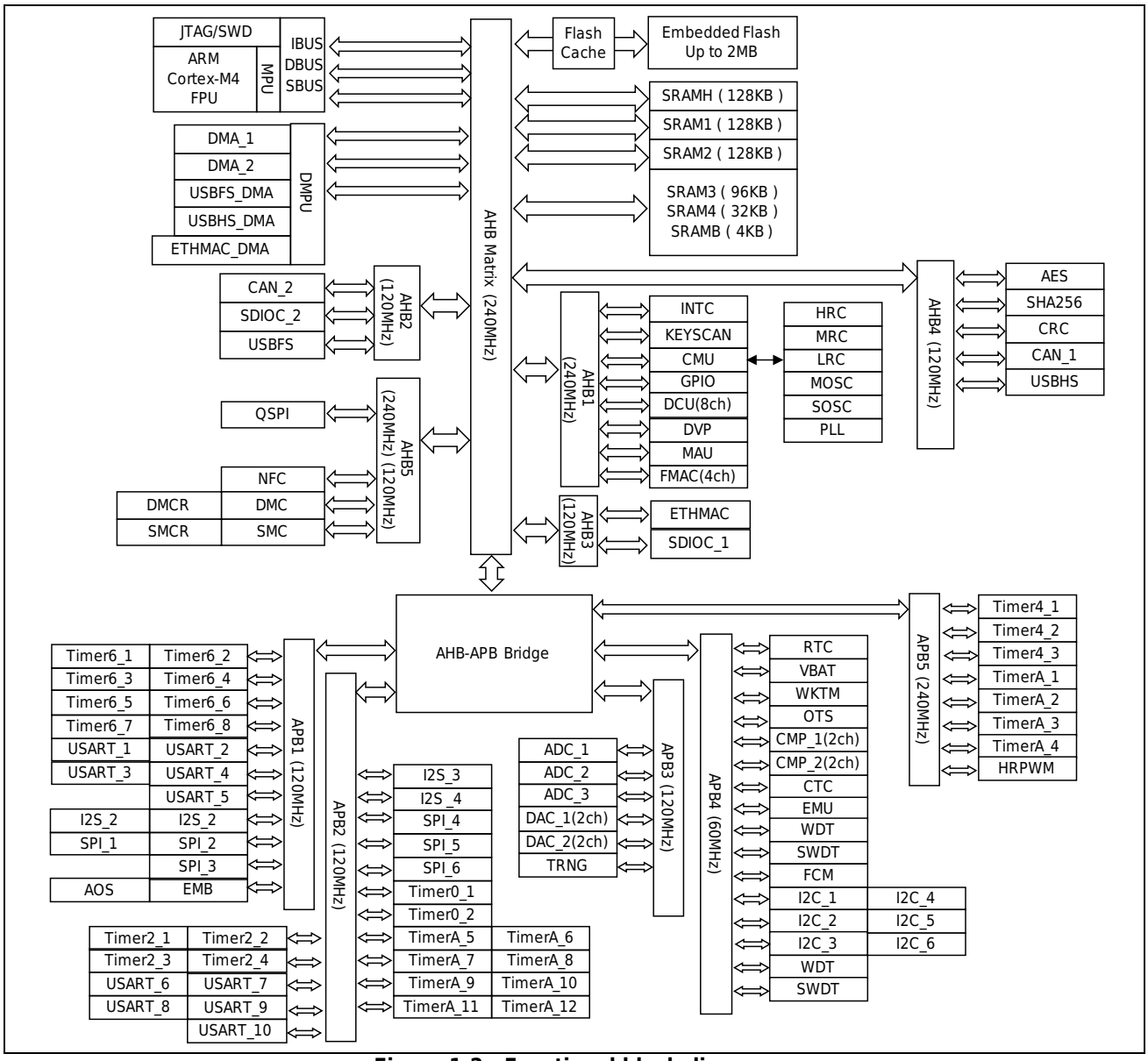


Figure 1-2 Functional block diagram

1.4 Feature Brief

1.4.1 CPU

The HC32A4A0 series integrates the latest generation of embedded ARM® Cortex®-M4 with FPU 32bit reduced instruction CPU, which achieves less pins and low power consumption, while providing excellent computing performance and rapid interrupt response capabilities. The on-chip integrated memory capacity can give full play to the excellent instruction efficiency of the ARM® Cortex®-M4 with FPU. The CPU supports DSP instructions, which can realize efficient signal processing operations and complex algorithms. The single-point precision FPU (Floating Point Unit) unit can avoid instruction saturation and speed up software development.

1.4.2 Bus Architecture (BUS)

The main system is composed of 32-bit multilayer AHB bus matrix, which can interconnect the following host bus and slave bus.

- Host bus
  - Cortex-M4F core CPU-I bus, CPU-D bus, CPU-S bus
  - System DMA_1 bus, system DMA_2 bus
  - USBFS_DMA bus
  - USBHS_DMA bus
  - ETHMAC_DMA bus
- Slave bus
  - Flash ICODE bus
  - Flash DCODE bus
  - Flash MCODE bus (bus for other hosts other than CPU to access Flash)
  - High-speed SRAMH (SRAMH 128kB) bus
  - System SRAMA (SRAM1 128KB) bus
  - System SRAMB (SRAM2 128KB) bus
  - System SRAMC (SRAM3 96KB, SRAM4 32KB, SRAMB 4KB)
  - APB1 peripheral bus (EMB/Timers/SPI/USART/I2S/HRPWM/EFM)
  - APB2 peripheral bus (Timers/SPI/USART/I2S)
  - APB3 peripheral bus (ADC/DAC/TRNG)
  - APB4 peripheral bus (FCM/WDT/SWDT/CMP/EMU/CTC/OTS/RTC/VBAT/WKTM/I2C)
  - APB5 peripheral bus (Timers/HRPWM)
  - AHB1 peripheral bus (DMPU/KEYSCAN/INTC/DCU/GPIO/DMA/CMU/DVP/MAU/FMAC)
  - AHB2 peripheral bus (CAN/SDIOC/USBFS)
  - AHB3 peripheral bus (SDIOC /ETHMAC)
  - AHB4 peripheral bus (AES/HASH/CRC/CAN/USBHS)
  - AHB5 peripheral bus (SMC/DMC/SMCR/DMCR/NFC/QSPI)

With the help of the bus matrix, high-efficiency concurrent access from the host bus to the slave bus can be realized.

1.4.3 Reset control (RMU)

The chip is configured with 15 reset modes.

- Power-on Reset (POR)
- NRST pin reset (NRST)
- Brown-out Reset (BOR)
- Programmable Voltage Detect 1 Reset (PVD1R)
- Programmable Voltage Detect 2 Reset (PVD2R)
- Watchdog Reset (WDTR)
- Special watchdog reset (SWDTR)
- Power-Down Wake-Up Reset (PDRST)
- Software Reset (SRST)
- MPU Error Reset (MPUR)
- RAM Parity Reset (RAMPR)
- RAMECC reset (RAMECCR)
- Clock Abnormal Reset (CKFER)
- External High Speed Oscillator Abnormal Shock Reset (XTALER)
- Cortex-M4 LOCKUP Reset (LKUPR)

1.4.4 Clock control (CMU)

The clock control unit provides clock functions for a range of frequencies, including: One external high-speed oscillator, one external low-speed oscillator, two PLL clock , one internal high-speed oscillator, a Internal medium speed oscillator , one internal low-speed oscillator, an internal low-speed oscillator for RTC, an SWDT dedicated internal low-speed oscillator , Clock prescaler, clock multiplexing and clock gating circuit.

The clock control unit also provides a clock frequency measurement function. The clock frequency measurement circuit (FCM) monitors and measures the measurement target clock using the measurement reference clock. An interrupt or reset occurs when the setting range is exceeded.

The AHB, APB and Cortex-M4 clocks are all derived from the system clock, and the source of the system clock can be selected from 6 clock sources:

1. External high-speed oscillator (XTAL)
2. External low speed oscillator (XTAL32)
3. PLLH clock (PLLH)
4. Internal high-speed oscillator (HRC)
5. Internal Medium Speed Oscillator (MRC)

6. Internal low-speed oscillator (LRC)

The maximum operating clock frequency of the system clock can reach 240MHz. SWDT has independent clock source: SWDT dedicated internal low-speed oscillator （SWDTLRC）. The real-time clock (RTC) uses the external low-speed oscillator or the internal low-speed oscillator as the clock source. The 48MHz clock of USB-FS can choose system clock, PLLH, PLLA as the clock source.

For each timer, you can turn it on and off separately when not in use to reduce power consumption.

1.4.5 Power control (PWC)

Power controller is used to control the supply, switching and detection of multiple power domains in multiple operation modes and low power modes. The power controller is composed of a power consumption control logic (PWC), a power supply voltage detection unit (PVD), and a battery backup control module (BATBKUP) that automatically switches between VCC and battery power.

The chip's operating voltage (VCC) is 1.8V to 3.6V. The voltage regulator (LDO) powers the VDD domain and the VDDR domain, and the VDDR voltage regulator (RLDO) powers the VDDR domain in power-down mode or VCC power-down conditions. The chip provides two operating modes such as high-speed and ultra-low speed through the power control logic (PWC), and three low-power modes such as sleep, stop and power-down.

Power supply voltage detection unit (PVD) provides power-on reset (POR), power-down reset (PDR), brown-out reset (BOR), programmable voltage detection 1 (PVD1), programmable voltage detection 2 (PVD2), reference voltage Measurement path, VBAT voltage detection, VBAT voltage measurement and other functions, among which POR, PDR, BOR control the reset action of the chip by detecting the VCC voltage. PVD1 resets or interrupts the chip according to the register setting by detecting the VCC voltage. PVD2 generates reset or interrupt according to register selection by detecting VCC voltage or external input detection voltage. The reference voltage measurement path is the function of using the ADC to measure the reference voltage. VBAT voltage detection is the function of reading the register to get the VBAT voltage higher or lower than the VBAT detection voltage. The VBAT detection voltage can be selected by register to 1.8V or 2.0V. The VBAT voltage measurement function refers to the function of using the ADC to measure the 1/2 voltage of VBAT to obtain the VBAT voltage.

The battery backup domain maintains the power supply through VBAT under the condition of VCC power failure, which ensures that the real-time clock module (RTC) and the wake-up timer (WKTM) can continue to operate, and provide power for the RLDO. The VDDR area can maintain the power supply through RLDO when the chip enters the power-down mode or the VCC is powered down, and maintains the data of the 4KB backup SRAM (Backup-SRAM). The analog modules are equipped with dedicated power supply pins for improved analog performance.

1.4.6 Initialization Configuration (ICG)

After the chip reset is released, the hardware circuit will read the FLASH address 0x0000_0400~0x0000_045F and load the data into the initialization configuration register. Addresses 0x0000_0408~0x0000_040B, 0x0000_0410~0x0000_041F, 0x0000_0438~0x0000_045F are reserved functional areas, please write all 1s to ensure the normal operation of the chip. When the FLASH boot exchange is invalid, there is FLASH block 0 sector 0 in this area; when the FLASH boot exchange is valid, there is FLASH block 1 sector 0 in this area. The user can modify the Initial ConfiG register by programming or erasing sector 0. The address 0x0000_0420~0x0000_0437 is the data security protection enable area. The register reset value is determined by the FLASH address data.

1.4.7 Embedded FLASH Interface (EFM)

The FLASH interface accesses FLASH through ICODE, DCODE and MCODE buses, and can perform programming, erasing and full erasing operations on FLASH; code execution is accelerated through instruction prefetching and caching mechanisms.

Main features:

- Two independent FLASH constitute dual bank, which can realize BGO (backgroud operation) function
- 134Kbytes of OTP space
- ICODE bus 16Bytes prefetch
- Two independent buffers: ICODE bus buffer space 4Kbytes (256x128); DCODE bus buffer space 1Kbytes (64x128)
- Supports boot swap function
- Support data security protection

1.4.8 Built-in SRAM (SRAM)

This product has 4KB power-down mode retention SRAM (SRAMB) and 512KB system SRAM (SRAMH/SRAM1/SRAM2/SRAM3/SRAM4).

Each SRAM can be accessed in bytes, half words (16 bits) or full words (32 bits). High-speed SRAM (SRAMH) read and write operations can be executed at the fastest CPU speed (240MHz) with 0 wait (ie 1 cycle), or a wait cycle can be inserted. The wait period for read and write access of each SRAM is set by the SRAM wait control register (SRAM_WTCR).

SRAMB can provide 4KB data retention space in Power down mode.

SRAM4 and SRAMB are equipped with ECC check (Error Checking and Correcting). ECC check is correct one and check two codes, which can correct one bit error and check two bit errors;

SRAMH/SRAM1/SRAM2/SRAM3 have parity check (Even-parity check), with one check bit per byte of data.

1.4.9 General IO (GPIO)

GPIO main features:

- Each port group has 16 I/O Pins, which may be less than 16 depending on actual configuration
- Support pull-up
- Support push-pull, open-drain output mode
- Supports high, medium and low drive modes
- Support for external interrupt input
- Support I/O pin peripheral function multiplexing, each I/O pin has up to 64 selectable multiplexing functions
- Individual I/O pins can be programmed independently
- Each I/O pin can select two functions to be active at the same time (two output functions are not supported to be active at the same time)

1.4.10 Interrupt control (INTC)

The function of the interrupt controller (INTC) is to select the interrupt event request as an interrupt input to the NVIC to wake up the WFI; as an event input, to wake up the WFE. Select interrupt event request as wake-up condition for low power consumption mode (sleep mode and stop mode); interrupt control function of external pin EIRQ; interrupt/event selection function of software interrupt.

Main specifications:

1. NVIC interrupt vector: For the actual number of interrupt vectors used, please refer to the interrupt vector table in the user manual (excluding the 16 interrupt lines of Cortex™-M4F). Each interrupt vector can select the corresponding peripheral interrupt event request according to the interrupt selection register. For more instructions on exceptions and NVIC programming, please refer to Chapter 5 of the ARM Cortex™-M4F Technical Reference Manual: Exceptions and Chapter 8: Nested vectored interrupt controller.
2. Programmable priority: 16 programmable priority levels (4-bit interrupt priority levels are used).
3. Non-maskable interrupts: A variety of system interrupt event requests can be independently selected as non-maskable interrupts, and each interrupt event request is equipped with an independent enable selection, suspend, and clear the suspend register.
4. Equipped with 16 external pin interrupts.
5. Configure various peripheral interrupt event requests. For details, please refer to the list of interrupt event request numbers.

6. Equipped with 32 software interrupt event requests.
7. Interrupt wakes up system sleep mode and stop mode.

1.4.11 Automatic Operating System (AOS)

The Automatic Operation System is used to realize the linkage between peripheral hardware circuits without the aid of the CPU. Use the events generated by the peripheral circuit as the AOS source (AOS Source), such as the comparison match of the timer, the timing overflow, the periodic signal of the RTC, the various states of the data sent and received by the communication module (idle, the received data is full, the sending data is over, Send data empty), ADC conversion ends, etc., to trigger other peripheral circuit actions. The peripheral circuit action that is triggered is called AOS Target (AOS Target).

1.4.12 Storage Protection Unit (MPU)

The MPU can provide memory protection and improve system security by preventing unauthorized access.

This chip has built-in six MPU units for the host and one MPU unit for the IP.

Among them, ARM MPU provides CPU access control to all 4G address space.

SMPU1/ SMPU2/ FMPU/ HMPU/ EMPU respectively provide system DMA_1/ system DMA_2/ USBFS-DMA/ USBHS-DMA/ ETH-DMA read and write access control to all 4G address space. When accessing the forbidden space, the MPU action can be set to ignore/bus error/non-maskable interrupt/reset.

IPMPU provides access control to system IP and security-related IP in unprivileged mode.

1.4.13 KEYSCAN

This product is equipped with a keyboard control module (KEYSCAN) unit. The KEYSCAN module supports keyboard array (row and column) scanning, the column is driven by the independent scan output KEYOUTm (m=0~7), and the row KEYINn (n=0~15) is input as EIRQn (n=0~15) be detected. This module realizes the key recognition function through the line scan query method.

1.4.14 Internal clock calibrator (CTC)

The Clock Trimming Controller (CTC) automatically calibrates the internal high-speed oscillator (HRC). Because the influence of working environment on HRC frequency may cause deviation, CTC can automatically adjust HRC frequency by hardware based on external high precision reference clock to obtain an accurate HRC clock.

The main features of CTC are as follows:

- Two external reference clock sources: XTAL, CTCREF
- 16-bit calibration counter for frequency measurement with heavy load function
- 8-bit calibration deviation and 6-bit calibration values for frequency calibration

- Error interrupt to prompt calibration failure

1.4.15 DMA controller (DMA)

DMA is used to transfer data between memory and peripheral functional modules. It can exchange data between memory, between memory and peripheral functional modules and between peripheral functional modules without CPU involvement.

- DMA bus is independent of CPU bus and transmitted according to AMBA AHB-Lite bus protocol.
- With 2 DMA control units, a total of 16 independent channels, can independently operate different DMA transfer functions
- The startup source of each channel is configured through the independent trigger source selection register
- One block per request
- The data block is a minimum of one data and can be up to 1024 data
- The width of each data can be configured as 8bit, 16bit or 32bit
- Up to 65535 transmissions can be configured
- Source and destination addresses can be independently configured as fixed, increment, decrement, loop or jump at specified offset
- Three types of interrupts can be generated: Block transfer complete interrupt, transfer complete interrupt, transfer error interrupt. Each interrupt can be configured with a mask or not. Among them, the block transmission is completed, and the transmission completion can be used as an event output and can be used as a trigger source for other peripheral modules
- Support for linked transmission to enable multiple blocks of data to be transmitted at a time
- Support external event-triggered channel reset
- You can set the module stop state to reduce power consumption when not in use

1.4.16 Voltage comparator (CMP)

The voltage comparator (Comparator, CMP for short) is a peripheral module that compares two analog voltages. There are four comparison channels CMP1~4.

CMP main features:

- CMP1~4 can be independently compared for voltage
- Window comparison can be completed when CMP1, 2 or CMP3, 4 are used at the same time
- Both positive and negative terminal voltages have multiple input voltage sources for selection
- Optional sampling clock for digital noise filter
- The output can be switched on and off using the PWM waveform output by the timer
- Can generate events that trigger other peripherals to start
- Interrupt and wake-up from system stop mode
- The comparison result can be output to the external pin VCOUT

1.4.17 Analog-to-digital converter (ADC)

12-bit ADC is an analog-to-digital converter with successive approximation. This MCU is equipped with 3 ADC units, units 1 and 2 support 16 channels, and unit 3 supports 20 channels, which can convert analog signals from external pins and inside the chip. Analog input channels can be arbitrarily combined into a sequence, a sequence can be single scan conversion, or continuous scan conversion. Supports continuous multiple conversions for any specified channel and averages the conversion results. The ADC module is also equipped with an analog watchdog function, which monitors the conversion result of any specified channel and detects whether it exceeds the range set by the user.

ADC main characteristics

- High performance
  - Configurable 12-bit, 10-bit and 8-bit resolution
  - ADC digital interface clock PCLK4 and conversion clock PCLK2 (Also called ADCLK) The frequency ratio can be set to 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
    PCLK2 can choose a PLL clock that is asynchronous with the system clock HCLK. At this time, the frequency is higher than
    PCLK4:PCLK2=1:1
    PCLK2 frequency supports up to 60MHz
  - Sampling Rate: 2.5MSPS (PCLK2=60MHz, 12 bits, sampling 11 cycles, conversion 13 cycles)
  - Independent programming of sampling time for each channel
  - Channel-independent data register
  - Data register configurable left/right justification
  - Continuous multiple conversion averaging function
  - Simulation watchdog, monitoring conversion results
  - The ADC module can be set to stop when not in use
- Analog input channel
  - Maximum 16 external analog input channels
  - 2 internal analog inputs: Internal reference voltage, divided by VBAT
- Conversion start condition
  - Software Setup Conversion Started
  - Start of Peripheral Device Synchronization Trigger Conversion
  - External Pin Triggering Start
- Conversion mode
  - 2 scan sequences A and B, optionally specifying a single or multiple channels
  - Sequence A single scan
  - Sequence A continuous scanning

  - Double sequence scanning, sequence A and B independently select trigger source, sequence B has higher priority than A
  - Cooperative mode (for devices with two or three ADCs)
- Interrupt and Event Signal Output
  - Sequence A Scan End Interrupt and Event ADC _ EOCA
  - Sequence B Scan End Interrupt and Event ADC _ EOCB
  - Analogwatchdog 0 compared interrupt and event ADC _ CMP0
  - Simulation watchdog 1 comparing interrupt and event ADC _ CMP1
  - All four of these event outputs can start the DMA

This MCU is equipped with 4 unit programmable gain amplifiers PGA, the gain range of x2~x32 can be selected. The analog input can be amplified by the PGA circuit first, and then input to the ADC module for conversion.

This MCU is equipped with a sample-and-hold circuit SH dedicated to three units. When the dedicated sample and hold circuit is valid, each time the sequence starts, all SH valid channels are sampled at the same time, and then the ADC is started to perform A/D conversion on each channel in the sequence in turn. In continuous scan mode, the sequence inserts the SH sample time at the start of the second and subsequent scans.

1.4.18 Digital-to-analog converter DAC

This MCU is equipped with two 12-bit digital-to-analog voltage converter units DAC1 and DAC2. Each DAC unit contains two D/A conversion channels, which can be converted independently or synchronously converted by synchronous update of conversion data. Each conversion channel features an output amplifier that can directly drive an external load without an external op amp. Independent pin input reference voltages VREFH and VREFL can be used to improve conversion accuracy.

DAC main features:

- Two DAC units, each with two D/A conversion channels
- 12-bit conversion data can be configured as left-aligned or right-aligned format
- Two conversion channels of the same DAC module can achieve simultaneous conversion
- Convert external data (from DCU) to output triangle wave and sawtooth wave
- Output amplification function, can directly drive external load
- A/D conversion priority mode reduces interference to A/D conversion
- Output available for voltage comparator as negative terminal voltage
- Independent pin input reference voltage VREFH/VREFL

1.4.19 Temperature Sensor (OTS)

The OTS can obtain the temperature inside the chip to support the reliable operation of the system. After using software or hardware to trigger and start the temperature measurement, OTS provides a set of digital quantities related to temperature, and the temperature value can be calculated through the calculation formula.

1.4.20 Advanced Control Timer (Timer6)

Advanced control timer 6 (Timer6) is a high-performance timer with a 16-bit count width, which can provide rich and flexible combinations and various interrupts, events, and PWM outputs in various complex application scenarios. The timer supports two waveform modes of sawtooth wave and triangle wave, and can generate various PWM waveforms (unilaterally aligned independent PWM, bilaterally symmetrical independent PWM, bilaterally symmetrical complementary PWM, bilaterally asymmetrical PWM, etc.); software synchronization and Hardware synchronization (synchronous start, stop, clear, refresh, etc.); each reference value register supports buffer function (single-level buffer and double-level buffer); supports pulse width measurement and period measurement; supports 2-phase quadrature encoding and 3-phase positive Interchange coding; support EMB control. This series of products are equipped with 8-unit Timer6 (U1~4 are 32bit timers; U5~U8 are 16bit timers).

1.4.21 High Precision PWM (HRPWM)

High Precision PWM (HRPWM) extends the resolution of Timer6's PWM signal. This module, paired with TMR6, can generate up to 16 channels of high-resolution PWM waveforms.

The characteristics of HRPWM are as follows:

- Extended PWM signal resolution
- Used to adjust the duty cycle and phase of the PWM waveform
- Can be used for rising edge, falling edge, rising edge and rising edge control
- Auto-calibration function to provide unit delay

1.4.22 General control timer (Timer4)

General control timer 4 (Timer4) is a timer module for three-phase motor control. It provides three-phase motor control schemes for various applications. The timer supports triangular wave and sawtooth wave modes and generates various PWM waveforms. Supporting cache function; Support EMB control. 3 unit of Timer 4 is carried in this product family.

1.4.23 Emergency Brake Module (EMB)

The emergency braking module is a functional module that generates control events and outputs them to the timer when certain conditions are met, so as to control the timer to stop outputting PWM signals to external motors. The following factors are used to generate control events:

- Change of input level of external port
- Level of PWM output port occurs in phase (same high or same low)
- Voltage comparator comparison results
- External oscillator stop oscillation
- Write register software control

1.4.24 General Timer (TimerA)

General Timer A (Timer A) is a timer with 16-bit count width and 4 PWM outputs. The timer supports two waveform modes of triangular wave and sawtooth wave, and can generate various PWM waveforms (unilaterally aligned PWM, bilaterally symmetrical PWM); supports synchronous start of counters; compares the reference value register to support the buffer function; supports cascaded implementation between units 32 Bit counting; supports 2-phase quadrature encoding counting and 3-phase quadrature encoding counting. This series of products is equipped with 12 units of TimerA, which can achieve a maximum of 48 PWM outputs.

1.4.25 General Timer (Timer2)

General-purpose timer 2 (Timer2) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains 2 channels (CH-A and CH-B). Each channel has an output port, which can realize basic square wave output; each channel has 2 input ports, one is a clock input port, which can realize asynchronous counting of ports; the other is a trigger input port, which can realize timer start , stop, clear, count action and count value capture input; support pulse width measurement and period measurement. 4 unit of Timer 2 is carried in this product family.

1.4.26 General Timer (Timer0)

General-purpose timer 0 (Timer0) is a basic timer that can realize synchronous counting and asynchronous counting. The timer contains 2 channels (CH-A and CH-B) that can generate compare match events during counting. The event can trigger interrupt, or can be output as an event to control other modules. This series of products is equipped with 2 units of Timer0.

1.4.27 Real Time Clock RTC

A real-time clock (RTC) is a counter that stores time information in BCD code format. Record specific calendar times from 00 to 99. Supports 12/24 hour two time systems, automatically calculates the number of days 28, 29 (leap year), 30 and 31 according to the month and year.

1.4.28 Watchdog Counter (WDT)

There are two watchdog counters, one is the dedicated watchdog counter (SWDT) whose counting clock source is dedicated internal RC (SWDTLRC: 10KHz), and the other is the general-purpose watchdog counter (WDT) whose counting clock source is PCLK3 . Dedicated watchdogs and general purpose watchdogs are 16-bit down counters used to monitor software faults caused by external disturbances or unforeseen logic conditions that cause the application to deviate from normal operation.

Both watchdogs support the window function. The window interval can be preset before the count starts. When the count value is in the window interval, the counter can be refreshed and the count restarts. .

1.4.29 Serial Communication Interface (USART)

This product is equipped with 10 units of Universal Serial Transceiver Module (USART). Universal Serial Transceiver Module (USART) can flexibly exchange full-duplex data with external devices; this USART supports Universal Asynchronous Serial Communication Interface (UART), Clock Synchronous Communication Interface, Smart Card Interface (ISO/IEC7816-3) and LIN communication interface. Support modem operation (CTS/RTS operation), multi-processor operation. Cooperate with Timer0 module to support UART receiving TIMEOUT function. USART_1 supports wake-up STOP mode function via RX line.

The specific function distribution is as follows:

- UART: Full channel support
- Multiprocessor Communication: Full channel support
- Clock synchronization communication: Full channel support
- RX line wake-up STOP mode function: USART_1 support
- Fractional baud rate: USART_1, USART_2, USART_3, USART_4, USART_6, USART_7, USART_8, USART_9 support
- LIN: USART_5, USART_10 support
- smart card: USART_1, USART_2, USART_3, USART_4, USART_6, USART_7, USART_8, USART_9 support
- UART receive timeout function: USART_1, USART_2, USART_6, USART_7 support

1.4.30 Inter-integrated circuit bus (I2C)

I2C (Integrated Circuit Bus) is used as the interface between the microcontroller and the I2C serial bus. Provides multi-master mode function, which can control the protocol and arbitration of all I2C buses. Standard mode and fast mode are supported. SMBus is also supported.

I2C main features:

1. I2C bus mode and SMBUS bus mode are optional. Host mode and slave mode are optional. Various prepare times, hold times, and bus idle times relative to the transfer rate are automatically ensured.
2. The standard mode is up to 100 Kbps, and the fast mode is up to 400 Kbps.
3. The start condition, restart condition, and stop condition are automatically generated, and the start condition, restart condition, and stop condition of the bus can be detected.
4. Two slave mode addresses can be set. 7-bit address format and 10-bit address format can be set at the same time. Broadcast call address, SMBus host address, SMBus device default address, SMBus alarm address can be detected.
5. Answer bits can be automatically determined when sent. Answer bits can be sent automatically upon reception.
6. Handshake function.
7. Arbitration function.
8. A time-out function can detect that the SCL clock is stopped for a long time.
9. SCL input and SDA input have built-in digital filters that are programmable to filter.
10. Communication error, receive data full, send data empty, one frame send end, address match unanimously interrupt.

1.4.31 Serial Peripheral Interface (SPI)

SPI is equipped with six channel serial peripheral interface, which supports high-speed full-duplex serial synchronous transmission and convenient data exchange with peripheral equipment. Users can set the range of 3/4-wire, host/slave and baud rate as needed.

Table 1-2 SPI main features

Essentials	Description
Number of channels	1 channel
Serial communication function	• Supporting 4-wire SPI mode and 3-wire clock synchronization mode • Support full-duplex and only send two communication methods • Polarity and phase of adjustable communication clock SCK
Data format	• Selectable data shift order: MSB start/LSB start • Selectable data width:4/5/6/7/8/9/10/11/12/13/14/15/16/20/24/32 bit • A maximum of 32 bits of data can be transmitted or received in four frames
Baud rate	• In the host mode, the baud rate can be adjusted through the built-in dedicated baud rate generator. The baud rate range is the frequency division of PCLK1 by 2~256. • The maximum baud rate allowed in slave mode is PCLK1 divided by 6
data buffer	• with 16-byte data buffer area • Support double buffering
Error monitoring	• Mode fault error monitoring • Data overload error monitoring • Data underload error monitoring • Parity error monitoring
Chip selection signal control	• Each channel is configured with four chip select signal lines • The relative timing relationship between the chip select signal and the communication clock can be adjusted • The chip select signal inactive time between two consecutive communications can be adjusted • Polarity adjustable

Essentials	Description
Transmission Control in Host Mode	• Start transmission by writing data to the data register • Communication auto-suspend function
Interrupt	• Received data area full • Sending data area is empty • SPI error (mode/overload/underload/parity) • SPI is vacant • Transfer complete (event source only)
Low power control	Configurable module stop
Other functions	• SPI initialization function

1.4.32 Four-Wire Serial Peripheral Interface (QSPI)

The Four-Wire Serial Peripheral Interface (QSPI) is a memory control module mainly used to communicate with a serial ROM with an SPI-compatible interface. Its objects mainly include serial flash memory, serial EEPROM and serial FeRAM.

1.4.33 Integrated circuit built-in audio bus (I2S)

I2S (Inter_IC Sound Bus), an integrated circuit built-in audio bus, which is dedicated to data transmission between audio devices.

Table 1-3 I2S main features

Function	Main characteristics
Communication mode	• Supports full-duplex and half-duplex communication • Support host mode or slave mode operation
Data format	• Optional channel lengths: 16/32 bits • Optional transmit data length: 16/24/32bits • Data shift order: MSB starts
Baud rate	• 8-bit programmable linear prescaler for precise audio sampling frequency • Support sampling frequency 192k, 96k, 48k, 44.1k, 32k, 22.05k, 16k, 8k • Can output drive clock to drive external audio components, the ratio is fixed at 256*Fs (Fs is the audio sampling frequency)
Support I2S protocol	• I2S Philips Standard • MSB alignment criteria • LSB alignment criteria • PCM standard
data buffer	• With 4-word deep, 32-bit wide input and output FIFO buffer area
Timer	• Can use internal I2SCLK (UPLLR/UPLLQ/UPLLP/MPLLR/MPLLQ/MPLLP); can also be provided by an external clock on the I2S_EXCK pin
Interrupt	• An interrupt is generated when the valid space of the send buffer reaches the alarm threshold • An interrupt is generated when the valid space of the receive buffer reaches the alarm threshold • The receive data area is full, there is still a write data request, and the receive overflows • The send data area is empty and there is still a send request, send underflow • The send data area is full and there is still a write data request, sending overflow

1.4.34 USB2.0 High Speed Module (USBHS)

This product is equipped with one unit of USB2.0 full-speed module (USBHS), built-in on-chip full-speed PHY, and supports ULPI (SDR) interface. USBHS is a dual role (DRD) controller that supports both slave and master functions. In host mode, USBHS supports high-speed, full-speed and low-speed transceivers, while in slave mode only high-speed and full-speed transceivers are supported. The USBHS controller supports all four transfer modes (control transfer, bulk transfer, interrupt transfer and isochronous transfer) defined by the USB 2.0 protocol. The USBHS controller supports LPM (Link Power Management) function.

1.4.35 USB2.0 Full Speed Module (USBFS)

The USB Full Speed (USBFS) controller provides a set of USB communication solutions for portable devices. The USBFS controller supports host mode and device mode, and the chip integrates a full-speed PHY. In host mode, the USBFS controller supports full-speed (FS, 12Mb/s) and low-speed (LS, 1.5Mb/s) transceivers, while in device mode only full-speed (FS, 12Mb/s) transceivers are supported. The USBFS controller supports all four transfer modes defined by the USB 2.0 protocol (control transfer, bulk transfer, interrupt transfer, and isochronous transfer). The USBFS controller supports LPM (Link Power Management) function.

1.4.36 CAN FD Controller (CAN FD)

CAN FD controller follows CAN bus CAN2.0 (2.0A, CAN2.0B) and CAN FD protocol.

The CAN bus controller can handle data transmission and reception on the bus. In this product, the CAN FD controller has 16 sets of filters. Filters are used to select messages for an application to receive.

The application program in the CAN FD controller can send data to the bus through a high-priority primary transmit buffer (Primary Transmit Buffer, hereinafter referred to as PTB) and 3 secondary transmit buffers (Secondary Transmit Buffer, hereinafter referred to as STB) , the sending order of mailboxes is determined by the sending scheduler. The bus data is acquired through 8 receive buffers (Receive Buffer, hereinafter referred to as RB). 3 STBs and 8 RBs can be understood as a 3-level FIFO and an 8-level FIFO, and the FIFO is completely controlled by hardware.

CAN FD bus controller can also support time-triggered CAN communication (Time-trigger communication).

1.4.37 CAN2.0B Controller (CAN2.0B)

The CAN2.0B controller follows the CAN bus CAN2.0 (2.0A, CAN2.0B) protocol.

The CAN bus controller can handle data transmission and reception on the bus. In this product, the CAN2.0B controller has 16 sets of filters. Filters are used to select messages for an application to receive.

The application program in the CAN2.0B controller can send data to a high-priority primary transmit buffer (Primary Transmit Buffer, hereinafter referred to as PTB) and 3 secondary transmit buffers (Secondary Transmit Buffer, hereinafter referred to as STB). Bus, the sending scheduler determines the sending order of mailboxes. The bus data is acquired through 8 receive buffers (Receive Buffer, hereinafter referred to as RB). 3 STBs and 8 RBs can be understood as a 3-level FIFO and an 8-level FIFO, and the FIFO is completely controlled by hardware.

CAN2.0B bus controller can also support time-triggered CAN communication (Time-trigger communication).

1.4.38 SDIO Controller (SDIOC)

SDIOC provides an SD host interface and an MMC host interface for communicating with SD cards supporting SD2.0 protocol, SDIO devices and MMC devices supporting eMMC4.2 protocol. This product has 2 SDIO controllers and can communicate with 2 SD/MMC/SDIO devices at the same time.

SDIOC features are as follows:

- Support SDSC, SDHC, SDXC format SD card and SDIO device
- Support one-line (1bit) and four-line (4bit) SD bus
- Support one-line (1bit), four-line (4bit) and eight-line (8bit) MMC bus
- SD clock up to 50MHz
- With card recognition and hardware write protection

1.4.39 Ethernet MAC Controller (ETHMAC)

The Ethernet MAC controller (ETHMAC) is used to send and receive data in accordance with the IEEE802.3-2002 standard in the Ethernet network, and has various application fields, such as switches, network interface cards, and so on. The MAC controller supports two industry standard interfaces to the external physical layer (PHY): Media Independent Interface (MII) (defined in the IEEE802.3 specification) and Reduced Media Independent Interface (RMII).

Mainly follow the following protocol specifications:

- IEEE802.3-2002 for Ethernet MAC
- IEEE1588-2008 standard for specifying networked clock synchronization
- AMBA2.0, used for AHB host/slave port
- RMII interface specification

1.4.40 External Memory Controller (EXMC)

The external memory controller EXMC (External Memory Controller) is an independent module used to access various off-chip memories and realize data exchange. EXMC can convert the internal AMBA protocol interface into various types of dedicated off-chip memory communication protocol interfaces through configuration, including SRAM, PSRAM, NOR Flash, NAND Flash and SDRAM. EXMC is divided into multiple sub-modules, each sub-module supports a specific memory type, and the user can control the external corresponding type of memory by configuring the registers of the sub-module.

1.4.41 Digital Video Interface (DVP)

The Digital Camera Interface (DVP) is a synchronous parallel interface that captures 8-, 10-, 12- or 14-bit high-speed data streams from an external CMOS camera module. Software synchronization and hardware synchronization are supported. Supports acquisition frequency control and window clipping control of data streams. Supports data stream capture in different formats such as monochrome or raw Bayer format/YCbCr4:2:2/RGB565 progressive video and compressed data (JPEG).

1.4.42 Cryptographic Coprocessing Module (CPM)

The encryption co-processing module (CPM) includes three sub-modules: AES encryption and decryption algorithm processor, HASH secure hash algorithm, and TRNG true random number generator.

The AES encryption and decryption algorithm processor follows the new data encryption standard officially announced by the National Institute of Standards and Technology (NIST) on October 2, 2000. The block length is fixed at 128 bits, and the key length supports 128/192/256 bits.

The HASH secure hash algorithm is the SHA-2 version of SHA-256 (Secure Hash Algorithm), which complies with the national standard "FIPS PUB 180-3" issued by the National Bureau of Standards and Technology of the United States. Produces 256-bit message digest output.

The TRNG true random number generator is a random number generator based on continuous analog noise, providing 64bit random numbers.

1.4.43 CRC Unit (CRC)

The CRC algorithm of this module complies with the definition of ISO/IEC 13239 and adopts 32-bit and 16-bit CRC respectively. The polynomial of CRC 32 is $X^{32}+ X^{26}+ X^{23}+ X^{22}+ X^{16}+ X^{12}+ X^{11}+ X^{10}+ X^{8}+ X^{7}+ X^{5}+ X^{4}+ X^{2}+ X+ 1$, 32-bit initial value is "0xFFFFFFFF". The polynomial of CRC 16 is $X^{16}+ X^{12}+ X^{5}+ 1$, the initial value of 16 bits is "0xFFFF".

1.4.44 Data Computation Unit (DCU)

The Data Computing Unit is a module that simply processes data without the aid of a CPU. Each DCU unit has 3 data registers, capable of adding and subtracting 2 data and comparing sizes, as well as a window comparison function. It can also be triggered by a timer to provide a digital-to-analog conversion module (DAC) with continuously changing digital quantities to generate triangular wave and sawtooth wave output. This product is equipped with 8 DCU units, each unit can independently complete its own function.

1.4.45 Mathematical Operations Unit (MAU)

The Mathematical Operation Unit (MAU) is a hardware-accelerated operation module that includes two types of operations, the square root operation and the sine operation, and supports the square root and sine operations of fixed-point numbers. The sine function supports 360°/2^12 arithmetic precision.

1.4.46 Filter Math Accelerator (FMAC)

Filter Math Accelerator (FMAC) is a hardware acceleration module for FIR filter computation. This module can perform up to 16-order FIR digital filtering with configurable orders. Built-in 16x16 bit multiplier, 32+5bit adder, users can customize the output data precision. This series is equipped with 4 FMAC modules.

1.4.47 Debug controller (DBGC)

The core of this MCU is Cortex™-M4F, which contains hardware for advanced debug functions and supports Embedded Trace Macrocell (ETM). With these debugging features, you can stop the kernel when fetching fingers (instruction breakpoints) or accessing data (data breakpoints). When the kernel stops, you can query the internal state of the kernel and the external state of the system. After the query completes, the kernel and system are restored and program execution is restored.

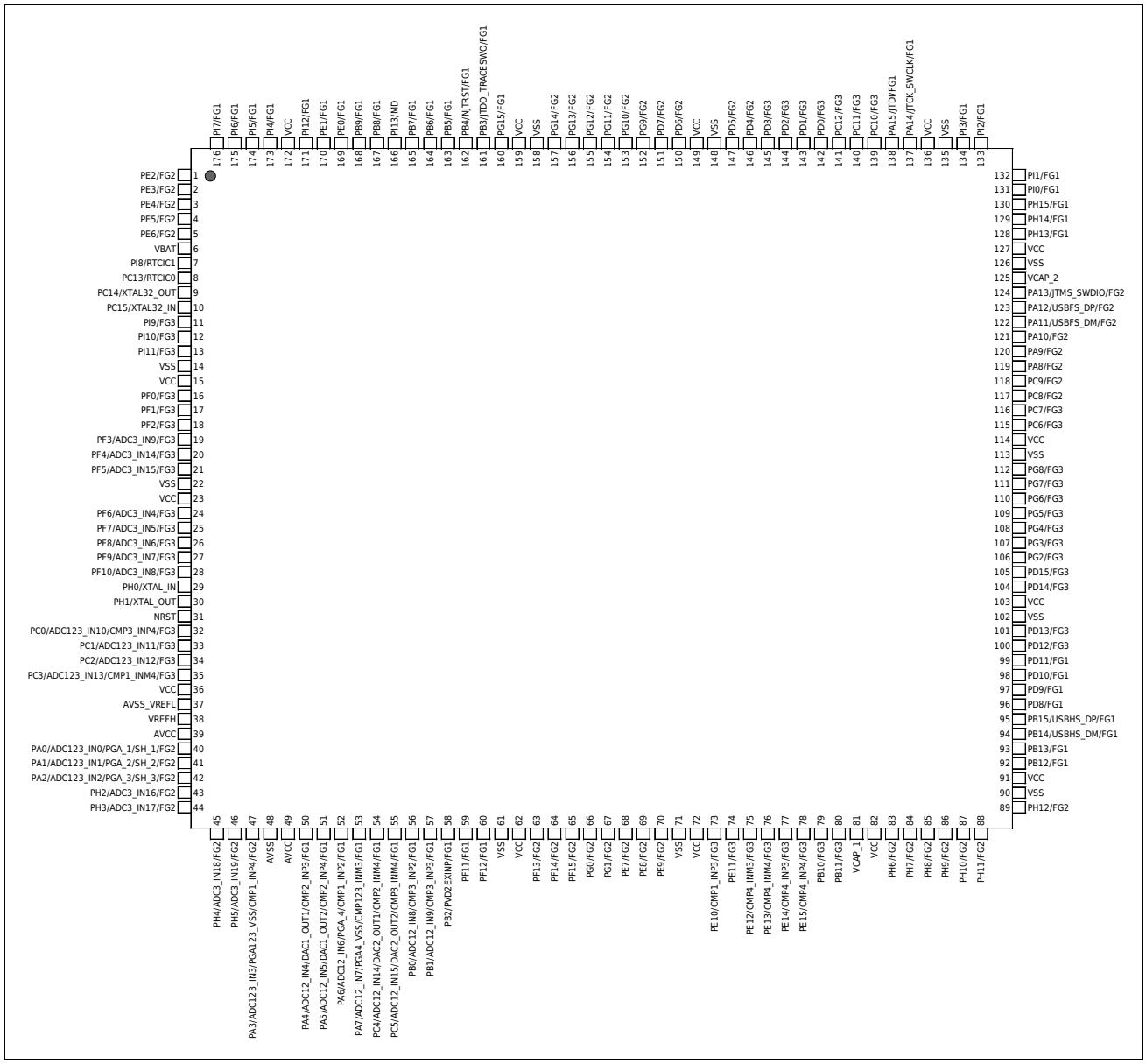
Provides two debugging interfaces:

- Serial Debugging Tracking Interface SWD
- Parallel Debug Trace Interface JTAG

2 Pin Configuration and Functions (Pinouts)

2.1 Pin configuration diagram

LQFP176



LQFP100

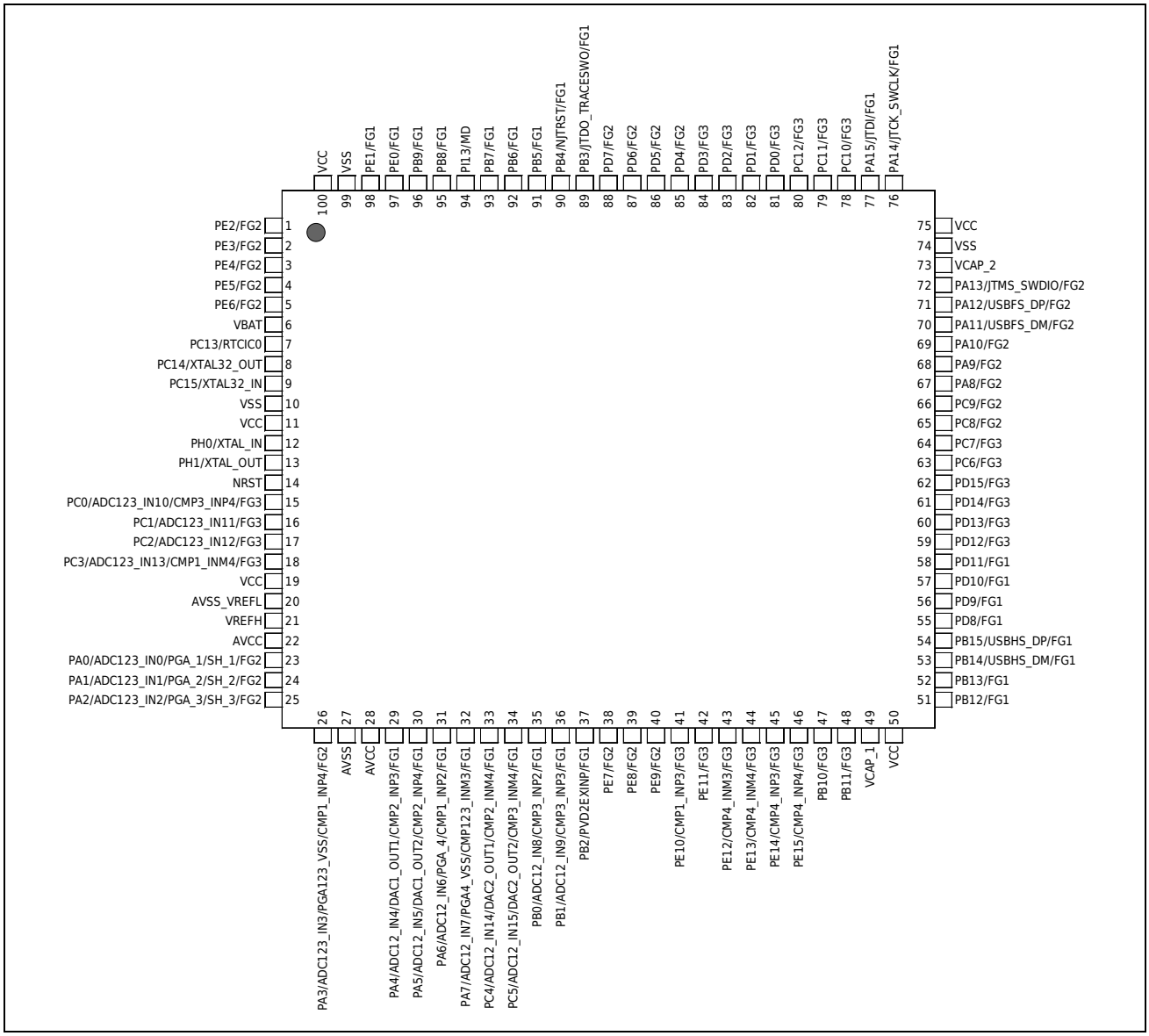


Figure 2-1 Pin configuration diagram

2.2 Pin function table

Table 2-1 Pin function table

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
1	1	PE2		EIRQ2	TRACECLK		FCMREF	TIM4_3_ADSM		TIMA_9_PWM1/TIMA_9_CLKA		TIMA_4_TRIG	USART3_CK				ETH_MII_TXD3	EXMC_AD D23			EVENTOUT		I2S3_MCK					FG2
2	2	PE3		EIRQ3	TRACED0					TIMA_9_PWM2/TIMA_9_CLKB	TIMA_4_PWM1/TIMA_4_CLKA		USART6_CK				ETH_MII_RMII_TXEN	EXMC_AD D19			EVENTOUT	TIM2_1_CLKA	I2S4_SD	SPI2_NSS0				FG2
3	3	PE4		EIRQ4	TRACED1					TIMA_9_PWM3	TIMA_4_PWM2/TIMA_4_CLKB		USART6_CTS					EXMC_AD D20	DVP_DATA4		EVENTOUT	TIM2_1_CLKB			SPI4_NSS0			FG2
4	4	PE5		EIRQ5	TRACED2		CTCREF			TIMA_9_PWM4	TIMA_4_PWM3		USART6_RTS					EXMC_AD D21	DVP_DATA6		EVENTOUT	TIM2_1_PWMA/TRIGA						FG2
5	5	PE6		EIRQ6	TRACED3						TIMA_4_PWM4	TIMA_9_TRIG						EXMC_AD D22	DVP_DATA7		EVENTOUT	TIM2_1_PWMB/TRIGB						FG2
6	6	VBAT																										
7	-	PI8	RTCIC1	EIRQ8																	EVENTOUT							
8	7	PC13	RTCIC0	EIRQ13+WKUP3_1			RTC_OUT			TIMA_10_PWM4					SDIO2_CK					EVNTP313	EVENTOUT		I2S3_MCK					
9	8	PC14	XTAL32_OUT	EIRQ14						TIMA_10_PWM1/TIMA_10_CLKA										EVNTP314	EVENTOUT							
10	9	PC15	XTAL32_IN	EIRQ15						TIMA_10_PWM2/TIMA_10_CLKB										EVNTP315	EVENTOUT							
11	-	PI9		EIRQ9								TIMA_6_TRIG						EXMC_DATA30			EVENTOUT							FG3
12	-	PI10		EIRQ10						TIMA_6_PWM3							ETH_MII_RXER	EXMC_DATA31			EVENTOUT							FG3
13	-	PI11		EIRQ11						TIMA_6_PWM4						USBHS_ULPI_DIR					EVENTOUT							FG3
14	-	VSS																										
15	-	VCC																										
16	-	PF0		EIRQ0			MCO_1				TIMA_11_PWM1/TIMA_11_CLKA		USART10_CK					EXMC_AD D0			EVENTOUT			SPI3_NSS1				FG3
17	-	PF1		EIRQ1							TIMA_11_PWM2/TIMA_11_CLKB		USART10_CTS					EXMC_AD D1			EVENTOUT			SPI3_NSS2				FG3
18	-	PF2		EIRQ2							TIMA_11_PWM3		USART10_RTS					EXMC_AD D2			EVENTOUT			SPI3_NSS3				FG3
19	-	PF3	ADC3_IN9	EIRQ3							TIMA_11_PWM4							EXMC_AD D3			EVENTOUT	TIM2_3_CLKA		SPI4_NSS1				FG3
20	-	PF4	ADC3_IN14	EIRQ4								TIMA_11_TRIG						EXMC_AD D4			EVENTOUT	TIM2_3_CLKB		SPI4_NSS2				FG3
21	-	PF5	ADC3_IN15	EIRQ5								TIMA_10_TRIG						EXMC_AD D5			EVENTOUT			SPI4_NSS3				FG3
22	10	VSS																										
23	11	VCC																										
24	-	PF6	ADC3_IN4	EIRQ6						TIMA_10_PWM1/TIMA_10_CLKA								EXMC_RB2			EVENTOUT	TIM2_3_PWMA/TRIGA			SPI5_NSS0	USART7_RX			FG3
25	-	PF7	ADC3_IN5	EIRQ7						TIMA_10_PWM2/TIMA_10_CLKB								EXMC_RB3			EVENTOUT	TIM2_3_PWMB/TRIGB	I2S4_MCK		SPI5_SCK	USART7_TX			FG3
26	-	PF8	ADC3_IN6	EIRQ8						TIMA_10_PWM3								EXMC_RB4			EVENTOUT	TIM2_4_PWMA/TRIGA			SPI5_MISO				FG3

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
27	-	PF9	ADC3_IN7	EIRQ9						TIMA_10_PWM4								EXMC_RB5	DVP_PIXCLK		EVENTOUT	TIM2_4_PWMB/TRIGB			SPI5_MOSI			FG3
28	-	PF10	ADC3_IN8	EIRQ10														EXMC_RB6	DVP_DATA11		EVENTOUT							FG3
29	12	PH0	XTAL_IN	EIRQ0							TIMA_5_PWM3										EVENTOUT							
30	13	PH1	XTAL_OUT	EIRQ1							TIMA_5_PWM4										EVENTOUT							
31	14	NRST																										
32	15	PC0	ADC123_IN10+CMP3_INP4	EIRQ0						TIMA_8_PWM1/TIMA_8_CLKA		TIMA_1_TRIG			SDIO2_D5	USBHS_ULPI_STP		EXMC_WE		EVNTP300	EVENTOUT	TIM2_4_PWMA/TRIGA	I2S1_EXCK					FG3
33	16	PC1	ADC123_IN11	EIRQ1						TIMA_8_PWM2/TIMA_8_CLKB		TIMA_1_TRIG			SDIO2_D6		ETH_SMI_MDC			EVNTP301	EVENTOUT	TIM2_4_PWMB/TRIGB	I2S1_MCK					FG3
34	17	PC2	ADC123_IN12	EIRQ2				TIM4_2_ADSM	TIM6_8_PWMA	TIMA_8_PWM3		EMB_PORT3			SDIO2_D7	USBHS_ULPI_DIR	ETH_MII_TXD2	EXMC_CE0		EVNTP302	EVENTOUT	TIM2_4_CLKA	I2S1_SDIN		SPI2_MISO			FG3
35	18	PC3	ADC123_IN13+CMP1_INM4	EIRQ3				TIM4_2_PCT	TIM6_8_PWMB	TIMA_8_PWM4					SDIO1_WP	USBHS_ULPI_NXT	ETH_MII_TXCLK	EXMC_ALE		EVNTP303	EVENTOUT	TIM2_4_CLKB			SPI2_MOSI			FG3
36	19	VCC																										
37	20	AVSS_VREFL																										
-	-	VREFL																										
38	21	VREFH																										
-	-	VREFH																										
39	22	AVCC																										
40	23	PA0	ADC123_IN0+PGA_1	EIRQ0+WKUP0_0				TIM4_2_OUH	TIM6_TRIGC	TIMA_2_PWM1/TIMA_2_CLKA	TIMA_2_TRIG	TIMA_5_PWM1/TIMA_5_CLKA	USART5_CTS		SDIO2_D4		ETH_MII_CRS			EVNTP100	EVENTOUT	TIM4_2_CLK		SPI5_NSS1		USART2_CTS		FG2
41	24	PA1	ADC123_IN1+PGA_2	EIRQ1				TIM4_2_OUL		TIMA_2_PWM2/TIMA_2_CLKB	TIMA_3_TRIG	TIMA_5_PWM2/TIMA_5_CLKB	USART5_RTS		SDIO2_D5		ETH_MII_RMII_RXCLK			EVNTP101	EVENTOUT	TIM2_1_CLKA		SPI5_NSS2		USART2_RTS		FG2
42	25	PA2	ADC123_IN2+PGA_3	EIRQ2				TIM4_2_OVH	TIM6_6_PWMA	TIMA_2_PWM3	TIMA_5_PWM1/TIMA_5_CLKA	TIMA_5_PWM3			SDIO2_D6		ETH_SMI_MDIO			EVNTP102	EVENTOUT	TIM2_1_PWMA/TRIGA		SPI5_NSS3		USART2_TX		FG2
43	-	PH2	ADC3_IN16	EIRQ2			FCMREF	TIM4_2_CLK	TIM6_TRIGB	TIMA_10_PWM3		EMB_PORT4			SDIO2_D4		ETH_MII_CRS	EXMC_ALE			EVENTOUT		I2S3_EXCK					FG2
44	-	PH3	ADC3_IN17	EIRQ3													ETH_MII_COL	EXMC_CE0			EVENTOUT							FG2
45	-	PH4	ADC3_IN18	EIRQ4												USBHS_ULPI_NXT					EVENTOUT							FG2
46	-	PH5	ADC3_IN19	EIRQ5														EXMC_WE			EVENTOUT	TIM2_1_CLKB		SPI5_NSS0				FG2
47	26	PA3	ADC123_IN3+PGA123_VSS+CMP1_INP4	EIRQ3				TIM4_2_OVL	TIM6_6_PWMB	TIMA_2_PWM4	TIMA_5_PWM2/TIMA_5_CLKB	TIMA_5_PWM4			SDIO2_D7	USBHS_ULPI_D0	ETH_MII_COL			EVNTP103	EVENTOUT	TIM2_1_PWMB/TRIGB				USART2_RX		FG2
48	27	AVSS																										
49	28	AVCC																										
50	29	PA4	ADC12_IN4+DAC1_OUT1+CMP2_INP3	EIRQ4				TIM4_2_OWH	TIM6_7_PWMA		TIMA_9_PWM1/TIMA_9_CLKA	TIMA_8_TRIG	USART5_CK	KEYOUT0				USBHS_SOF	DVP_HSYNC	EVNTP104	EVENTOUT	TIM2_4_CLKA	I2S1_EXCK		SPI1_NSS0	USART2_CK		FG1
51	30	PA5	ADC12_IN5+DAC1_OUT2+CMP2_INP4	EIRQ5				TIM4_2_OWL	TIM6_7_PWMB	TIMA_2_PWM1/TIMA_2_CLKA	TIMA_9_PWM2/TIMA_9_CLKB	TIMA_2_TRIG		KEYOUT1		USBHS_ULPI_CK				EVNTP105	EVENTOUT	TIM4_2_OUL	I2S1_MCK					FG1
52	31	PA6	ADC12_IN6+PGA_4+CMP1_INP2	EIRQ6							TIMA_3_PWM1/TIMA_3_CLKA	EMB_PORT2		KEYOUT2	SDIO1_CMD	TIM2_4_PWMA/TRIGA		EXMC_AD D26	DVP_PIXCLK	EVNTP106	EVENTOUT	TIM2_4_CLKB						FG1
53	32	PA7	ADC12_IN7+PGA4_VSS+CMP123_INM3	EIRQ7				TIM4_1_OUL	TIM6_1_PWMB	TIMA_7_PWM1/TIMA_7_CLKA	TIMA_3_PWM2/TIMA_3_CLKB	EMB_PORT3		KEYOUT3	SDIO2_WP	TIM2_4_PWMB/TRIGB	ETH_MII_RMII_RXDV	EXMC_AD D27		EVNTP107	EVENTOUT	TIM4_2_OUL						FG1

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
54	33	PC4	ADC12_IN14 +DAC2_OUT1 +CMP2_INM4	EIRQ4				TIM4_2_OUH	TIM6_5_PWMA		TIMA_9_PWM3	TIMA_7_TRIG	USART1_CK		SDIO2_CD		ETH_MII_RMII_RXD0	EXMC_AD D28		EVNTP304	EVENTOUT	TIM2_4_PWMA/TRIGA		SPI1_NSS1				FG1
55	34	PC5	ADC12_IN15 +DAC2_OUT2 +CMP3_INM4	EIRQ5				TIM4_2_OUL	TIM6_5_PWMB		TIMA_9_PWM4	EMB_PORT1			SDIO2_CMD		ETH_MII_RMII_RXD1	EXMC_AD D29		EVNTP305	EVENTOUT	TIM2_4_PWMB/TRIGB		SPI1_NSS2				FG1
56	35	PB0	ADC12_IN8+ CMP3_INP2	EIRQ0				TIM4_1_OVL	TIM6_2_PWMB	TIMA_7_PWM2/TIMA_7_CLKB	TIMA_3_PWM3		USART4_CK	KEYOUT4	SDIO2_CMD	USBHS_ULPI_D1	ETH_MII_RXD2			EVNTP200	EVENTOUT	TIM4_2_OVL		SPI1_NSS3				FG1
57	36	PB1	ADC12_IN9+ CMP3_INP3	EIRQ1+WKUP0_1				TIM4_1_OWL	TIM6_3_PWMB	TIMA_7_PWM3	TIMA_3_PWM4			KEYOUT5	SDIO2_D3	USBHS_ULPI_D2	ETH_MII_RXD3			EVNTP201	EVENTOUT	TIM4_2_OWL	I2S2_EXCK	QSPI_NSS				FG1
58	37	PB2	PVD2EXINP	EIRQ2+WKUP0_2			VCOUT		TIM6_TRIGB	TIMA_7_PWM4	TIMA_9_TRIG	EMB_PORT1	USART2_CK		SDIO2_D2			EXMC_CLE	DVP_PIXCLK	EVNTP202	EVENTOUT		I2S2_MCK	QSPI_IO3				FG1
59	-	PF11		EIRQ11				TIM4_2_PCT		TIMA_4_PWM1/TIMA_4_CLKA			USART2_CTS					EXMC_OE	DVP_DATA12		EVENTOUT				SPI5_MOSI			FG1
60	-	PF12		EIRQ12				TIM4_2_ADSM		TIMA_4_PWM2/TIMA_4_CLKB			USART2_RTS					EXMC_AD D6			EVENTOUT							FG1
61	-	VSS																										
62	-	VCC																										
63	-	PF13		EIRQ13					TIM6_1_PWMA	TIMA_4_PWM3		TIMA_10_TRIG						EXMC_AD D7			EVENTOUT			SPI6_NSS3				FG2
64	-	PF14		EIRQ14					TIM6_1_PWMB	TIMA_4_PWM4								EXMC_AD D8			EVENTOUT			SPI6_NSS2				FG2
65	-	PF15		EIRQ15					TIM6_2_PWMA			TIMA_12_TRIG	USART7_RTS					EXMC_AD D9			EVENTOUT			SPI6_NSS1				FG2
66	-	PG0		EIRQ0					TIM6_2_PWMB		TIMA_12_PWM3		USART7_CTS					EXMC_AD D10			EVENTOUT							FG2
67	-	PG1		EIRQ1					TIM6_TRIGA		TIMA_12_PWM4		USART7_CK					EXMC_AD D11			EVENTOUT							FG2
68	38	PE7		EIRQ7			ADTRG1	TIM4_1_CLK	TIM6_TRIGB	TIMA_1_TRIG	TIMA_3_PWM3		USART1_CK					EXMC_DAT A4			EVENTOUT			SPI4_NSS1				FG2
69	39	PE8		EIRQ8			CTCREF	TIM4_1_OUL	TIM6_1_PWMB	TIMA_7_PWM1/TIMA_7_CLKA	TIMA_3_PWM4							EXMC_DAT A5			EVENTOUT			SPI4_NSS2				FG2
70	40	PE9		EIRQ9			ADTRG3	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA								EXMC_DAT A6			EVENTOUT			SPI4_NSS3				FG2
71	-	VSS																										
72	-	VCC																										
73	41	PE10	CMP1_INP3	EIRQ10				TIM4_1_OVL	TIM6_2_PWMB	TIMA_7_PWM2/TIMA_7_CLKB		TIMA_3_TRIG						EXMC_DAT A7			EVENTOUT							FG3
74	42	PE11		EIRQ11				TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB	TIMA_3_PWM1/TIMA_3_CLKA					USBHS_ULPI_D7		EXMC_DAT A8			EVENTOUT							FG3
75	43	PE12	CMP4_INM3	EIRQ12				TIM4_1_OWL	TIM6_3_PWMB	TIMA_7_PWM3	TIMA_3_PWM2/TIMA_3_CLKB					USBHS_ULPI_CK		EXMC_DAT A9			EVENTOUT	TIM2_2_CLKA		SPI1_NSS1				FG3
76	44	PE13	CMP4_INM4	EIRQ13				TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_3_PWM3					USBHS_ULPI_D0		EXMC_DAT A10			EVENTOUT	TIM2_2_CLKB	I2S4_SDIN	SPI1_NSS2				FG3
77	45	PE14	CMP4_INP3	EIRQ14				TIM4_1_CLK	TIM6_4_PWMA	TIMA_1_PWM4	TIMA_3_PWM4				SDIO1_CD	USBHS_ULPI_D1		EXMC_DAT A11			EVENTOUT	TIM2_2_PWMA/TRIGA	I2S4_EXCK	SPI1_NSS3				FG3
78	46	PE15	CMP4_INP4	EIRQ15				TIM4_1_PCT	TIM6_TRIGA	TIMA_7_PWM4	TIMA_5_TRIG	EMB_PORT2	USART10_CK		SDIO1_WP	USBHS_ULPI_D2		EXMC_DAT A12			EVENTOUT	TIM2_2_PWMB/TRIGB	I2S4_MCK					FG3
79	47	PB10		EIRQ10			ADTRG2	TIM4_2_OVH	TIM6_4_PWMB	TIMA_2_PWM3	TIMA_11_PWM4				SDIO1_D7	USBHS_ULPI_D3	ETH_MII_RXER			EVNTP210	EVENTOUT		I2S3_EXCK	QSPI_IO2	SPI2_SCK			FG3
80	48	PB11		EIRQ11				TIM4_1_ADSM		TIMA_2_PWM4		EMB_PORT2				USBHS_ULPI_D4	ETH_MII_RMII_TXEN			EVNTP211	EVENTOUT							FG3
81	49	VCAP_1																										
-	-	VSS																										
82	50	VCC																										

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
83	-	PH6		EIRQ6						TIMA_2_PWM3			USART5_CTS				ETH_MII_RXD2	EXMC_CE1	DVP_DATA8		EVENTOUT	TIM2_2_PWMA/TRIGA						FG2
84	-	PH7		EIRQ7						TIMA_2_PWM2/TIMA_2_CLKB			USART5_RTS				ETH_MII_RXD3	EXMC_ALE	DVP_DATA9		EVENTOUT							FG2
85	-	PH8		EIRQ8					TIM6_3_PWMA	TIMA_2_PWM3			USART5_CK					EXMC_DATA16	DVP_HSYNC		EVENTOUT			SPI5_NSS0				FG2
86	-	PH9		EIRQ9					TIM6_3_PWMB	TIMA_2_PWM4								EXMC_DATA17	DVP_DATA0		EVENTOUT	TIM2_2_PWMB/TRIGB		SPI5_NSS1				FG2
87	-	PH10		EIRQ10					TIM6_4_PWMA		TIMA_5_PWM1/TIMA_5_CLKA							EXMC_DATA18	DVP_DATA1		EVENTOUT			SPI5_NSS2				FG2
88	-	PH11		EIRQ11					TIM6_4_PWMB		TIMA_5_PWM2/TIMA_5_CLKB							EXMC_DATA19	DVP_DATA2		EVENTOUT			SPI5_NSS3				FG2
89	-	PH12		EIRQ12							TIMA_5_PWM3							EXMC_DATA20	DVP_DATA3		EVENTOUT							FG2
90	-	VSS																										
91	-	VCC																										
92	51	PB12		EIRQ12			VCOUT1	TIM4_2_OVL	TIM6_TRIGB	TIMA_7_PWM4	TIMA_5_TRIG	EMB_PORT2	USART3_CK		SDIO2_D1	USBHS_ULPI_D5	ETH_MII_RMII_TXD0	USBHS_ID		EVNTP212	EVENTOUT		I2S3_MCK	QSPI_IO1	SPI2_NSS0				FG1
93	52	PB13		EIRQ13			VCOUT2	TIM4_1_OUL	TIM6_1_PWMB	TIMA_7_PWM1/TIMA_7_CLKA			USART3_CTS		SDIO2_D0	USBHS_ULPI_D6	ETH_MII_RMII_TXD1	USBHS_VBUS		EVNTP213	EVENTOUT			QSPI_IO0				FG1
94	53	PB14	USBHS_DM	EIRQ14			VCOUT3	TIM4_1_OVL	TIM6_2_PWMB	TIMA_7_PWM2/TIMA_7_CLKB			USART3_RTS		SDIO1_D6	TIM2_2_PWMA/TRIGA				EVNTP214	EVENTOUT	TIM4_2_OVL	I2S1_SDIN	QSPI_SCK				FG1
95	54	PB15	USBHS_DP	EIRQ15			RTC_OUT	TIM4_1_OWL	TIM6_3_PWMB	TIMA_7_PWM3	TIMA_6_TRIG	EMB_PORT4	USART3_CK		SDIO1_CK	TIM2_2_PWMB/TRIGB				EVNTP215	EVENTOUT	TIM4_2_OWL						FG1
96	55	PD8		EIRQ8			VCOUT4	TIM4_3_OUL	TIM6_1_PWMB		TIMA_6_PWM1/TIMA_6_CLKA		USART1_CTS	KEYOUT7		USBHS_DRVVBUS		EXMC_DATA13		EVNTP408	EVENTOUT	TIM2_2_CLKA		QSPI_IO0				FG1
97	56	PD9		EIRQ9			VCOUT3	TIM4_3_OVL	TIM6_2_PWMB	TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM2/TIMA_6_CLKB	EMB_PORT3	USART1_RTS	KEYOUT6		USBHS_ULPI_D4		EXMC_DATA14		EVNTP409	EVENTOUT	TIM2_2_CLKB		QSPI_IO1				FG1
98	57	PD10		EIRQ10			CAN2_TST_SAMPLE	TIM4_3_OWL	TIM6_3_PWMB	TIMA_2_PWM2/TIMA_2_CLKB	TIMA_6_PWM3		USART3_CK	KEYOUT5				EXMC_DATA15		EVNTP410	EVENTOUT	TIM2_2_PWMA/TRIGA	I2S2_EXCK	QSPI_IO2				FG1
99	58	PD11		EIRQ11			CAN2_TST_CLOCK	TIM4_3_CLK	TIM6_TRIGB		TIMA_6_PWM4	TIMA_11_TRIG	USART3_CTS	KEYOUT4				EXMC_AD D16		EVNTP411	EVENTOUT	TIM2_2_PWMB/TRIGB	I2S2_MCK	QSPI_IO3				FG1
100	59	PD12		EIRQ12				TIM4_1_ADSM	TIM6_4_PWMB	TIMA_4_PWM1/TIMA_4_CLKA	TIMA_11_PWM1/TIMA_11_CLKA		USART3_RTS					EXMC_AD D17		EVNTP412	EVENTOUT							FG3
101	60	PD13		EIRQ13				TIM4_1_PCT	TIM6_4_PWMB	TIMA_4_PWM2/TIMA_4_CLKB	TIMA_11_PWM2/TIMA_11_CLKB		USART9_RTS					EXMC_AD D18		EVNTP413	EVENTOUT							FG3
102	-	VSS																										
103	-	VCC																										
104	61	PD14		EIRQ14			ADTRG1			TIMA_4_PWM3	TIMA_11_PWM3		USART9_CTS					EXMC_DATA0		EVNTP414	EVENTOUT		I2S4_EXCK					FG3
105	62	PD15		EIRQ15			ADTRG2			TIMA_4_PWM4	TIMA_11_PWM4		USART9_CK					EXMC_DATA1		EVNTP415	EVENTOUT		I2S4_MCK					FG3
106	-	PG2		EIRQ2			ADTRG3											EXMC_AD D12			EVENTOUT							FG3
107	-	PG3		EIRQ3								TIMA_9_TRIG						EXMC_AD D13	DVP_DATA10		EVENTOUT							FG3
108	-	PG4		EIRQ4						TIMA_9_PWM1/TIMA_9_CLKA								EXMC_AD D14	EXMC_AD D16		EVENTOUT							FG3
109	-	PG5		EIRQ5						TIMA_9_PWM2/TIMA_9_CLKB								EXMC_AD D15	EXMC_AD D17		EVENTOUT							FG3
110	-	PG6		EIRQ6						TIMA_9_PWM3								EXMC_RB0	DVP_DATA12		EVENTOUT							FG3

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
111	-	PG7		EIRQ7						TIMA_9_PWM4			USART8_CK					EXMC_RB13	DVP_DATA		EVENTOUT		I2S1_EXCK			USART6_CK		FG3
112	-	PG8		EIRQ8									USART8_RTS				ETH_PPS_OUT	EXMC_CLK			EVENTOUT		I2S1_SDIN		SPI6_NSS0	USART6_RTS		FG3
113	-	VSS																										
114	-	VCC																										
115	63	PC6		EIRQ6			CTCREF	TIM4_2_OUH		TIMA_3_PWM1/TIMA_3_CLKA	TIMA_11_PWM4	TIM6_5_PWMA		KEYOUT3	SDIO1_D6				DVP_DATA0	EVNTP306	EVENTOUT	TIM4_3_ADSM	I2S1_MCK	QSPI_SCK		USART6_TX		FG3
116	64	PC7		EIRQ7				TIM4_2_OVH	TIM6_TRIGD	TIMA_3_PWM2/TIMA_3_CLKB	TIMA_11_PWM3	TIM6_6_PWMA		KEYOUT2	SDIO1_D7			I2S2_EXCK	DVP_DATA1	EVNTP307	EVENTOUT	TIM4_2_CLK	I2S2_MCK	QSPI_NSS		USART6_RX		FG3
117	65	PC8		EIRQ8				TIM4_2_OWH	TIM6_8_PWMA	TIMA_3_PWM3	TIMA_11_PWM2/TIMA_11_CLKB	TIM6_7_PWMA	USART8_CK	KEYOUT1	SDIO1_D0				DVP_DATA2	EVNTP308	EVENTOUT		I2S2_MCK			USART6_CK		FG2
118	66	PC9		EIRQ9			MCO_2	TIM4_2_OWL	TIM6_8_PWMB	TIMA_3_PWM4	TIMA_11_PWM1/TIMA_11_CLKA	TIM6_8_PWMA		KEYOUT0	SDIO1_D1	USBFS_DRVVBUS		EXMC_CLE	DVP_DATA3	EVNTP309	EVENTOUT		I2S3_EXCK					FG2
119	67	PA8		EIRQ8+WKUP2_0			MCO_1	TIM4_1_OUH	TIM6_1_PWMA	TIMA_1_PWM1/TIMA_1_CLKA		TIMA_7_TRIG	USART4_CK		SDIO1_D1	USBFS_SOF				EVNTP108	EVENTOUT	TIM2_1_CLKA	I2S3_MCK			USART1_CK		FG2
120	68	PA9		EIRQ9+WKUP2_1				TIM4_1_OVH	TIM6_2_PWMA	TIMA_1_PWM2/TIMA_1_CLKB		TIMA_2_TRIG			SDIO1_D2	USBFS_VBUS			DVP_DATA0	EVNTP109	EVENTOUT	TIM2_1_CLKB	I2S3_SDIN			USART1_TX		FG2
121	69	PA10		EIRQ10+WKUP2_2				TIM4_1_OWH	TIM6_3_PWMA	TIMA_1_PWM3	TIMA_5_TRIG	TIMA_11_TRIG			SDIO1_CD	USBFS_ID			DVP_DATA1	EVNTP110	EVENTOUT	TIM2_1_PWMA/TRIGA				USART1_RX		FG2
122	70	PA11	USBFS_DM	EIRQ11+WKUP2_3				TIM4_1_CLK	TIM6_4_PWMA	TIMA_1_PWM4		EMB_PORT1	USART4_CTS		SDIO2_CD					EVNTP111	EVENTOUT	TIM2_1_PWMA/TRIGA				USART1_CTS		FG2
123	71	PA12	USBFS_DP	EIRQ12+WKUP3_0				TIM4_3_OWL	TIM6_TRIGA	TIMA_1_TRIG	TIMA_6_PWM1/TIMA_6_CLKA		USART4_RTS		SDIO2_WP					EVNTP112	EVENTOUT	TIM4_1_CLK				USART1_RTS		FG2
124	72	PA13		EIRQ13	JTMS_SWDIO				TIM6_TRIGD	TIMA_8_PWM1/TIMA_8_CLKA	TIMA_6_PWM2/TIMA_6_CLKB				SDIO2_D3					EVNTP113	EVENTOUT			SPI2_NSS1				FG2
125	73	VCAP_2																										
126	74	VSS																										
127	75	VCC																										
128	-	PH13		EIRQ13				TIM4_2_OUL	TIM6_5_PWMB	TIMA_6_PWM1/TIMA_6_CLKA								EXMC_DATA21			EVENTOUT							FG1
129	-	PH14		EIRQ14				TIM4_2_OVL	TIM6_6_PWMB	TIMA_6_PWM2/TIMA_6_CLKB								EXMC_DATA22	DVP_DATA4		EVENTOUT							FG1
130	-	PH15		EIRQ15				TIM4_2_OWL	TIM6_7_PWMB									EXMC_DATA23	DVP_DATA11		EVENTOUT							FG1
131	-	PI0		EIRQ0							TIMA_5_PWM4							EXMC_DATA24	DVP_DATA13		EVENTOUT			SPI2_NSS0				FG1
132	-	PI1		EIRQ1								TIMA_8_TRIG						EXMC_DATA25	DVP_DATA8		EVENTOUT							FG1
133	-	PI2		EIRQ2					TIM6_8_PWMB									EXMC_DATA26	DVP_DATA9		EVENTOUT		I2S1_SDIN					FG1
134	-	PI3		EIRQ3				TIM4_2_CLK	TIM6_TRIGD									EXMC_DATA27	DVP_DATA10		EVENTOUT							FG1
135	-	VSS																										
136	-	VCC																										
137	76	PA14		EIRQ14+WKUP3_2	JTCK_SWCLK			TIM4_2_ADSM	TIM6_TRIGC	TIMA_8_PWM2/TIMA_8_CLKB	TIMA_6_PWM3	TIMA_4_TRIG	USART2_RTS		SDIO2_D2					EVNTP114	EVENTOUT		I2S1_EXCK	SPI2_NSS2					FG1
138	77	PA15		EIRQ15+WKUP3_3	JTDI			TIM4_2_PCT	TIM6_TRIGA	TIMA_2_PWM1/TIMA_2_CLKA	TIMA_6_PWM4	TIMA_2_TRIG	USART2_CTS		SDIO2_D1					EVNTP115	EVENTOUT		I2S1_MCK	SPI2_NSS3	SPI1_NSS0				FG1

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
139	78	PC10		EIRQ10			CAN1_TST_SAMPLE	TIM4_3_OUH	TIM6_5_PWMA	TIMA_8_PWM3	TIMA_5_PWM1/TIMA_5_CLKA	TIMA_9_TRIG	USART2_CK		SDIO1_D2				DVP_DATA8	EVNTP310	EVENTOUT		I2S2_CK	SPI1_NSS1	SPI3_SCK	USART4_TX		FG3
140	79	PC11		EIRQ11			CAN1_TST_CLOCK	TIM4_3_OVH	TIM6_6_PWMA	TIMA_8_PWM4	TIMA_5_PWM2/TIMA_5_CLKB	TIMA_9_PWM1/TIMA_9_CLKA		KEYOUT0	SDIO1_D3				DVP_DATA4	EVNTP311	EVENTOUT	TIM2_4_PWMA/TRIGA	I2S2_SDIN	SPI1_NSS2	SPI3_MISO	USART4_RX		FG3
141	80	PC12		EIRQ12				TIM4_3_OWH	TIM6_7_PWMA	TIMA_4_TRIG	TIMA_5_PWM3	TIMA_9_PWM2/TIMA_9_CLKB	USART3_CK	KEYOUT1	SDIO1_CK				DVP_DATA9	EVNTP312	EVENTOUT	TIM2_4_PWMB/TRIGB	I2S2_SD	SPI1_NSS3	SPI3_MOSI	USART5_TX		FG3
142	81	PD0		EIRQ0			VCOUT	TIM4_3_OUL	TIM6_5_PWMB		TIMA_5_PWM4	TIMA_9_PWM3	USART8_CTS	KEYOUT2				EXMC_DATA2		EVNTP400	EVENTOUT	TIM2_4_CLKA						FG3
143	82	PD1		EIRQ1				TIM4_3_OVL	TIM6_6_PWMB	TIMA_3_TRIG	TIMA_12_PWM1/TIMA_12_CLKA	TIMA_9_PWM4	USART8_RTS	KEYOUT3				EXMC_DATA3		EVNTP401	EVENTOUT	TIM2_4_CLKB						FG3
144	83	PD2		EIRQ2			VCOUT4	TIM4_3_OWL	TIM6_7_PWMB	TIMA_2_PWM4	TIMA_12_PWM2/TIMA_12_CLKB	TIMA_3_TRIG	USART7_CTS	KEYOUT4	SDIO1_CMD				DVP_DATA11	EVNTP402	EVENTOUT					USART5_RX		FG3
145	84	PD3		EIRQ3			VCOUT1				TIMA_12_PWM3	TIMA_6_TRIG	USART5_CTS	KEYOUT5				EXMC_CLK	DVP_DATA5	EVNTP403	EVENTOUT				SPI2_SCK	USART2_CTS		FG3
146	85	PD4		EIRQ4			VCOUT2			TIMA_6_PWM1/TIMA_6_CLKA	TIMA_12_PWM4	EMB_PORT4	USART5_RTS	KEYOUT6				EXMC_OE	DVP_DATA12	EVNTP404	EVENTOUT					USART2_RTS		FG2
147	86	PD5		EIRQ5			VCOUT3			TIMA_6_PWM2/TIMA_6_CLKB			USART7_RTS	KEYOUT7				EXMC_WE		EVNTP405	EVENTOUT			SPI6_NSS1		USART2_TX		FG2
148	-	VSS																										
149	-	VCC																										
150	87	PD6		EIRQ6			ADTRG1	TIM4_2_CLK	TIM6_TRIGC	TIMA_6_PWM3			USART7_CK					EXMC_RB0	DVP_DATA10	EVNTP406	EVENTOUT		I2S2_SD	SPI6_NSS2	SPI3_MOSI	USART2_RX		FG2
151	88	PD7		EIRQ7			ADTRG2		TIM6_TRIGD	TIMA_6_PWM4		EMB_PORT1	USART5_CK					EXMC_CE0		EVNTP407	EVENTOUT			SPI6_NSS3		USART2_CK		FG2
152	-	PG9		EIRQ9			ADTRG3				TIMA_12_PWM1/TIMA_12_CLKA		USART4_CK					EXMC_CE1	DVP_VSYNC		EVENTOUT							FG2
153	-	PG10		EIRQ10				TIM4_3_ADSM	TIM6_8_PWMA		TIMA_12_PWM2/TIMA_12_CLKB		USART4_CTS					EXMC_CE2	DVP_DATA2		EVENTOUT							FG2
154	-	PG11		EIRQ11				TIM4_3_PCT	TIM6_8_PWMB	TIMA_8_PWM1/TIMA_8_CLKA			USART4_RTS				ETH_MII_RMII_TXEN	EXMC_RB7	DVP_DATA3		EVENTOUT							FG2
155	-	PG12		EIRQ12						TIMA_8_PWM2/TIMA_8_CLKB			USART6_RTS					EXMC_CE3			EVENTOUT							FG2
156	-	PG13		EIRQ13						TIMA_8_PWM3			USART6_CTS				ETH_MII_RMII_TXD0	EXMC_AD24	DVP_VSYNC		EVENTOUT							FG2
157	-	PG14		EIRQ14				TIM4_3_ADSM	TIM6_4_PWMB	TIMA_8_PWM4							ETH_MII_RMII_TXD1	EXMC_AD25	DVP_DATA2		EVENTOUT		I2S3_EXCK					FG2
158	-	VSS																										
159	-	VCC																										
160	-	PG15		EIRQ15				TIM4_3_PCT	TIM6_4_PWMA			TIMA_5_TRIG	USART6_CTS					EXMC_BAA	DVP_DATA13		EVENTOUT		I2S3_MCK					FG1
161	89	PB3		EIRQ3+WKUP0_3	JTDO_SWO		FCMREF	TIM4_3_CLK	TIM6_TRIGC	TIMA_2_PWM2/TIMA_2_CLKB	TIMA_12_PWM1/TIMA_12_CLKA				SDIO2_D0					EVNTP203	EVENTOUT							FG1
162	90	PB4		EIRQ4+WKUP1_0	NJTRST			TIM4_3_OWL	TIM6_3_PWMB	TIMA_3_PWM1/TIMA_3_CLKA	TIMA_12_PWM2/TIMA_12_CLKB				SDIO1_D0				DVP_DATA13	EVNTP204	EVENTOUT		I2S2_SDIN					FG1
163	91	PB5		EIRQ5+WKUP1_1			ADTRG3	TIM4_3_OWH	TIM6_3_PWMA	TIMA_3_PWM2/TIMA_3_CLKB	TIMA_12_PWM3	TIMA_10_TRIG			SDIO1_D3	USBHS_ULPI_D7	ETH_PPS_OUT	EXMC_ALE	DVP_DATA10	EVNTP205	EVENTOUT		I2S4_EXCK	SPI3_NSS3				FG1
164	92	PB6		EIRQ6+WKUP1_2			ADTRG2	TIM4_3_OVL	TIM6_2_PWMB	TIMA_4_PWM1/TIMA_4_CLKA	TIMA_12_PWM4	TIMA_10_PWM1/TIMA_10_CLKA			SDIO2_CK		ETH_MII_TXCLK	EXMC_CE1	DVP_DATA5	EVNTP206	EVENTOUT		I2S4_MCK	SPI3_NSS2				FG1
165	93	PB7		EIRQ7+WKUP1_3			ADTRG1	TIM4_3_OVH	TIM6_2_PWMA	TIMA_4_PWM2/TIMA_4_CLKB		TIMA_10_PWM2/TIMA_10_CLKB			SDIO1_D0		ETH_MII_TXER	EXMC_ADV	DVP_VSYNC	EVNTP207	EVENTOUT		I2S2_EXCK	SPI3_NSS1				FG1
166	94	PI13/MD											USART3_TX															

LQFP 176	LQFP 100	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	Func4	Func5	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
						GPO		TIM4	TIM6	TIMA	TIMA	EMB, TIM6, TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2, TIM4	I2S	SPI, QSPI	SPI	USART		Communication Function Group
167	95	PB8		EIRQ8				TIM4_3_OUL	TIM6_1_PWMB	TIMA_4_PWM3		TIMA_10_PWM3	USART1_CK	KEYOUT7	SDIO1_D4	USBFS_DRVVBUS	ETH_MII_TXD3		DVP_DATA6	EVNTP208	EVENTOUT	TIM2_3_PWMA/TRIGA	I2S2_MCK	SPI2_NSS0				FG1
168	96	PB9		EIRQ9				TIM4_3_OUH	TIM6_1_PWMA	TIMA_4_PWM4	TIMA_6_TRIG	TIMA_10_PWM4	USART1_CTS	KEYOUT6	SDIO1_D5		ETH_MII_TXD2		DVP_DATA7	EVNTP209	EVENTOUT	TIM2_3_PWMB/TRIGB	I2S2_SDIN	SPI2_NSS1	SPI2_NSS0			FG1
169	97	PE0		EIRQ0			MCO_1	TIM4_3_PCT		TIMA_4_TRIG		TIMA_2_TRIG	USART1_RTS				ETH_MII_RMII_TXD1	EXMC_CE4	DVP_DATA2		EVENTOUT	TIM2_3_CLKA		SPI2_NSS2		USART8_RX		FG1
170	98	PE1		EIRQ1			MCO_2	TIM4_3_CLK	TIM6_TRIGC			TIMA_12_TRIG					ETH_MII_RMII_TXD0	EXMC_CE5	DVP_DATA3		EVENTOUT	TIM2_3_CLKB		SPI2_NSS3		USART8_TX		FG1
171	-	PI12		EIRQ12														EXMC_CLE										FG1
-	99	VSS																										
172	100	VCC																										
173	-	PI4		EIRQ4						TIMA_1_PWM1/TIMA_1_CLKA		EMB_PORT4						EXMC_CE6	DVP_DATA5		EVENTOUT							FG1
174	-	PI5		EIRQ5				TIM4_2_OUH	TIM6_5_PWMA	TIMA_1_PWM2/TIMA_1_CLKB								EXMC_CE7	DVP_VSYNC		EVENTOUT							FG1
175	-	PI6		EIRQ6				TIM4_2_OVH	TIM6_6_PWMA	TIMA_1_PWM3								EXMC_DATA28	DVP_DATA6		EVENTOUT							FG1
176	-	PI7		EIRQ7				TIM4_2_OWH	TIM6_7_PWMA	TIMA_1_PWM4								EXMC_DATA29	DVP_DATA7		EVENTOUT							FG1

Note:

– In the above table, Func32~63 are mainly serial communication functions (including USART, SPI, I2C, I2S, CAN), which are divided into three groups of FunctionGroup, referred to as FG1, FG2, FG3. For details, please refer to Table 2-2 .

Table 2-2 Func32~63 table

	Func32	Func33	Func34	Func35	Func36	Func37	Func38	Func39	Func40	Func41	Func42	Func43	Func44	Func45	Func46	Func47
FG1	USART1_TX	USART1_RX	USART2_TX	USART2_RX	USART3_TX	USART3_RX	USART4_TX	USART4_RX	SPI1_SCK	SPI1_MOSI	SPI1_MISO	SPI2_SCK	SPI2_MOSI	SPI2_MISO	SPI3_SCK	SPI3_MOSI
FG2	USART4_TX	USART4_RX	USART5_TX	USART5_RX	USART6_TX	USART6_RX	USART7_TX	USART7_RX	SPI4_SCK	SPI4_MOSI	SPI4_MISO	SPI5_SCK	SPI5_MOSI	SPI5_MISO	SPI6_SCK	SPI6_MOSI
FG3	USART3_TX	USART3_RX	USART8_TX	USART8_RX	USART9_TX	USART9_RX	USART10_TX	USART10_RX	SPI1_SCK	SPI1_MOSI	SPI1_MISO	SPI4_SCK	SPI4_MOSI	SPI4_MISO	SPI4_NSS0	SPI1_NSS0

	Func48	Func49	Func50	Func51	Func52	Func53	Func54	Func55	Func56	Func57	Func58	Func59	Func60	Func61	Func62	Func63
FG1	SPI3_MISO	SPI3_NSS0	I2C1_SDA	I2C1_SCL	I2C3_SDA	I2C3_SCL	I2S1_CK	I2S1_WS	I2S1_SD	I2S2_CK	I2S2_WS	I2S2_SD	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX
FG2	SPI6_MISO	SPI6_NSS0	I2C2_SDA	I2C2_SCL	I2C4_SDA	I2C4_SCL	I2C5_SDA	I2C5_SCL		I2S3_CK	I2S3_WS	I2S3_SD	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX
FG3	I2C1_SDA	I2C1_SCL	I2C2_SDA	I2C2_SCL	I2C6_SDA	I2C6_SCL	I2S1_CK	I2S1_WS	I2S1_SD	I2S4_CK	I2S4_WS	I2S4_SD	CAN1_TX	CAN1_RX	CAN2_TX	CAN2_RX

Table 2-3 Port configuration

Package	Port Group	Bits																Pin Count Total	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
LQFP176	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	142
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortF	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortG	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortI	-	-	o	o	o	o	o	o	o	o	o	o	o	o	o	o	14	
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	2	
	PortI	-	-	o	-	-	-	-	-	-	-	-	-	-	-	-	-	1	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Table 2-4 General Functional Specifications

Port		Pull up	Open-drain output	Driving capacity	5V withstand voltage
PortA	PA3~PA5 PA7~PA10 PA13~PA15	Support	Support	Low Medium High	Support
	PA0,PA1,PA2, PA6,PA11,PA12	Support	Support	Low Medium High	not support
PortB	PB0~PB13	Support	Support	Low Medium High	Support
	PB14,PB15	Support	Support	Low Medium High	not support
PortC	PC0~PC15	Support	Support	Low Medium High	Support
PortD	PD0~PD15	Support	Support	Low Medium High	Support
PortE	PE0~PE15	Support	Support	Low Medium High	Support
PortF	PF0~PF15	Support	Support	Low Medium High	Support
PortG	PG0~PG15	Support	Support	Low Medium High	Support
PortH	PH0~PH15	Support	Support	Low Medium High	Support
PortI	PI0~PI13	Support	Support	Low Medium High	Support

Note:

– When used as an analog function, the input voltage must not be higher than VREFH/AVCC.

2.3 Pin function description

Table 2-5 Pin function description

Categories	Functional name	I/O	Note
Power	VCC	I	Power supply
	VSS	I	Source ground
	VCAP_x (x=1~2)	-	Core voltage
	AVCC	I	Analog power
	VREFH	I	Analog reference voltage
	AVSS	I	analog power ground
	VREFL	I	Analog reference voltage
	AVSS_VREFL	I	Analog power ground, reference ground shared pin
	VBAT	I	Backup battery power
System	NRST	I	Reset terminal, low effective
	MD	I	Mode terminal
PVD	PVD2EXINP	I	PVD2 external input compare voltage
Clock	XTAL_IN	I	External master clock oscillator interface
	XTAL_OUT	O	
	XTAL32_IN	I	External sub-clock (32K) oscillator interface
	XTAL32_OUT	O	
	MCO_x (x=1~2)	O	Internal clock output
GPIO	GPIOxy (x=A~I y=0~15)	IO	General input/output
EVENTOUT	EVENTOUT	O	Cortex-M4 CPU event output
EIRQ	EIRQx (x=0~15)	I	Shielded external interrupt
	WKUPx_y (x=0~3 y=0~3)	I	PowerDown mode external wake-up input
Event Port	EVNTPxy (x=1~4 y=0~15)	IO	Event port input and output function
Key	KEYOUTx(x=0~7)	O	KEYSCAN scan output signal
JTAG/SWD	JTCK_SWCLK	I	Online debugging interface
	JTMS_SWDIO	IO	
	JTDO_TRACESWO	O	
	JTDI	I	
	NJTRST	I	
TRACE	TRACECLK	O	Trace debug sync clock output
	TRACEDx (x=0~3)	O	Trace debug data output
FCM	FCMREF	I	External reference clock input for clock frequency measurement
RTC	RTC_OUT	O	1Hz clock output
	RTCICx (x=0~1)	I	Timestamp event input
Timer2 (x=1~4)	TIM2_x_CLKA	I	Counting clock port input
	TIM2_x_CLKB	I	Counting clock port input

Categories	Functional name	I/O	Note
	TIM2_x_PWMA/TRIGA	IO	External Event Trigger Input or PWM Port Output
	TIM2_x_PWMB/TRIGB	IO	External Event Trigger Input or PWM Port Output
Timer4 (x=1~3)	TIM4_x_CLK	I	Counting clock port input
	TIM4_x_OUH	IO	PWM port U-phase output
	TIM4_x_OUL	IO	PWM port U-phase output
	TIM4_x_OVH	IO	PWM port V-phase output
	TIM4_x_OVL	IO	PWM port V-phase output
	TIM4_x_OWH	IO	PWM port W-phase output
	TIM4_x_OWL	IO	PWM port W-phase output
	TIM4_x_ADSM	O	Dedicated event output monitoring
	TIM4_x_PCT	O	PWM period output monitoring
Timer6 (x=1~8)	TIM6_TRIGA	I	External event trigger A input
	TIM6_TRIGB	I	External event trigger B input
	TIM6_TRIGC	I	External event trigger C input
	TIM6_TRIGD	I	External event trigger D input
	TIM6_x_PWMA	IO	External Event Trigger Input or PWM Port Output
	TIM6_x_PWMB	IO	External Event Trigger Input or PWM Port Output
TimerA (x=1~12)	TIMA_x_TRIG	I	External event trigger input
	TIMA_x_PWM1/TIMA_x_CLKA	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWM2/TIMA_x_CLKB	IO	External event trigger input or PWM port output or count clock port input
	TIMA_x_PWMy (y=3~4)	IO	External Event Trigger Input or PWM Port Output
EMB	EMB_PORTx (x=1~4)	I	Port input control signal
USARTx (x=1~10)	USARTx_TX	IO	Send data
	USARTx_RX	IO	Receiving data
	USARTx_CK	IO	Communication clock
	USARTx_RTS	O	request to send signal
	USARTx_CTS	I	clear to send signal
SPIx (x=1~6)	SPIx_MISO	IO	Primary input/secondary output data transfer pin
	SPIx_MOSI	IO	Primary output/slave input data transfer pin
	SPIx_SCK	IO	Transmission clock
	SPIx_NSS0	IO	Select input/output pin from machine
	SPIx_NSSy (y=1~3)	O	Slave select output pin
QSPI	QSPI_IOx (x=0~3)	IO	Data line
	QSPI_SCK	O	clock output
	QSPI_NSS	O	Slave selection
I2Cx (x=1~6)	I2Cx_SCL	IO	Clock line
	I2Cx_SDA	IO	Data line
I2Sx	I2Sx_SD	IO	Serial data

Categories	Functional name	I/O	Note
(x=1~4)	I2Sx_SDIN	I	Full-duplex serial data input
	I2Sx_WS	IO	word choice
	I2Sx_CK	IO	Serial clock
	I2Sx_EXCK	I	External timer
	I2Sx_MCK	O	master clock
CANx (x=1~2)	CANx_TX	O	Send data
	CANx_RX	I	Receiving data
SDIOx (x=1~2)	SDIOx_Dy (y=0~7)	IO	SD data signal
	SDIOx_CK	O	SD clock output signal
	SDIOx_CMD	IO	SD command and reply signal
	SDIOx_CD	I	SD card identification status signal
	SDIOx_WP	I	SD card write protection status signal
USB_FS	USBFS_DM	IO	USBFS on-chip full-speed PHY D-signal
	USBFS_DP	IO	USBFS on-chip full-speed PHY D+ signal
	USBFS_VBUS	I	USBFS VBUS signal
	USBFS_ID	I	USBFS ID signal
	USBFS_SOF	O	USBFS SOF pulse output signal
	USBFS_DRVVBUS	O	USBFS VBUS driver permission signal
USB_HS	USBHS_DP	IO	USBHS on-chip full-speed PHY D+ signal
	USBHS_DM	IO	USBHS on-chip full-speed PHY D-signal
	USBHS_VBUS	I	USBHS VBUS signal
	USBHS_ID	I	USBHS ID signal
	USBHS_SOF	O	USBHS SOF pulse output signal
	USBHS_DRVVBUS	O	USBHS VBUS drive enable signal
	USBHS_ULPI_CLK	I	ULPI interface clock signal
	USBHS_ULPI_DIR	I	ULPI interface dir signal
	USBHS_ULPI_STP	O	ULPI interface stp signal
	USBHS_ULPI_NXT	I	ULPI interface nxt signal
	USBHS_ULPI_Dx (x=0~7)	IO	ULPI interface data signal
ETHMAC	ETH_SMI_MDC	O	SMI interface clock
	ETH_SMI_MDIO	IO	SMI interface data
	ETH_PPS_OUT	IO	PPS output
	ETH_MII_RMII_RXCLK	I	MII receive action clock or RMII reference clock
	ETH_MII_RMII_RXDV	I	MII receive data valid or RMII receive data valid
	ETH_MII_RMII_RXD0	I	MII receive data 0 or RMII receive data 0
	ETH_MII_RMII_RXD1	I	MII receive data 1 or RMII receive data 1
	ETH_MII_RMII_TXEN	O	MII transmit data enable or RMII transmit data enable
	ETH_MII_RMII_TXD0	O	MII sends data 0 or RMII sends data 0

Categories	Functional name	I/O	Note
	ETH_MII_RMII_TXD1	O	MII send data 1 or RMII send data 1
	ETH_MII_RXD2	I	MII receive data 2
	ETH_MII_RXD3	I	MII receive data 3
	ETH_MII_RXER	I	MII receive data error
	ETH_MII_TXCLK	I	MII send action clock
	ETH_MII_TXD2	O	MII send data 2
	ETH_MII_TXD3	O	MII send data 3
	ETH_MII_TXER	O	MII send data error
	ETH_MII_COL	I	MII carrier sense
	ETH_MII_CRS	I	MII collision detection
CMP	VCOUT1	O	CMP1 result output
	VCOUT2	O	CMP2 result output
	VCOUT3	O	CMP3 result output
	VCOUT4	O	CMP4 result output
	VCOUT	O	CMP1~4 result OR output
	CMPx_INPy (x=1~4 y=2~4)	I	CMPx positive analog input
	CMPx_INM4 (x=1~4)	I	CMPx negative terminal analog input
	CMP123_INM3	I	CMP1,2,3 negative terminal analog input
	CMP4_INM3	I	CMP4 negative terminal analog input
ADC	ADTRG1	I	ADC1 AD conversion external startup source
	ADTRG2	I	ADC2 AD conversion external startup source
	ADTRG3	I	ADC3 AD conversion external startup source
	ADC123_INx (x=0~3,10~13)	I	ADC1,2,3 share external analog input port
	ADC12_INx (x=4~9,14,15)	I	ADC1,2 share external analog input port
	ADC3_INx (x=4~9,14,15)	I	ADC3 external analog input port
	PGA123_VSS	I	PGA1~3 Ground input
	PGA4_VSS	I	PGA4 Ground input
DAC	DACx_OUTy (x=1,2 y=1,2)	O	DAC analog output
DVP	DVP_HSYNC	I	Line sync input port
	DVP_VSYNC	I	Frame sync input port
	DVP_PIXCLK	I	clock input port
	DVP_DATAx (x=0~13)	I	data input port
EXMC	EXMC_CLK	IO	For details, please refer to the EXMC Port Function Assignment Table in the **External Memory Controller** chapter of the reference manual.
	EXMC_OE	O	
	EXMC_WE	O	
	EXMC_CLE	O	

Categories	Functional name	I/O	Note
	EXMC_ALE	O	
	EXMC_BAA	O	
	EXMC_ADV	O	
	EXMC_CEx (x=0~7)	O	
	EXMC_RBx(x=0~7)	I	
	EXMC_ADDx (x=0~29)	IO	
	EXMC_DATAx (x=0~31)	IO	

2.4 Pin instruction

Table 2-6 Pin instructions

Pin name	Usage notes
VCC	Power supply, connect to 1.8V~3.6V voltage, and connect a decoupling capacitor to the VSS pin nearby (refer to electrical characteristics)
VSS	Source ground, connected to 0V
VBAT	Backup power, connected to battery or other powered device Short-circuit with VCC when not in use, and connect an external 100nF decoupling capacitor
VCAP_x (x=1~2)	Core voltage, connected to VSS pin to stabilize core voltage (refer to electrical characteristics)
AVCC	Analog power supply, supply power to the analog module, connect to the same voltage as VCC (refer to electrical characteristics) When not using the analog module, please short-circuit with VCC
AVSS	Analog power ground, supply power to the analog module, connect to the same voltage as VSS (refer to electrical characteristics) When not using analog module, please short circuit with VSS
VREFL	Analog reference voltage, connected to the same voltage as AVSS (refer to electrical characteristics) When not using analog module, please short circuit with AVSS
VREFH	Analog reference voltage, connected to a voltage not higher than AVCC When not using ADC, please short to AVCC
PI13/MD	mode input. When the reset pin (NRST) is released (from low level to high level), this pin must be fixed to low level. It is recommended to connect a resistor (4.7kΩ) to VSS (pull down)
NRST	Reset pin, low effective. Connect a resistor to VCC when not in use (pull-up)
Pxy (x=A~I y=0~15)	General pin. When used as an input function, the input voltage of pins that support 5V withstand voltage should not exceed 5V, and the input voltage of pins that do not support 5V withstand voltage should not exceed VCC. When used as an analog input, the analog voltage should not exceed VREFH/AVCC Float when not in use, or connect a resistor to VCC (pull-up)/VSS (pull-down)

3 Electrical Characteristics (ECs)

3.1 Parameter conditions

All voltages are VSS-based unless otherwise specified.

3.1.1 Minimum and maximum

Unless otherwise specified, the minimum and maximum values of all devices are guaranteed by design or performance tests at worst ambient temperature, supply voltage and clock frequency.

3.1.2 Typical value

Unless otherwise specified, typical data are analyzed by design or characterization at T_A = 25 °C, V_{CC} = 3.3 V.

3.1.3 Typical curve

Unless otherwise specified, all typical curves are not tested for design reference only.

3.1.4 Load capacitance

The load conditions used to measure the pin parameters are shown in Figure 3-1 (left).

3.1.5 Pin input voltage

The measurement method for the input voltage at the device pins is shown in Figure 3-1 (right).

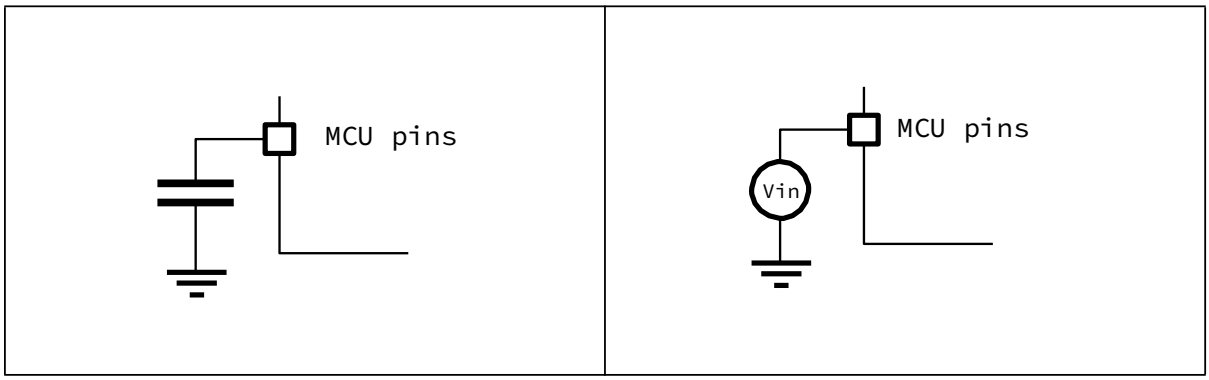


Figure 3-1 Pin Load Condition (Left) vs Input Voltage Measurement (right)

3.1.6 Power supply scheme

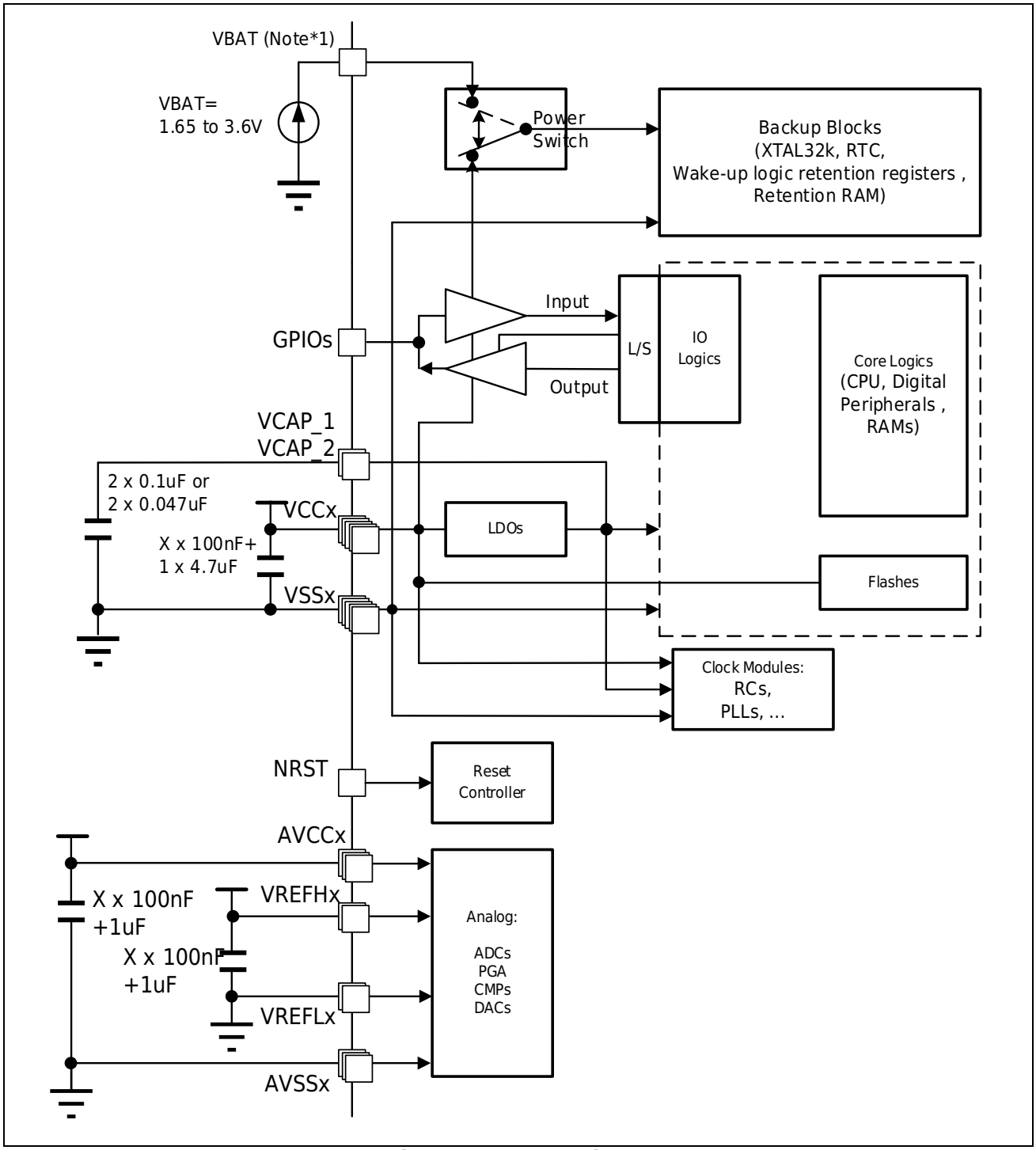


Figure 3-2 Power scheme

Note *1 : For non-rechargeable batteries, it is strongly recommended to connect a low drop diode between the battery and the VBAT pin.

1. A 4.7μF ceramic capacitor must be connected to one of the VCC pins.
2. AVSS=VSS.
3. Each power supply pair (eg VCC/VSS, AVCC/AVSS...) Decoupling with filter ceramic capacitors as described above must be used. These capacitors must be as close to or

below the appropriate pins as possible under the PCB to ensure proper device operation. Filtering capacitors are not recommended to reduce PCB size or cost. This may result in abnormal operation of the device.

4. The capacitors used by the VCAP_1/VCAP_2 pins of the chip are as follows: 1) For chips with both VCAP_1 and VCAP_2 pins, each pin can use a 0.047uF or 0.1uF capacitor (the total capacity is 0.094uF or 0.2uF). 2) For chips with only VCAP_1 pin, 0.1uF or 0.22uF capacitors can be used. When waking up from power-down mode, VCAP_1/VCAP_2 needs to be charged during core voltage establishment. On the one hand, the smaller VCAP_1/VCAP_2 total capacity can shorten the charging time and bring fast response capability to the application; on the other hand, the larger VCAP_1/VCAP_2 total capacity will prolong the charging time, but also provide stronger electromagnetic compatibility (EMC). Users can choose a larger or smaller capacitance value according to the requirements of electromagnetic compatibility and system response speed. The total VCAP_1/VCAP_2 capacity of the chip must match the assignment of the PWC_PWRC3.PDTS bits. When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is cleared before entering the power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is set before entering the power-down mode.
5. The stability of the main regulator is achieved by connecting an external capacitor to the VCAP_1 (or VCAP_1/VCAP_2) pin with a value of C_{EXT} Determined according to the stability requirements of the system. Capacitance value C_{EXT} and ESR requirements are as follows:

Table 3-1 VCAP_1/VCAP_2 working conditions

Symbol	Parameter	Conditions
C_{EXT}	Capacitance value of external capacitance	0.047 μF / 0.1 μF
ESR	Equivalent Series Resistance ESR of External Capacitor	< 0.3 Ω

3.1.7 Current consumption measurement

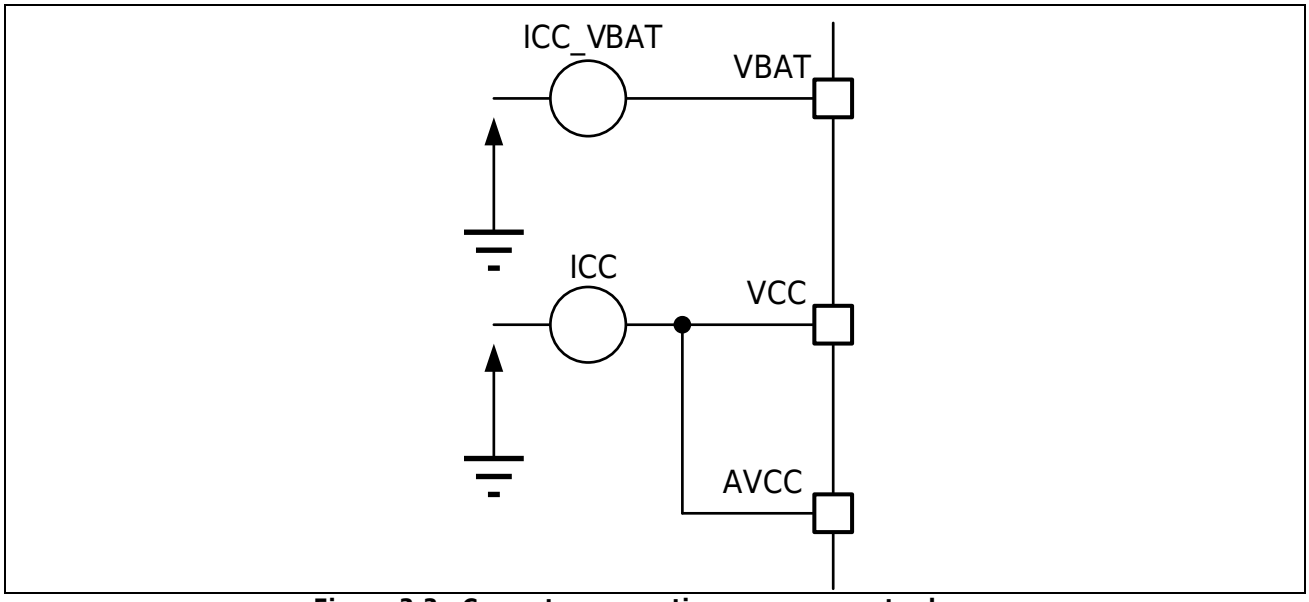


Figure 3-3 Current consumption measurement scheme

3.2 Absolute maximum ratings

Loads applied to the device in excess of the absolute maximum ratings listed in Table 3-2 Voltage characteristics, Table 3-3 Current characteristics, and Table 3-4 Thermal characteristics may cause permanent damage to the device. These values are just rated stresses and do not mean that the device works properly under these conditions. Long-term operation may affect the reliability.

Table 3-2 Voltage characteristics

Symbol	Item	Minimum value	Maximum value	Unit
V_{CC} -V_{SS}	External mains voltage (including AVCC, VCC, and VBAT) (1)	-0.3	4.0	V
V_{IN}	Input voltage on pins other than PA11/USBFS_DM, PA12/USBFS_DP, PB14_USBHS_DM, PB15_USBHS_DP, PA0, PA1, PA2, PA6 (2)	V_{SS} –0.3	V_{CC} +4.0 (Max 5.8V)	
	PA11/USBFS_DM, PA12/USBFS_DP Input voltage on pins PB14/USBHS_DM, PB15/USBHS_DP, PA0, PA1, PA2, PA6	V_{SS} –0.3	Vcc+0.7(Max 4.0V)	
$V_{ESD(HBM)}$	Electrostatic discharge voltage	Please refer to Electrical Sensitivity		-

1. All mains (VCC, AVCC, VBAT) and ground (VSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. The maximum value of V_{IN} must always be followed. For information on the maximum allowable injection current value, see Table 3-3 .

Table 3-3 Current characteristics

Symbol	Item	Maximum value	Unit
ΣI_{VCC}	Total current flowing into all VCC x power lines (sourced) (1)	240	mA
ΣI_{VSS}	Total current flowing out of all VSS x ground wires (sinking current) (1)	-240	
I_{VCC}	Maximum current flowing into each VCC x power line (source current) (1)	100	
I_{VSS}	Maximum current flowing out of each VSS x ground wire (sink current) (1)	-100	
I_{IO}	Arbitrary I/O and control pin output current	20	
	Output pull current of any I/O and control pin	-20	
ΣI_{IO}	Total output sink current on all I/O and control pins	120	
	Total output source current on all I/O and control pins	-120	

1. All mains (VCC, AVCC, VBAT) and ground (VSS, AVSS) pins must always be connected to an external power supply within the allowable range.

Table 3-4 Thermal characteristics

Symbol	Item	Numerical value	Unit
T_{STG}	Storage temperature range	–65~150	°C
T_J	Maximum Junction Temperature Range	-40~125	°C

3.3 Operating conditions

3.3.1 General operating conditions

Table 3-5 General working conditions

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	High Speed Mode (1) PWRC2.DVS=11 PWRC2.DDAS=1111 PWRC3.DDAS=0xff	-	-	240	MHz
		Super low speed mode PWRC2.DVS=10 PWRC2.DDAS= 0000 PWRC3.DDAS=0x00	-	-	8	
V_{CC}	Standard operating voltage	-	1.8	-	3.6	V
V_{AVCC}(2)	Analog working voltage	-	1.8	-	3.6	
V_{BAT}	Backup working voltage	-	1.65	-	3.6	
V_{IN}	Input Voltage on 5V Tolerant Pin (3)	2 V ≤ VCC ≤ 3.6 V 2 V ≤ AVCC ≤ 3.6 V	–0.3	-	5.5	
		VCC < 2 V AVCC < 2V	–0.3	-	5.2	
	PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM, PB15/USBHS_DP, Input voltage on pins PA0, PA1, PA2, PA6	-	–0.3	-	VCC+0.3	

1. Guarantee of mass production test.
2. If the VREFH pin is present, the following conditions must be considered: $0 \le V_{AVCC}-V_{REFH} \le 1.2$ V.
3. To keep the voltage above V_{CC} +0.3, the internal pull-up/pull-down resistors must be disabled.

3.3.2 Operationg conditions in case of power-on/power-off

TA obeys general operating conditions.

Table 3-6 Operating Conditions at Power-Up/Power-Down

Symbol	Parameter	Minimum value	Maximum value	Unit
t_{VCC}	VCC rise time rate	20	20000	μs/V
	VCC fall time rate	20	20000	

3.3.3 Reset and power control module characteristics

Table 3-7 Reset and Power Control Module Features

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{BOR}	Monitoring voltage of BOR (1)	ICG1.BOR_LEV[1:0]=00	1.85	2.00	2.10	V
		ICG1.BOR_LEV[1:0]=01	1.96	2.10	2.20	V
		ICG1.BOR_LEV[1:0]=10	2.06	2.20	2.30	V
		ICG1.BOR_LEV[1:0]=11	2.27	2.40	2.50	V
V_{PVD1}	PVD1 monitoring voltage (1) (3)	PVD1LVL[2:0]=000	1.96	2.10	2.20	V
		PVD1LVL[2:0]=001	2.06	2.20	2.30	V
		PVD1LVL[2:0]=010	2.27	2.40	2.52	V
		PVD1LVL[2:0]=011	2.48	2.60	2.72	V
		PVD1LVL[2:0]=100	2.58	2.70	2.82	V
		PVD1LVL[2:0]=101	2.69	2.80	2.92	V
		PVD1LVL[2:0]=110	2.79	2.95	3.07	V
		PVD1LVL[2:0]=111	2.90	3.05	3.17	V
V_{PVD2}	PVD2 monitoring voltage (1) (3)	PVD2LVL[2:0]=000	2.06	2.20	2.30	V
		PVD2LVL[2:0]=001	2.27	2.40	2.50	V
		PVD2LVL[2:0]=010	2.48	2.60	2.72	V
		PVD2LVL[2:0]=011	2.58	2.70	2.82	V
		PVD2LVL[2:0]=100	2.69	2.85	2.94	V
		PVD2LVL[2:0]=101	2.79	2.95	3.07	V
		PVD2LVL[2:0]=110 (1)	2.90	3.05	3.17	V
		PVD2LVL[2:0]=111 (2)	1.05	1.15	1.25	V
V_{pvd}hyst	Hysteresis of PVD1,2 (4)		-	100	-	mV
V_{POR}(1)	Power-on/power-off reset threshold	Rising edge VPOR	1.60	1.68	1.80	V
		Falling edge VPOR	1.56	1.64	1.76	V
V_{POR}hyst	POR hysteresis		-	40	-	mV
I_{RUSH}	Surge current when the voltage regulator is powered on (POR or awakens from standby)		-	160	200	mA
T_{NRST}	NRST reset minimum width		10	-	-	μs
T_{IPVD1}	PVD1 reset release time		300	380	460	μs
T_{IPVD2}	PVD2 reset release time		300	380	460	μs
T_{INRST}	NRST reset release time		25	35	50	μs
T_{RIPT}	Internal reset time		140	160	200	μs
T_{RSTBOR}	BOR reset release time		440	520	610	μs
T_{RSTPOR}	Power-on reset release time		-	2500	3000	μs

1. Guarantee of mass production test.

2. When PVD2LVDL[2:0] = 111, the compare voltage is External input compare voltage of PVD2EXINP pin
3. The PVD1 monitoring voltage is the monitoring voltage when the VCC voltage drops; when the PVD2LVL[2:0] is set to 111, the PVD2 monitoring voltage is the monitoring voltage when the PVDEXINP voltage drops, when the PVD2LVD[2:0] is set to a value other than 111 The PVD2 monitoring voltage is the monitoring voltage when the VCC voltage drops.
4. The hysteresis of PVD1,2 is the difference between the monitoring voltage when VCC is rising and the monitoring voltage when VCC is falling.
   PVD1 monitoring voltage when VCC rises=Vpvd1+Vpvdhyst;
   PVD2 monitoring voltage when VCC rises = Vpvd2 + Vpvdhyst.

3.3.4 Supply Current characteristics

The current consumption is affected by several parameters and factors, including operating voltage, ambient temperature, I/O pin load, device software configuration, operating frequency, I/O pin switch rate, program position in memory and running code.

The measurement method for current consumption is described in Figure 3-3. The current consumption measurements in the various modes described in this section are derived from a set of test code running in FLASH under laboratory conditions.

The specific conditions are as follows:

1) All I/O pins are in high impedance mode (no load).
2) The clock frequency selects high speed mode f_{HCLK} = 240MHz/120MHz/24MHz and ultra low speed mode f_{HCLK} = 8MHz/1MHz.
3) The power modes are divided into: Normal working mode ICC_RUN, sleep mode ICC_SLEEP, stop mode ICC_STP, power-down mode ICC_PD, Dhrystone working mode ICC_DHRYSTONE and VBAT power supply mode ICC_VBAT.
4) Please refer to the description of specific current conditions for peripheral clock ON/OFF.
5) In high speed mode f_{HCLK} = 240MHz/120MHz PLL is on.

Table 3-8 High-speed mode current consumption 1

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
high speed mode	f_{HCLK} = 240MHz	ICC_RUN (3)	While (1), full-module clock OFF	-40	-	33	-	mA
			While (1), full module clock ON	-40	-	73	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	37	-	mA
			CACHE ON	-40	-	38	-	mA
		ICC_SLEEP (3)	Full module clock OFF	-40	-	26	-	mA
			Full module clock ON	-40	-	66	-	mA
		ICC_RUN (3)	While (1), full-module clock OFF	25	-	33	-	mA
			While (1), full module clock ON	25	-	74	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	38	-	mA
			CACHE ON	25	-	39	-	mA
		ICC_SLEEP (3)	Full module clock OFF	25	-	26	-	mA
			Full module clock ON	25	-	67	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	70	mA
			While (1), full module clock ON	85	-	-	120	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	77	mA
			CACHE ON	85	-	-	78	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	60	mA
			Full module clock ON	85	-	-	110	mA
		ICC_RUN (3)	While (1), full-module clock OFF	105	-	-	110	mA
			While (1), full module clock ON	105	-	-	160	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	120	mA
			CACHE ON	105	-	-	121	mA
		ICC_SLEEP (3)	Full module clock OFF	105	-	-	100	mA
			Full module clock ON	105	-	-	150	mA

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Mass production guarantee

Table 3-9 High Speed Mode Current Consumption 2

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
high speed mode	f_{HCLK} = 120MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	21	-	mA
			While (1), full module clock ON	-40	-	42	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	21	-	mA
			CACHE ON	-40	-	22	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	16	-	mA
			Full module clock ON	-40	-	37	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	22	-	mA
			While (1), full module clock ON	25	-	43	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	22	-	mA
			CACHE ON	25	-	23	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	16	-	mA
			Full module clock ON	25	-	38	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	52	mA
			While (1), full module clock ON	85	-	-	78	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	53	mA
			CACHE ON	85	-	-	54	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	44	mA
			Full module clock ON	85	-	-	71	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	84	mA
			While (1), full module clock ON	105	-	-	108	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	88	mA
			CACHE ON	105	-	-	89	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	77	mA
			Full module clock ON	105	-	-	101	mA

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Mass production guarantee

Table 3-10 High-speed mode current consumption 3

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
high speed mode	f_{HCLK} = 24MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	6	-	mA
			While (1), full module clock ON	-40	-	13	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	6	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	4	-	mA
			Full module clock ON	-40	-	12	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	6	-	mA
			While (1), full module clock ON	25	-	14	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	7	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	4	-	mA
			Full module clock ON	25	-	13	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	27	mA
			While (1), full module clock ON	85	-	-	36	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	29	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	24	mA
			Full module clock ON	85	-	-	33	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	54	mA
			While (1), full module clock ON	105	-	-	61	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	59	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	52	mA
			Full module clock ON	105	-	-	59	mA

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Mass production test guarantee

Table 3-11 Ultra-low speed mode current consumption 1

Pattern	Parameter	Symbol	Conditions	Ta	Product Specifications			Unit
				(°C)	Min	Typ (1)	Max (2)	
Super low speed mode	f_{HCLK} = 8MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	3	-	mA
			While (1), full module clock ON	-40	-	6	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	3	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	2	-	mA
			Full module clock ON	-40	-	6	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	3	-	mA
			While (1), full module clock ON	25	-	7	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	3	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	3	-	mA
			Full module clock ON	25	-	7	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	22	mA
			While (1), full module clock ON	85	-	-	28	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	25	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	22	mA
			Full module clock ON	85	-	-	27	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	48	mA
			While (1), full module clock ON	105	-	-	50	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	49	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	48	mA
			Full module clock ON	105	-	-	50	mA

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Mass production test guarantee

Table 3-12 Ultra-low speed mode current consumption2

Pattern	Parameter	Symbol	Conditions	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
ultra low speed Pattern	f_{HCLK} = 1MHz	ICC_RUN	While (1), full-module clock OFF	-40	-	1	-	mA
			While (1), full module clock ON	-40	-	4	-	mA
		ICC_DHRYSTONE	CACHE OFF	-40	-	2	-	mA
		ICC_SLEEP	Full module clock OFF	-40	-	1	-	mA
			Full module clock ON	-40	-	3	-	mA
		ICC_RUN	While (1), full-module clock OFF	25	-	2	-	mA
			While (1), full module clock ON	25	-	4	-	mA
		ICC_DHRYSTONE	CACHE OFF	25	-	2	-	mA
		ICC_SLEEP	Full module clock OFF	25	-	2	-	mA
			Full module clock ON	25	-	4	-	mA
		ICC_RUN	While (1), full-module clock OFF	85	-	-	20	mA
			While (1), full module clock ON	85	-	-	24	mA
		ICC_DHRYSTONE	CACHE OFF	85	-	-	23	mA
		ICC_SLEEP	Full module clock OFF	85	-	-	20	mA
			Full module clock ON	85	-	-	24	mA
		ICC_RUN	While (1), full-module clock OFF	105	-	-	46	mA
			While (1), full module clock ON	105	-	-	47	mA
		ICC_DHRYSTONE	CACHE OFF	105	-	-	47	mA
		ICC_SLEEP	Full module clock OFF	105	-	-	46	mA
			Full module clock ON	105	-	-	47	mA

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Mass production test guarantee

Table 3-13 Low Power Mode Current Consumption

Pattern	Parameter	Symbol	Condition(VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
Stop mode	-	ICC_STP	PWC_PWRC1.STPDAS=00 (3)	-40	-	191	-	uA
			PWC_PWRC1.STPDAS=11 (3)	-40	-	56	-	uA
			PWC_PWRC1.STPDAS=00 (3)	25	-	396	-	uA
			PWC_PWRC1.STPDAS=11 (3)	25	-	248	-	uA
			PWC_PWRC1.STPDAS=00	85	-	-	15	mA
			PWC_PWRC1.STPDAS=11	85	-	-	16	mA
			PWC_PWRC1.STPDAS=00 (3)	105	-	-	40 (3)	mA
			PWC_PWRC1.STPDAS=11 (3)	105	-	-	41 (3)	mA
Power-down mode	-	ICC_PD	Power Down Mode 1 (3)	-40	-	9.1	-	uA
			Power Down Mode 2 (3)	-40	-	3.8	-	uA
			Power Down Mode 3 (3)	-40	-	1.6	-	uA
			Power Down Mode 4 (3)	-40	-	1.6	-	uA
			Power-down mode 2 +XTAL32+RTC	-40	-	5.1	-	uA
			Power-down mode 2 +LRC+RTC (3)	-40	-	7.5	-	uA
			Power-down mode 2 +XTAL32+RTC+Backup SRAM (3)	-40	-	5.5	-	uA
			Power Down Mode 1 (3)	25	-	10.5	-	uA
			Power Down Mode 2 (3)	25	-	4.3	-	uA
			Power Down Mode 3 (3)	25	-	2	-	uA
			Power Down Mode 4 (3)	25	-	2	-	uA
			Power-down mode 2 +XTAL32+RTC	25	-	5.8	-	uA
			Power-down mode 2 +LRC+RTC (3)	25	-	8.1	-	uA
			Power-down mode 2 +XTAL32+RTC+Backup SRAM (3)	25	-	6.3	-	uA
			Power-down mode 1	85	-	-	24	uA
			Power-down mode 2	85	-	-	17	uA
			Power-down mode 3	85	-	-	14	uA
			Power-down mode 4	85	-	-	14	uA
			Power-down mode 2 +XTAL32+RTC	85	-	-	18	uA
			Power-down mode 2 +LRC+RTC	85	-	-	19	uA
			Power-down mode 2 +XTAL32+RTC+Backup SRAM	85	-	-	23	uA
			Power Down Mode 1 (3)	105	-	-	75 (3)	uA
			Power Down Mode 2 (3)	105	-	-	68 (3)	uA
			Power Down Mode 3 (3)	105	-	-	65 (3)	uA
			Power Down Mode 4 (3)	105	-	-	65 (3)	uA
			Power-down mode 2 +XTAL32+RTC	105	-	-	69	uA

Pattern	Parameter	Symbol	Condition(VCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ(1)	Max(2)	
			Power-down mode 2 +LRC+RTC (3)	105	-	-	70 (3)	uA
			Power-down mode 2 +XTAL32+RTC+Backup SRAM (3)	105	-	-	87 (3)	uA

1. Typ voltage condition V_{CC} =3.3V
2. Max voltage condition V_{CC} =1.8~3.6V
3. Guarantee of mass production test.

Table 3-14 Backup domain current consumption

Item	Parameter	Symbol	Condition (VBAT=3.3V) (1)	Ta (°C)	Product Specifications			Unit
					Min	Typ	Max	
VBAT powered by	-	ICC_VBAT	VBAT area module fully closed (2)	-40	-	0.05	-	uA
			XTAL32 ON	-40	-	1.0	-	uA
			XTAL32 ON+ XTAL32 filter ON	-40	-	1.4	-	uA
			XTAL32 ON+ XTAL32 filter ON+RTC count	-40	-	1.5	-	uA
			Backup SRAM ON (2)	-40	-	0.6	-	uA
			RTCLRC ON (2)	-40	-	3.8	-	uA
			RTCLRC ON + WKTM count	-40	-	3.9	-	uA
			VBAT area module fully closed (2)	25	-	0.1	-	uA
			XTAL32 ON	25	-	1.2	-	uA
			XTAL32 ON+ XTAL32 filter ON	25	-	1.5	-	uA
			XTAL32 ON+ XTAL32 filter ON+RTC count	25	-	1.6	-	uA
			Backup SRAM ON (2)	25	-	0.9	-	uA
			RTCLRC ON (2)	25	-	3.8	-	uA
			RTCLRC ON + WKTM count	25	-	3.9	-	uA
			VBAT area module is fully closed	85	-	-	1.4	uA
			XTAL32 ON	85	-	-	3.3	uA
			XTAL32 ON+ XTAL32 filter ON	85	-	-	3.8	uA
			XTAL32 ON+ XTAL32 filter ON+RTC count	85	-	-	3.9	uA
			Backup SRAM on	85	-	-	6.3	uA
			RTCLRC on	85	-	-	7.6	uA
			RTCLRC ON + WKTM count	85	-	-	7.8	uA
			VBAT area module fully closed (2)	105	-	-	3.6	uA
			XTAL32 ON	105	-	-	5.6	uA
			XTAL32 ON+ XTAL32 filter ON	105	-	-	6.2	uA
			XTAL32 ON+ XTAL32 filter ON+RTC count	105	-	-	6.3	uA
			Backup SRAM ON (2)	105	-	-	15.2	uA
			RTCLRC ON (2)	105	-	-	9.8	uA
			RTCLRC ON + WKTM count	105	-	-	9.9	uA

1. In the condition description, the unlisted VBAT power supply modules are turned off.
2. Guarantee of mass production test.

Table 3-15 Analog Module Current Consumption

Item	Parameter	Symbol	Condition(VCC=AVCC=3.3V)	Ta (°C)	Product Specifications			Unit
					Min	Typ	Max	
Modules Current	-	ICC_MODULE	XTAL Oscillation Mode Maximum Drive 24MHz	25	-	1.8	-	mA
			Drive 16 MHz in Oscillation Mode	25	-	1.0	-	mA
			Oscillation mode small drive 10MHz	25	-	0.8	-	mA
			Oscillation mode ultra-small drive 8MHz	25	-	0.6	-	mA
			XTAL 32.768kHz	25	-	1.1	-	uA
			HRC	25	-	0.3	-	mA
			PLLH (VCO=1200MHz)	25	-	4	-	mA
			PLLH (VCO=600MHz)	25	-	2.4	-	mA
			PLLA (VCO=480MHz)	25	-	2.8	-	mA
			PLLA (VCO=240MHz)	25	-	1.6	-	mA
			ADC	25	-	1.2	-	mA
			DAC	25	-	0.2	-	mA
			CMP	25	-	0.4	-	mA
			PGA	25	-	0.7	-	mA
			USBFS (1)	25	-	6	-	mA

1. Including the current when the control part communicates with the USBPHY, the load is 50pf.

3.3.5 Low power mode wake-up timing

The wake-up time measurement method is from the wake-up event triggering to the CPU execution of the first instruction:

- For stop or sleep mode: The wakeup event is WFE.
- WKUP pins are used to wake up from standby, stop, and sleep modes. All timings are tested at ambient temperature and VCC=3.3V.

Table 3-16 Low power mode wake-up time

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
T_{STOP1}	Wakeup from stop mode	PWC_PWRC1.VHRCSD=1 and PWC_PWRC1.VPLLSD=1, the system clock is MRC, and the program is executed on RAM	2	5	us
T_{STOP2}	Wakeup from stop mode	The system clock is MRC, and the program is executed on the Flash	8	15	
T_{PD1} (1)	Wake-up from Power-down Mode 1	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	25	35	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	30	40	
T_{PD2} (1)	Wake-up from Power-down Mode 2	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	70	80	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	75	85	
T_{PD3} (1)	Wake-up from Power-down Mode 3	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	2500	3000	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	2500	3000	
T_{PD4} (1)	Wake-up from Power-down Mode 4	The total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF	130	140	
		The total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF	140	150	

1. The total VCAP_1/VCAP_2 capacity of the chip must match the assignment of the PWC_PWRC3.PDTS bits. When the total capacity of VCAP_1/VCAP_2 is 0.2uF or 0.22uF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is cleared before entering the power-down mode. When the total capacity of VCAP_1/VCAP_2 is 0.094uF or 0.1uF, it is necessary to ensure that the PWC_PWRC3.PDTS bit is set before entering the power-down mode.

3.3.6 External timer characteristic

3.3.6.1 High-speed external subscriber clock generated by external source

In bypass mode, XTAL oscillator is off and the input pin is standard I/O. External clock signals must take into account I/O static characteristics.

Table 3-17 High-speed external user clock features

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{XTAL_EXT} (1)	User external timer frequency	-	1	-	25	MHz
V_{IH_XTAL} (1)	XTAL_IN input pin high level voltage		0.8*V_{CC}	-	VCC	V
V_{IL_XTAL} (1)	XTAL_IN input pin low level voltage		VSS	-	0.2*V_{CC}	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_IN rise or fall time		-	-	5	ns
$Duty_{(XTAL)}$	Duty ratio	-	40	-	60	%

1. Mass production test guarantee

3.3.6.2 High-speed external clock produced by crystal oscillator/ceramic resonator

High-speed external (XTAL) clocks can be produced using a 4 to 25 MHz crystal oscillator/ceramic resonator oscillator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-18 XTAL 4-25 MHz Oscillator Features

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{XTAL_IN}	Oscillator frequency		4	-	25	MHz
R_F (1)	Feedback resistance		-	300	-	kΩ
A_{XTAL} (2)	XTAL accuracy	-	-500	-	500	ppm
G_{mmmax}	-	Wake up	4	-	-	mA/V
$t_{SU(XTAL)}$ (3)	Start time	VCC is stable, crystal oscillator=8MHz	-	-	2.0	ms
		VCC is stable, crystal oscillator=4MHz	-	-	4.0	ms

1. Guarantee of mass production test.
2. This parameter depends on the resonator used on the application system.
3. $T_{SU\ (XTAL)}$ is the start-up time, that is, the time between the software enabling the XTAL to measure until the stable 8MHz oscillation frequency is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors between 5 pF and 25 pF (typ.) designed for high frequency applications that meet the requirements of a crystal or resonator (see diagram below)). C_{L1} and C_{L2} are usually the same size. The load capacitance specified by the crystal oscillator manufacturer is usually a product family combination of C_{L1} and C_{L2}. In determining the specifications of C_{L1} and C_{L2}, the capacitance of the PCB and MCU pins must be taken into account (the capacitance of the pin and the circuit board can be roughly estimated to be 10 pF).

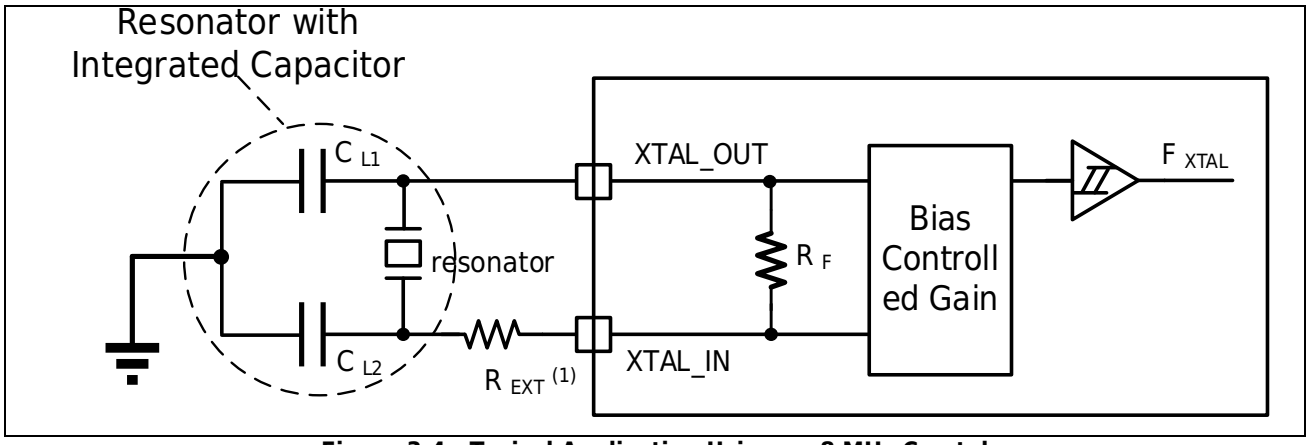


Figure 3-4 Typical Application Using an 8 MHz Crystal

1. The value of R_{EXT} depends on the crystal oscillator characteristics.

3.3.6.3 Low-speed external clock generated by crystal oscillator/ceramic resonator

A low-speed external clock can be generated using an oscillator consisting of a 32.768 kHz crystal/ceramic resonator. In applications, the resonator and load capacitance must be as close to the oscillator pin as possible to minimize output distortion and vibration stabilization time. For more information on the resonator characteristics (frequency, encapsulation, accuracy, etc.), please consult the crystal resonator manufacturer.

Table 3-19 XTAL32 Oscillator Features

Symbol	Parameter	Conditions	Specifications			Unit
			Min	Typ	Max	
F_{XTAL32}	Frequency	-	-	32.768	-	kHz
R_F	Feedback resistance	-	-	15	-	MΩ
I_{DD_XTAL32}	Power consumption	XTAL32DRV[2:0]=000	-	0.8	-	μA
A_{XTAL32} (2)	XTAL32 precision	-	-500	-	500	ppm
G_{mmmax}	G_m	-	-	-	5.6	μA/V
$T_{SUXTAL32}$	Start Time (3)	VCC steady state	-	2	-	s

1. Guarantee of mass production test.
2. This parameter depends on the resonator used on the application system.
3. $T_{SUXTAL32}$ is the start-up time, which starts with the software enabling XTAL 32 to measure until a stable oscillation frequency of 32.768 kHz is obtained. This value is measured based on the standard crystal resonator and may vary significantly with the crystal resonator manufacturer.

For C_{L1} and C_{L2} , a high-quality external ceramic capacitor between 5 pF and 18 pF (typ) is recommended (see figure below). C_{L1} and C_{L2} are usually the same size. The load capacitance specified by the crystal oscillator manufacturer is usually a product family combination of C_{L1} and C_{L2}. When sizing C_{L1} and C_{L2} , the capacitance of the PCB and MCU pins must be taken into account (the pin capacitance can be roughly estimated as 5 pF). If C_{L1} and C_{L2} are greater than 18pF, it is recommended to set XTAL32DRV[2:0]=001 (large drive, typical power consumption increases by 0.2uA).

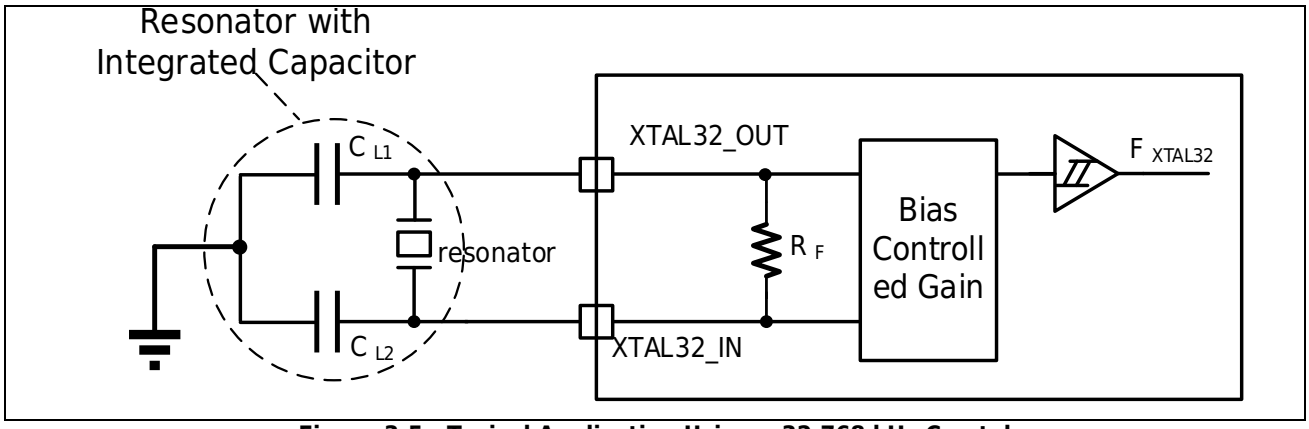


Figure 3-5 Typical Application Using a 32.768 kHz Crystal

3.3.7 Internal timer characteristics

3.3.7.1 Internal High Speed (HRC) oscillator

Table 3-20 HRC Oscillator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{HRC}	Frequency (1)	Pattern 1	-	16	-	MHz
		Pattern 2	-	20	-	
	User adjust scale	-	-	-	0.2	%
	Frequency Accuracy (1)	TA = -40 to 105 ℃	-3 (1)	-	3 (1)	%
		TA = -20 to 105 ℃	-2.5	-	2.5	%
		TA = 25℃	-1.5 (1)	-	1.5 (1)	%
$t_{st(HRC)}$	HRC oscillator oscillation stabilization time (1)	-	-	-	15	μs

1. Guarantee of mass production test.

3.3.7.2 Internal Medium Speed (MRC) Oscillator

Table 3-21 MRC oscillator characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{MRC}(1)	Frequency	7.2 (1)	8	8.8 (1)	MHz
$t_{st(MRC)}$(1)	MRC oscillator stabilization time	-	-	3	μs

1. Guarantee of mass production test.

3.3.7.3 Internal Low Speed (LRC) oscillator

Table 3-22 LRC oscillator characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{LRC}(1)	Frequency	27.853 (1)	32.768	37.683 (1)	kHz
$t_{st(LRC)}$(1)	LRCoscillator Stabilization Time	-	-	36	μs

1. Guarantee of mass production test.

3.3.7.4 SWDT dedicated internal low speed (SWDTLRC) oscillator

Table 3-23 SWDTLRC oscillator characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$f_{SWDTLRC}$ (1)	Frequency	9 (1)	10	11 (1)	kHz
tst(SWDTLRC) (1)	SWDTLRC oscillator stabilization time	-	-	57.1	μs

1. Guarantee of mass production test.

3.3.7.5 RTC dedicated internal low speed (RTCRC) oscillator

Table 3-24 RTCRC Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{RRC} (1)	Frequency	29.5 (1)	32.768	36 (1)	kHz
tst(RRC) (1)	RTCRC oscillator stabilization time	-	-	36	μs

1. Guarantee of mass production test.

3.3.8 PLL characteristics

Table 3-25 I2S-PLL (PLLA) main performance indicators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(2)	PLL PFD (Phase Frequency Detector) input clock (1)	-	1	-	25	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	15	-	240	MHz
f_{VCO_OUT}(2)	PLL VCO output	-	240	-	480	MHz
$Jitter_{PLL}$	Period Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±100	-	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±150	-	
t_{LOCK}(2)	PLL lock time	-	-	80	120	μs

Table 3-26 System PLL (PLLH) main performance indicators

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(2)	PLL PFD (Phase Frequency Detector) input clock (1)	-	8	-	25	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	37.5	-	600	MHz
f_{VCO_OUT}(2)	PLL VCO output	-	600	-	1200	MHz
$Jitter_{PLL}$	Period Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±70	-	ps
	Cycle-to-Cycle Jitter	PLL PFD input clock=8MHz, System clock=120MHz, Peak-to-Peak	-	±100	-	
t_{LOCK}(2)	PLL lock time	-	-	80	120	μs

1. A higher input clock is recommended for good jitter characteristics.
2. Mass production test guarantee.

3.3.9 Memory (Flash) Characteristics

Flash memory was erased when the device was delivered to the customer.

Table 3-27 Flash Features

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
I_{VCC}	Supply current	Read mode, V_{CC} =1.8 V~3.6V	-	-	5	mA
		Programming mode, V_{CC} =1.8 V~3.6V	-	-	10	
		Block erase mode, V_{CC} =1.8 V~3.6V	-	-	10	
		Full erase mode, V_{CC} =1.8 V~3.6V	-	-	10	

Table 3-28 Flash Program Erase Time

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
T_{prog}(1)	Word programming time	Single programming mode	43+2* T_{hclk}(2)	48+4* T_{hclk}(2)	53+6* T_{hclk}(2)	μs
	Word programming time	Continuous programming mode	12+2* T_{hclk}(2)	14+4* T_{hclk}(2)	16+6* T_{hclk}(2)	μs
T_{erase}(1)	Block erase time	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms
T_{mas}(1)	Full erase time	-	16+2* T_{hclk}(2)	18+4* T_{hclk}(2)	20+6* T_{hclk}(2)	ms

1. Guarantee of mass production test.
2. Thclk is one cycle of CPU clock.

Table 3-29 Flash Erasable Times and Data Retention Period

Symbol	Parameter	Conditions	Numerical value	Unit
			Minimum value	
N_{end}	Programming, number of block erases	T_A = 85℃	10	kcycles
N_{end}	Number of whole erases	T_A = 85℃	10	kcycles
T_{ret}	Data retention period	T_A = 85℃, after 10 kcycles	10	Years

3.3.10 Electrical sensitivity

The chip is tested differently (ESD, LU) using specific measurements to determine its electrical sensitivity performance.

3.3.10.1 Electrostatic discharge (ESD)

Electrostatic discharge is applied to the pins of each sample according to each pin combination. This test complies with JESD22-A114/C101 standard.

Table 3-30 ESD characteristics

Symbol	Parameter	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage	T_A = + 25 ° C, compliant with JESD22-A114	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charging equipment model)	T_A = + 25 ° C, JESD22-C101 compliant	500	

3.3.10.2 Static Latch-up

To assess static Latch-up performance, two complementary static Latch-up tests are required on the chip:

- Over-voltage applied to each power supply and analog input pin
- Apply current injection to other input, output and configurable I/O pins

These tests met the EIA/JESD 78A IC Latch-up standard.

Table 3-31 Static Latch-up feature

Symbol	Parameter	Conditions	Maximum value	Unit
LU	Static Latch-up	T_A =+105 °C per JESD78A	200	mA

3.3.11 I/O port characteristics

General input/output characteristics

Table 3-32 I/O static characteristics

Symbol	Parameter		Conditions	Minimum value	Typical value	Max.	Unit
V_{IL} (1)	Schmitt input low		1.8≤V_{CC}≤3.6	-	-	0.2V_{CC}	V
V_{IH} (1)	Schmitt input high		1.8≤V_{CC}≤3.6	0.8V_{CC}	-	-	V
V_{HYS}	Schmitt Input Hysteresis		1.8≤V_{CC}≤3.6	-	0.2	-	V
V_{IL} (1)	CMOS input low level		1.8≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH} (1)	CMOS input high level		1.8≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
I_{LKG} (1)	I/O input leakage current		V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
			V_{IN} = 5.5V(2)	-	-	10	μA
R_{PU} (1)(2)(3)	weak pull-up Equivalent resistance	-	V_{IN} = V_{SS}	-	30	-	kΩ
R_{PD} (2)(4)	Weak pulldown Equivalent resistance	PA11/USBFS_DM PA12/USBFS_DP PB14/USBHS_DM PB15/USBHS_DP	V_{IN} = V_{CC}	-	500	-	kΩ
C_{IO}	I/O pin capacitance	PA11/USBFS_DM PA12/USBFS_DP PB14/USBHS_DM PB15/USBHS_DP	-	-	10	-	pF
		Other input pins except for PA11/USBFS_DM PA12/USBFS_DP PB14/USBHS_DM PB15/USBHS_DP	-	-	5	-	pF

1. Guarantee of mass production test.
2. To keep the voltage above V_{CC} +0.3V, the internal pull-up/pull-down resistors must be disabled.
3. For PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM, PB15/USBHS_DP, it indicates the weak pull-up equivalent resistance value of GPIO when the USB function is turned off. For the pull-up/pull-down resistors for the USB function, please refer to the "USB Interface Features" chapter.
4. Only PA11/USBFS_DM, PA12/USBFS_DP, PB14/USBHS_DM, PB15/USBHS_DP have weak pull-down resistors, which are always valid.

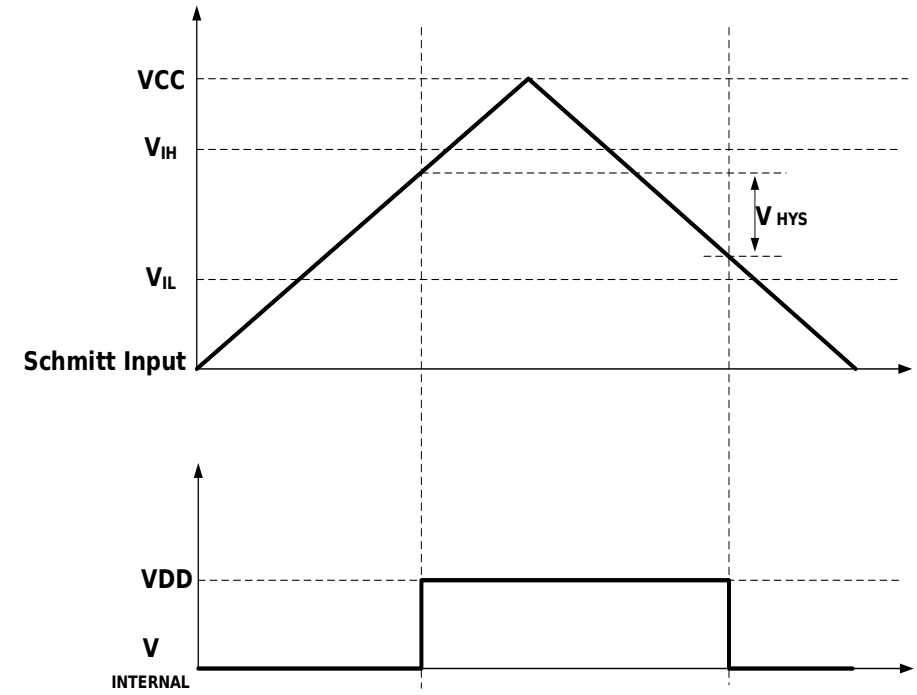


Figure 3-6 Schmitt input DC electrical characteristics definition

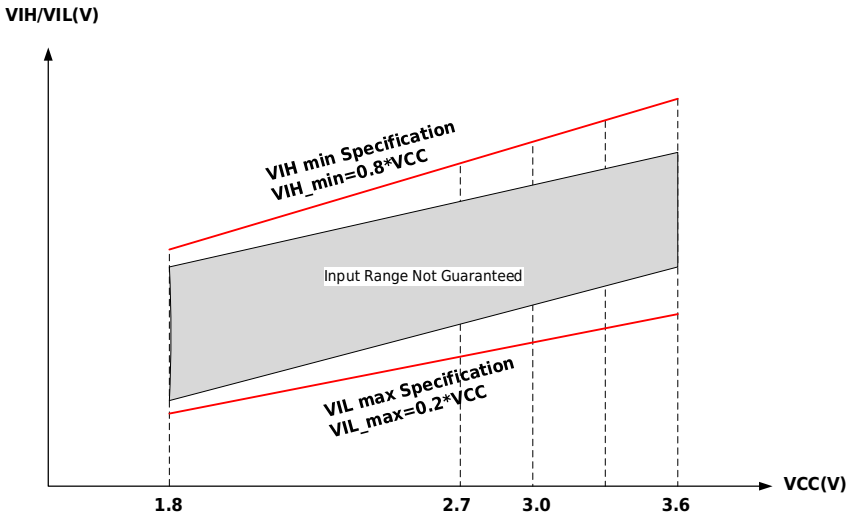


Figure 3-7 VIH/VIL versus VCC (Schmitt Input)

Output current

GPIO (General Purpose Input/Output) provides maximum ± 20mA source or sink current.

The source or sink current of PC13, PC14, PC15, and PI8 must meet the following restrictions: $\sum I_{IO}$ (PC13, PC14, PC14, PI8)≤20mA.

Output voltage

Table 3-33 Output Voltage Characteristics

Drive settings	Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
Low drive	V_{OL}(1)(2)	Low level output	I_{IO}=±1.5mA, 1.8≤V_{CC}<2.7	-	-	0.6	V
	V_{OH}(1)(3)	High level output		V_{CC}-0.6	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±3mA, 2.7≤V_{CC}≤3.6	-	-	0.6	
	V_{OH}(1)(3)	High level output		V_{CC}-0.6	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±6mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}(1)(3)	High level output		V_{CC}-1.3	-	-	
middle drive	V_{OL}(1)(2)	Low level output	I_{IO}=±3mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±5mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±12mA, 2.7≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}(1)(3)	High level output		V_{CC}-1.3	-	-	
High drive	V_{OL}(1)(2)	Low level output	I_{IO}=±6mA, 1.8≤V_{CC}<2.7	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±8mA, 2.7≤V_{CC}≤3.6	-	-	0.4	
	V_{OH}(1)(3)	High level output		V_{CC}-0.4	-	-	
	V_{OL}(1)(2)	Low level output	I_{IO}=±20mA, 2.7 ≤V_{CC}≤3.6	-	-	1.3	
	V_{OH}(1)(3)	High level output		V_{CC}-1.3	-	-	

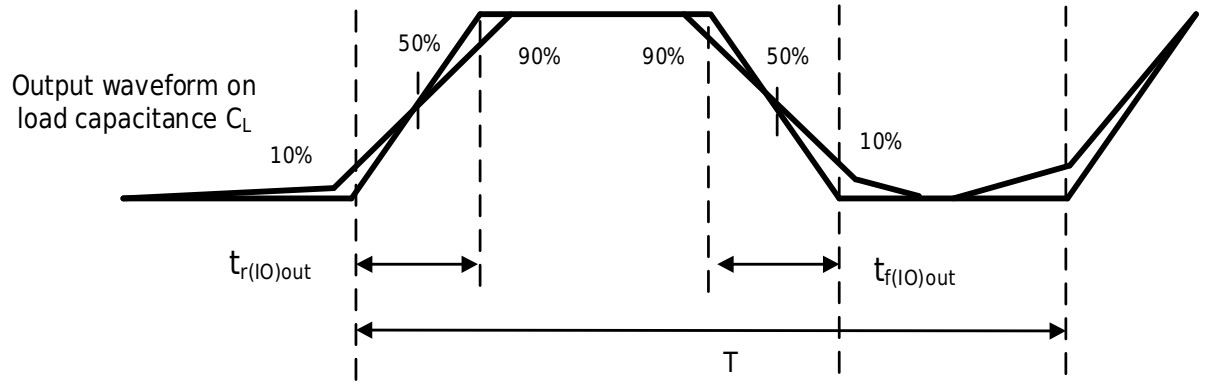
1. Guarantee of mass production test.
2. The device's I_{IO} sink current must always consider the absolute maximum ratings specified in Table 3-3. The sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The device's I_{IO} sourcing current must always adhere to the absolute maximum ratings listed in Table 3-3, and the sum of the I_{IO} (I/O ports and control pins) must not exceed I_{VCC}.

Input/output AC characteristics

Table 3-34 I/O AC Characteristics

Drive settings	Symbol	Parameter	Condition (3)	Minimum value	Typical value	Maximum value	Unit
Low drive	f_{max}(IO)out	Maximum frequency (1)	C_L=30 pF, V_{CC}≥ 2.7V	-	-	20	MHz
			C_L=30 pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	40	
			C_L=10pF, V_{CC}≥1.8V	-	-	20	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7V	-	-	15	ns
			C_L=30 pF, V_{CC}≥1.8V	-	-	25	
			C_L=10pF, V_{CC}≥2.7V	-	-	7.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	15	
Middle drive	f_{max}(IO)out	Maximum frequency (1)	C_L=30 pF, V_{CC}≥ 2.7V	-	-	45	MHz
			C_L=30 pF, V_{CC}≥1.8V	-	-	22.5	
			C_L=10pF, V_{CC}≥2.7V	-	-	90	
			C_L=10pF, V_{CC}≥1.8V	-	-	45	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7V	-	-	6	ns
			C_L=30 pF, V_{CC}≥1.8V	-	-	10	
			C_L=10pF, V_{CC}≥2.7V	-	-	4	
			C_L=10pF, V_{CC}≥1.8V	-	-	6	
High drive	f_{max}(IO)out	Maximum frequency (1)	C_L=30 pF, V_{CC}≥2.7V	-	-	100	MHz
			C_L=30 pF, V_{CC}≥1.8V	-	-	50	
			C_L=10pF, V_{CC}≥2.7V	-	-	180	
			C_L=10pF, V_{CC}≥1.8V	-	-	100	
	t_f(IO)out t_r(IO)out	Output high to low level drop time and output low to high level rise time	C_L=30 pF, V_{CC}≥2.7V	-	-	4	ns
			C_L=30 pF, V_{CC}≥1.8V	-	-	6	
			C_L=10pF, V_{CC}≥2.7V	-	-	2.5	
			C_L=10pF, V_{CC}≥1.8V	-	-	3.5	

1. The maximum frequency is defined in Figure 3-8.
2. The load capacitance C_L must take into account the capacitance of the PCB and MCU pins (the pin-to-board capacitance can be roughly estimated as 10 pF).



Maximum frequency conditions: ($t_r + t_f$) ≤ (2/3)T and Duty cycle= 50%±5% (load capacitance C_L is indicated in the "Conditions" column of the "Input/Output AC Characteristics" table)

Figure 3-8 I/O AC Characteristics Definition

3.3.12 HRPWM characteristics

Table 3-35 HRPWM characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
t_hrpwmres	HRPWM resolution	-	50	-	ps

3.3.13 I2C interface characteristics

Table 3-36 I2C Electrical Characteristics

Symbol	Parameter	Standard mode (SM)		Fast mode (FM)		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL frequency	0	100	0	400	kHz
$t_{HD;STA}$	Start condition/restart condition Hold	4.0	-	0.6	-	us
t_{LOW}	SCL Low Level	4.7	-	1.3	-	us
t_{HIGH}	SCL High Level	4	-	0.6	-	us
$t_{SU;STA}$	Restarting Condition Setup	4.7	-	0.6	-	us
$t_{HD;DAT}$	Data Hold	0	-	0	-	us
$t_{SU;DAT}$	Data Setup	50+ $t_{I2C\ reference\ clock\ period}$	-	50+ $t_{I2C\ reference\ clock\ period}$	-	ns
t_R	Ascending time of SCL/SDA	-	1000	6.5	300	ns
t_F	Falling time of SCL/SDA	-	300	6.5	300	ns
$t_{SU;STO}$	Stop Condition Setup	4	-	0.6	-	us
t_{BUF}	BUS Idle Time Between Stop Condition and Start Condition	4.7	-	1.3	-	us
C_b	Load capacitance	-	400	-	400	pF

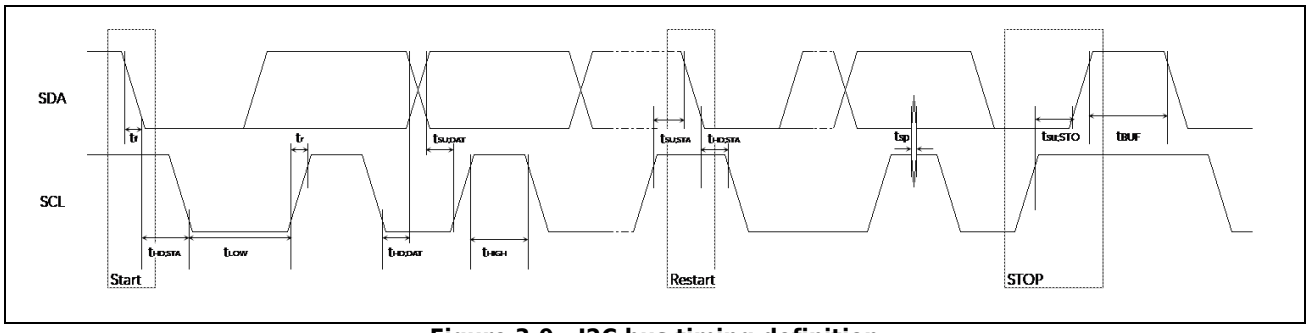


Figure 3-9 I2C bus timing definition

3.3.14 SPI Interface Characteristics

Table 3-37 SPI Electrical Characteristics

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
t_w(SCKH)	SCK high and low time	master mode *4 1.8V≤Vcc≤3.6V	T_{pclk1}-1*1	T_{pclk1}+1*1	ns
		slave mode 1.8V≤Vcc≤3.6V	3xT_{pclk1}-1*1	3xT_{pclk1}+1*1	ns
t_w(SCKL)		master mode *4 1.8V≤Vcc＜3.6V	T_{pclk1}-1*1	T_{pclk1}*1+1	ns
		slave mode 1.8V≤Vcc＜3.6V	3xT_{pclk1}-1*1	3xT_{pclk1}+1*1	ns
t_{su}(SI)	Data input setup time(5)	slave mode 1.8V≤Vcc≤3.6V	4	-	ns
t_h(SI)	Data input hold time(5)	slave mode 1.8V≤Vcc≤3.6V	3	-	ns
t_v(SO)	Data output valid time(5)	slave mode 2.7V≤Vcc≤3.6V	-	15	ns
		slave mode 1.8V≤Vcc＜2.7V	-	26	ns
t_{su}(MI)	Data input setup time(5)	master mode 2.7V≤Vcc≤3.6V	5	-	ns
		master mode 1.8V≤Vcc＜2.7V	9	-	ns
t_h(MI)	Data input hold time(5)	master mode 1.8V≤Vcc≤3.6V	T_{pclk1}*1	-	ns
t_{su}(SS)	SS setup time	slave mode 1.8V≤Vcc≤3.6V	6 x T_{pclk1} *1	-	ns
		master mode 2.7V≤Vcc≤3.6V	-5+N x T_{sck} *1*2	-	ns
		master mode 1.8V≤Vcc＜2.7V	-10+N x T_{sck} *1*2	-	ns
t_h(SS)	SS hold time	slave mode 1.8V≤Vcc≤3.6V	6 x T_{pclk1} *1	-	ns
		master mode 2.7V≤Vcc≤3.6V	-5+N x T_{sck} *1*3	-	ns
		master mode 1.8V≤Vcc＜2.7V	-10+N x T_{sck} *1*3	-	ns
t_v(MO)	Data output valid time(5)	master mode 2.7V≤Vcc≤3.6V	-	4	ns
		master mode 1.8V≤Vcc≤2.7V	-	9	ns

*1:T_{pclk1} refers to 1 cycle of the clock PCLK1, and T_{sck} refers to 1 cycle of the SPI communication clock.

*2:N=1~8 is determined by register SPI_CFG1.MSSI[2:0].

*3:N=1~8 is determined by register SPI_CFG1.MSSDL[2:0].

*4:The values of t_w(SCKH) and t_w(SCKL) are given by SPI_ CFG2.MBR decision, the values listed in the table are SPI_ The value of CFG2.MBR=0.

*5:Mass production test guarantee.

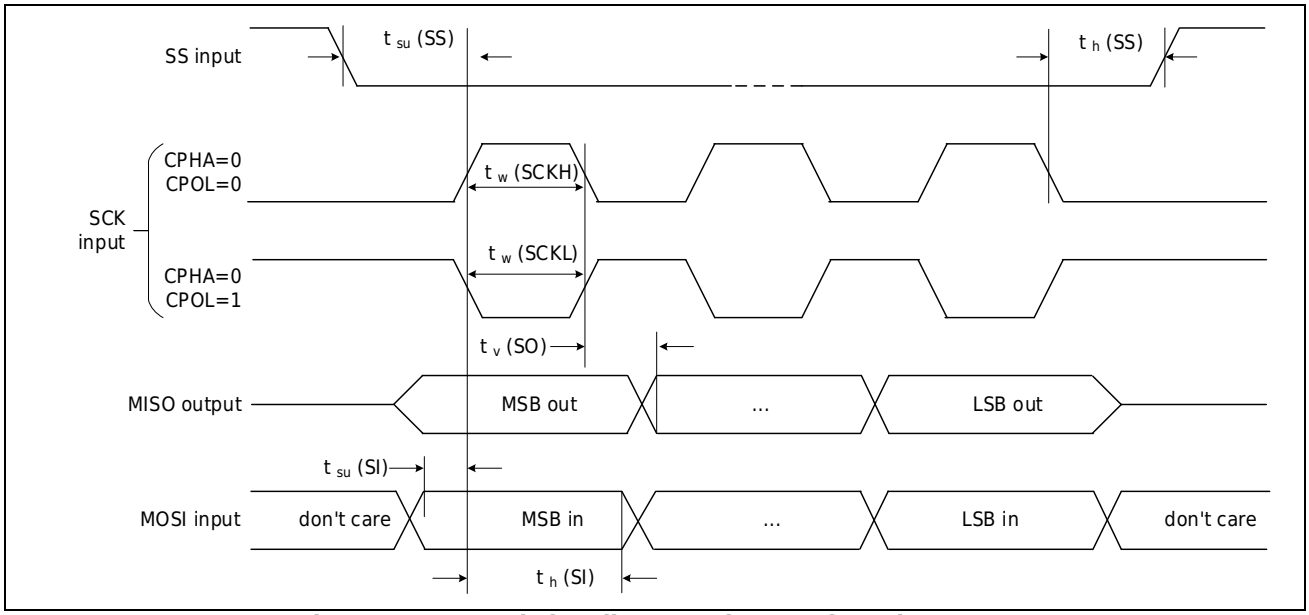


Figure 3-10 SPI timing diagram -slave mode and CPHA=0

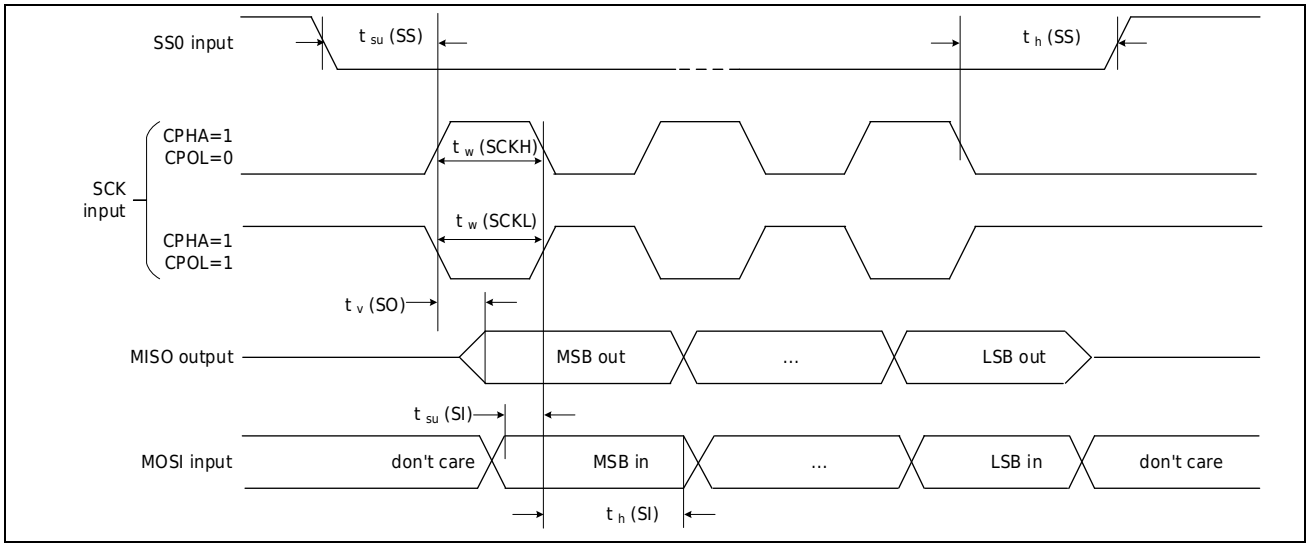


Figure 3-11 SPI timing diagram -slave mode and CPHA=1

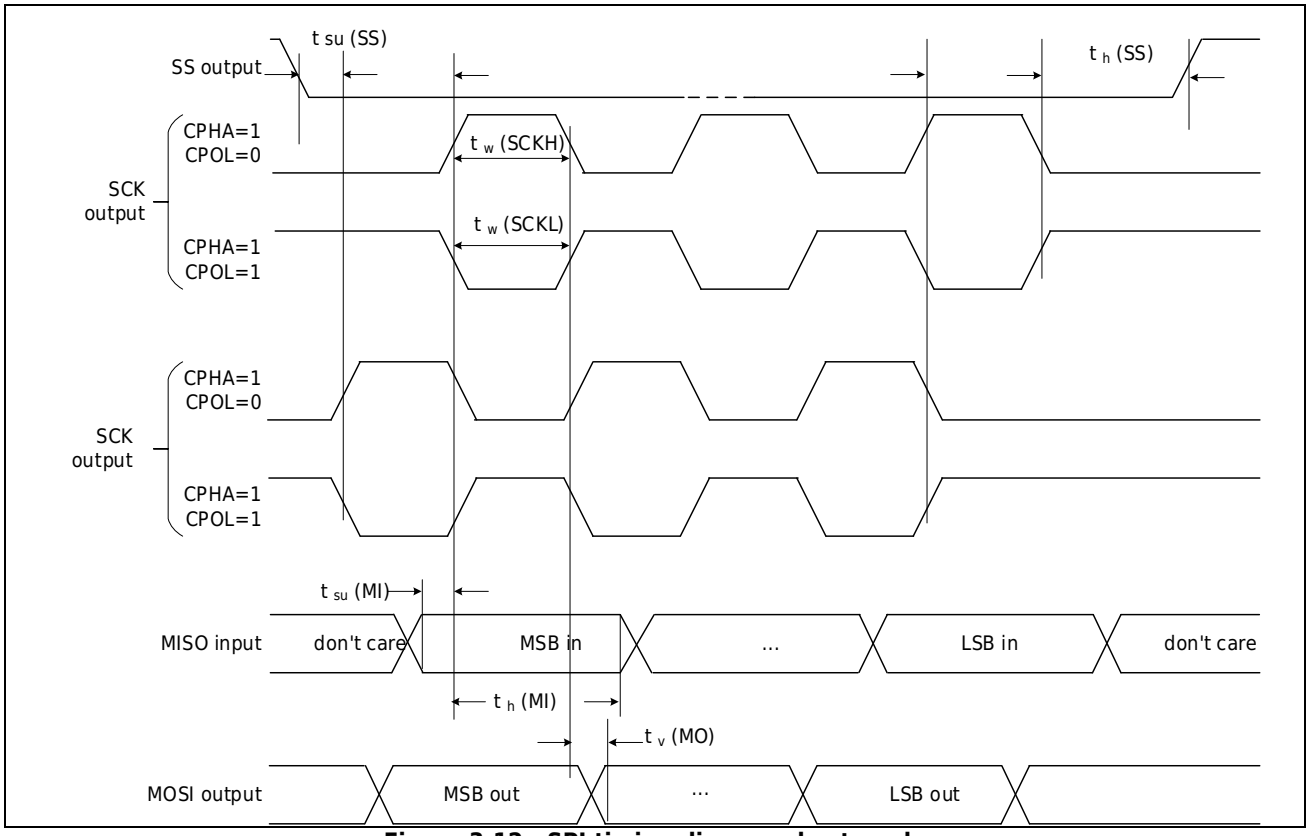


Figure 3-12 SPI timing diagram -host mode

3.3.15 QSPI interface features

Table 3-38 QSPI Electrical Characteristics

Symbol	Parameter	Minimum value	Maximum value	Unit
t_{Qscyc}	QSPCK clock cycle	2	48	thclk
t_{QSWH}	QSPCK high level	t_{Qscyc}×0.4	-	ns
t_{QSWL}	QSPCK low level	t_{Qscyc}×0.4	-	ns
t_{SU}(1)	data input setup time（2.7V~3.6V）	5	-	ns
	data input setup time（1.8V~2.7V）	5		ns
t_{IH}(1)	data input hold time（2.7V~3.6V）	11	-	ns
	data input hold time（1.8V~2.7V）	15		ns
t_{OD}(1)	data output delay	-	4	ns
t_{OH}	data output hold time	0	-	ns

*1: Mass production test guarantee .

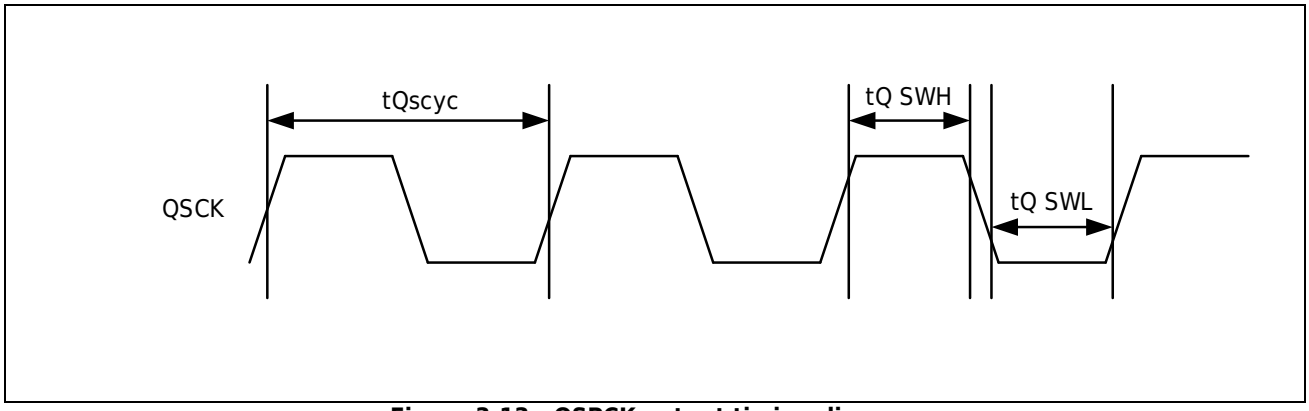


Figure 3-13 QSPCK output timing diagram

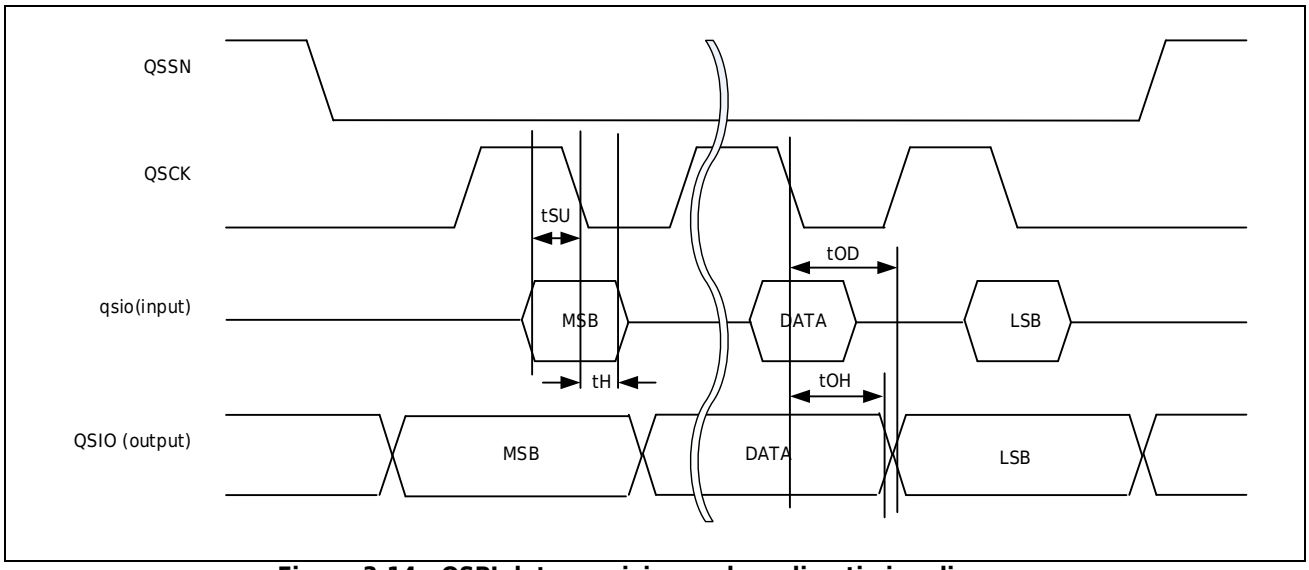


Figure 3-14 QSPI data receiving and sending timing diagram

3.3.16 I2S interface features

Table 3-39 I2S Electrical Characteristics

Symbol	Performance	Conditions	Minimum value	Maximum value	Unit
f_{MCK}	I2S main clock output	-	256 *8K	256*Fs	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	20	64*Fs	MHz
		Slave data: 32 bits	-	64*Fs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
t_v(WS) (2)	WS valid time	Master mode	-	6	ns
t_{su}(WS) (2)	WS setup time	Slave mode	7.5	-	
t_h(WS) (2)	WS hold time	Slave mode	6	-	
t_{su}(SD_MR) (2)	Data input setup time	Master receiver（2.7V~3.6V）	22	-	
		Master receiver（1.8V~2.7V）	25		
t_{su}(SD_SR) (2)		Slave receiver	7	-	
t_h(SD_MR) (2)	Data input hold time	Master receiver	0	-	
t_h(SD_SR) (2)		Slave receiver	7	-	
t_v(SD_ST) (2) t_h(SD_ST)	Data output valid time	Slave transmitter(after enable edge)	-	24	
t_v(SD_MT) (2)		Master transmitter(after enable edge)	-	10	

1. Fs: I2S sampling frequency
2. Mass production test guarantee

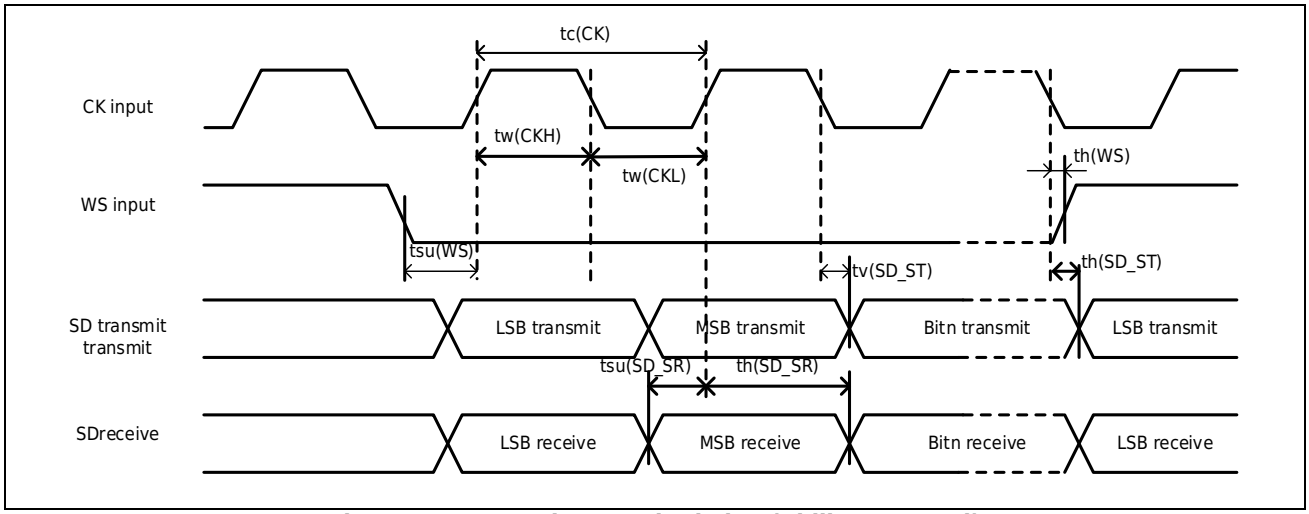


Figure 3-15 I2S slave mode timing (Philips protocol)

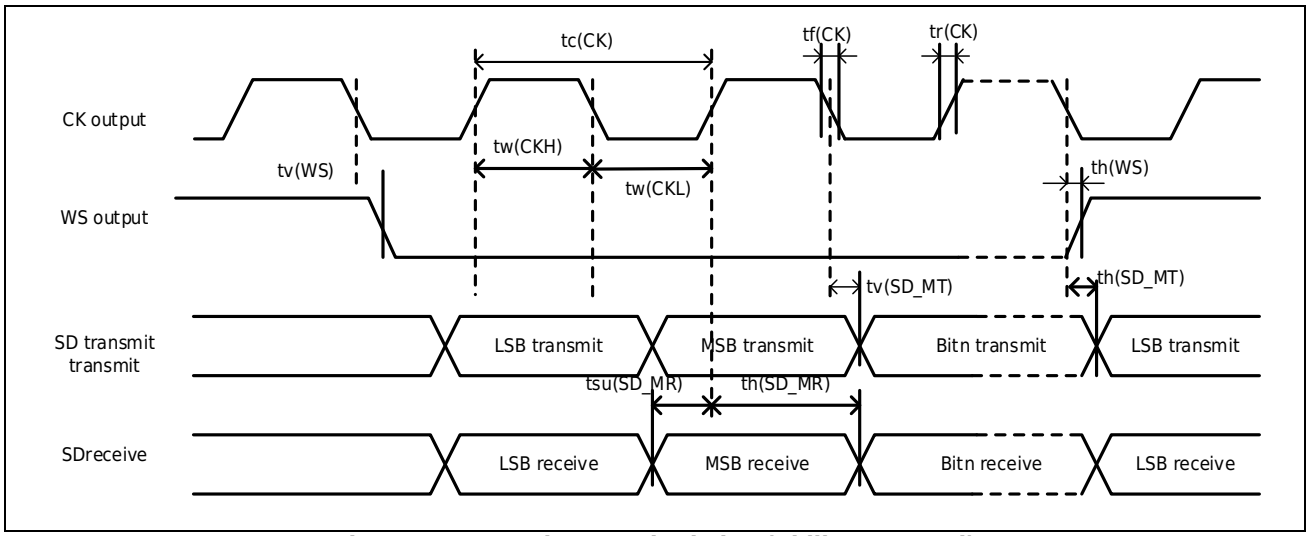


Figure 3-16 I2S host mode timing (Philips protocol)

3.3.17 CAN FD/CAN2.0B interface characteristics

For the port characteristics of CANx_TX and CANx_RX, please refer to 3.3.11 I/O port characteristics .

3.3.18 USB interface features

Table 3-40 USB Full-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input	V_{CC}	Operating Voltage	-	3.0(2)	-	3.6	V
	V_{IL} (3)	input low level	-	-	-	0.8	V
	V_{IH} (3)	input high level	-	2.0	-	-	V
	V_{DI} (3)	Differential Input Sensitivity	-	0.2	-	-	V
	V_{CM} (3)	Differential Common Mode Voltage	-	0.8	-	2.5	V
Output	V_{OL} (3)	Static output low level	R_L=1.5kΩ to 3.6V(4)	-	-	0.3	V
	V_{OH} (3)	Static output high	R_L=15kΩ to VSS(4)	2.8	-	3.6	V
	V_{CRS}	Cross-over voltage	C_L=50pF	1.3	-	2.0	V
	t_R	Rise Time	C_L=50pF，10%~90% of |V_{OH}-V_{OL}|	4	-	20	ns
	t_F	fall time	C_L=50pF，10%~90% of |V_{OH}-V_{OL}|	4	-	20	ns
	t_{RFMA}	Rise and fall time ratio t_R/t_F	C_L=50pF	90	-	111	%
R_{PD} (3)		下拉电阻	pull-down resistor	-	15.0	-	kΩ
R_{PU}(3)		上拉电阻	Pull-up resistance	0.900	1.2	1.575	kΩ
			V_{IN}= V_{SS}, in device mode	1.425	2.3	3.090	kΩ
Z_{DRV}		输出阻抗(5)	Output Impedance (5)	28	36	44	Ω

1. All voltages are measured based on local ground potential.
2. When operating down to 2.7V, the functionality of the USB full-speed transceiver is still guaranteed, but the full USB full-speed electrical characteristics are not guaranteed, which degrades over the V_{CC} voltage range of 2.7 to 3.0V.
3. Guarantee of mass production test.
4. R_L is the load connected to the USB full speed drive.
5. The DP and DM ports do not need an external series resistor for impedance matching, and the driver output already includes the matching resistor.
6. The DP and DM ports do not need external pull-up/pull-down resistors, and the PHY is integrated inside.

Table 3-41 USB Low-Speed Electrical Characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input	V_{CC}	Operating Voltage	-	3.0(2)	-	3.6	V
	V_{IL} (3)	input low level	-	-	-	0.8	V
	V_{IH} (3)	input high level	-	2.0	-	-	V
	V_{DI} (3)	Differential Input Sensitivity	-	0.2	-	-	V
	V_{CM} (3)	Differential Common Mode Voltage	-	0.8	-	2.5	V
Output	V_{OL} (3)	Static output low level	R_L=1.5kΩ to 3.6V(4)	-	-	0.3	V
	V_{OH} (3)	Static output high	R_L=15kΩ to VSS(4)	2.8	-	3.6	V
	V_{CRS}	Cross-over voltage	C_L=200pF~600pF	1.3	-	2.0	V
	t_R	Rise Time	C_L=200pF~600pF，10%~90% of |V_{OH}-V_{OL}|	75	-	300	ns
	t_F	fall time	C_L=200pF~600pF，10%~90% of |V_{OH}-V_{OL}|	75	-	300	ns
	t_{RFMA}	Rise and fall time ratio t_R/t_F	C_L=200pF~600pF	80	-	125	%
R_{PD} (3)		pull-down resistor	V_{IN}= V_{CC}，in host mode	-	15.0	-	kΩ
R_{PU}(3)		Pull-up resistance	V_{IN}= V_{SS}, idle state	0.900	1.2	1.575	kΩ
			V_{IN}= V_{SS}, in device mode	1.425	2.3	3.090	kΩ
Z_{DRV}		Output Impedance (5)	Driving high or low	28	36	44	Ω

1. All voltages are measured based on local ground potential.
2. When operating down to 2.7V, the functionality of the USB low-speed transceiver is still guaranteed, but the full USB low-speed electrical characteristics are not guaranteed, which will degrade over the V_{CC} voltage range of 2.7 to 3.0V.
3. Guarantee of mass production test.
4. R_L is the load connected to the USB low speed drive.
5. The DP and DM ports do not need an external series resistor for impedance matching, and the driver output already includes the matching resistor.
6. The DP and DM ports do not need external pull-up/pull-down resistors, and the PHY is integrated inside.

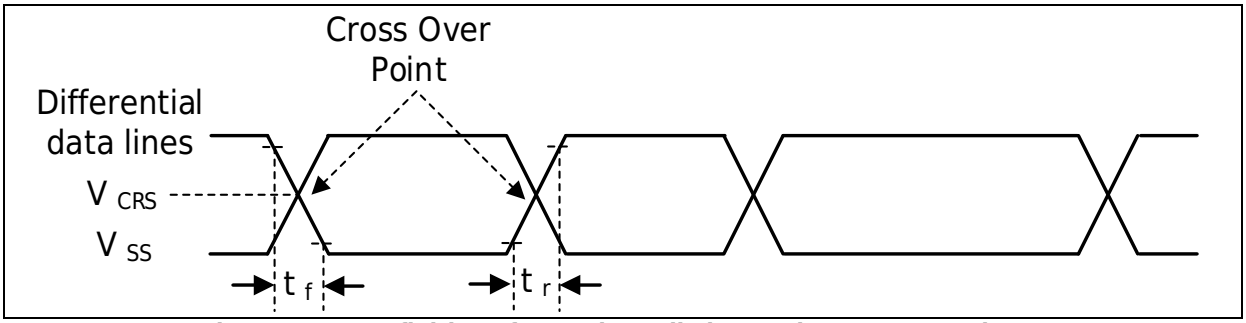


Figure 3-17 Definition of USB Rise/Fall Time and Cross Over Voltage

Table 3-42 ULPI HS Clock Timing Parameters

Symbol	Parameters (1)	Conditions	Minimum(2) (2)	Typical(2) value (2)	Max(2)	Unit
t_{SC}(3)	Control signal setup time (ULPI_DIR, ULPI_NXT) setup time	2.7V≤Vcc≤3.6V C_L=20pF -40~105℃	3.0	-	-	ns
t_{HC}(3)	Control signal hold time (ULPI_DIR, ULPI_NXT) hold time		2.0	-	-	ns
t_{SD}(3)	data creation time		3.0	-	-	ns
t_{HD}(3)	data retention time		2.2		-	ns
t_{DC}/t_{DD}(3)	Data/Control Signal Output Delay		4.5	7.5	10.6	ns

1. The ULPI_CLK clock needs to follow the UTMI+ Low Pin Interface Specification, Revision 1.1, 20/10/2004 protocol.
2. The corresponding IO should be set to high drive.
3. Mass production test guarantee

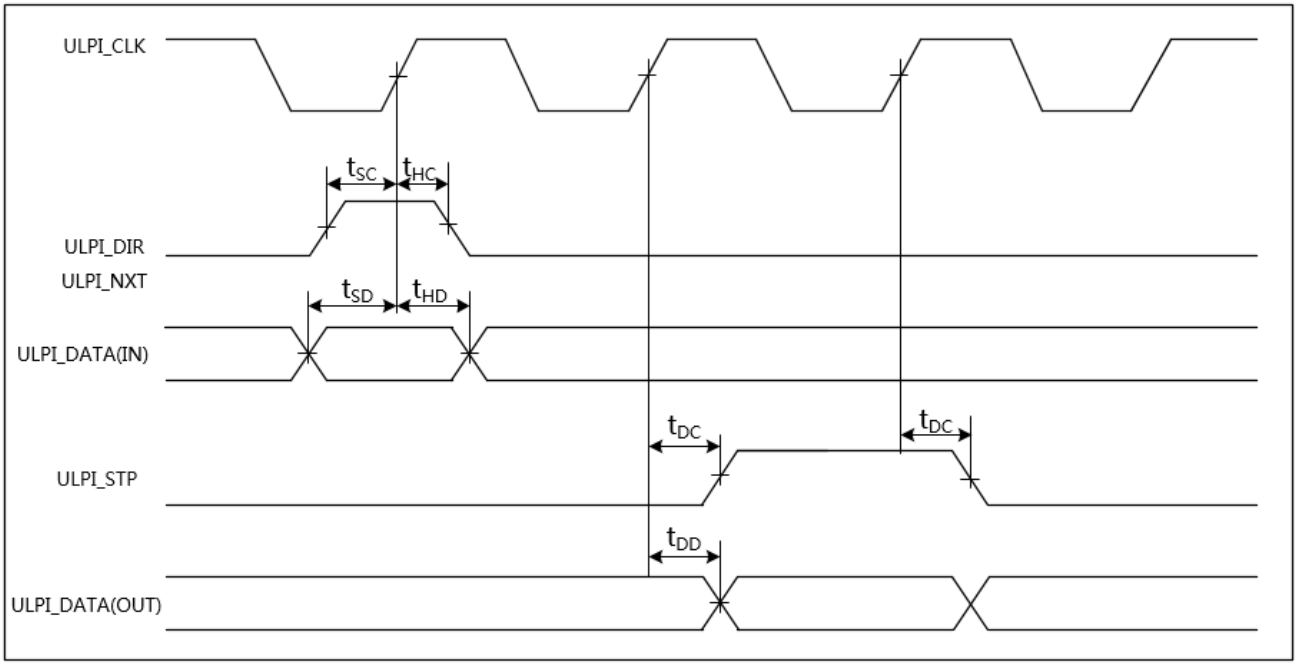


Figure 3-18 ULPI Timing Diagram

3.3.19 ETHMAC features

3.3.19.1 SMI interface

Table 3-43 ETHMAC_SMI interface characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_mdc	SMI_MDC output frequency	405	420	425	ns
t_mdo_d	SMI_MDO output delay time (2.7V~3.6V)	-	-	Tpclk1+9	ns
	SMI_MDO output delay time (1.8V~2.7V)	-		Tpclk1+12	ns
t_mdi_s	SMI_MDI input Setup time	11	-	-	ns
t_mdi_h	SMI_MDI input Hold time	0	-	-	ns

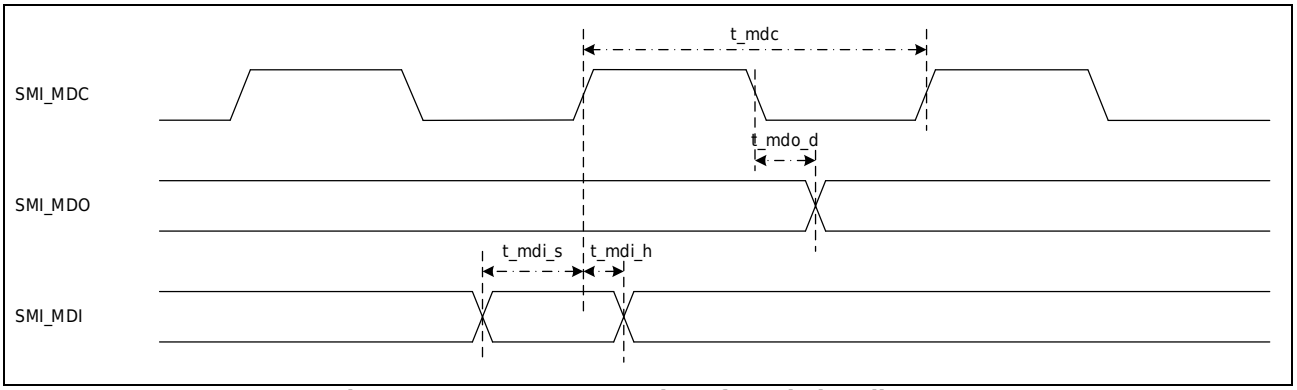


Figure 3-19 ETHMAC-SMI interface timing diagram

3.3.19.2 MII interface

Table 3-44 ETHMAC_MII interface characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_mii_tx_clk	MII_TX_CLK clock input frequency	-	40	-	ns
t_mii_txen_d(1)	MII_TX_EN output delay time (2.7V~3.6V)	5	-	15	ns
	MII_TX_EN output delay time (1.8V~2.7V)	5		21	ns
t_mii_txer_d	MII_TX_ER output delay time (2.7V~3.6V)	5	-	15	ns
	MII_TX_ER output delay time (1.8V~2.7V)	5		21	ns
t_mii_txd_d(1)	MII_TXD output delay time (2.7V~3.6V)	5	-	15	ns
	MII_TXD output delay time (1.8V~2.7V)	5		21	ns
t_mii_rx_clk	MII_RX_CLK clock input frequency	-	40	-	ns
t_mii_rxdv_s(1)	MII_RX_DV input Setup time	8	-	-	ns
t_mii_rxdv_h(1)	MII_RX_DV input Hold time	4	-	-	ns
t_mii_rxer_s(1)	MII_RX_ER input Setup time	8	-	-	ns
t_mii_rxer_h(1)	MII_RX_ER input Hold time	4	-	-	ns
t_mii_rxd_s(1)	MII_RXD input Setup time	8	-	-	ns
t_mii_rxd_h(1)	MII_RXD input Hold time	4	-	-	ns

1. Mass production test guarantee

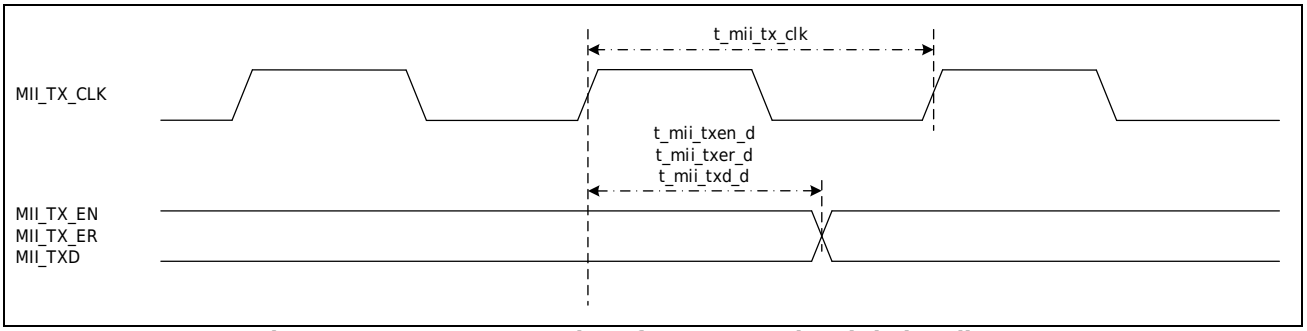


Figure 3-20 ETHMAC-MII interface output signal timing diagram

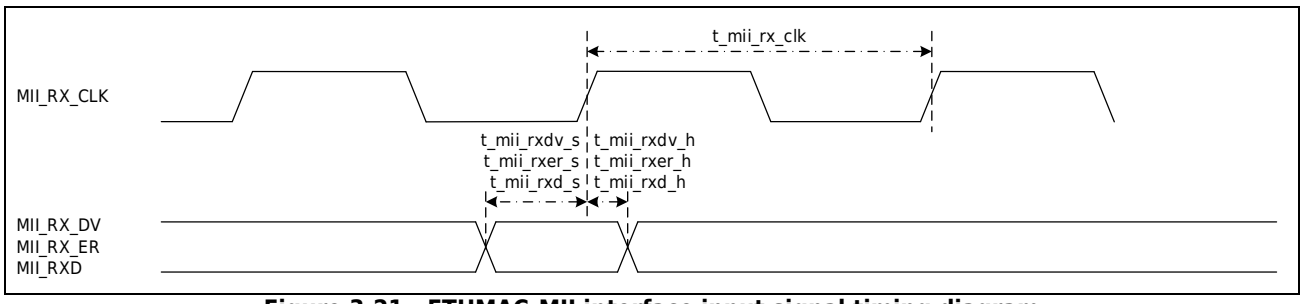


Figure 3-21 ETHMAC-MII interface input signal timing diagram

3.3.19.3 RMII interface

Table 3-45 ETHMAC_RMII interface characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_rmii_clk	RMII_REF_CLK reference clock input frequency	-	20	-	ns
t_rmii_txen_d(1)	RMII_TX_EN output delay time (2.7V~3.6V)	5	-	12.5	ns
	RMII_TX_EN output delay time (1.8V~2.7V)	5		15	ns
t_rmii_txd_d(1)	RMII_TXD output delay time (2.7V~3.6V)	5	-	12.5	ns
	RMII_TXD output delay time (1.8V~2.7V)	5		15	ns
t_rmii_crsdv_s(1)	RMII_CRS_DV input Setup time	4	-	-	ns
t_rmii_crsdv_h(1)	RMII_CRS_DV input Hold time	2	-	-	ns
t_rmii_rxer_s	RMII_RX_ER input Setup time	4	-	-	ns
t_rmii_rxer_h	RMII_RX_ER input Hold time	2	-	-	ns
t_rmii_rxd_s(1)	RMII_RXD input Setup time	4	-	-	ns
t_rmii_rxd_h(1)	RMII_RXD input Hold time	2	-	-	ns

1. Mass production test guarantee

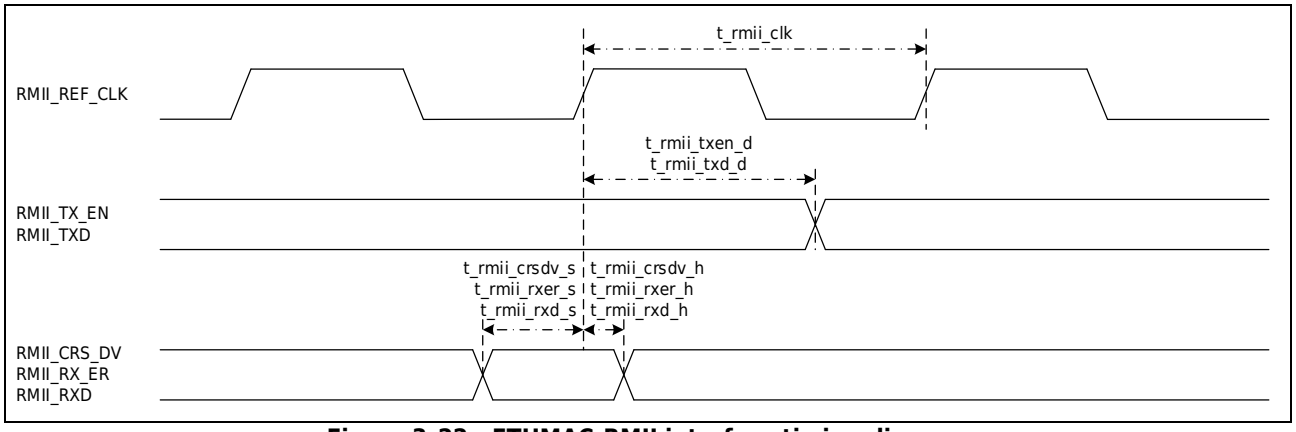


Figure 3-22 ETHMAC-RMII interface timing diagram

3.3.20 USART Interface Characteristics

Table 3-46 USART AC Timing

Symbol	Parameter		Minimum value	Maximum value	Unit
t_{cyc}	Input clock cycles	UART	4	-	t_{PCLK1}
		Clock synchronization mode	6	-	
t_{CKw}	input clock width		0.4	0.6	t_{cyc}
t_{CKr}	Input clock rise time		-	5	ns
t_{CKf}	Input clock fall time		-	5	ns
t_{TD}(1)	send delay time 2.7V≤Vcc≤3.6V	Clock synchronization mode	-	23	ns
	send delay time 1.8V≤Vcc＜2.7V	Clock synchronization mode	-	30	ns
t_{RDS}(1)	Receive data setup time 2.7V≤Vcc≤3.6V	Clock synchronization mode	17	-	ns
	Receive data setup time 1.8V≤Vcc＜2.7V	Clock synchronization mode	23	-	ns
t_{RDH}(1)	Receive data hold time	Clock synchronization mode	5	-	ns

1. Mass production test guarantee

Table 3-47 USART AC Timing

Pattern		Highest baud rate
UART	Internal timer	PCLK1/8
	External timer	PCLK1/32
Clock synchronization mode 2.7V≤Vcc≤3.6V		12.0Mbps
Clock synchronization mode 1.8V≤Vcc＜2.7V		8.0Mbps

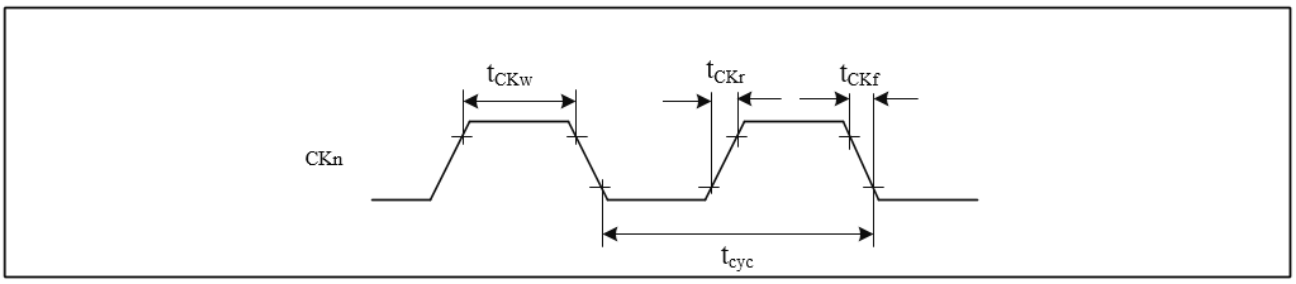


Figure 3-23 USART clock timing

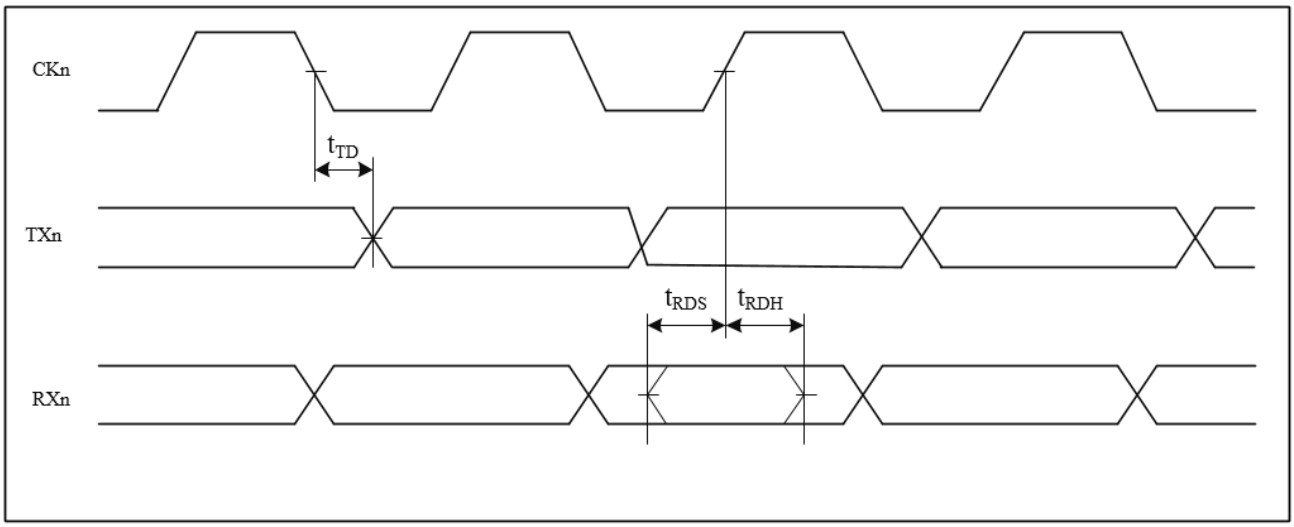


Figure 3-24 USART (CSI) input and output timing

3.3.21 JTAG interface features

Table 3-48 JTAG interface features

Synbol	Item	Min	Typ	Max	Unit
t_{TCKcyc}	JTCK clock cycle time	50	-	-	ns
t_{TCKH}	JTCK clock high pulse width	15	-	-	ns
t_{TCKL}	JTCK clock low pulse width	15	-	-	ns
t_{TCKr}	JTCK clock rise time	-	-	5	ns
t_{TCKf}	JTCK clock fall time	-	-	5	ns
t_{TMSs}	JTMS setup time(1)	10	-	-	ns
t_{TMSh}	JTMS hold time(1)	10	-	-	ns
t_{TDIs}	JTDI setup time(1)	10	-	-	ns
t_{TDIh}	JTDI hold time(1)	10	-	-	ns
t_{TDOd}	JTDO data delay time(1)	10	-	25	ns

1. Mass production test guarantee

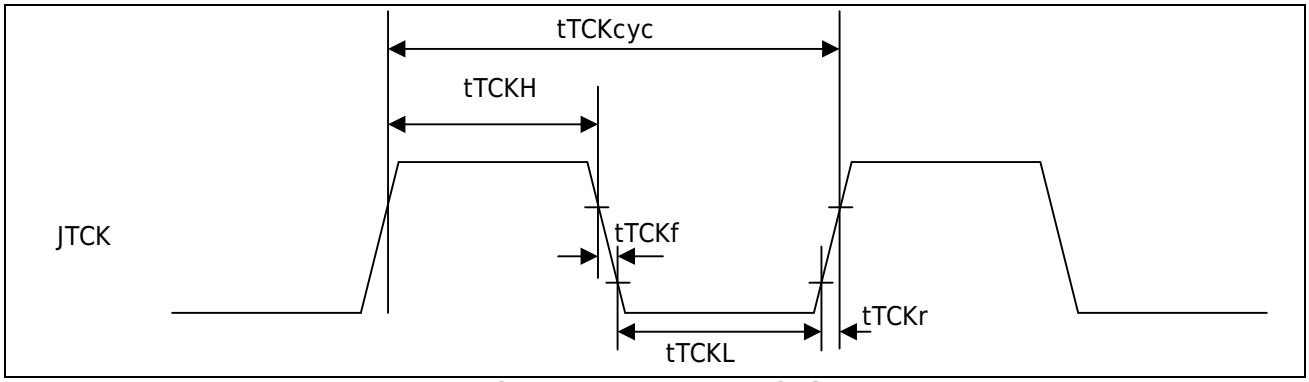


Figure 3-25 JTAG TCK clock

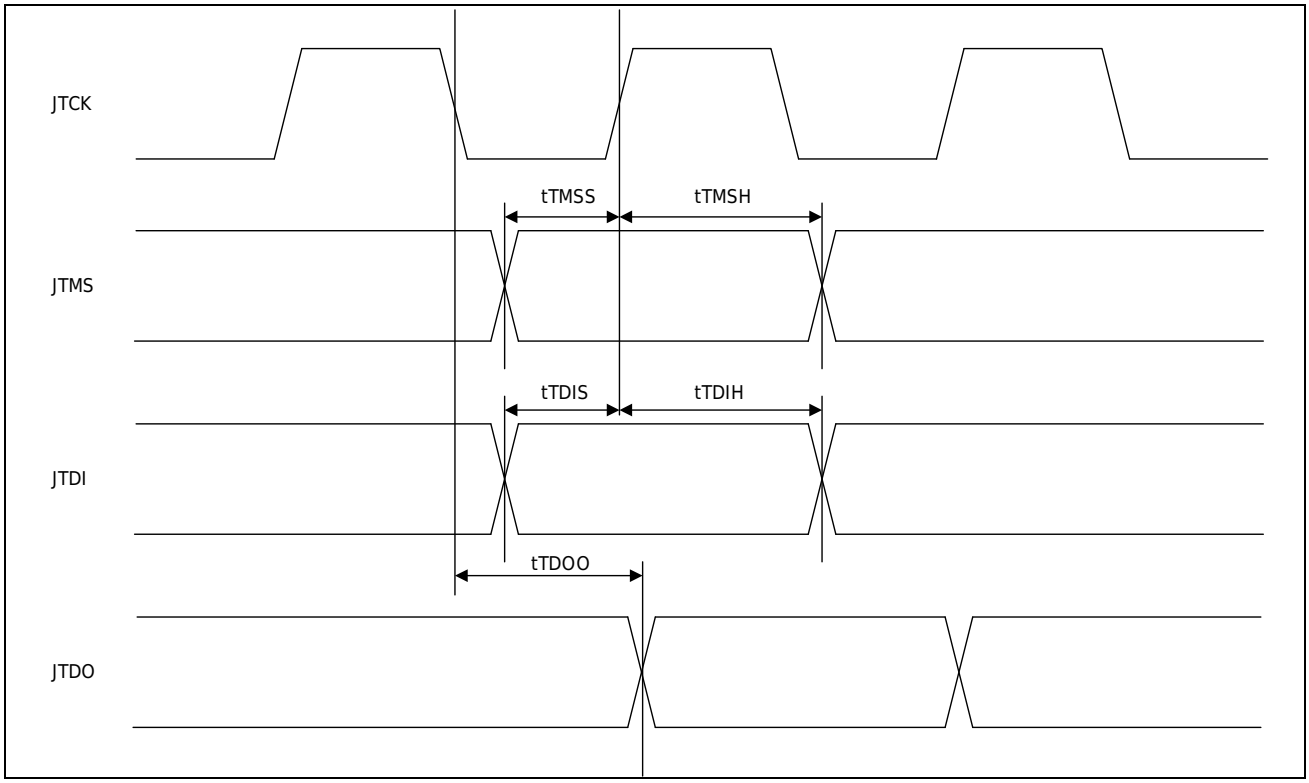


Figure 3-26 JTAG input and output

3.3.22 SWD Interface Characteristics

Table 3-49 SWD interface features

Synbol	Item	Min	Typ	Max	Unit
$t_{SWCLKcyc}$	SWCLK clock cycle time	50	-	-	ns
t_{SWCLKH}	SWCLK clock high pulse width	15	-	-	ns
t_{SWCLKL}	SWCLK clock low pulse width	15	-	-	ns
t_{SWCLKr}	SWCLK clock rise time	-	-	5	ns
t_{SWCLKf}	SWLCK clock fall time	-	-	5	ns
t_{SWDIs}	SWDI setup time(1)	10	-	-	ns
t_{SWDIh}	SWDI hold time(1)	10	-	-	ns
t_{SWDOd}	SWDO data delay time(1)	10	-	25	ns

1. Mass production test guarantee

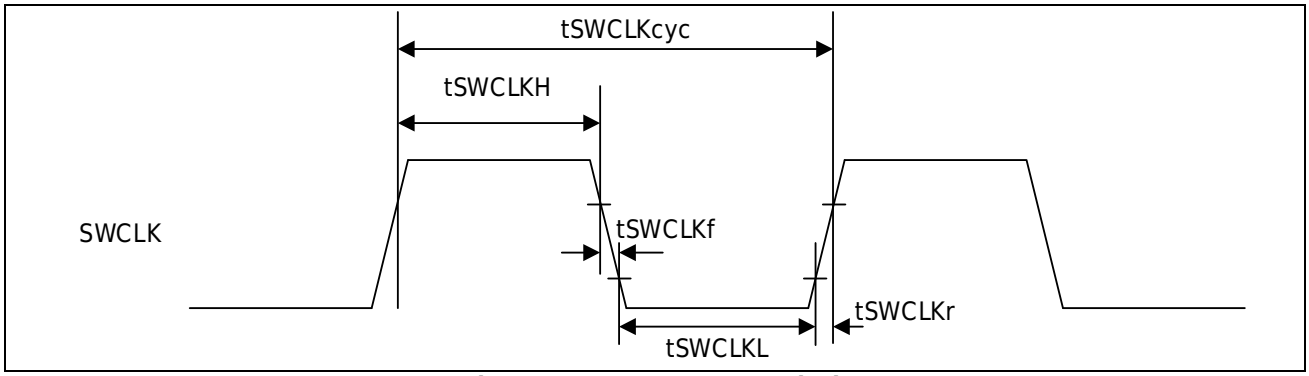


Figure 3-27 SWD SWCLK clock

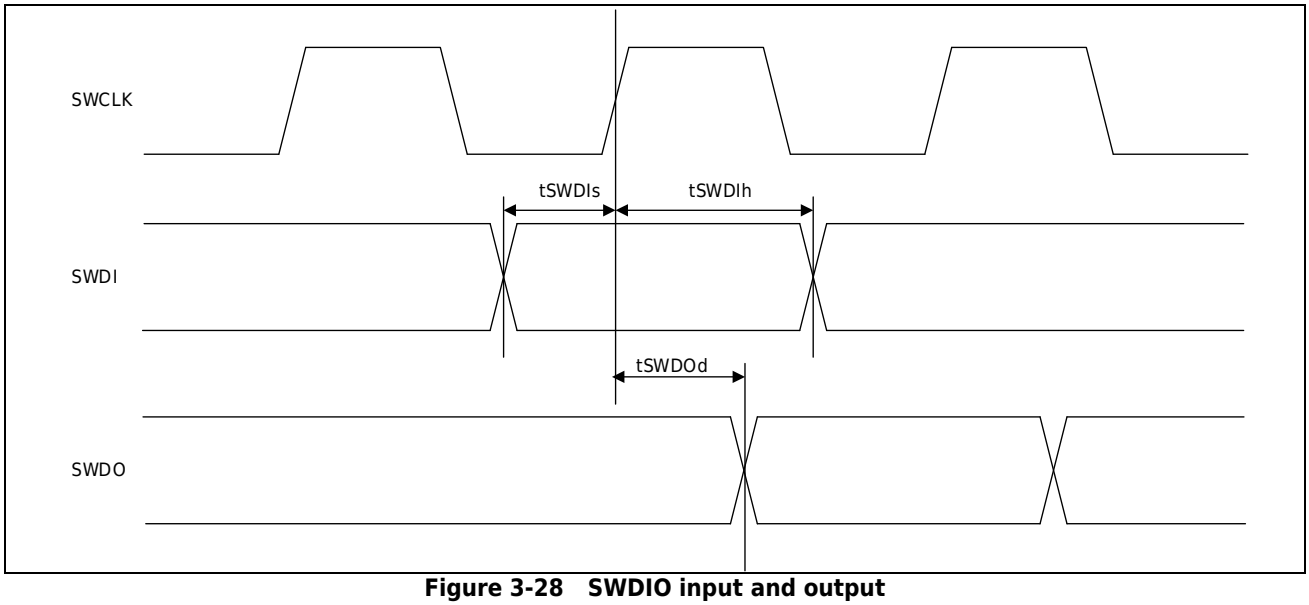


Figure 3-28 SWDIO input and output

3.3.23 ETM interface features

Table 3-50 ETM interface features

Synbol	Item	Min	Typ	Max	Unit
$t_{TRCLKcyc}$	TRACECK clock cycle time	20	-	-	ns
t_{TRCKH}	TRACECK clock high pulse width	7	-	-	ns
t_{TRCKL}	TRACECK clock low pulse width	7	-	-	ns
t_{TRCKr}	TRACECK clock rise time	-	-	2.5	ns
t_{TRCKf}	TRACECK clock fall time	-	-	2.5	ns
t_{TRDd}	TRACED[3:0] output delay time(1)	1.6	-	8.4	ns

1. Mass production test guarantee.

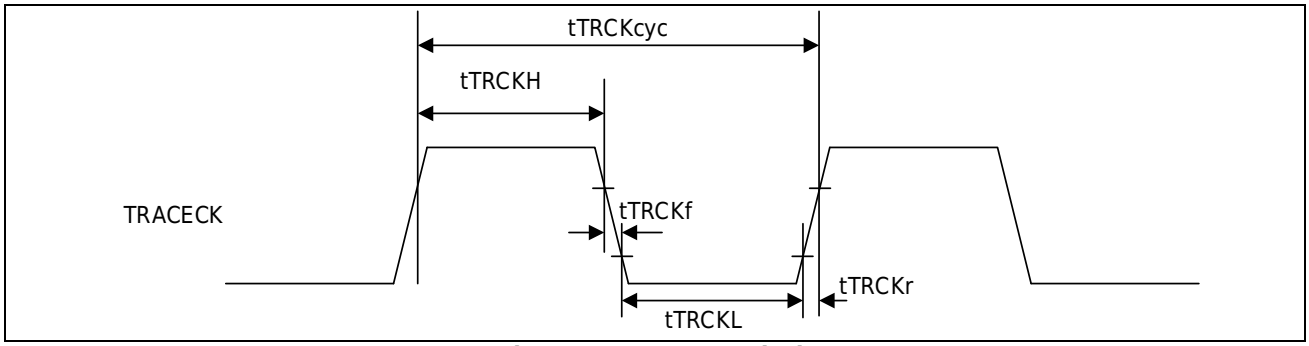


Figure 3-29 TRACE clock

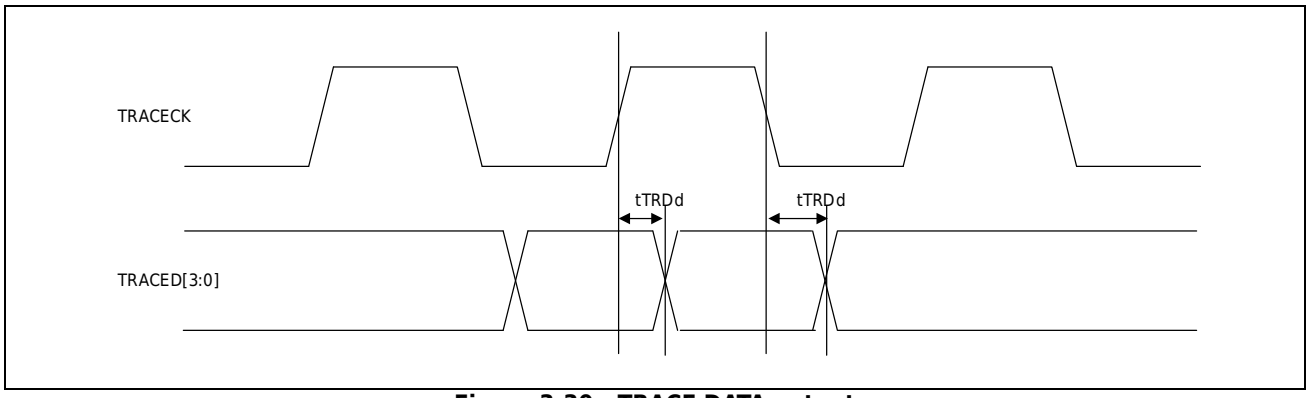


Figure 3-30 TRACE DATA output

3.3.24 12-bit ADC characteristic

Table 3-51 ADC characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{AVCC}	Power supply	-	1.8	-	3.6	V
V_{REFH}(1)	Positive reference voltage	-	1.8	-	V_{AVCC}	V
f_{ADC}	ADC conversion clock frequency	In high-speed working mode V_{AVCC} =2.4 ~3.6V	1	-	60	MHz
		In low speed working mode V_{AVCC} =1.8 ~2.4V	1	-	30	
		Ultra-low speed working mode	1	-	8	
V_{AIN}	Conversion voltage range	-	V_{REFL}	-	V_{REFH}	V
R_{AIN}	External input impedance	Refer to Formula 1 for details	-	-	50	kΩ
R_{ADC}	Sampling switch resistance	-	-	3	6	kΩ
C_{ADC}	Internal sampling and retention capacitance	-	-	4	7	Pf
t_D	Trigger conversion delay	f_{ADC} = 60 MHz	-	-	0.3	μs

Table 3-52 ADC Characteristics (continued)

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
t_S	Sampling time	f_{ADC} = 60MHz	0.183	-	4.266	μs
			11	-	255	$1/f_{ADC}$
t_{CONV}	Single-channel total conversion time (Including sampling time)	f_{ADC} = 60 MHz 12 bit resolution	0.4	-	-	μs
		f_{ADC} = 60 MHz 10-bit resolution	0.37	-	-	μs
		f_{ADC} = 60 MHz 8-bit resolution	0.34	-	-	μs
		20 to 268 (Sampling time Ts+ successively approaching n-bit resolution+1)				$1/f_{ADC}$
f_S	Sampling rate f_{ADC} = 60 MHz	12-Bit Resolution Single ADC	-	-	2.5	Msps
t_{ST}	Power-on time	-	-	1	2	μs

1. 0≤VAVCC-VREFH≤1.2 V

Formula 1: RAIN maximum formula

$$R_{AIN} = \frac{k-1}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Formula 1) is used to determine the maximum external impedance to make the error lower than 1/4 LSB. Where N = 12 (12 bit resolution), k is the number of sampling cycles defined in the ADC _ SSTR register.

Table 3-53 ADC123_IN0~3, ADC12_IN4~9, ADC12_IN14~15, ADC3_IN16~19 input channel accuracy @ f_{ADC} =60MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	f_{ADC}=60MHz Input source impedance <1 KΩ V_{REFH} =V_{AVCC}=2.4 ~3.6V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D	Differential Nonlinear Error		±1	±3	LSB
E_L	Integral nonlinear error		±1.5	±4	LSB

Table 3-54 ADC123_IN0~3, ADC12_IN4~9, ADC12_IN14~15, ADC3_IN16~19 input channel accuracy @ f_{ADC} =8/30MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	f_{ADC}=8/30MHz Input source impedance <1KΩ V_{REFH} =V_{AVCC}=1.8V	±4.5	±6	LSB
E_O	Offset error		±3.5	±6	LSB
E_G	Gain error		±3.5	±6	LSB
E_D(1)	Differential Nonlinear Error		±1	±3	LSB
E_L(1)	Integral nonlinear error		±1.5	±4	LSB

1. Guarantee of mass production test.

Table 3-55 ADC123_IN0~3, ADC12_IN4~9, ADC12_IN14~15, ADC3_IN16~19 Input Channel Accuracy @ f_{ADC} =60MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	significant digits	f_{ADC} = 60MHz Input signal frequency = 2kHz Input source impedance = 0ohm V_{REFH} =V_{AVCC}=2.4 ~3.6V	10.5	-	Bits
SINAD	Signal-to-noise harmonic ratio		64.3	-	dB
SNR	signal to noise ratio		64.4	-	dB
THD	total harmonic distortion		-	-78.1	dB

Table 3-56 ADC123_IN0~3, ADC12_IN4~9, ADC12_IN14~15, ADC3_IN16~19 Input Channel Accuracy @ f_{ADC} =8/30MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	significant digits	f_{ADC} = 8/30MHz Input signal frequency = 2kHz Input source impedance = 0ohm V_{REFH} =V_{AVCC}=1.8V	10.6	-	Bits
SINAD	Signal-to-noise harmonic ratio		67.0	-	dB
SNR	signal to noise ratio		67.1	-	dB
THD	total harmonic distortion		-	-75.1	dB

Table 3-57 ADC12_IN10~13, ADC3_IN4~15 input channel accuracy @f_{ADC} =60MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	f_{ADC} = 60MHz Input source impedance <1KΩ V_{REFH} =V_{AVCC}=2.4 ~3.6V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D	Differential Nonlinear Error		±1.5	±3	LSB
E_L	Integral nonlinear error		±2.0	±4	LSB

Table 3-58 ADC12_IN10~13, ADC3_IN4~15 input channel accuracy @ f_{ADC} =30MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	f_{ADC} = 8/30MHz Input source impedance <1KΩ V_{REFH} =V_{AVCC}=1.8V	±5.5	±7	LSB
E_O	Offset error		±4.5	±7	LSB
E_G	Gain error		±4.5	±7	LSB
E_D(1)	Differential Nonlinear Error		±1.5	±3	LSB
E_L(1)	Integral nonlinear error		±2.0	±4	LSB

1. Guarantee of mass production test.

Table 3-59 ADC12_IN10~12, ADC3_IN4~15 Input Channel Input Channel Dynamic Accuracy @f_{ADC} =60MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	significant digits	f_{ADC} = 60MHz Input signal frequency = 2kHz Input source impedance = 0ohm V_{REFH} =V_{AVCC}=2.4 ~3.6V	10.5	-	Bits
SINAD	Signal-to-noise harmonic ratio		64.4	-	dB
SNR	signal to noise ratio		64.4	-	dB
THD	total harmonic distortion		-	-80.3	dB

Table 3-60 ADC12_IN10~13, ADC3_IN4~15 input channel input channel dynamic accuracy @ f_{ADC} =8/30MHz

Symbol	Parameter	Conditions	Minimum value	Maximum value	Unit
ENOB	significant digits	f_{ADC} = 8/30MHz Input signal frequency = 2kHz Input source impedance = 0ohm V_{REFH} =V_{AVCC}=1.8V	10.6	-	Bits
SINAD	Signal-to-noise harmonic ratio		66.6	-	dB
SNR	signal to noise ratio		66.8	-	dB
THD	total harmonic distortion		-	-79.4	dB

Table 3-61 ADC+Sample and Hold Circuit Channel Accuracy @ f_{ADC} =60MHz

Symbol	Parameter	Conditions	Typical value	Maximum value	Unit
E_T	Absolute error	f_{ADC} = 60MHz Input source impedance = 1KΩ V_{REFH} =V_{AVCC}=2.7 ~3.6V	±6.0	±8.0	LSB
E_O	Offset error		±6.0	±8.0	LSB
E_G	Gain error		±6.0	±8.0	LSB
E_D	Differential Nonlinear Error		±2	±3	LSB
E_L	Integral nonlinear error		±3	±4	LSB

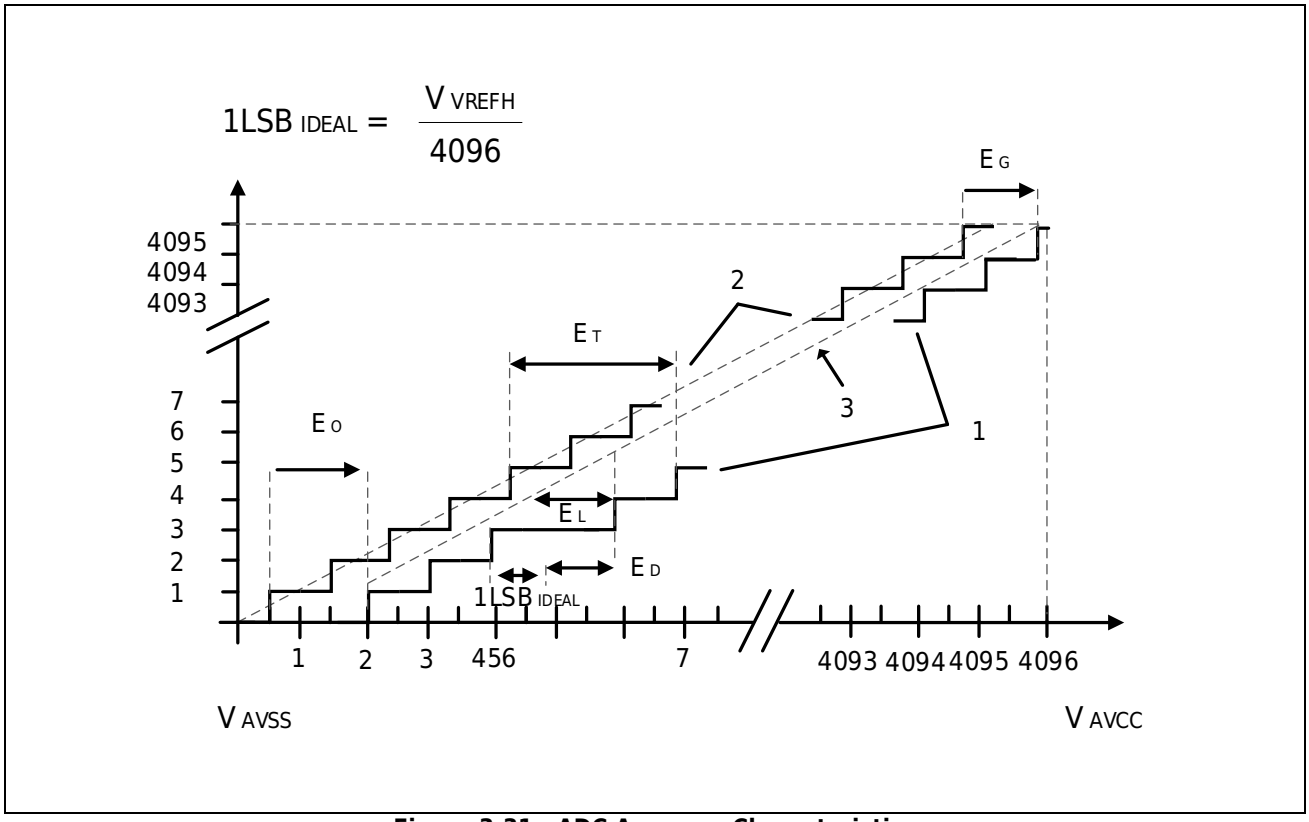


Figure 3-31 ADC Accuracy Characteristics

1. Refer to also table above.
2. Examples of actual transmission curves.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = total unadjusted error: Maximum deviation between actual and ideal transmission curves.

   E_O = offset error: Deviation between the first actual transition and the first ideal transition.

   E_G = gain error: Deviation between the last ideal conversion and the last actual conversion.

   E_D = differential nonlinearity error: Maximum deviation between actual step and ideal value.

   E_L = integral nonlinearity error: The maximum deviation between any actual transformation and the endpoint correlation line.

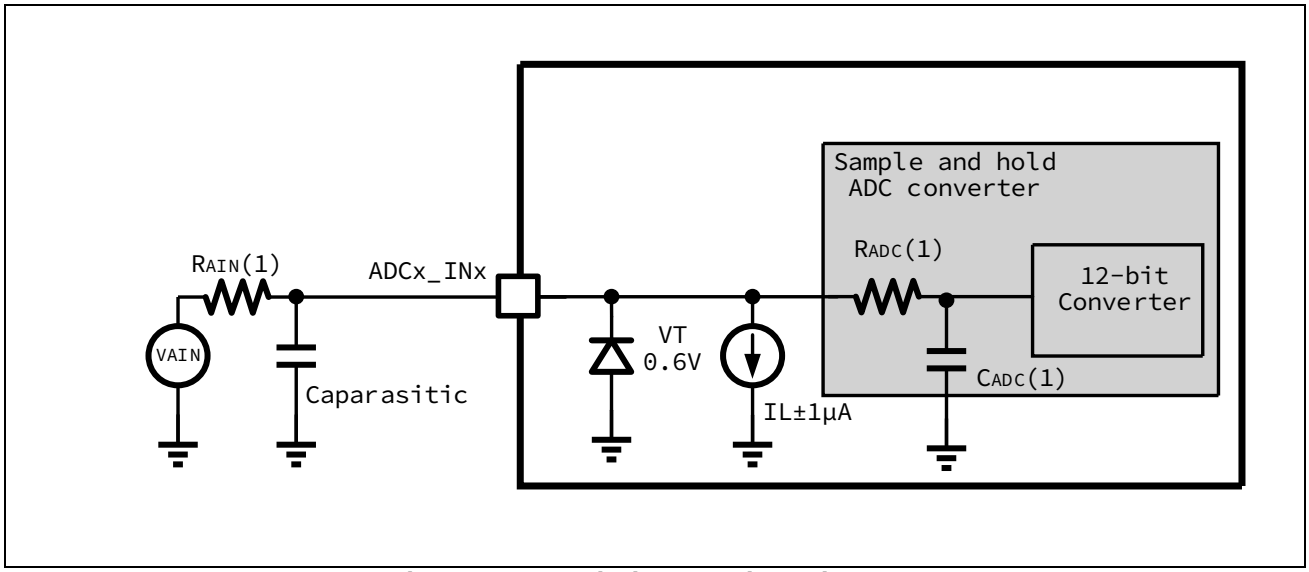


Figure 3-32 Typical Connection Using ADC

1. About R_{AIN} , R_{ADC} and C_{ADC} value information, see Table 3-51.
2. Cparasitic means PCB capacitance (depending on soldering and PCB routing quality) and pad capacitance (about 5 Pf). Higher Cparasitic value will result in lower conversion accuracy. To solve this problem, the F_{adc} .

General PCB design guidelines

The power supply should be decoupled as shown in the diagram below, depending on whether VREFH is connected to AVCC and the number of AVCC pins. The 0.1μF capacitor should be a (high quality) ceramic capacitor. These capacitors should be as close as possible to the core piece.

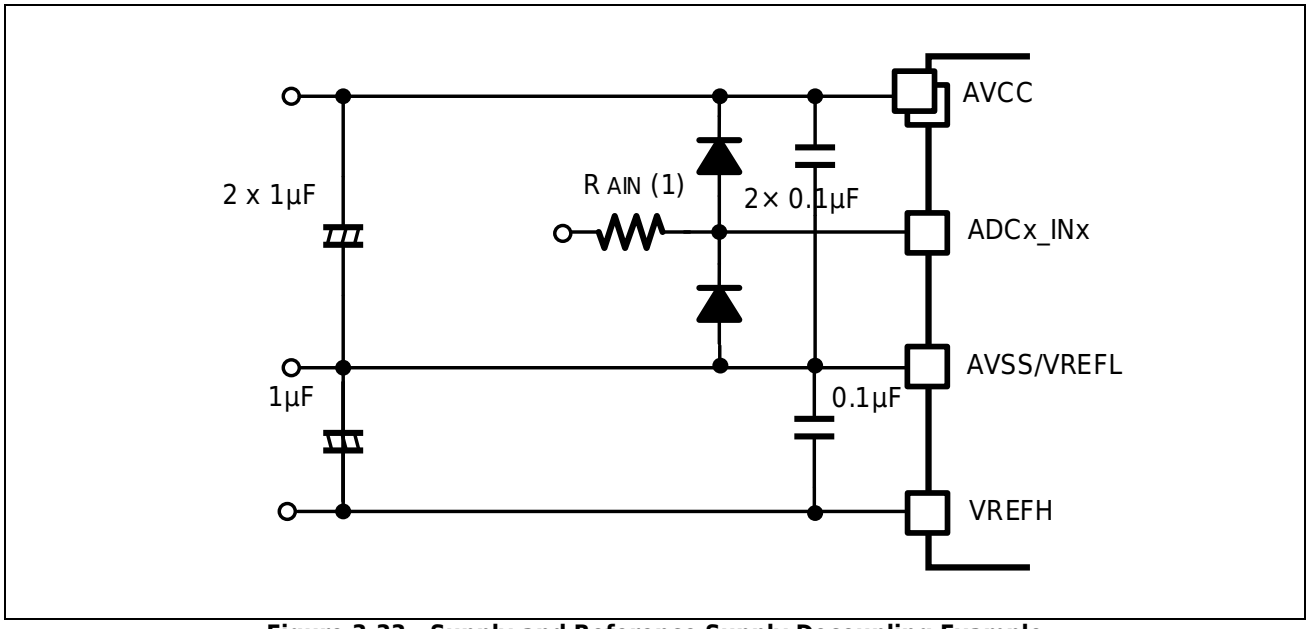


Figure 3-33 Supply and Reference Supply Decoupling Example

3.3.25 12-bit DAC characteristics

Table 3-62 12-bit DAC port output enabled and output amplifier enabled characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
Aref	Reference Supply Voltage (V_{REFH})	= V_{AVCC}	1.8	3.3	3.6	V
AO	Output voltage range	-	0.2	-	Aref-0.2	-
RL	Load Resistance	-	5	-		kΩ
CL	Load capacitance	-		-	50	Pf
DNL(1)	Differential nonlinearity error (deviation between two consecutive codes - 1LSB)	-	-	-	3(1)	LSB
INL(1)	Integral nonlinearity error (difference between the value measured at code I and the value at code I on the line between code 0 and the last code 4095)	-	-	-	5(1)	LSB
OE	Offset error (difference between measured value at code (0x800) and ideal value VREF+/2)	-	-	-	±15	LSB
GE	Gain error	-	-	-	±1	%
T_{st}	Settling time (full scale: Applies to 12-bit input code conversion between the lowest input code and the highest input code until the DAC output reaches the final value ±4LSB)	-	-	1.2	2.1	μs
Iavcc	Analog supply current (quiescent current, no load)	-	-	604	800	μA
Iaref	Reference supply current (quiescent current)	-	-	161	270	μA

1. Guarantee of mass production test.

Table 3-63 12-bit DAC port output enabled and output amplifier disabled characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
Aref	Reference supply voltage	= V_{AVCC}	1.8	3.3	3.6	V
AO	Output voltage range	-	0	-	Aref-1LSB	V
CL	Load capacitance	-	-	-	20	Pf
RO	output resistance	-	-	8.6	12	kΩ
DNL	Differential nonlinearity error (deviation between two consecutive codes - 1LSB)	-	-	-	±2	LSB
TUE	total unadjustable error	-	-	-	±24	LSB
T_{st}	Settling time (applies to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value ±4LSB, CL=10Pf)	-	-	0.9	1.2	μs
Iavcc	Analog supply current (quiescent current)	-	-	0.1	2	μA
Iaref	Reference supply current (quiescent current)	-	-	146	260	μA

Table 3-64 12-bit DAC port output disabled and output amplifier disabled characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
Aref	Reference supply voltage	= V_{AVCC}	1.8	3.3	3.6	V
AO	Output voltage range		0		Aref-1LSB	
DNL	Differential nonlinearity error (deviation between two consecutive codes - 1LSB)	-	-	-	±2	LSB
TUE	total unadjustable error	-	-	-	±5	LSB
T_{st}	Settling time (applies to 12-bit input code conversion between the lowest input code and the highest input code until the DAC output reaches the final value ±1 LSB, Vavcc≥2.7)	-	-	65.3	81	ns
	Settling time (applies to 12-bit input code conversion between the lowest input code and the highest input code when the DAC output reaches the final value ±32 LSB, Vavcc≥2.7)	-	-	36	44.9	ns
	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches final value ±1 LSB, Vavcc<2.7)	-	-	-	83.82	ns
	Settling Time (Applies to 12-bit input code transition between lowest input code and highest input code until DAC output reaches final value ±32 LSB, Vavcc<2.7)	-	-	-	48.55	ns
Iavcc	Analog supply current (quiescent current)	-	-	0.1	2	μA
Iaref	Reference supply current (quiescent current)	-	-	146	260	μA

3.3.26 Temperature Sensor

Table 3-65 Temperature sensor characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
T_L	temperature linearity	-	-2	-	+2	°C
T_E	Absolute Accuracy (1)	25°C, 105°C two-point calibration	-2	-	+2	°C

1. Actual characteristics are related to the accuracy of the calibration point temperature. If the preset data calibration of the chip is used, the characteristics are not guaranteed due to the temperature deviation of the mass production test environment.

3.3.27 Comparator characteristics

Table 3-66 Comparator Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{AVCC}	Analog supply voltage	-	1.8	3.3	3.6	V
V_I	Input voltage range	-	0	-	V_{AVCC}	V
T_{cmp}	Comparison time	Comparator resolution voltage = 100 mV	-	30	50	ns
T_{set}	Input channel switching stabilization time	-	-	100	200	ns

3.3.28 EXMC features

Table 3-67 EXMC features

Symbol	Parameter	Min	Typ	Max	Unit
t_add_d	Address line output delay time (2.7V~3.6V) (1)	-	-	12	ns
	Address line output delay time (1.8V~2.7V)	-	-	18	ns
t_data_d	Data line output delay time (2.7V~3.6V) (1)	-	-	12	ns
	Data line output delay time (1.8V~2.7V)	-	-	18	ns
t_ce_d	CE output delay time (2.7V~3.6V) (1)	-	-	9	ns
	CE output delay time (1.8V~2.7V)	-	-	12	ns
t_we_d	WE output delay time (2.7V~3.6V) (1)	-	-	9	ns
	WE output delay time (1.8V~2.7V)	-	-	12	ns
t_oe_d	OE output delay time (2.7V~3.6V) (1)	-	-	9	ns
	OE output delay time (1.8V~2.7V)	-	-	12	ns
t_baa_d	BAA output delay time (2.7V~3.6V) (1)	-	-	9	ns
	BAA output delay time (1.8V~2.7V)	-	-	12	ns
t_adv_d	ADV output delay time (2.7V~3.6V) (1)	-	-	9	ns
	ADV output delay time (1.8V~2.7V)	-	-	12	ns
t_ale_d	ALE output delay time (2.7V~3.6V) (1)	-	-	9	ns
	ALE output delay time (1.8V~2.7V)	-	-	12	ns
t_data_s	Data line input Setup time (2.7V~3.6V) (1)	24	-	-	ns
	Data line input Setup time (1.8V~2.7V)	28	-	-	ns
t_data_h	Data line input Hold time (1)	0	-	-	ns
t_rb_s	RB input Setup time (2.7V~3.6V) (1)	24	-	-	ns
	RB input Setup time (1.8V~2.7V)	28	-	-	ns
t_rb_h	RB input Hold time (1)	0	-	-	ns

1. Mass production test guarantee

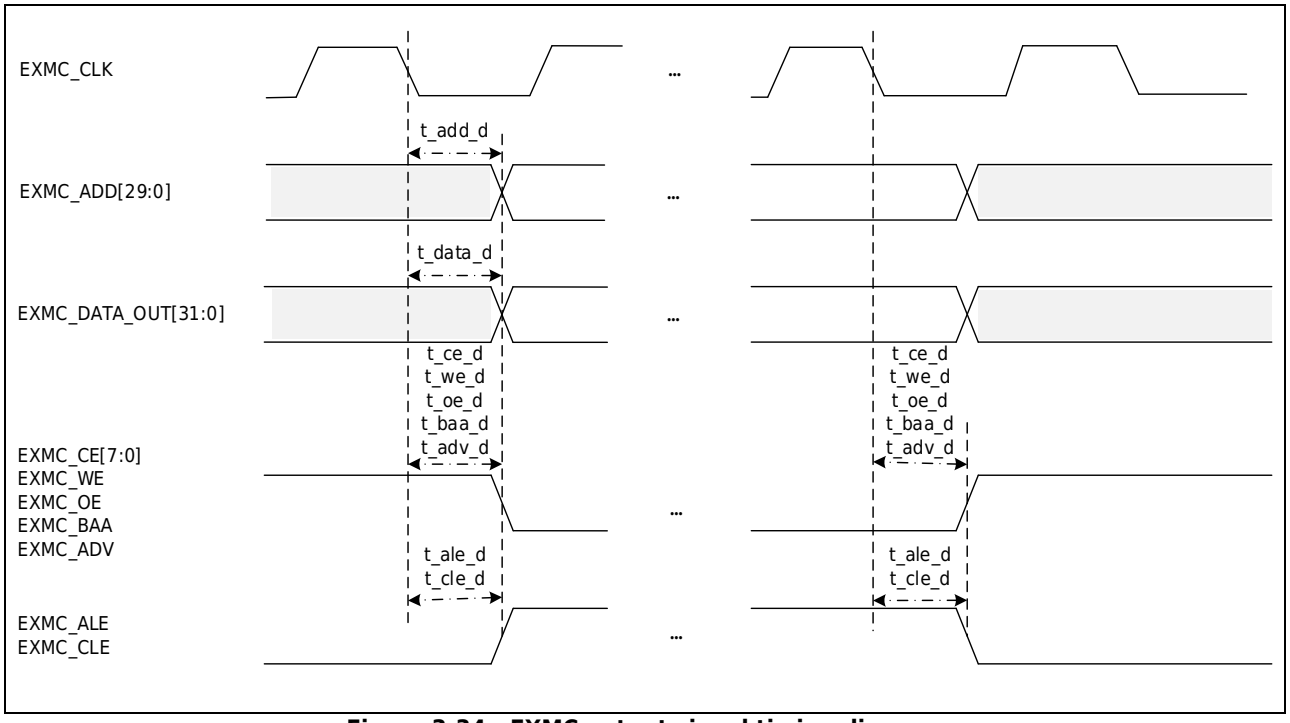


Figure 3-34 EXMC output signal timing diagram

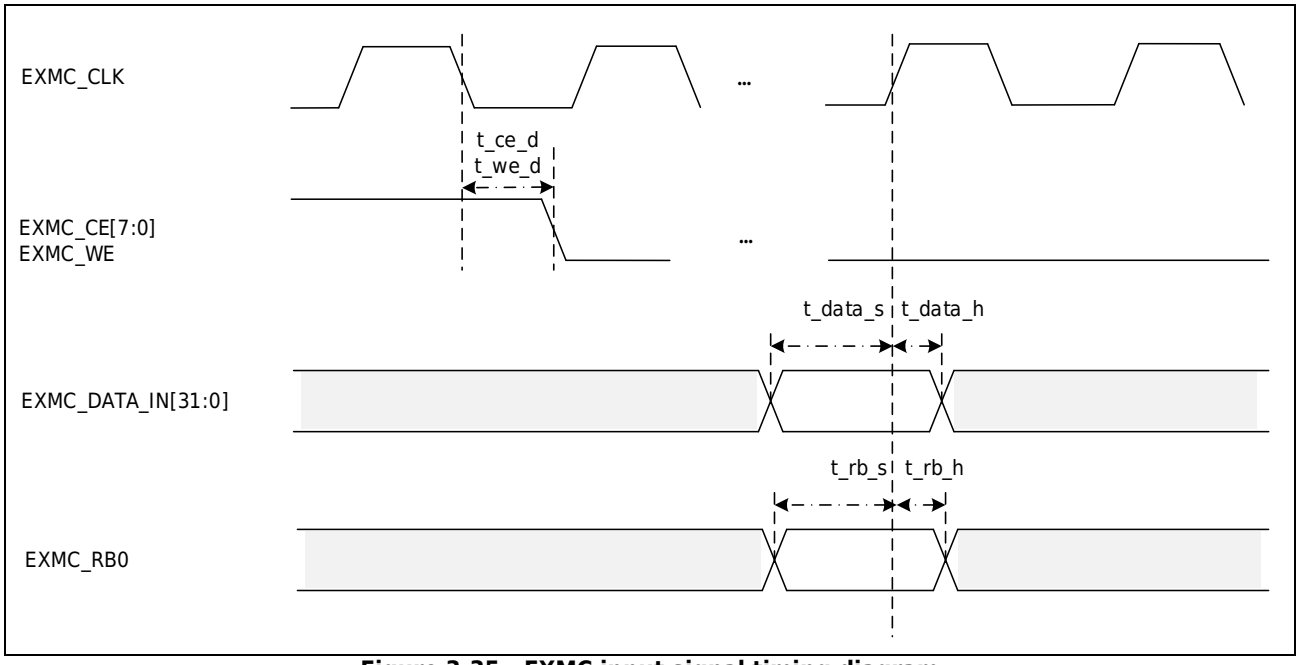


Figure 3-35 EXMC input signal timing diagram

3.3.29 DVP features

Table 3-68 DVP features

Symbol	Parameter	Min	Typ	Max	Unit
t_pixclk_s	Input data DVP_PIXCLK Setup time (2.7V~3.6V)	6	-	-	ns
	Input data DVP_PIXCLK Setup time (1.8V~2.7V)	9	-	-	ns
t_pixclk_h	Input data DVP_PIXCLK Hold time (2.7V~3.6V)	6	-	-	ns
	Input data DVP_PIXCLK Hold time (1.8V~2.7V)	9	-	-	ns
t_data_s	Input data DVP_DATA Setup time (2.7V~3.6V) (1)	2.5	-	-	ns
	Input data DVP_DATA Setup time (1.8V~2.7V)	4	-	-	ns
t_data_h	Input data DVP_DATA Hold time (2.7V~3.6V) (1)	2	-	-	ns
	Input data DVP_DATA Hold time (1.8V~2.7V)	3	-	-	ns
t_vsync_s	Input data DVP_VSYNC Setup time (2.7V~3.6V) (1)	2.5	-	-	ns
	Input data DVP_VSYNC Setup time (1.8V~2.7V)	4	-	-	ns
t_vsync_h	Input data DVP_VSYNC Hold time (2.7V~3.6V) (1)	1.5	-	-	ns
	Input data DVP_VSYNC Hold time (1.8V~2.7V)	3	-	-	ns
t_hsync_s	Input data DVP_HSYNC Setup time (2.7V~3.6V) (1)	2.5	-	-	ns
	Input data DVP_HSYNC Setup time (1.8V~2.7V)	4	-	-	ns
t_hsync_h	Input data DVP_HSYNC Hold time (2.7V~3.6V) (1)	1.5	-	-	ns
	Input data DVP_HSYNC Hold time (1.8V~2.7V)	3	-	-	ns

1. Mass production test guarantee

The following figure takes the setting conditions of DVP_VSYNC and DVP_HSYNC as the synchronization interval and the falling edge of DVP_PIXCLK to collect data as an example.

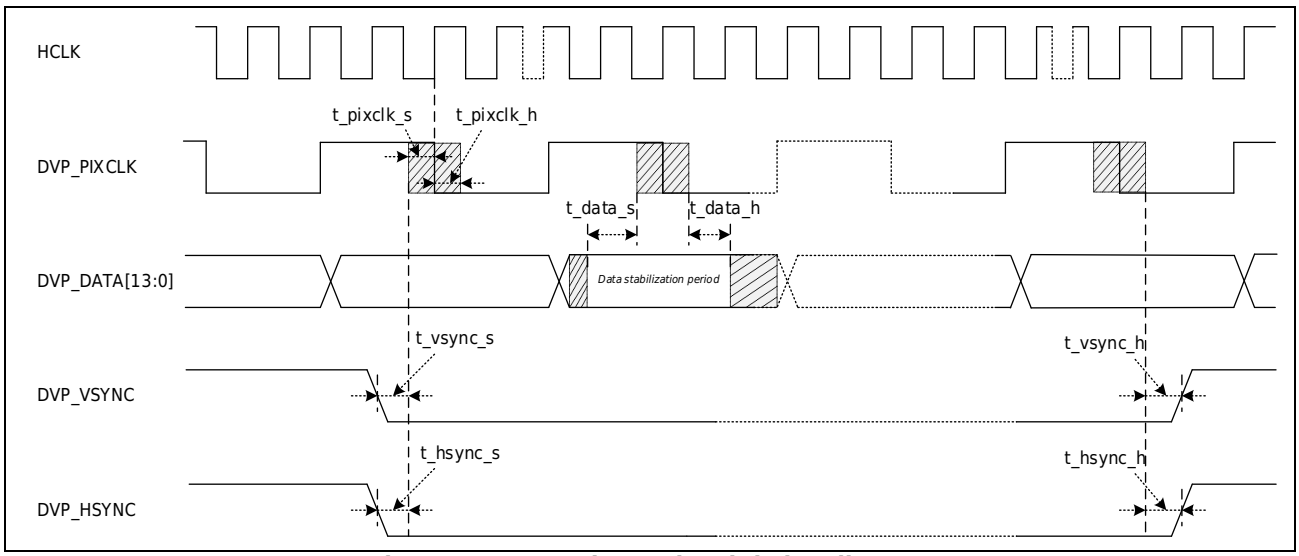


Figure 3-36 DVP input signal timing diagram

3.3.30 SD/SDIO MMC Card host interface (SDIO) features

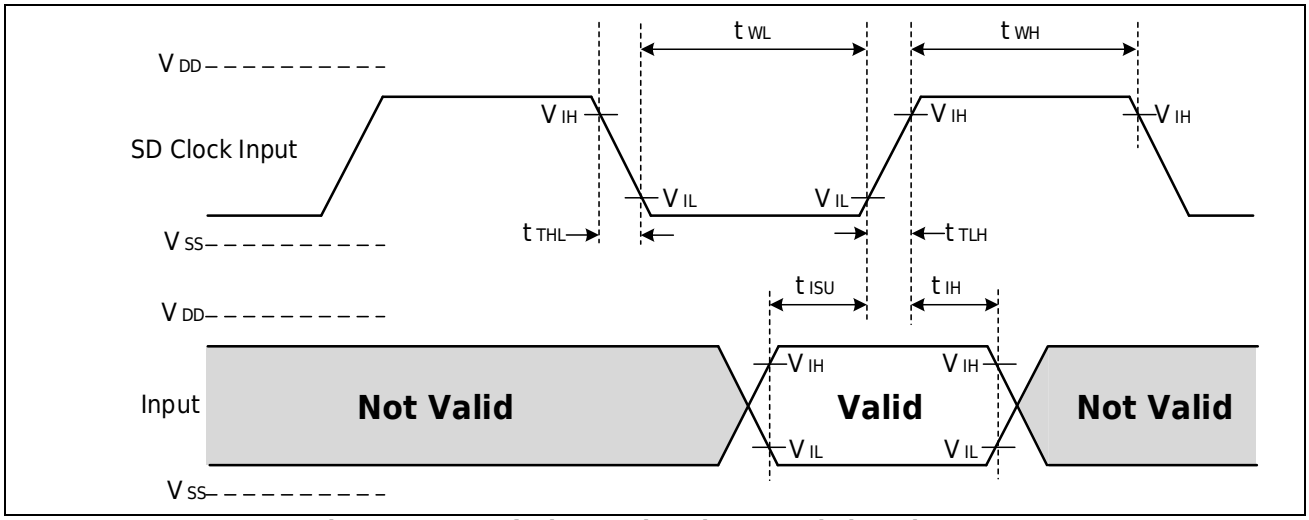


Figure 3-37 Default Speed Mode Input Timing Diagram

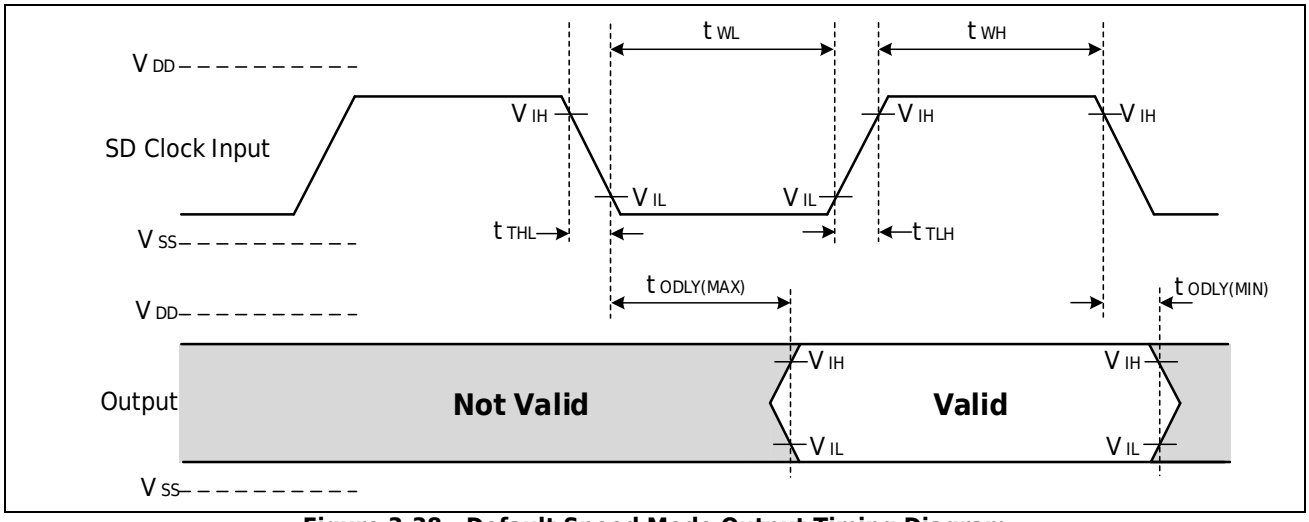


Figure 3-38 Default Speed Mode Output Timing Diagram

Table 3-69 Default Speed Mode Timing Parameters

Symbol	Parameter	Minimum value	Maximum value	Unit	Remark
-	Operating Voltage	1.8	3.6	V	
f_{PP}	transfer mode clock frequency	-	25	MHz	Load C = 30 Pf
f_{OD}	Card Identification Mode Clock Frequency	-	400	kHz	Load C = 30 Pf
t_{WL}	clock low time	10	-	ns	Load C = 30 Pf
t_{WH}	clock high time	10	-	ns	Load C = 30 Pf
t_{TLH}	clock rise time	-	10	ns	Load C = 30 Pf
t_{THL}	clock fall time	-	10	ns	Load C = 30 Pf
t_{ISU}	Data Input Setup Time (1)	5	-	ns	Load C = 30 Pf
t_{IH}	Data Input Hold Time (1)	14	-	ns	Load C = 30 Pf
t_{ODLY}	Data output delay (1)	1	14	ns	Load C = 30 Pf

1. Mass production test guarantee

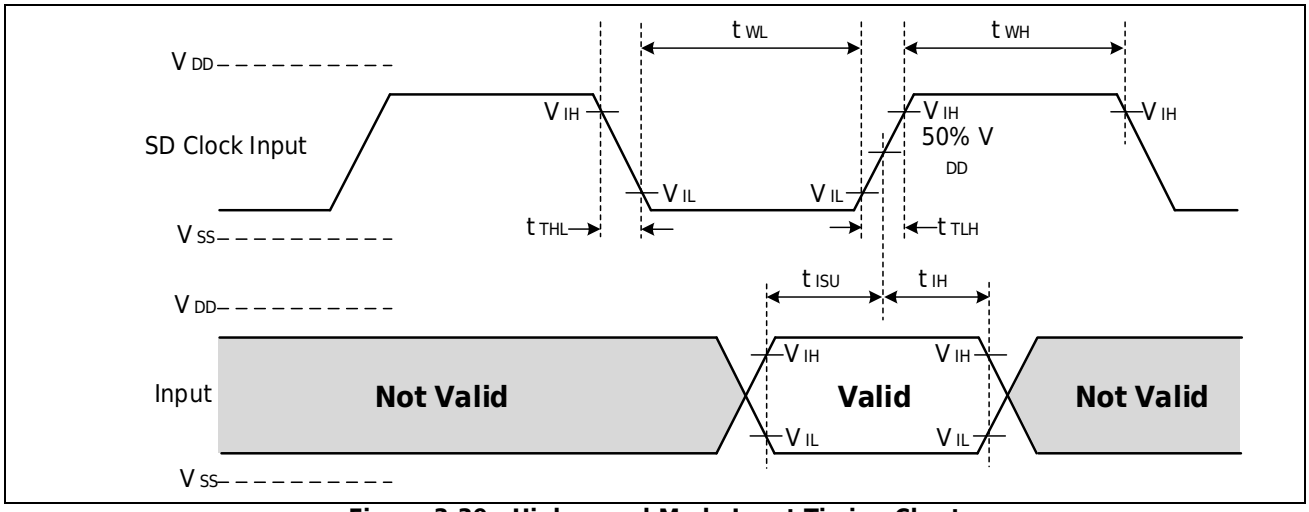


Figure 3-39 High-speed Mode Input Timing Chart

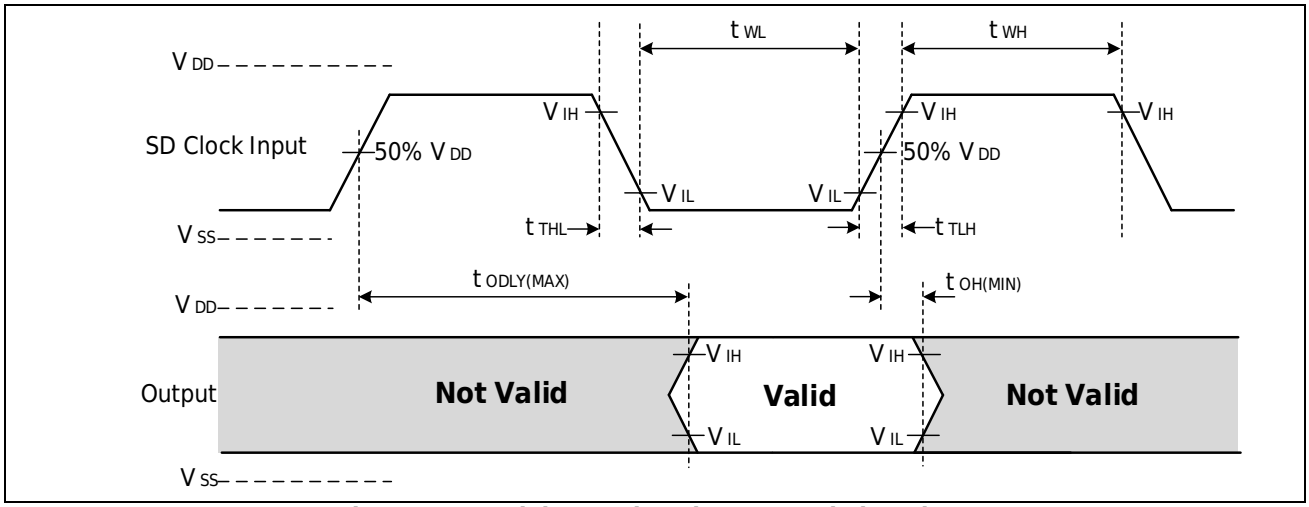


Figure 3-40 High Speed Mode Output Timing Chart

Table 3-70 High Speed Mode Timing Parameters

Symbol	Parameter	Minimum value	Maximum value	Unit	Remark
-	Operating Voltage	1.8	3.6	V	
f_{PP}	transfer mode clock frequency	-	50	MHz	Load C = 30 Pf
f_{OD}	Card Identification Mode Clock Frequency	-	400	kHz	Load C = 30 Pf
t_{WL}	clock low time	7	-	ns	Load C = 30 Pf
t_{WH}	clock high time	7	-	ns	Load C = 30 Pf
t_{TLH}	clock rise time	-	3	ns	Load C = 30 Pf
t_{THL}	clock fall time	-	3	ns	Load C = 30 Pf
t_{ISU}	Data Input Setup Time (1)	5	-	ns	Load C = 30 Pf
t_{IH}	Data Input Hold Time (1)	14	-	ns	Load C = 30 Pf
t_{ODLY}	Data output delay (1)	-	14	ns	Load C = 30 Pf
t_{OH}	Data output hold time	3	-	ns	Load C = 30 Pf

1. Mass production test guarantee

3.3.31 Adjustable Gain Amplifier Characteristics

Table 3-71 Adjustable Gain Amplifier Characteristics

Symbol	Parameter		Conditions	Minimum value	Typical value	Maximum value	Unit
V_{AVCC}	Analog supply voltage		-	1.8	3.3	3.6	V
V_{OS} (1)	Input offset voltage		-	-8	-	8	Mv
V_I	Input voltage range		-	0.1*V_{AVCC} /Gain	-	0.9*V_{AVCC} /Gain	V
G_E	Gain error	Use external port PGAVSS as PGA negative input	Gain=2 (1)	-1	-	1	%
			Gain=2.133	-1	-	1	%
			Gain=2.286	-1	-	1	%
			Gain=2.667	-1	-	1	%
			Gain=2.909	-1	-	1	%
			Gain=3.2	-1.5	-	1.5	%
			Gain=3.556	-1.5	-	1.5	%
			Gain=4.0	-1.5	-	1.5	%
			Gain=4.571	-2	-	2	%
			Gain=5.333	-2	-	2	%
			Gain=6.4	-3.0	-	3.0	%
			Gain=8	-3.0	-	3.0	%
			Gain=10.667	-4.0	-	4.0	%
			Gain=16	-4.0	-	4.0	%
			Gain=32 (1)	-7.0	-	7.0	%
		Use the internal analog ground AVSS as the negative input of the PGA	Gain=2 (1)	-2	-	2	%
			Gain=2.133	-2	-	2	%
			Gain=2.286	-2	-	2	%
			Gain=2.667	-2	-	2	%
			Gain=2.909	-2	-	2	%
			Gain=3.2	-2.5	-	2.5	%
			Gain=3.556	-2.5	-	2.5	%
			Gain=4.0	-2.5	-	2.5	%
			Gain=4.571	-3.0	-	3.0	%
			Gain=5.333	-3.0	-	3.0	%
			Gain=6.4	-4.0	-	4.0	%
			Gain=8	-4.0	-	4.0	%
			Gain=10.667	-5.0	-	5.0	%
			Gain=16	-5.0	-	5.0	%
			Gain=32 (1)	-8.0	-	8.0	%

1. Guarantee of mass production test.

3.3.32 VBAT features

Table 3-72 Backup Battery Domain Electrical Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
V_{BATLVD}	Low voltage monitoring voltage	PWC_PWRC4.VBATREFSEL=0	1.70	1.80	1.90	V
		PWC_PWRC4.VBATREFSEL=1	2.00	2.10	2.20	V

3.3.33 EIRQ Filtering Characteristics

Table 3-73 EIRQ Filtering Characteristics

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
W_{F_EIRQ}	EIRQ input filter width	INTC_NOCCR.NOCSEL = 00b	0.4	-	0.9	us
		INTC_NOCCR.NOCSEL = 01b	0.8	-	1.6	us
		INTC_NOCCR.NOCSEL = 10b	1.5	-	3.0	us
		INTC_NOCCR.NOCSEL = 11b	3.1	-	5.9	us

3.3.34 RX filter characteristics in USART1 STOP mode

Table 3-74 RX filter characteristics in USART1 STOP mode

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
W_{F_USART1}	USART1 input filter width	USART1_NFC.USART1_NFS = 00b	0.4	-	0.9	us
		USART1_NFC.USART1_NFS = 01b	0.8	-	1.6	us
		USART1_NFC.USART1_NFS = 10b	1.5	-	3.0	us
		USART1_NFC.USART1_NFS = 11b	3.1	-	5.9	us

3.3.35 Filtering Characteristics in USB On-Chip Full-Speed PHY STOP Mode

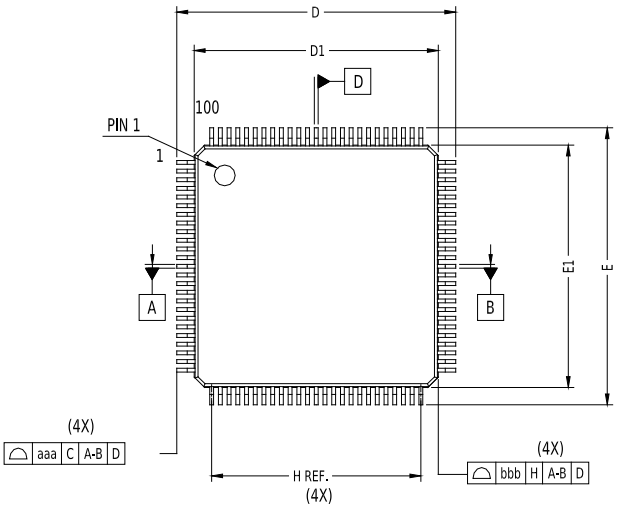
Table 3-75 Filtering Characteristics in USB On-Chip Full-Speed PHY STOP Mode

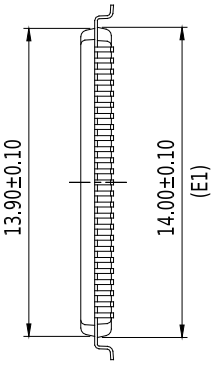
Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
W_{F_USB}	USB input filter width	USB_SYCTLREG.USBFS_NFS = 00b USB_SYCTLREG.USBHS_NFS = 00b	0.4	-	0.9	us
		USB_SYCTLREG.USBFS_NFS = 01b USB_SYCTLREG.USBHS_NFS = 01b	0.8	-	1.6	us
		USB_SYCTLREG.USBFS_NFS = 10b USB_SYCTLREG.USBHS_NFS = 10b	1.5	-	3.0	us
		USB_SYCTLREG.USBFS_NFS = 11b USB_SYCTLREG.USBHS_NFS = 11b	3.1	-	5.9	us

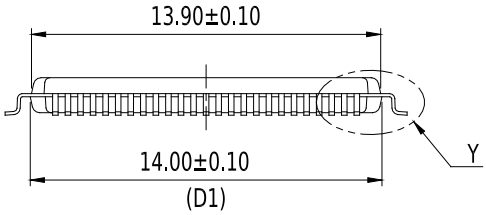
4 Package information

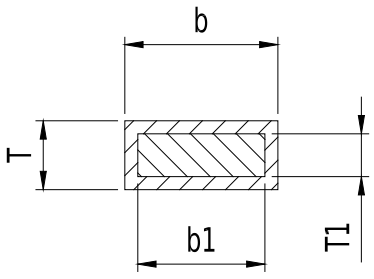
4.1 Package dimensions

LQFP100 package

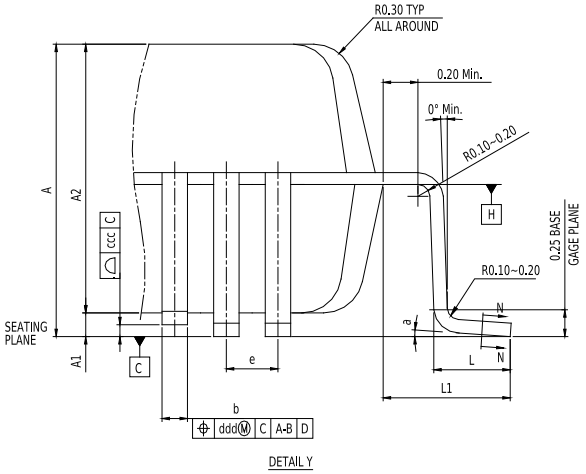








SECTION N-N



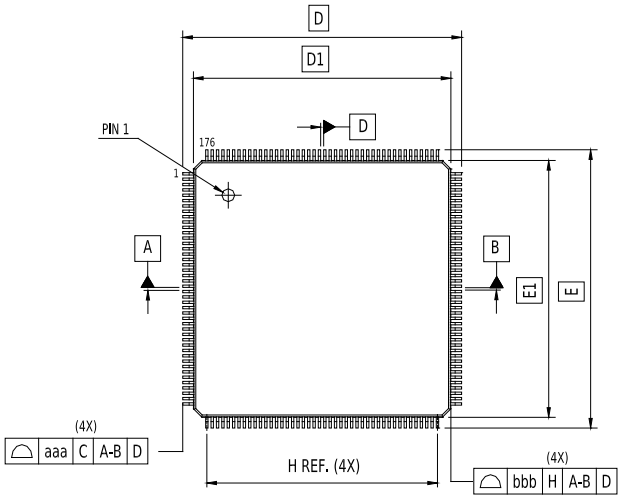
DIMENSION LIST (FOOTPRINT: 2.00)

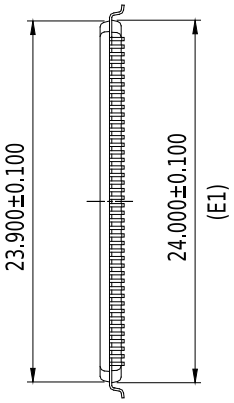
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.60	OVERALL HEIGHT
2	A1	0.10±0.05	STANDOFF
3	A2	1.40±0.05	PKG THICKNESS
4	D	16.00±0.20	LEAD TIP TO TIP
5	D1	14.00±0.10	PKG LENGTH
6	E	16.00±0.20	LEAD TIP TO TIP
7	E1	14.00±0.10	PKG WIDTH
8	L	0.60±0.15	FOOT LENGTH
9	L1	1.00 REF.	LEAD LENGTH
10	T	$0.15^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.03	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.22±0.05	LEAD WIDTH
14	b1	0.20±0.03	LEAD BASE METAL WIDTH
15	e	0.50 BASE	LEAD PITCH
16	H(REF.)	(12.00)	CUM. LEAD PITCH
17	aaa	0.20	PROFILE OF LEAD TIPS
18	bbb	0.20	PROFILE OF MOLD SURFACE
19	ccc	0.08	FOOT COPLANARITY
20	ddd	0.08	FOOT POSITION

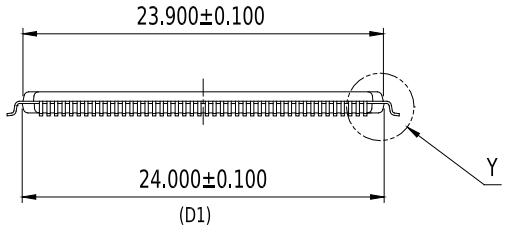
NOTE:

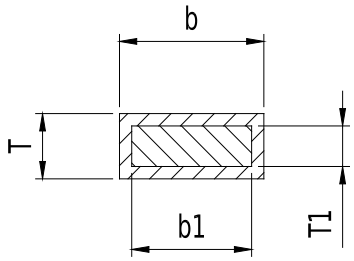
– Dimensions “D1” and “E1” do not include mold flash.

LQFP176 package

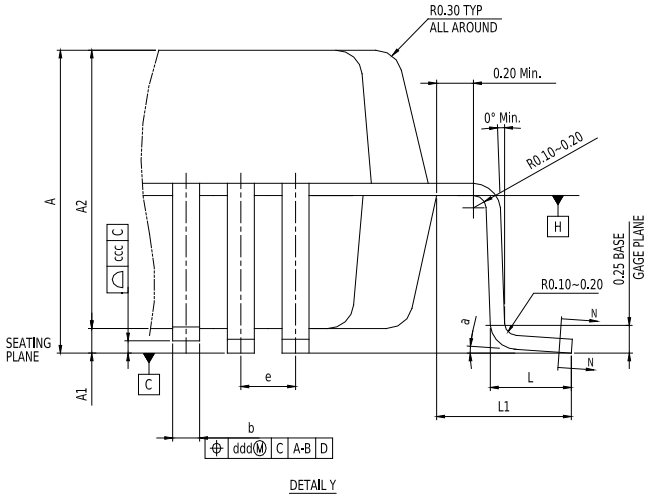








SECTION N-N



DIMENSION LIST (FOOTPRINT: 2.00)

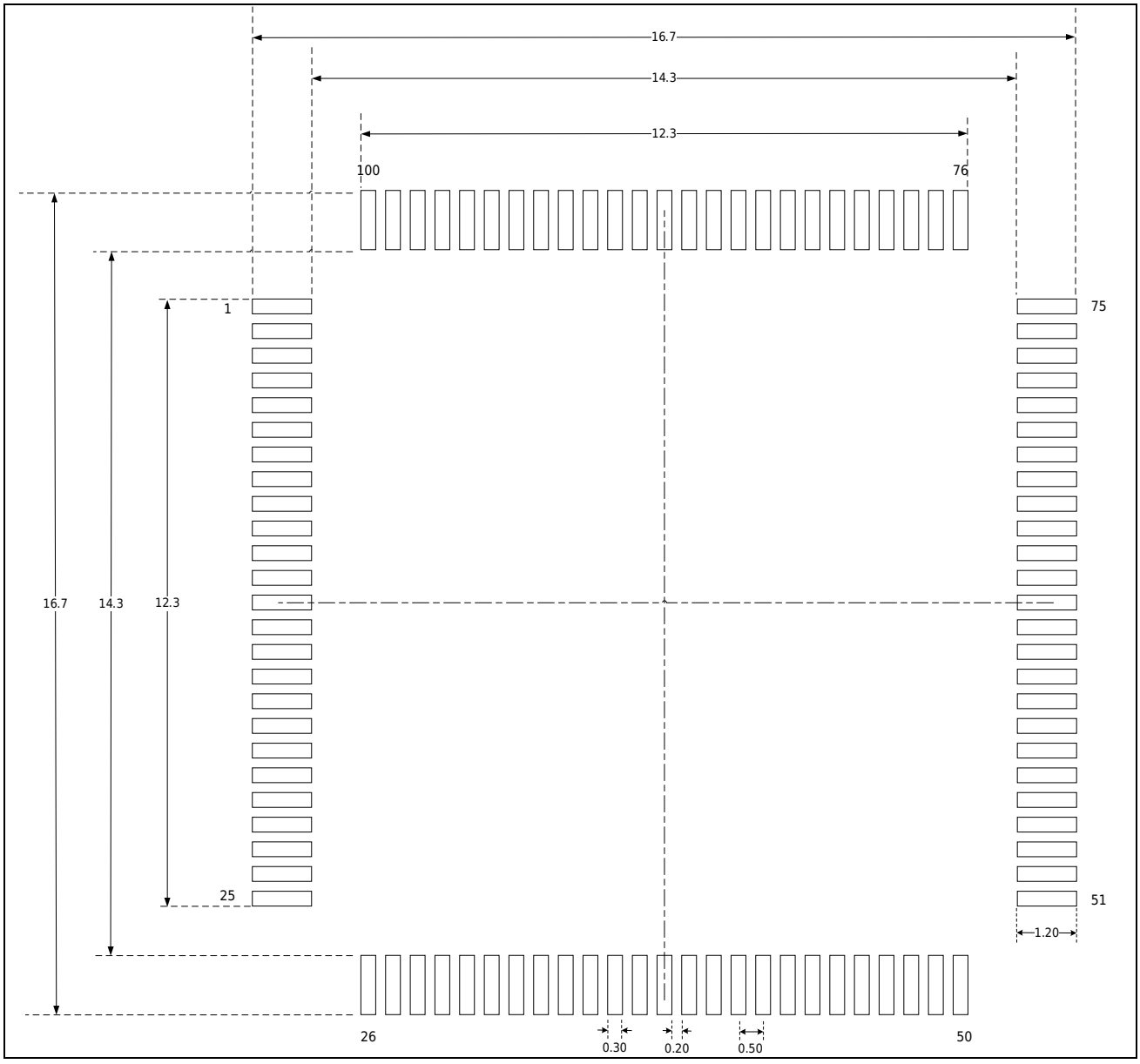
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	0.100±0.050	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	26.000±0.200	LEAD TIP TO TIP
5	D1	24.000±0.100	PKG LENGTH
6	E	26.000±0.200	LEAD TIP TO TIP
7	E1	24.000±0.100	PKG WIDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF.	LEAD LENGTH
10	T	$0.150^{+0.050}_{-0.060}$	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.220±0.050	LEAD WIDTH
14	b1	0.200±0.030	LEAD BASE METAL WIDTH
15	e	0.500	LEAD PITCH
16	H (REF.)	(21.500)	CUM. LEAD PITCH
17	aaa	0.200	PROFILE OF LEAD TIPS
18	bbb	0.200	PROFILE OF MOLD SURFACE
19	ccc	0.080	FOOT COPLANARITY
20	ddd	0.070	FOOT POSITION

NOTE:

– Dimensions “D1” and “E1” do not include mold flash.

4.2 Schematic diagram of the pad

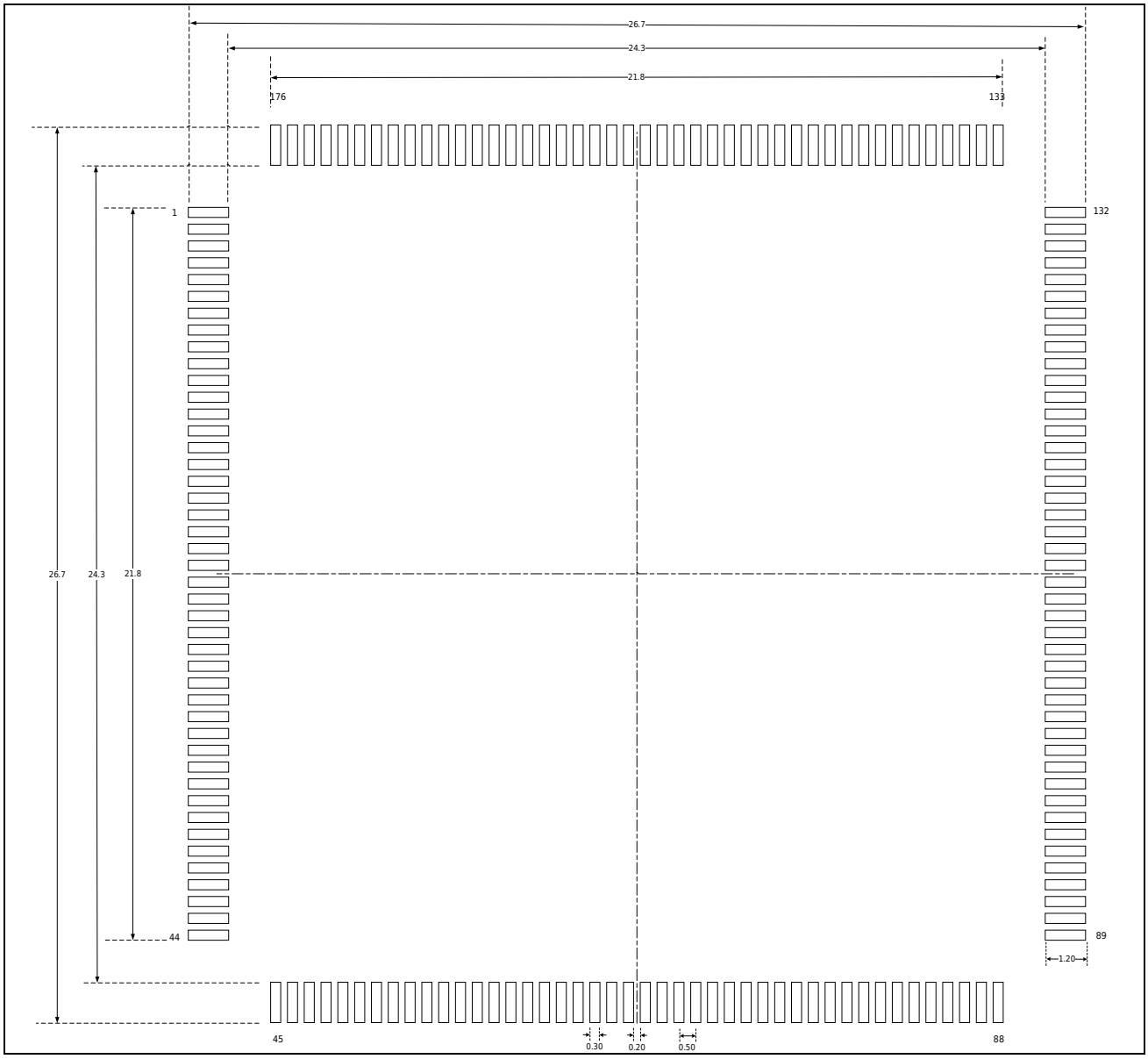
LQFP100 package (14mm x 14mm)



NOTE:

- Dimensions are expressed in millimeters.
- Dimensions are for reference only.

LQFP176 package (24mm x 24mm)



NOTE:

– Dimensions are expressed in millimeters.

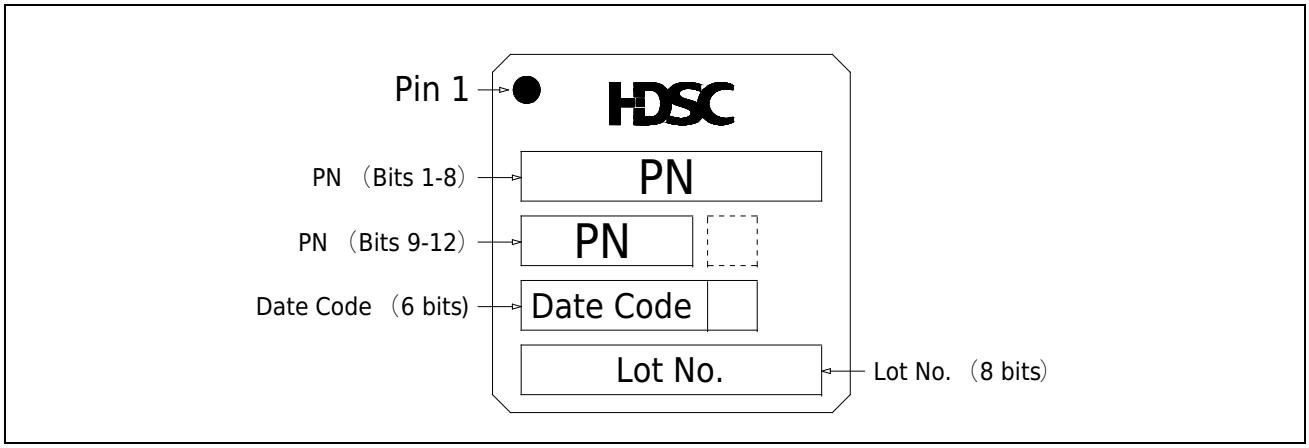
– Dimensions are for reference only.

4.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

LQFP100 package (14mm x 14mm)

LQFP176 package (24mm x 24mm)



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

4.4 Package thermal resistance coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_J = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's I_{DD} x V_{DD} , I/O power consumption refers to the power consumption generated by I/O pins when the chip is working, usually this part is small and can be ignored.

The junction temperature T_j on the surface of the chip when the chip is operating at the specified operating ambient temperature must not exceed the maximum junction temperature T_J allowed by the chip.

Table 4-1 Thermal resistance coefficient table of each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
LQFP100 14mm x 14mm / 0.5mm pitch	50 +/- 10%	℃/W
LQFP176 24mm x 24mm / 0.5mm pitch	30 +/- 10%	℃/W

5 Ordering Information

Product		HC32A4A0SITI-LQFP176	HC32A4A0PITI-LQFP100
Main frequency (MHz)		240	240
Kernel		M4	M4
Flash(KB)		2048	2048
RAM(KB)		516	516
GPIO		142	83
Voltage (V)		1.8 - 3.6	1.8 - 3.6
DMA		2*8ch	2*8ch
Timing and counting	Timer	32	32
	HRPWM	16	16
	RTC	✓	✓
Communication Interface	UART	10	10
	I²C	6	6
	SPI	6	6
	QSPI	1	1
	USB	USB 2.0 HS + USB 2.0 FS	
	CAN	CAN 2.0 + CAN FD	CAN 2.0 + CAN FD
	EXMC	1	1
	ETH	1	1
	DVP	1	1
	I²S	4	4
	SDIO	2	2
Simulation	ADC 12bit	3*16ch	3*16ch
	DAC 12bit	4ch	4ch
	SH	3ch	3ch
	PGA	4	4
	OTS	✓	✓
	Vcomp	4	4
	PVD	✓	✓
	VBAT	✓	✓
Co-processing	FMAC	✓	✓
	DCU	8ch	8ch
	MAU	✓	✓
Safety	AES	AES256	AES256
	TRNG	1	1
	Hash	SHA256/HMAC	SHA256/HMAC
Working temperature (℃)		-40~105	-40~105
Encapsulation packaging	Encapsulation form	LQFP176 (24*24)	LQFP100 (14*14)
	Packaging form	TRAY	TRAY

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

version number	Revision Date	modify the content
Rev1.0	2022/11/24	First edition release.

If you have any comments or suggestions during your purchase and use, please feel free to contact us.

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