

Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)			
30	$0.022 \text{ at V}_{GS} = 10 \text{ V}$	6.8	15 nC			
30	0.026 at V _{GS} = 4.5 V	6.0	13110			

SO-8 D_1 D_2

Top View

FEATURES

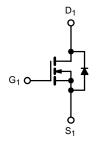
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % UIS Tested
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

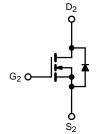


COMPLIANT HALOGEN **FREE**

APPLICATIONS

- Set Top Box
- Low Current DC/DC





N-Channel MOSFET

N-Channel MOSFET

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current (T _J = 150 °C)	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I _D	6.8 ^a 5.6 6.2 ^{b, c} 5.2 ^{b, c}	
Pulsed Drain Current		I _{DM}	30	Α
Continuous Source-Drain Diode Current	$T_C = 25 ^{\circ}C$ $T_A = 25 ^{\circ}C$	- I _S	2.25 1.48 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	5	
Single Pulse Avalanche Energy		E _{AS}	1.25	mJ
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P _D	2.7 1.77 1.78 ^{b, c} 1.14 ^{b, c}	W
Operating Junction and Storage Temperature Range		T _J , T _{sta}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, c, d}	t ≤ 10 s	R _{thJA}	58	70	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	$R_{th,IF}$	38	45			

Notes:

- a. Package limited, T_C = 25 °C.
 b. Surface Mounted on 1" x 1" FR4 board.
- d. Maximum under Steady State conditions is 110 °C/W.



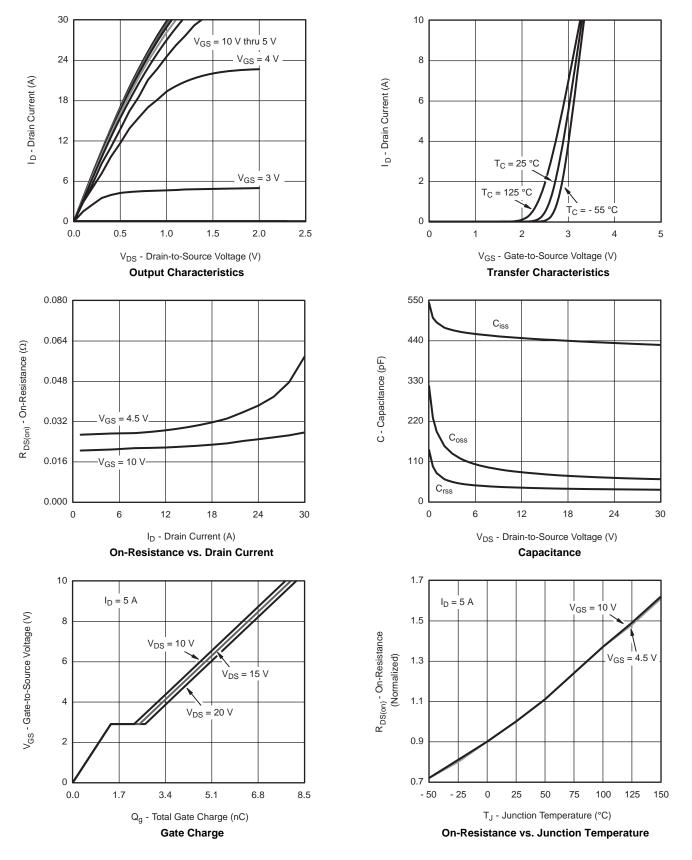
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			ı		1	1	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		32		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.0			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1.0		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Valtana Brain Oamant	1	V _{DS} = 30 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			Α	
		$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		0.022			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$		0.026		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 5 A		16		S	
Dynamic ^b			1	1	1		
Input Capacitance	C _{iss}			586			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		117		pF	
Reverse Transfer Capacitance	C _{rss}			55			
Total Gate Charge	0	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		15		nC	
	Qg			3.7	5.6		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 5 \text{ A}$		1.4			
Gate-Drain Charge	Q_{gd}			1.05			
Gate Resistance	R _g	f = 1 MHz	0.8	4.3	8.6	Ω	
Turn-On Delay Time	t _{d(on)}			12	24		
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 3 \Omega$		55	100		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		11	22		
Fall Time	t _f			8	16		
Turn-On Delay Time	t _{d(on)}			4	8	ns -	
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		9	18		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω		10	20		
Fall Time	t _f			6	12		
Drain-Source Body Diode Characteristi	cs		•	•	•		
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			2.25	۸	
Pulse Diode Forward Current	I _{SM}				24	A	
Body Diode Voltage	V_{SD}	I _S = 2 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			11	20	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 5 A, dI/dt = 100 A/μs, T _{.I} = 25 °C		4	8	nC	
Reverse Recovery Fall Time	t _a	$I_F = 5 \text{ A}$, $\Omega / \Omega I = 100 \text{ A} / \mu \text{ S}$, $I_J = 25 \text{ C}$		7			
Reverse Recovery Rise Time	t _b			4	İ	ns	

Notes:

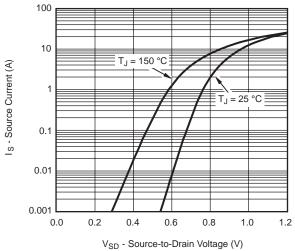
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

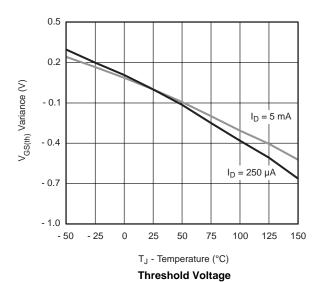


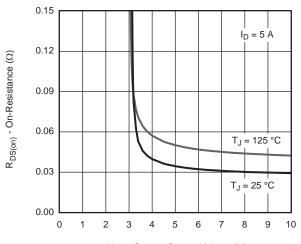






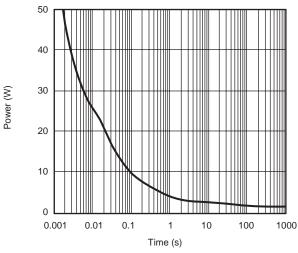
Source-Drain Diode Forward Voltage



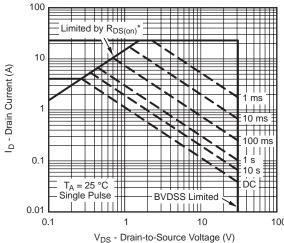


 V_{GS} - Gate-to-Source Voltage (V)

On-Resistance vs. Gate-to-Source Voltage



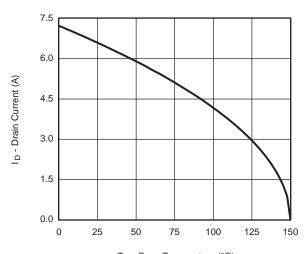
Single Pulse Power



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

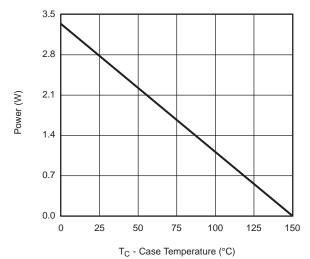
Safe Operating Area, Junction-to-Ambient

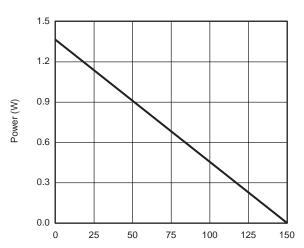




T_C - Case Temperature (°C)

Current Derating*





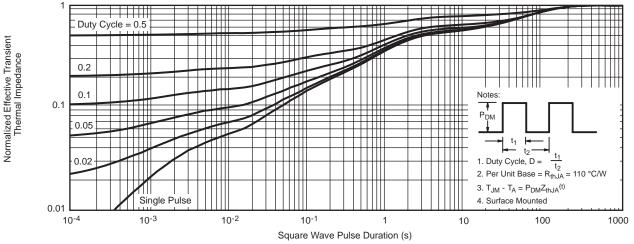
T_A - Ambient Temperature (°C)

Power, Junction-to-Foot

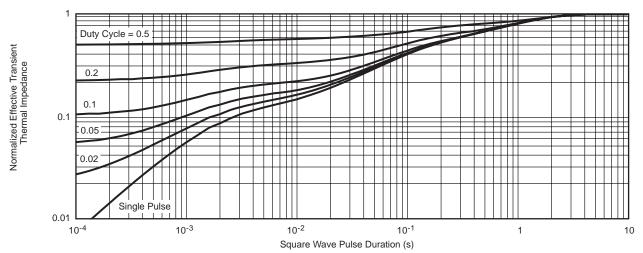
Power, Junction-to-Ambient

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





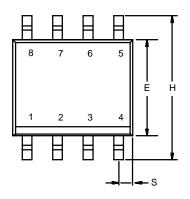
Normalized Thermal Transient Impedance, Junction-to-Ambient

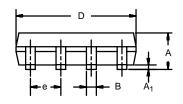


Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







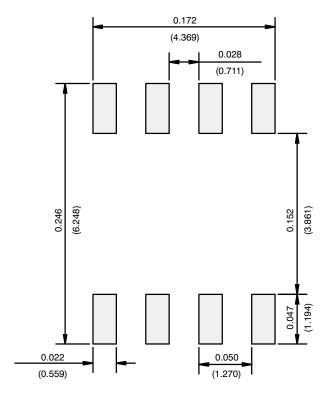
	MILLIM	IETERS	INC	INCHES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
FCN: C-06527-Rev I 11-Sen-06						

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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