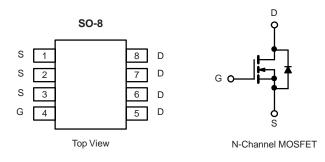


N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)			
60	0.025 at V _{GS} = 10 V	7.6	10.5 nC			
	0.035 at V _{GS} = 4.5 V	6.5	10.5110			



FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Power MOSFET
- Optimized for "Low Side" Synchronous Rectifier Operation
- 100 % R_g and UIS Tested

APPLICATIONS

CCFL Inverter

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	± 20	v	
	T _C = 25 °C		7.6 ^a	
Continuous Drain Current ($T_{I} = 150 \text{ °C}$)	T _C = 70 °C		6.8	
Continuous Drain Current (1j = 150°C)	T _A = 25 °C		6.1 ^{b, c}	
	T _A = 70 °C		4.8 ^{b, c}	
Pulsed Drain Current	I _{DM}	25	Α	
Continuous Source Drein Diede Current	T _C = 25 °C	1-	4.2	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.1 ^{b, c}	
Avalanche Current	1 0 4	I _{AS}	15	
Single-Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	11.2	mJ
	T _C = 25 °C		5	
Mauinum Davies Disais stien	T _C = 70 °C		3.2	14/
Maximum Power Dissipation	T _A = 25 °C	P _D	2.5 ^{b, c}	W
	T _A = 70 °C	1	1.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	38	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	20	25	C/VV	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 85 °C/W.



COMPLIANT HALOGEN FREE Available



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 250 \mu A$	60			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 250 1		55		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6.3			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1.2		2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
Zaro Cata Voltago Drain Current	lana	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	25			А	
	P	V _{GS} = 10 V, I _D = 4.6 A		0.025		0	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.2 A		0.035		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 4.6 A		20		S	
Dynamic ^b			•	•			
Input Capacitance	C _{iss}			1100		pF	
Output Capacitance	C _{oss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		90			
Reverse Transfer Capacitance	C _{rss}			55			
Tatal Cata Charge		$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 4.6 \text{ A}$		21	32	nC	
Total Gate Charge	Qg			10.5	16		
Gate-Source Charge	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 4.6 \text{ A}$		3.5			
Gate-Drain Charge	Q _{gd}			4.2			
Gate Resistance	R _g	f = 1 MHz		3.3	5	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	V_{DD} = 30 V, R_L = 5.4 Ω		150	225	-	
Turn-Off DelayTime	t _{d(off)}	${\sf I}_{\sf D}\cong$ 5.6 A, ${\sf V}_{\sf GEN}$ = 4.5 V, ${\sf R}_{\sf g}$ = 1 Ω		20	30		
Fall Time	t _f			60	90	20	
Turn-On Delay Time	t _{d(on)}			10	15	ns	
Rise Time	t _r	V_{DD} = 30 V, R_L = 5.4 Ω		15	25	-	
Turn-Off DelayTime	t _{d(off)}	${\sf I}_{\sf D}\cong$ 5.6 A, ${\sf V}_{\sf GEN}$ = 10 V, ${\sf R}_{\sf g}$ = 1 Ω		25	40		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characterist	ics						
Continous Source-Drain Diode Current	۱ _S	T _C = 25 °C			4.2	^	
Pulse Diode Forward Currenta	I _{SM}				25	A	
Body Diode Voltage	V _{SD}	I _S = 2 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			25	50	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			25	50	nC	
Reverse Recovery Fall Time	$I_{r} = 5.5 \text{ A} \cdot \text{d}/\text{d}t = 100 \text{ A/us} \cdot I_{r} = 25 ^{\circ}\text{C}$			19		~~~	
Reverse Recovery Rise Time	t _b	1		6		ns	

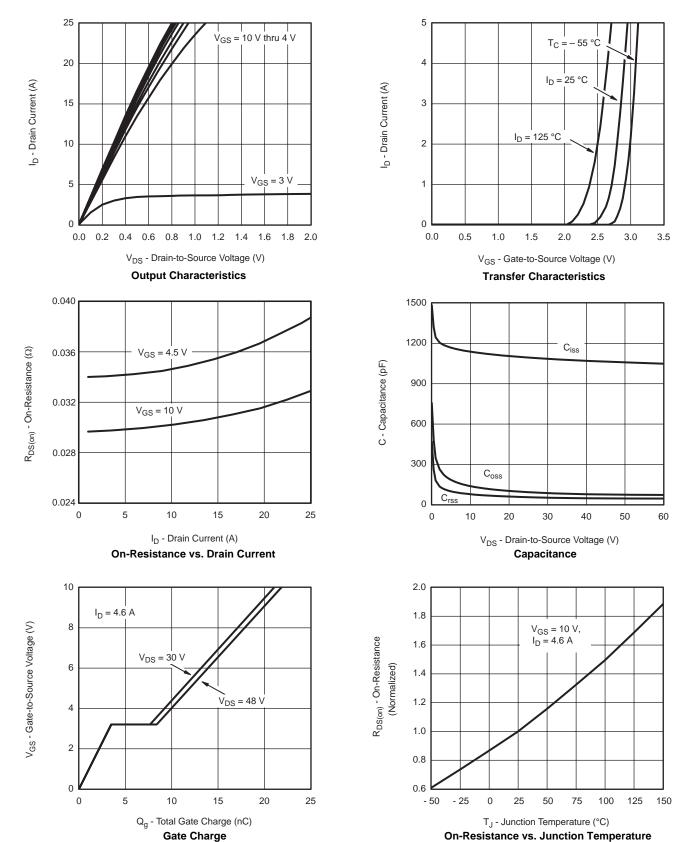
Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

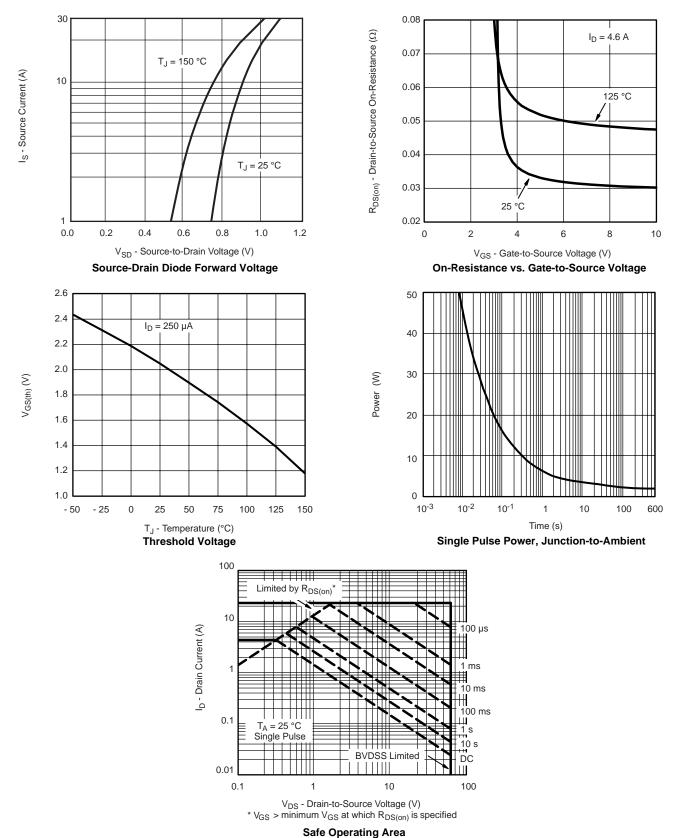




TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

60

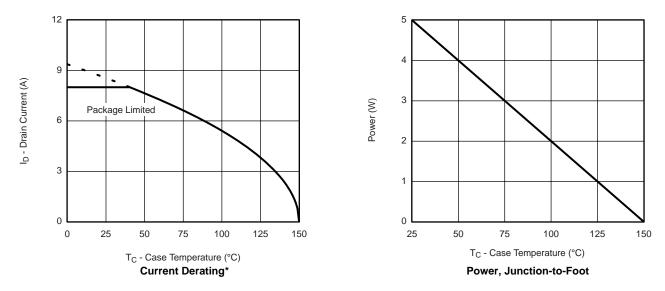




TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



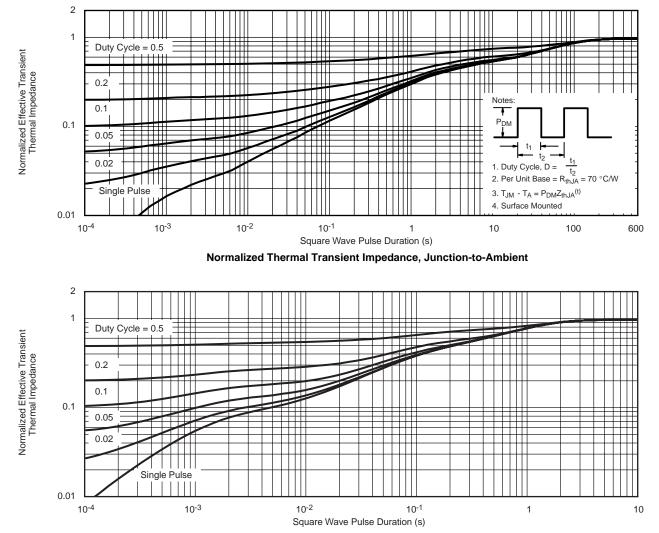




* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





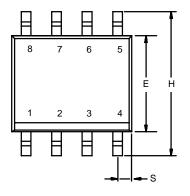


Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)



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