

# N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)			
60	0.076 at V <sub>GS</sub> = 10 V	4.5	10 nC			
	0.085 at V <sub>GS</sub> = 4.5 V	3.5	10110			

#### **FEATURES**

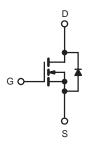
- · Halogen-free
- TrenchFET® Power MOSFET



### **APPLICATIONS**

· Load Switches for Portable Devices





N-Channel MOSFET

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	60	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	v
	T <sub>C</sub> = 25 °C		4.5	
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	1 .	3.2 <sup>a</sup>	
Continuous Brain Current (1) = 100 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	2.7	
	T <sub>A</sub> = 70 °C		2.3	A
Pulsed Drain Current		I <sub>DM</sub>	20	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	3.2	
Continuous Source-Diam Diode Current	T <sub>A</sub> = 25 °C	'5	2.1 <sup>b, c</sup>	
	T <sub>C</sub> = 25 °C		4.0	
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	3.0	W
Maximum Fower Dissipation	T <sub>A</sub> = 25 °C	1 'U	2.5 <sup>b, c</sup>	VV
	T <sub>A</sub> = 70 °C		1.6 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Tempera	Soldering Recommendations (Peak Temperature) <sup>e, f</sup>		260	

THERMAL RESISTANCE RATINGS								
Parameter		Symbol	Typical	Maximum	Unit			
Maximum Junction-to-Ambient <sup>a, c, d</sup>	t ≤ 5 s	R <sub>thJA</sub>	40	50	°C/W			
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	15	20	7 3/1			

- a. Package limited, T<sub>C</sub> = 25 °C.
  b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 95 °C/W.
- e. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



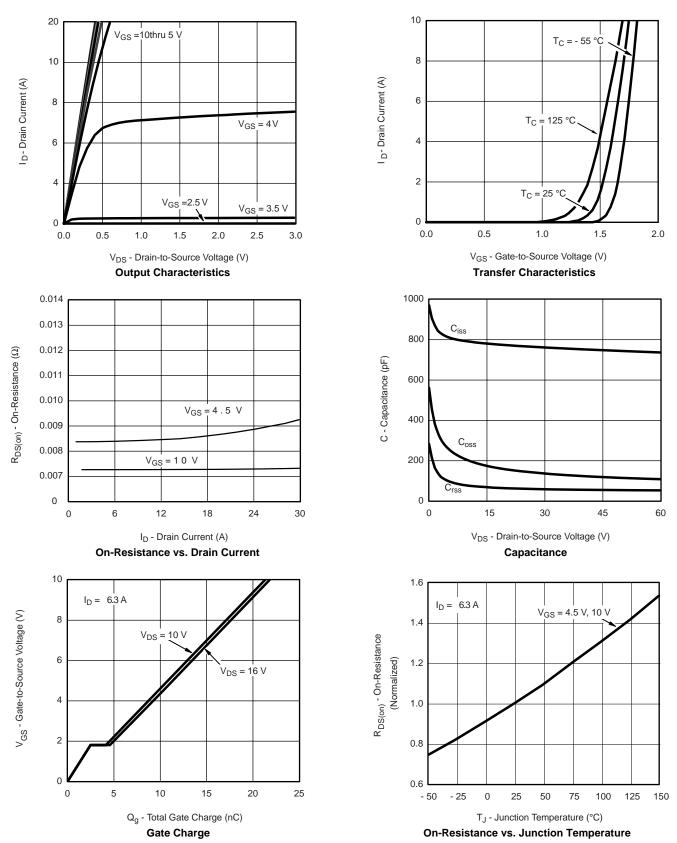
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					L	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 250		25		
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 4.0		mV/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	1.0		2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
7 0		V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			1	
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30			Α
_		$V_{GS} = 10 \text{ V}, I_D = 4.0 \text{ A}$	0.07			Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 3.0 \text{ A}$				
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.0 A		45		S
Dynamic <sup>b</sup>	<u> </u>	- <del>-</del>				
Input Capacitance	C <sub>iss</sub>	Piss		810		
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 30V, V_{GS} = 0 V, f = 1 MHz$		120		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge		$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 4.0 \text{ A}$		22	33	nC
	Q <sub>g</sub>	50 00 5		10	15	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 30 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.0 \text{ A}$		2.5		
Gate-Drain Charge	$Q_{gd}$			1.7		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.4		Ω
Turn-on Delay Time	t <sub>d(on)</sub>			15	25	
Rise Time	t <sub>r</sub>	$V_{DD}$ =30V, , $R_L$ = 1.5 $\Omega$		10	15	- - - ns
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 4.0$ A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		35	55	
Fall Time	t <sub>f</sub>			12	20	
Turn-on Delay Time	t <sub>d(on)</sub>			10	15	
Rise Time	t <sub>r</sub>	$V_{DD} = 30V$ , $R_L = 1.5 \Omega$		12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 4.0 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	40	
Fall Time	t <sub>f</sub>			10	15	
<b>Drain-Source Body Diode Characteristi</b>	cs			l		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			7.2	
Pulse Diode Forward Current	I <sub>SM</sub>				30	A
Body Diode Voltage	V <sub>SD</sub>	$I_S = 4.0 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			20	40	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1 40 A 41/4 400 A/2 T 05 00		10	20	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 4.0 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		10		
Reverse Recovery Rise Time	t <sub>b</sub>			10		ns

#### Notes:

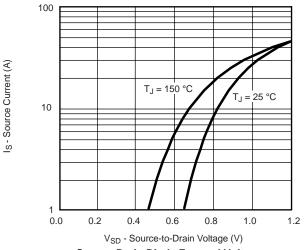
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

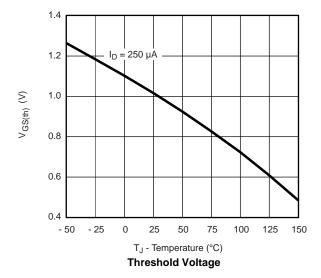


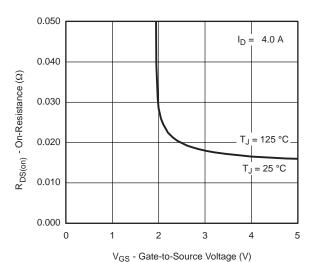




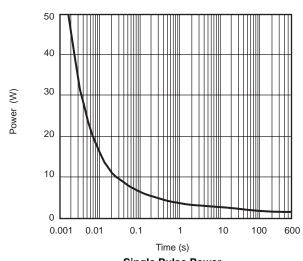


#### Source-Drain Diode Forward Voltage

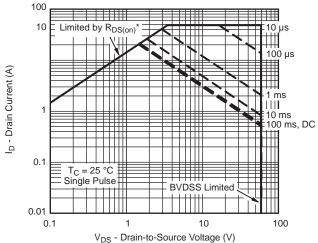




On-Resistance vs. Gate-to-Source Voltage



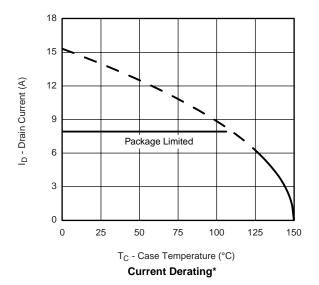
Single Pulse Power

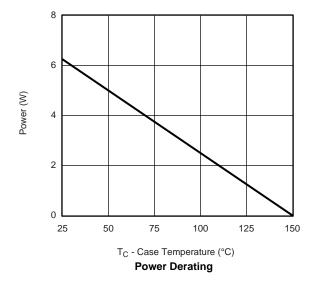


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Single Pulse Power, Junction-to-Case





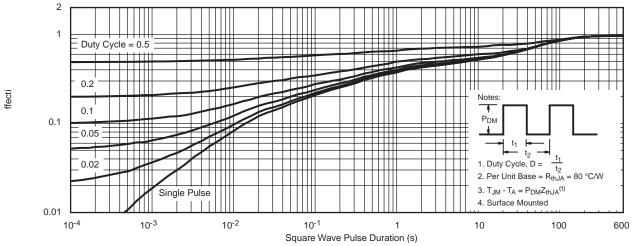


服务热线:400-655-8788

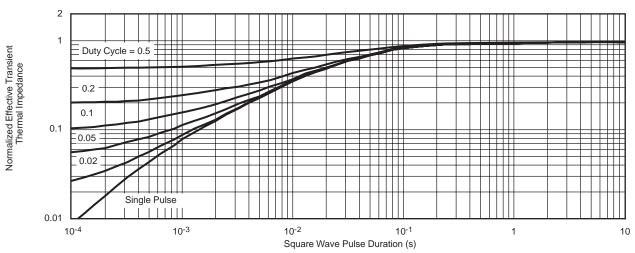
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<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





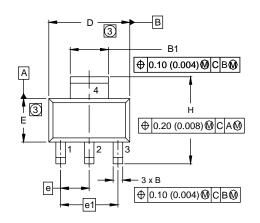
Normalized Thermal Transient Impedance, Junction-to-Ambient

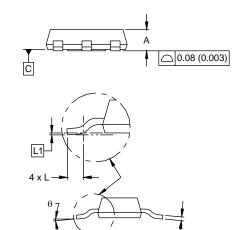


Normalized Thermal Transient Impedance, Junction-to-Foot



## **SOT-223 (HIGH VOLTAGE)**





DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
Α	1.55	1.80	0.061	0.071
В	0.65	0.85	0.026	0.033
B1	2.95	3.15	0.116	0.124
С	0.25	0.35	0.010	0.014
D	6.30	6.70	0.248	0.264
Е	3.30	3.70	0.130	0.146
е	2.30 BSC		0.0905 BSC	
e1	4.60 BSC		0.181	BSC
Н	6.71	7.29	0.264	0.287
L	0.91	-	0.036	-
L1	0.061 BSC		0.0024	4 BSC
θ	-	10'	-	10'

ECN: S-82109-Rev. A, 15-Sep-08

DWG: 5969

#### Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension do not include mold flash.
- 4. Outline conforms to JEDEC outline TO-261AA.



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