

74HC165 8-Bit Parallel-Load Shift Registers

1. General description

The 74HC165; are 8-bit serial or parallel-in / serial-out shift registers. The device features a serial data input (DS), eight parallel data inputs (D0 to D7) and two complementary serial outputs (Q7 and $\overline{Q7}$). When the parallel load input (\overline{PL}) is LOW the data from D0 to D7 is loaded into the shift register asynchronously. When \overline{PL} is HIGH data enters the register serially at DS. When the clock enable input (\overline{CE}) is LOW data is shifted on the LOW-to-HIGH transitions of the CP input. A HIGH on \overline{CE} will disable the CP input. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Asynchronous 8-bit parallel load
- Synchronous serial input

3. Applications

- Parallel-to-serial data conversion

4. Functional diagram

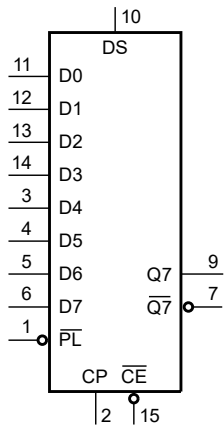


Fig. 1. Logic symbol

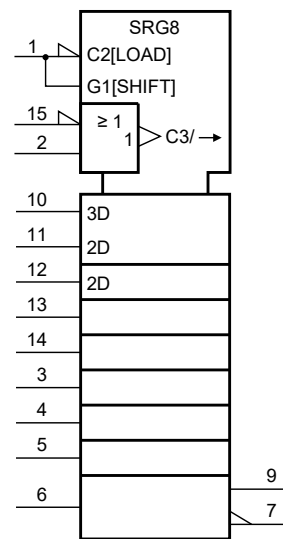


Fig. 2. IEC logic symbol

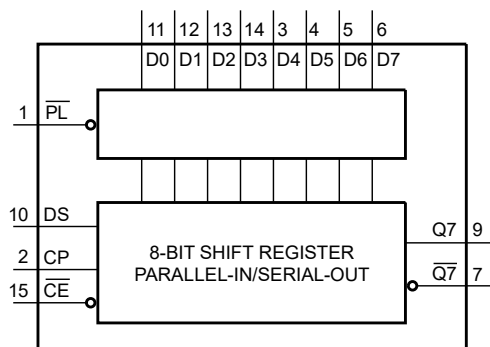


Fig. 3. Functional diagram

5. Pinning information

5.1. Pinning

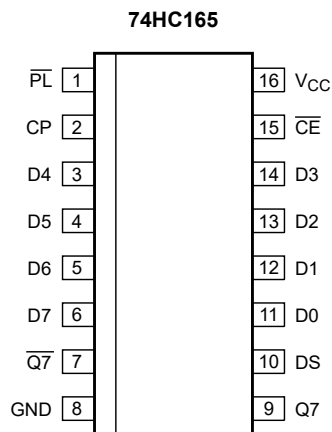


Fig. 4

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
PL	1	asynchronous parallel load input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
Q7	7	complementary output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs (also referred to as D _n)
CE	15	clock enable input (active LOW)
V _{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs					Qn registers		Outputs	
	PL	CE	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	Q7
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	L	↑	h	X	H	q0 to q5	q6	$\overline{q6}$
	H	↑	L	l	X	L	q0 to q5	q6	$\overline{q6}$
	H	↑	L	h	X	H	q0 to q5	q6	$\overline{q6}$
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	$\overline{q7}$
	H	X	H	X	X	q0	q1 to q6	q7	$\overline{q7}$

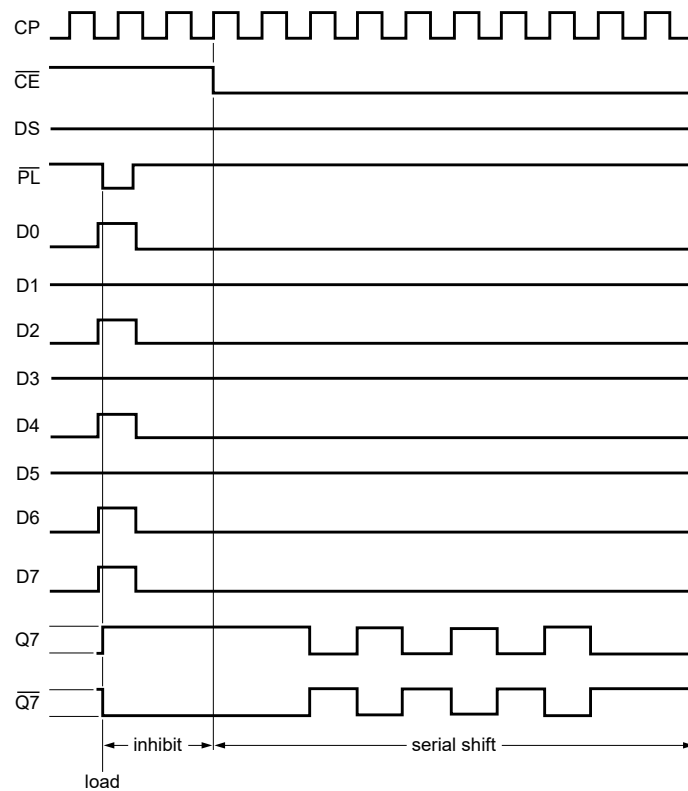


Fig. 6. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC165			Unit
			Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
74HC165								
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	μA
C _I	input capacitance		-	3.5	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);
 $C_L = 50 \text{ pF}$ unless otherwise specified; for test circuit, see Fig. 12

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
74HC165								
t_{pd}	propagation delay	CP or \overline{CE} to Q7, $\overline{Q7}$; see Fig. 7 [1]						
		$V_{CC} = 2.0 \text{ V}$	-	52	165	-	205	ns
		$V_{CC} = 4.5 \text{ V}$	-	19	33	-	41	ns
		$V_{CC} = 6.0 \text{ V}$	-	15	28	-	35	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	16	-	-	-	ns
		PL to Q7, $\overline{Q7}$; see Fig. 8						
		$V_{CC} = 2.0 \text{ V}$	-	50	165	-	205	ns
		$V_{CC} = 4.5 \text{ V}$	-	18	33	-	41	ns
		$V_{CC} = 6.0 \text{ V}$	-	14	28	-	35	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	15	-	-	-	ns
		D7 to Q7, $\overline{Q7}$; see Fig. 9						
		$V_{CC} = 2.0 \text{ V}$	-	36	120	-	150	ns
		$V_{CC} = 4.5 \text{ V}$	-	13	24	-	30	ns
$V_{CC} = 6.0 \text{ V}$	-	10	20	-	26	ns		
$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	11	-	-	-	ns		
t_t	transition time	Q7, $\overline{Q7}$ output; see Fig. 7 [2]						
		$V_{CC} = 2.0 \text{ V}$	-	19	75	-	95	ns
		$V_{CC} = 4.5 \text{ V}$	-	7	15	-	19	ns
		$V_{CC} = 6.0 \text{ V}$	-	6	13	-	16	ns
t_w	pulse width	CP input HIGH or LOW; see Fig. 7						
		$V_{CC} = 2.0 \text{ V}$	80	17	-	100	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	6	-	20	-	ns
		$V_{CC} = 6.0 \text{ V}$	14	5	-	17	-	ns
		\overline{PL} input LOW; see Fig. 8						
		$V_{CC} = 2.0 \text{ V}$	80	14	-	100	-	ns
		$V_{CC} = 4.5 \text{ V}$	16	5	-	20	-	ns
$V_{CC} = 6.0 \text{ V}$	14	4	-	17	-	ns		
t_{rec}	recovery time	\overline{PL} to CP, \overline{CE} ; see Fig. 8						
		$V_{CC} = 2.0 \text{ V}$	100	22	-	125	-	ns
		$V_{CC} = 4.5 \text{ V}$	20	8	-	25	-	ns
		$V_{CC} = 6.0 \text{ V}$	17	6	-	21	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t _{su}	set-up time	DS to CP, \overline{CE} ; see Fig. 10						
		V _{CC} = 2.0 V	80	11	-	100	-	ns
		V _{CC} = 4.5 V	16	4	-	20	-	ns
		V _{CC} = 6.0 V	14	3	-	17	-	ns
		\overline{CE} to CP and CP to \overline{CE} ; see Fig. 10						
		V _{CC} = 2.0 V	80	17	-	100	-	ns
		V _{CC} = 4.5 V	16	6	-	20	-	ns
		V _{CC} = 6.0 V	14	5	-	17	-	ns
		Dn to \overline{PL} ; see Fig. 11						
		V _{CC} = 2.0 V	80	22	-	100	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	ns
t _h	hold time	DS to CP, \overline{CE} and Dn to \overline{PL} ; see Fig. 10						
		V _{CC} = 2.0 V	5	2	-	5	-	ns
		V _{CC} = 4.5 V	5	2	-	5	-	ns
		V _{CC} = 6.0 V	5	2	-	5	-	ns
		\overline{CE} to CP and CP to \overline{CE} ; see Fig. 10						
		V _{CC} = 2.0 V	5	-17	-	5	-	ns
		V _{CC} = 4.5 V	5	-6	-	5	-	ns
		V _{CC} = 6.0 V	5	-5	-	5	-	ns
		f _{max}	maximum frequency	CP input; see Fig. 7				
V _{CC} = 2.0 V	6			17	-	5	-	MHz
V _{CC} = 4.5 V	30			51	-	24	-	MHz
V _{CC} = 6.0 V	35			61	-	28	-	MHz
V _{CC} = 5.0 V; C _L = 15 pF	-			56	-	-	-	MHz
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} [3]	-	35	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

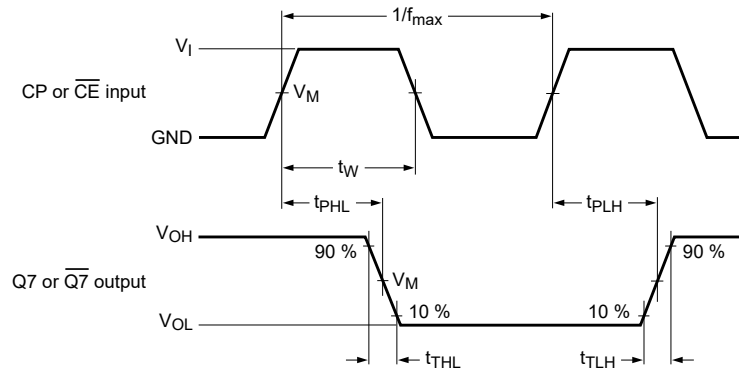
f_o = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

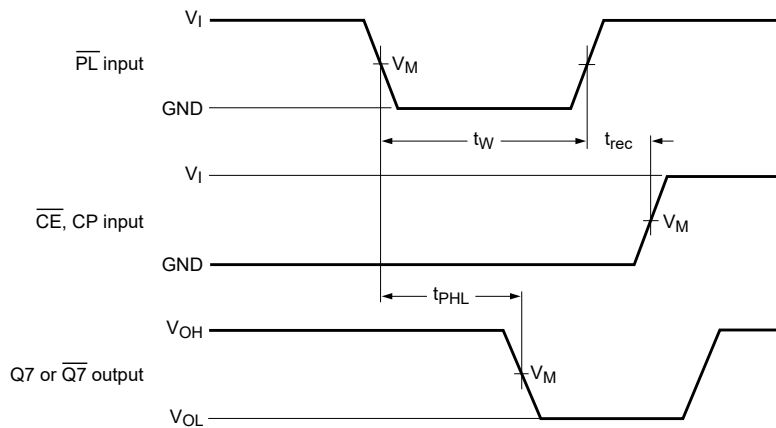
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

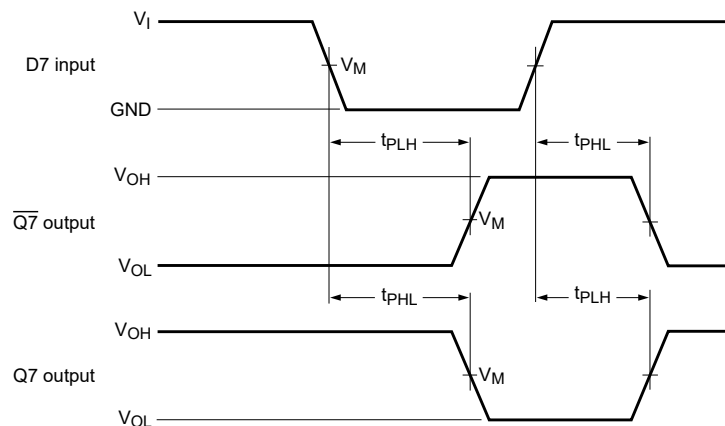
Fig. 7. The clock (CP) or clock enable (CE) to output (Q7 or Q7) propagation delays, the clock pulse width, the maximum clock frequency and the output transition times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

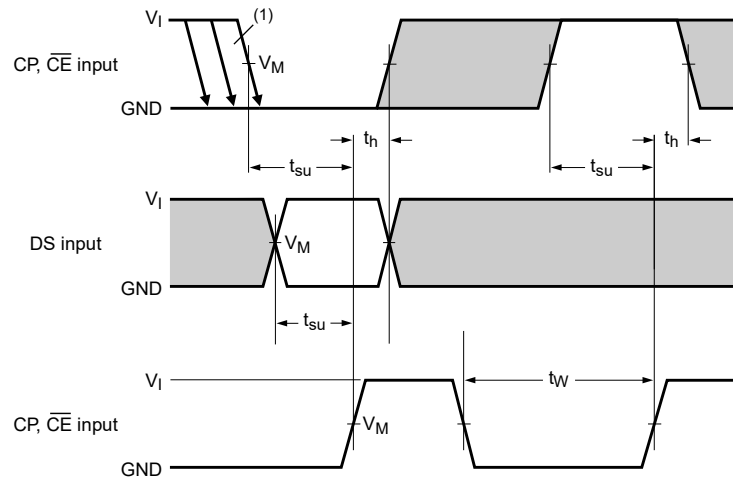
Fig. 8. The parallel load (PL) pulse width, the parallel load to output (Q7 or Q7) propagation delays, the parallel load to clock (CP) and clock enable (CE) recovery time



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. The data input (D7) to output (Q7 or Q7) propagation delays when PL is LOW

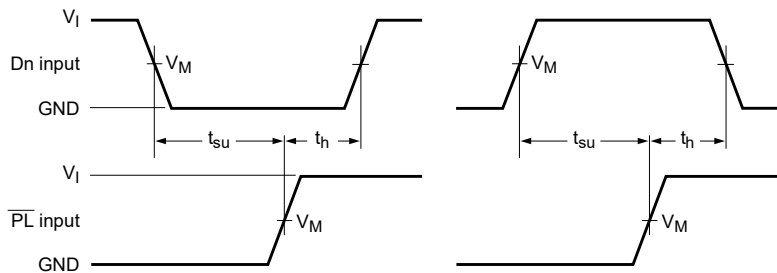


(1) \overline{CE} may change only from HIGH-to-LOW while CP is LOW.

The shaded areas indicate when the input is permitted to change for predictable output performance
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. The set-up and hold times from the serial data input (DS) to the clock (CP) and clock enable (\overline{CE}) inputs, from the clock enable input (\overline{CE}) to the clock input (CP) and from the clock input (CP) to the clock enable input (CE)



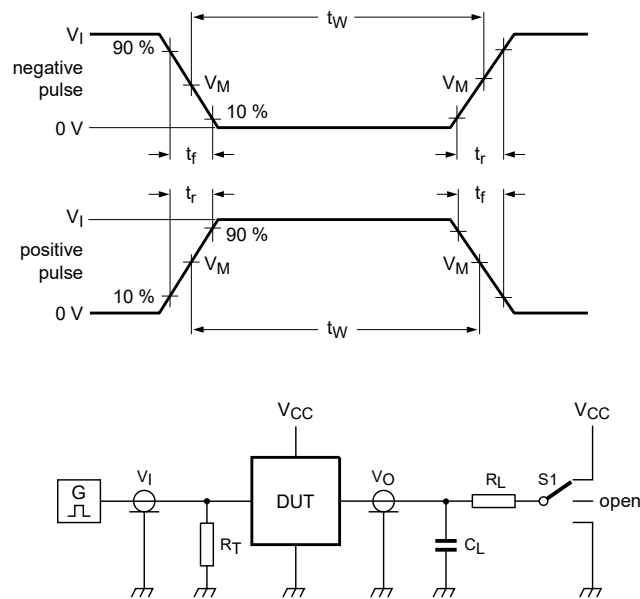
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 11. The set-up and hold times from the data inputs (Dn) to the parallel load input (\overline{PL})

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC165	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch

Fig. 12. Test circuit for measuring switching times

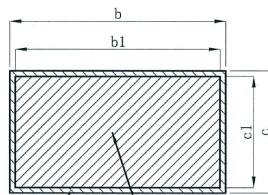
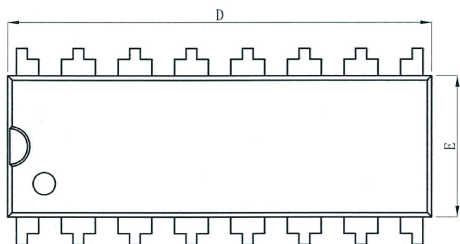
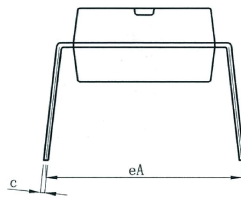
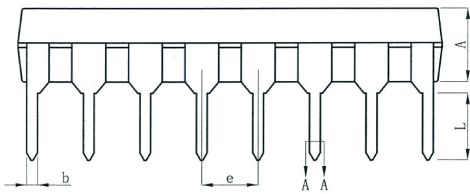
Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC165	V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open

Ordering Information

part Number	Device Marking	Package type	Body size (mm)	Temperature (°C)	MSL	Transport	Package Quantit
XL74HC165	XL74HC165	SOP16	10.00*3.95	-40 to +85	MSL3	T&R	2500
XL74HC165-TS	XL74HC165-TS	TSSOP16	5.00*3.90	-40 to +85	MSL3	T&R	2500
XD74HC165	XD74HC165	DIP16	19.05*6.35	-40 to +85	MSL3	Tube 25	1000

DIP16封装尺寸图

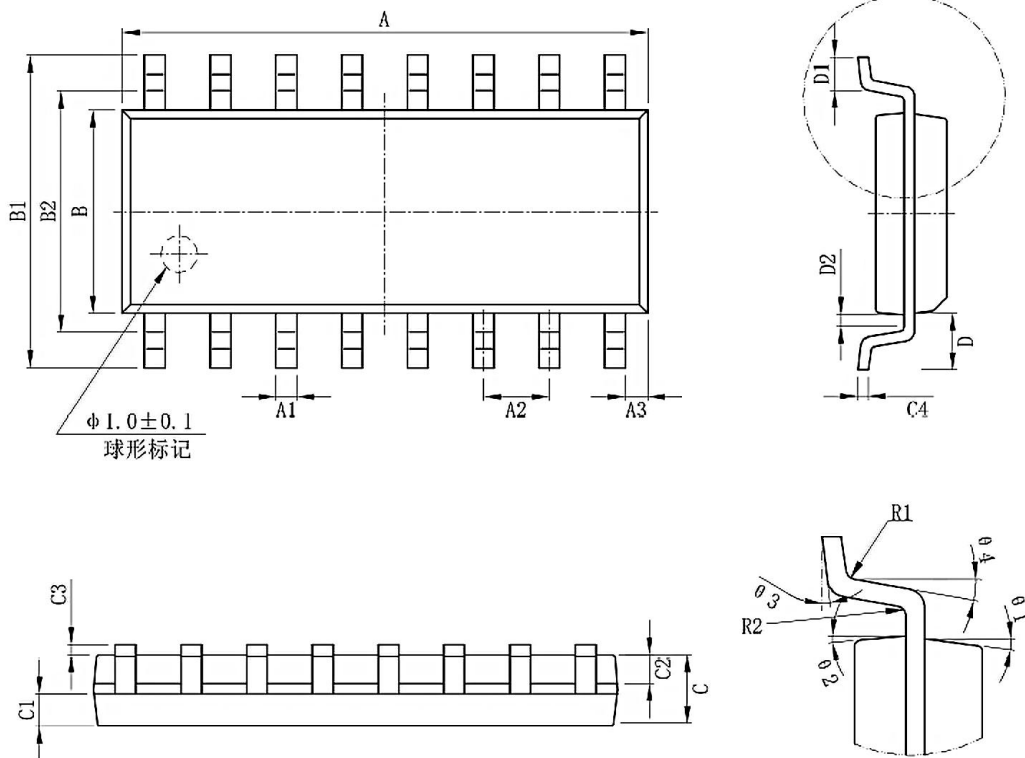


WITH PLATING ——— BASE METAL

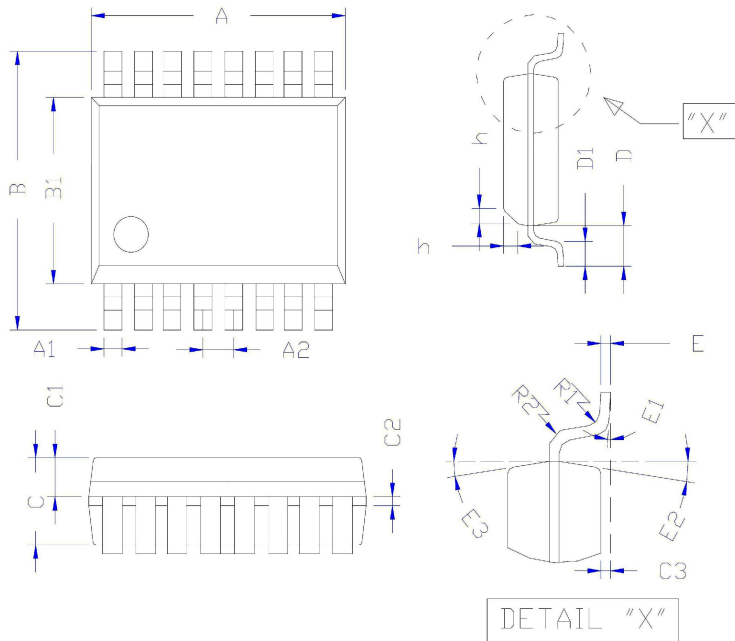
symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

SOP16封装尺寸图

标注	尺寸	最小 (mm)	最大 (mm)	标注	尺寸	最小 (mm)	最大 (mm)
A		9.80	10.00	C4		0.203	0.233
A1		0.356	0.456	D		1.05TYP	
A2		1.27TYP		D1		0.40	0.70
A3		0.302TYP		D2		0.15	0.25
B		3.85	3.95	R1		0.20TYP	
B1		5.84	6.24	R2		0.20TYP	
B2		5.00TYP		θ 1		8° ~ 12° TYP4	
C		1.40	1.60	θ 2		8° ~ 12° TYP4	
C1		0.61	0.71	θ 3		0° ~ 8°	
C2		0.54	0.64	θ 4		4° ~ 12°	
C3		0.05	0.25				



TSSOP16封装尺寸图



标注	表示	MIN	NOM	MAN
A	总长	4.95	5.00	5.05
A1	脚宽	0.20	0.22	0.24
A2	脚间距	0.60	0.65	0.70
B	跨度	5.70	6.00	6.30
B1	胶体宽度	3.80	3.90	4.00
C	胶体厚度	0.95	1.00	1.05
C1	上胶体厚	0.40	0.41	0.42
C2		0.05	0.15	0.25
C3	站高	0.02	0.08	0.10
D	单边长	0.85	1.05	1.25
D1	脚长	0.40	0.65	0.85
E	脚厚	0.15	0.20	0.25
E1	脚角度	0°		8°
h		0.30	0.40	0.50

Xinluda reserves the right to change the above information without prior notice.