500V Half-Bridge Module

For Small Appliance Motor Drive Applications

LAS1M0750

Overview


LasSOP-10

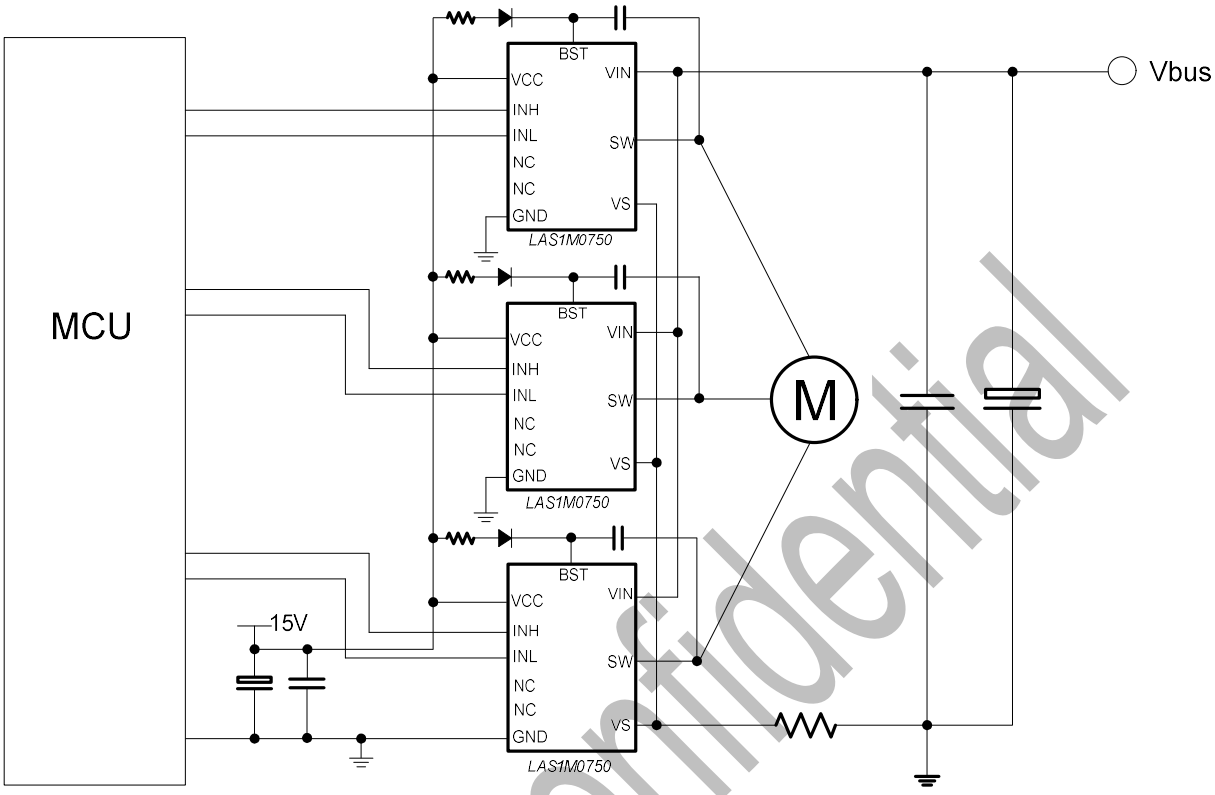
LAS1M0750 is a half-bridge module designed for advanced appliance motor drive applications such as energy efficient fans and pumps. LASemi's technology offers an extremely compact, high performance half-bridge topology in an isolated package. The advanced IPM offers a combination of LASemi's low $R_{DS(on)}$ MOSFET technology and the industry benchmark half-bridge high voltage, rugged driver in a small LasSOP-10 package. The dedicated open-source pin from low side MOSFET is provided for current sensing. The input works with Schmitt-trigger and the logic voltage is compatible with 3.3V/5V/15V signal. The UVLO, deadtime and thermal shutdown are also provided.

Features

- Built-in high-performance 500V/7A FRMOSFET and >5us short circuit tolerance
- Robust at negative transient voltage
- Gate drive supply range from 10 to 20V
- UVLO for both high side and low side
- Built-in dead time to avoid cross-conduction
- Thermal Shutdown (TSD) protection
- Available in LasSOP-10 package customized with compact size and low thermal resistance feature

Typical Application

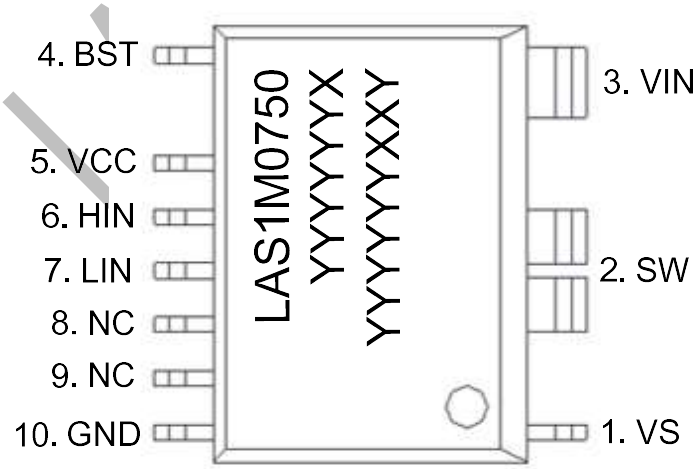
- BLDC fan/pumps



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LAS1M0750	LasSOP-10	-40 to 125^{0}C	T/R 1500 pcs/roll	sales@latticeart.com

Pin Diagram

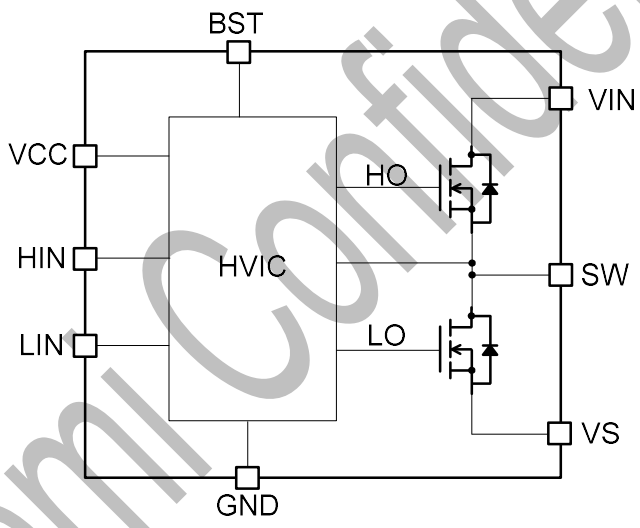


YYYYYY: IC Lot number
X: version
YYYYYY: MOS Lot Number
XX: week number
Y: Year code

Pin Description

Pin No.	Symbol	Pin Description
1	VS	Open source for low side MOSFET
2	SW	SW phase output
3	VIN	DC bus
4	BST	High side floating supply
5	VCC	Power supply for low side
6	HIN	High side gate driver input
7	LIN	Low side gate driver input
8	NC	No Connect
9	NC	No Connect
10	GND	Ground pin

Block Diagram



Absolute Maximum Ratings (note 1)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
VCC	Power supply voltage for low side	20	V
BST-SW	Power supply voltage for high side	20	V
VIN	DC bus	500	V
I_D	Each MOSFET current, continues, Tj<150°C	3.5	A
I_{DM}	Each MOSFET pulse current<100us	7	A
HIN, LIN	Input logic voltage	20	V
VS	Open source voltage	10	V
T_{STG}	Storage temperature	-55 to150	°C
T_j	Junction temperature	-40 to150	°C
$R_{th(j-c)}$	Junction to case thermal resistance	6	°C/W
P_D	Total power dissipation	8.3	W

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
VCC	Power supply pin for low side	11 to 17	V
BST	High side floating supply voltage	SW+11 to SW+17	V
VIN	DC bus voltage	<400	V
HIN/LIN	Logic input voltage	VCC	V
F_{PWM}	PWM carrier frequency	<50	kHz

Electrical Characteristics

T_A=25^{0}C, unless otherwise specified.

Gate driver part

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{QVCC}	Quiescent VCC supply current	VCC=15V, HIN=LIN=0V	70	95	125	uA
I_{BST-SW}	Quiescent V_{BST-SW} supply current	V_{BST-SW}=15V, HIN=LIN=0V	15	30	45	uA
VCC_{ON}	VCC under-voltage rising threshold		8.3	9.1	9.9	V
VBS_{ON}	V_{BST-SW} under voltage rising threshold		8	8.5	9.1	V
VCC_{OFF}	VCC under-voltage falling threshold		7.5	8.1	8.8	V
VBS_{OFF}	VBS under-voltage falling threshold		7.5	7.8	8.2	V
VCC_{HYS}	VCC UVLO hysteresis			1		V
VBS_{HYS}	BST-SW UVLO hysteresis			0.7		V
I_{IN_LKG}	Logic “1” input bias current	HIN,LIN=5V		5		uA
I_{IN_SINK}	Logic “0” input bias current	HIN,LIN=0V			1	uA
V_{IL}	OFF threshold voltage	Logic low level			0.8	V
V_{IH}	ON threshold voltage	Logic high level	3			V
DT	Dead time			100		ns
T_{FLT_IN}	Input filter			100		ns
MT	High side and low side delay match time				60	ns
T_{OTP}	Over temperature protection shutdown rising threshold			138		°C
T_{OTP_HYS}	OTP hysteresis			28		°C

Power MOS part

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	VCC=0V, I_D=500uA	500			V
I_{DSS}	Zero Gate voltage Drain Current	VCC=0V, V_{DS}=500V			3	uA
V_{SD}	Drain-source diode forward voltage	VCC=V_{BS}=15V I_D=2.5A		0.95		V
$R_{DS(ON)}$	Drain-source Turn-On Resistance	VCC=V_{BS}=15V VIN=5V, I_D=2.5A		1.0	1.5	ohm
Trr	Reverse recovery time	VIN=400V, VCC=V_{BST-SW}=15V, I_D=3A; Inductive Load, High-side and Low-side Switching		110		ns
E_{ON}	Turn-on switching lost			150		uJ
E_{OFF}	Turn-off switching lost			15		uJ
T_{ON}	Turn-on propagation delay time			600		ns
T_{OFF}	Turn-off propagation delay time			450		ns
dV/dt_{rising}	SW rising dV/dt slaw rate			30		V/ns
dI/dt_{rising}	SW rising dI/dt slaw rate			75		A/us
$dV/dt_{falling}$	SW falling dV/dt slaw rate			10		V/ns
$dI/dt_{falling}$	SW falling dI/dt slaw rate			250		A/us

Function Descriptions

1. Input and output True Table

HIN	LIN	OUTPUT	Description
0	0	Hi-Z	High side and low side OFF
0	1	0	Low side ON, High side OFF
1	0	VIN	High side ON, Low side OFF
1	1	Hi-Z	Forbidden input, High side and low side OFF
Open	Open	Hi-Z	Input internal pull-down resistor 1M ohm

2. Dynamic switching diagram

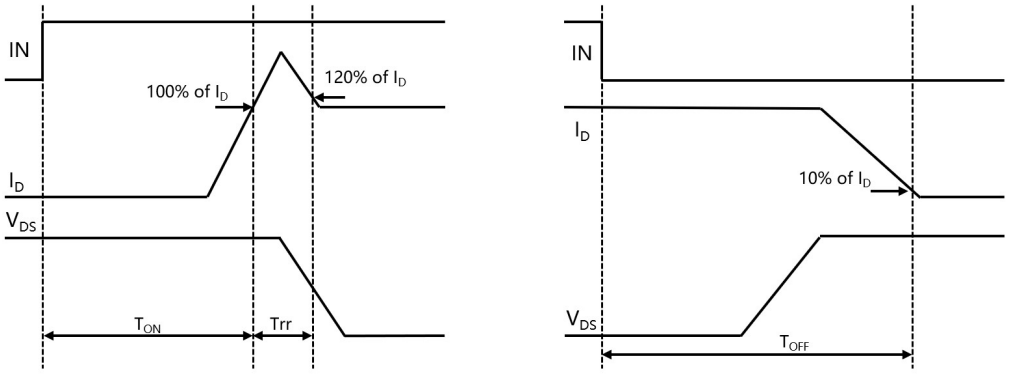


Figure 1 Dynamic switching diagram

3. Delay Match Time

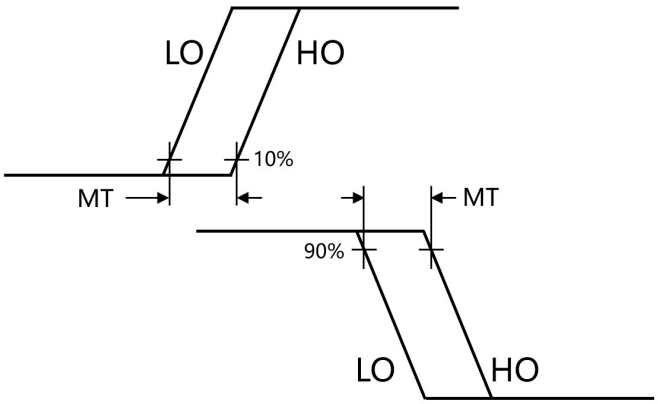


Figure 2 Delay match time

4. Thermal Shutdown (TSD)

LAS1M0750 incorporates a thermal shutdown (TSD) circuit. Figure 3 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, a rise in ambient temperature at the device, etc.), LAS1M0750 shuts down both high-side and low-side output transistors.

The TSD circuit in HVIC can monitor the power MOSFET with a relative accuracy since the compact module package makes the power device and HVIC closely placed. When the temperature of HVIC exceeds the TSD operating temperature (T_{TSD}, typ.138°C), the TSD circuit is activated. When the temperature of the HVIC decreases to the TSD

releasing Temperature(typ.110°C) or less, the shutdown condition is released. The output transistors then resume operating according to input signals.

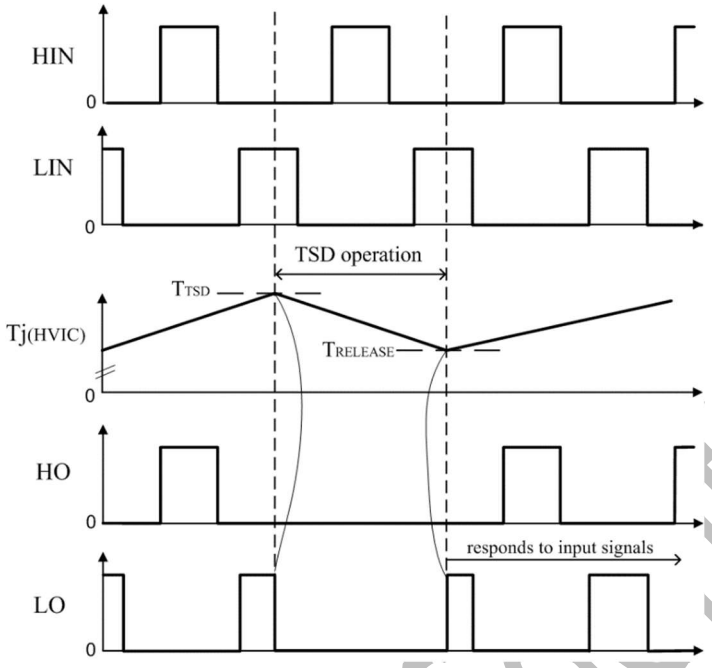


Figure 3 Thermal Shutdown Protection

5. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 4 shows operational waveforms of undervoltage lockout for low-side power supply (i.e., UVLO_VCC).

When the VCC pin voltage decreases to the logic operation stop voltage(typ.8.1V) or less, the UVLO_VCC circuit in the corresponding phase gets activated and sets both of HO and LO signals to logic low. When the VCC pin voltage increases to the logic operation start voltage (typ.9.1V) or more, LAS1M0750 releases the UVLO_VCC operation. Then, LAS1M0750 resumes the following transmissions: a LO signal according to the LIN pin input command; a HO signal according to the rising edge of the first HIN pin input command after the UVLO_VCC release.

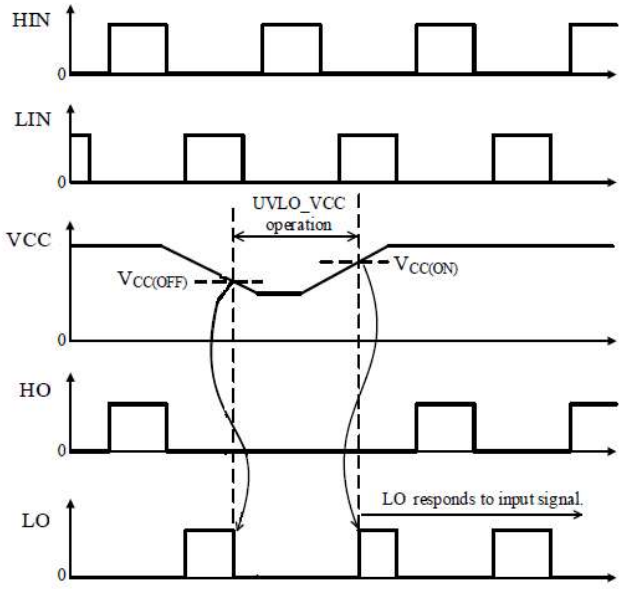


Figure 4 UVLO_VCC Operational Waveform

6. Undervoltage Lockout for High-side Power Supply (UVLO_BST)

Figure 5 shows operational waveforms of undervoltage lockout for high-side power supply (i.e., UVLO_BST).

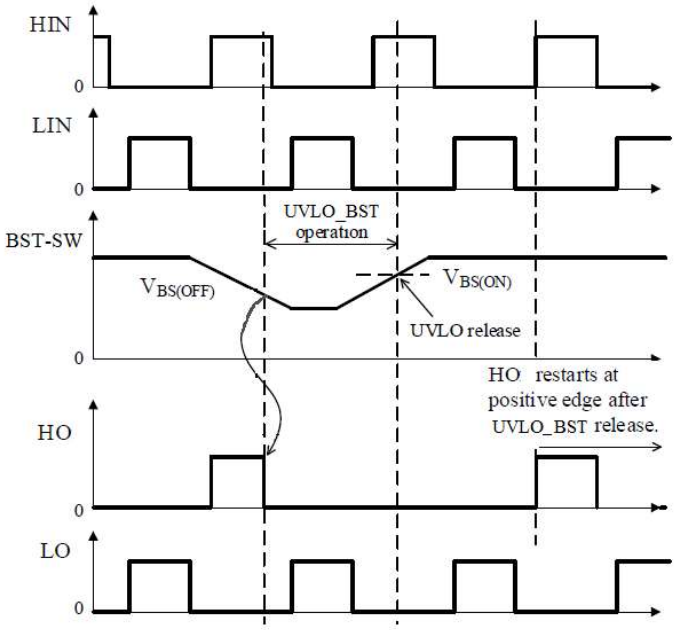


Figure 5 UVLO_BST Operational Waveform

When the voltage between the BST and SW pins decreases to the logic operation stop voltage(typ.7.8V) or less, the UVLO_BST circuit in corresponding phase gets activated and sets an HO signal to logic low. When the voltage between BST and SW pins increases to the logic operation start voltage(typ.8.5V) or more, LAS1M0750 releases the UVLO_VB operation. Then, the HO signal becomes logic high at the rising edge of the first input command after the UVLO_VB release.

7. PCB Design Guidelines

LAS1M0750's VIN and SW wide-lead pin layout is configured to provided sufficient copper area for heat sinking. Figure 6 gives an example of the PCB layout.

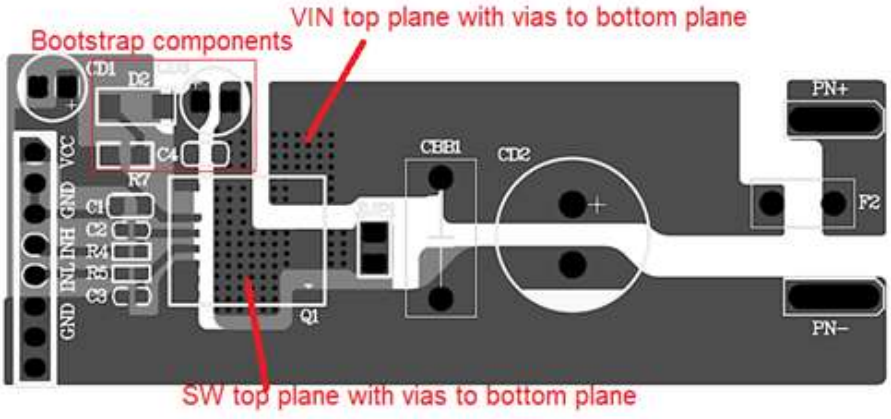
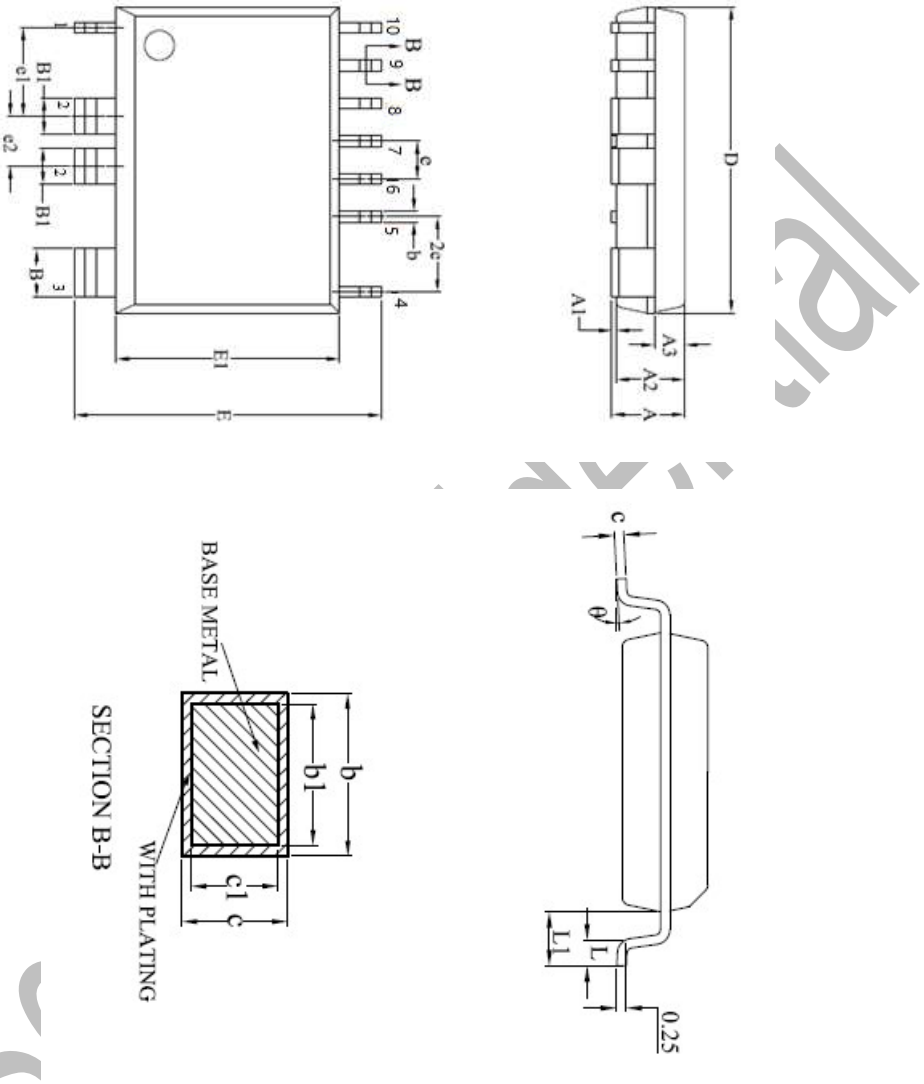


Figure 6 PCB Design example

Detail Package Outline Drawing

Package type: LasSOP-10



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
B	1.62	—	1.70
B1	1.21	—	1.29
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
e1	2.97BSC		
e2	1.68BSC		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°