650V, 300mA Non-Isolated Off-line Step-Down Converter

LA4100

Description


SOP 7L

LA4100 is a 650V step down converter. It can convert 650V input voltage to 12V~30V output. LA4100 integrates 650V power MOS with low R_{DSON}, to achieve low power loss. It applies variable off-time control mode with frequency jitter to achieve easy EMI design. The startup current is as low as 3uA, easy to use in low power design. Built-in loop compensation, no need for extra compensation components. DCM mode operation with adjustable current limit. Innovated FB2 design, make the high side buck structure better. The transient and no-load performance are optimized. The system solution size is minimized. LA4100 available in space-saving SOP7L package.

Feature

- Low No-load Power Consumption Down to 35mW
- Fast Loop Response
- Maximum 30V V_{CC} Operation Voltage
- 650V/16.5Ω Internal MOSFET
- Peak Current Limit Adjustable
- Frequency Spread Spectrum
- 63μA Low Quiescent Current
- Low Audible Nosie Control
- Full Protection Over current protection (OCP), Short-circuit protection (SCP), Output Under-voltage (UVP), Output Over-voltage protection (OVP),Input Under-voltage lockout (ULVO), Over temperature protection (OTP)
- Available in a SOP7L Package

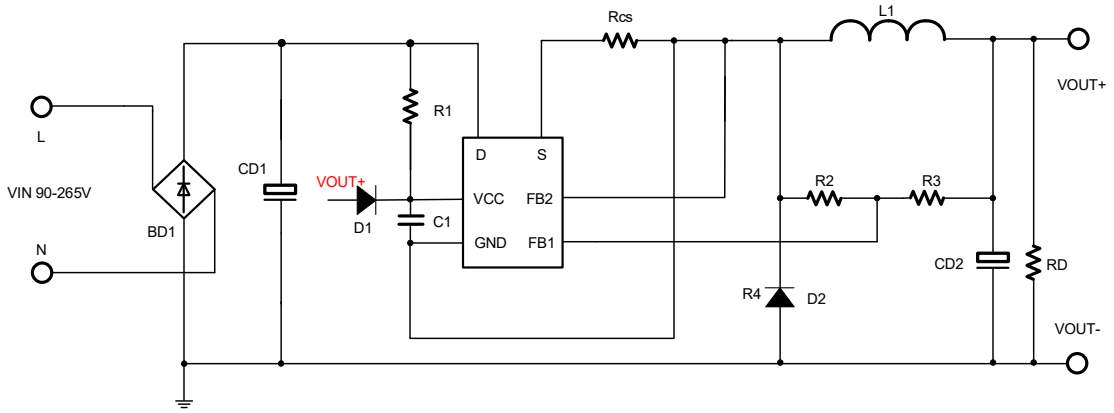
Application

- Motor Driver Aux Power Supply
- Home Appliance, Whitegoods
- Industrial Control

• Maximum Output Current

Package		Max Output Current（A）	
		90Vac ~ 265Vac	230Vac±15%
SOP7L	Open Frame	0.2	0.3

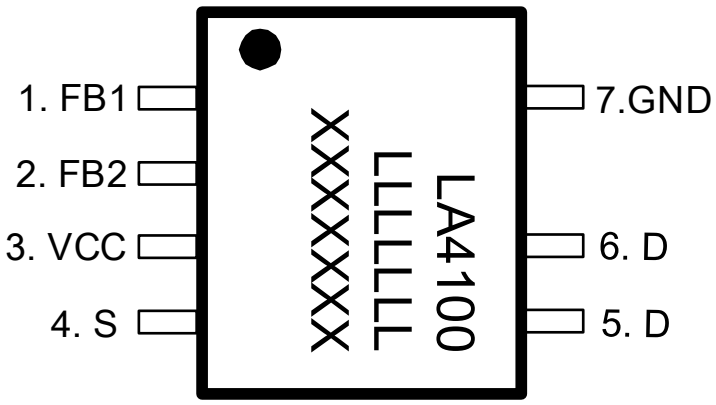
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA4100	SOP7L	-40 to 125^{0}C	T/R 2500pcs/roll	sales@latticeart.com

Pin Diagram

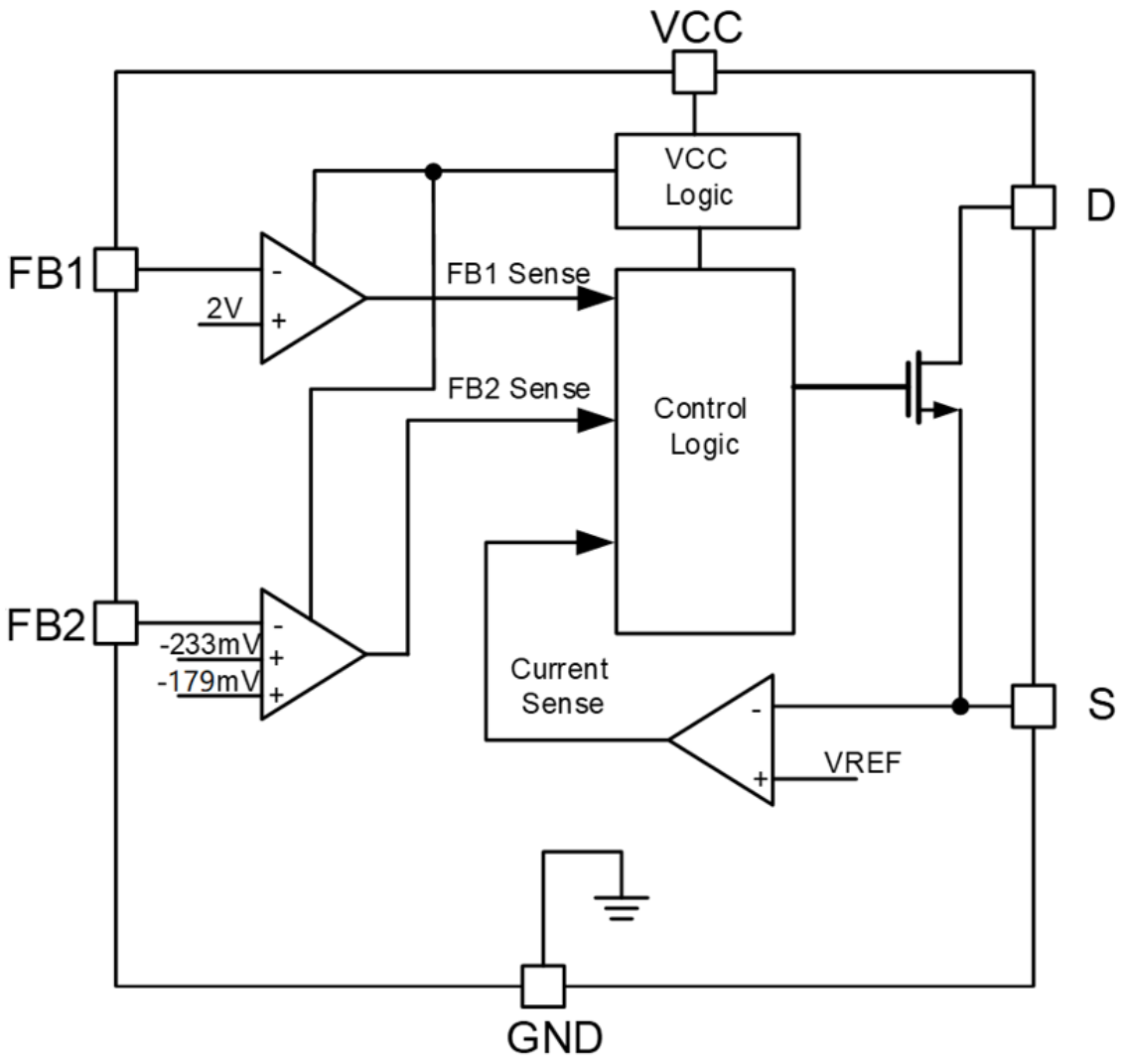


LA4100: Product code
LLLLLLL: Lot number
XXY: Date code

Pin Description

Pin No.	Symbol	Pin Description
1	FB1	Feedback pin. This pin will sense the voltage of the output when diode is conducting current. Connect a resistor divider between OUT and chip GND to set the output voltage.
2	FB2	Feed back2. this pin will sense the output voltage at Hi-Z state and wake up IC from low power mode. Connect a resistor divider between chip GND and output GND to sense the output voltage.
3	VCC	IC internal logic circuitry power supply.
4	S	Source of the power MOS, also served as the current sense pin
5,6	D	Drain node of the 650V power MOS. In buck configuration, connect this pin to VIN of the system.
7	GND	IC ground. In high-side buck configuration need to be connected on the SW node after the current sense resistor.

Block Diagram



Absolute Maximum Ratings (Note 1)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
VIN	D to S	-0.5~650	V
VCC	VCC to GND	-0.5~32	V
FB1	FB1 to GND	-0.5~4.5	V
FB2	FB2 to GND	-0.5~0.3	V
S	S to GND	-0.5~4.5	V
T_{STG}	Storage temperature	-55 to150	°C
T_j	Junction temperature	-40 to150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
Iout	Output Current	0~0.3	A
VCC	VCC to GND	-0.5~30	V
T_j	Junction temperature	-40~125	°C

Thermal Resistance (note 2)

Symbol	Definition	Ratings	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	100	°C/W

Note 2: Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

Electrical Characteristics

T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
VCC						
V_{CC_clamp}	V_{CC} clamp voltage	I_{CC}=2mA		20		V
V_{CC_OVP}	V_{CC} over-voltage threshold		28.6	30	31.4	V
V_{CC_START}	V_{CC} startup voltage	Rising threshold	15	16	17	V
V_{CC_STOP}	V_{CC} shutdown voltage	Falling threshold	7.5	7.8	8.2	V
I_{ST}	VCC startup current	Vcc=V_{CC_START} -1V T_J= -40° ~ +125°C		3.1	10	uA
I_{OP}	VCC operating current	VFB=2.2V, Vcc=19V		63		uA
FB1						
V_{ref}	Reference voltage		1.99	2.05	2.11	V
T_{FB1_LEB}	FB1 sense blanking time			1.4		us
FB2						
V_{OVP_HOLD}	Output over-voltage threshold		-244	-233	-221	mV
V_{WAKEUP}	Output wake up threshold		-191	-179	-167	mV
T_{FB2_BLK}	FB2 sense blanking time			75		us
Current Sense						
V_{CS_PK}	Current sense threshold		284	295	308	mV
V_{CS_MIN}	Min current sense threshold			0.4		V_{CS_PK}
T_{blk}	Current sense blanking time			250		ns
Frequency						
T_{MINOFF}	Min off time		4.5	5	5.5	us
T_{ONMAX}	Max on time			38		us
T_{OFFMAX_ECO}	Max off time		14	20		ms

Electrical Characteristics

T_A=25ºC, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Internal Power MOSFET						
V_{BV}(3)	Breakdown voltage		650			V
R_{DSON}	On state Resistance	TA=25℃		16.5		Ω
Over Temperature Protection (OTP)						
T_{OTP}(3)	Over temperature threshold			150		℃

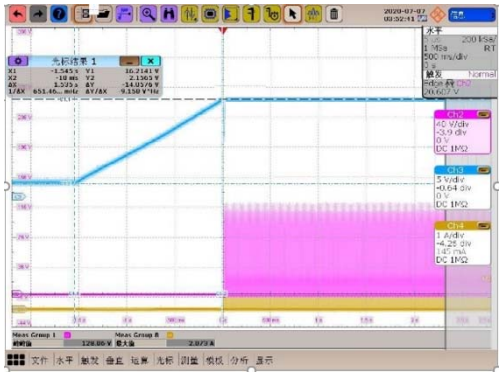
Note 3: Not tested in production and derived from bench characterization.

Typical Performance Characteristic

Vin=230Vac, Vout=15V, Iout=0.3A, and T_A = +25°C, unless otherwise noted.

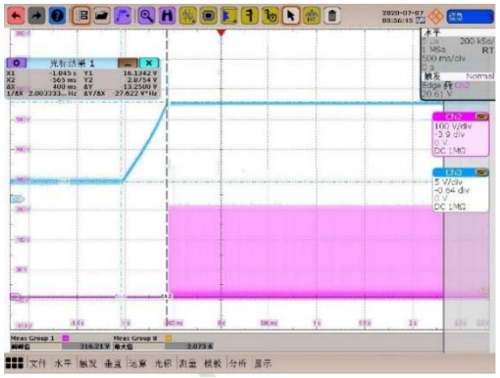
Startup with 90Vin

CH2 SW
CH3 VCC
CH4 Ipk



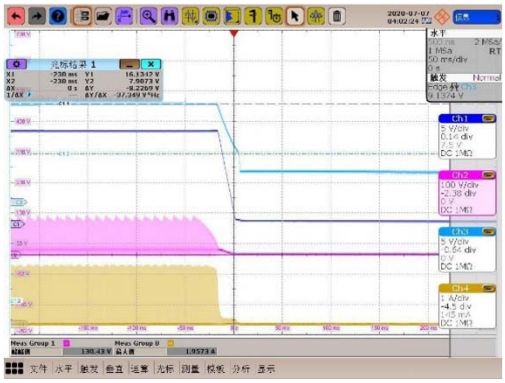
Startup with 230Vin

CH2 SW
CH3 VCC
CH4 Ipk



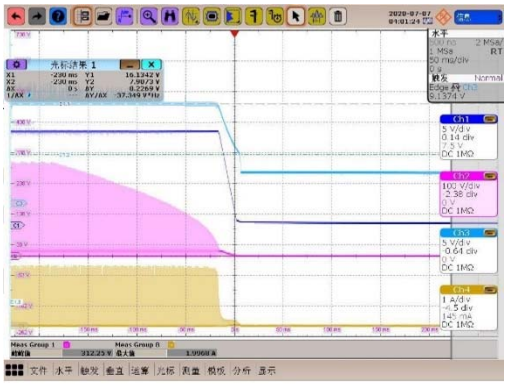
Shutdown with 90Vin

CH2 SW
CH3 VCC
CH4 Ipk



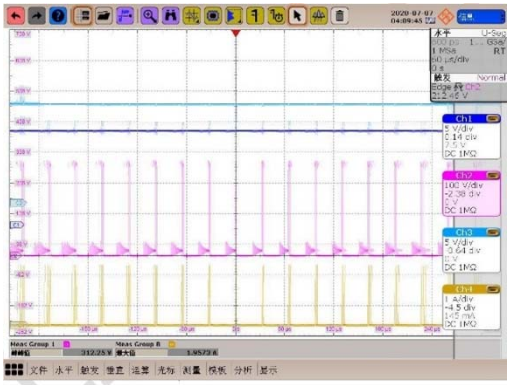
Shutdown with 230Vin

CH2 SW
CH3 VCC
CH4 Ipk



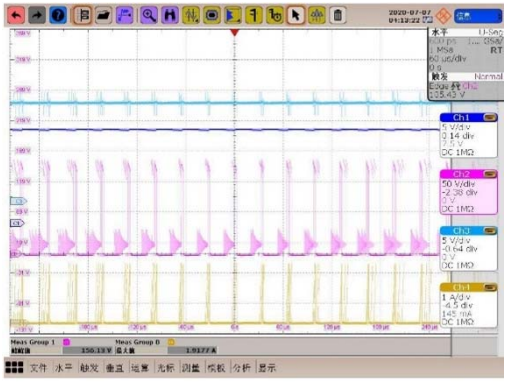
220Vin Output Full Load

CH1 VO
CH2 SW
CH3 VCC
CH4 Ipk



110Vin Output Full Load

CH1 VO
CH2 SW
CH3 VCC
CH4 Ipk

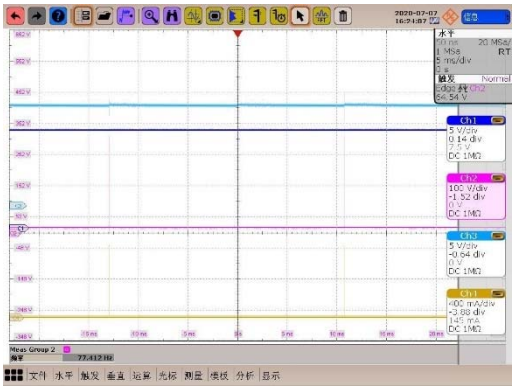


Typical Performance Characteristic

Vin=230Vac, Vout=15V, Iout=0.3A, and T_A = +25°C, unless otherwise noted.

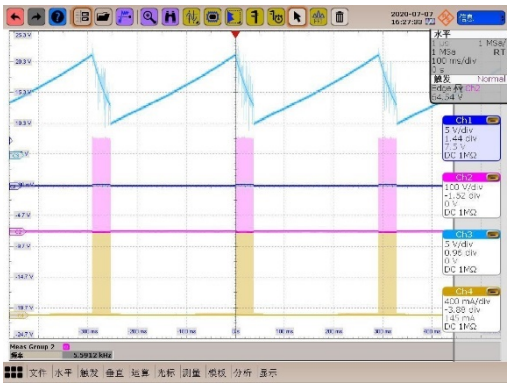
220V Output No Load

CH1 VO
CH2 SW
CH3 VCC
CH4 Ipk



220V Output Short

CH1 VO
CH2 SW
CH3 VCC
CH4 Ipk



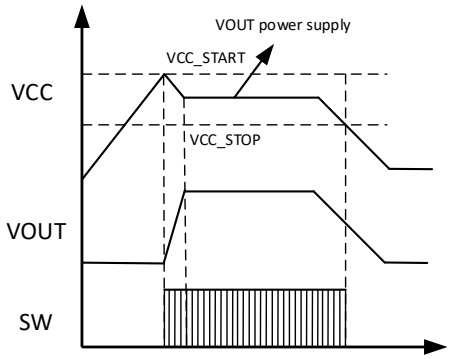
Function Descriptions

LA4100 is peak current mode control green mode operation regulator. The power MOSFET ON time is controlled by the peak current limit. IC controls the OFF time to regulate the output voltage. LA4100 switching frequency will decrease with load decreasing. As a result, LA4100 can achieve excellent light load efficiency. LA4100 always works in discontinuous current mode (DCM). Built-in loop compensation, no need for extra compensation components and simple the design.

Startup and Input Under Voltage Lockout

Before IC starts switching, LA4100 VCC start current is as low as 3.1μA typ. VCC can be charged by the pull resistor from VIN. IC remains low start current consumption until VCC charged above (V_{CC_START})15.5V. After VCC charged above V_{CC_START}, IC starts switching output will go up and supply the VCC via the external diode. The VCC supply voltage needs to be higher than (V_{CC_STOP}) 7.8V.

When VCC voltage falls below the V_{CC_STOP}, LA4100 will stops switching to avoid abnormal operation. VCC need to be recharged to V_{CC_START} to restart the IC. Proper pull-up resistor needs to be designed to achieve short circuit or over temperature protection.



Startup Timing

Output Voltage Regulation

LA4100 works in DCM mode operation and it can regulate the output voltage under different load and input voltage condition. Whenever High-side (HS) power MOSFET is off, FB1 will become the sense of the output voltage. After a Tsenseblk blanking time when the HS power MOSFET is off, VOUT will be sensed via FB1 and send to internal error amplifier. The output of the error amplifier will control the timing of next on pulse, also it controls the peak current. To keep the VOUT stable at different load condition: it adjust the switching frequency and I_{PK} to regulation the output voltage.

LA4100 will enter Eco mode under extremely light load or no-load condition to avoid IC cannot monitor FB1 for a long time. In Eco mode, the maximum off time is 20ms typical.

Output Under Voltage Protection and Over Voltage Protection

LA4100 has innovated FB2 to improve the load transient performance of High-side buck structure design. When HS power MOSFET is off, the inductor current will drops to 0A and then IC enters Hi-Z state. FB2 monitors the VOUT via the shunt resistor from VOUT+ to VOUT-. At this period IC GND connect to VOUT+ via the inductor. VOUT- is negative VOUT voltage to the IC. In normal operation FB2 is designed in the range between -179mV and -233mV. If the voltage of FB2 is higher than -179mV in Hi-Z state, IC will consider it to be VOUT under voltage which might be caused by load transient. Then it will start a new pulse immediately to avoid VOUT drops lower. On the other hand if FB2's

voltage is lower than -233mV in the Hi-Z state, then IC will consider it to be VOUT over voltage. No pulse will be allowed any more to avoid VOUT overshoot higher even if the off time is longer than the MAX off time 20ms.

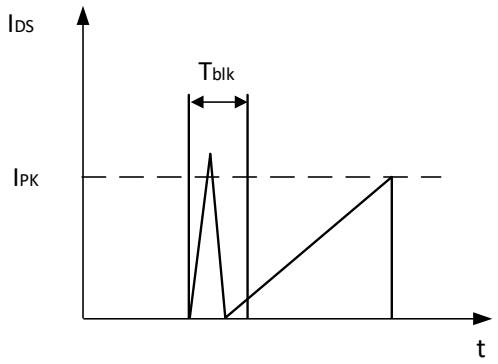
Feedback Open Output Over Voltage Protection

LA4100 can achieve VOUT over voltage protection in feedback open condition via VCC pin. LA4100 VCC working range is from 7.8V to 30V. Because VCC voltage is bias by VOUT through the external diode, VCC voltage will increase with VOUT. When VCC voltage goes above 30V, the VCC over voltage protection will be triggered. IC will be shut down and stop switching. VCC will be discharged by an internal 6mA current source. IC will stops switching until VCC drops to V_{CC_STOP}. Then the internal 6mA current source will be disconnected and VCC will be recharged up by the external pull up resistor. IC restart when VCC voltage rise above V_{CC_START}. LA4100 repeats this operation cycle until the VCC over-voltage condition disappears and the output voltage rise smoothly back the regulation level.

Current Sense

The LA4100 sensed the current in HS power MOSFET through the external Rcs resistor. When the sense voltage Vcs_pk IC will shut down the power MOSFET. The peak current determined by the Rcs resistor. The maximum I_{PK} is V_{CS_PK}/R_{CS}. When load decreases, the minimum I_{PK_MIN} is $V_{CS\_MIN}/R_{CS} = V_{CS\_PK}/2.5xR_{CS}$. To avoid V_{CS_PK} triggered by the spike current cause by the parasitic capacitance and reverse recovery current of the freewheeling diode and result in HS power MOSFET falsely off. LA4100 has implemented a blanking time (Tblk) after HS power MOSFET turns on. During the blanking time, the current limit comparator will be disabled.

LA4100 I_{PK} can be programmed by the external Rcs resistor. Recommend not to set I_{PK} higher than 3A.



Current Sense Blanking

Over Current and Short-Circuit Protection

The LA4100 max output current is limited by minimum off time and peak current limit. To avoid the current run away in the high voltage condition, LA4100 always works in DCM operation mode HS power MOSFET won't be turned on until the inductor current drops to 0A. Increase the load current the IC switching frequency will increase until reaches the DCM to CCM critical condition. If keep increasing the load the frequency cannot be increased due to inductor current peak and value limitation and VOUT starts to drop. Due to VCC is biased by VOUT via the diode, VCC will drop follow the VOUT. When VCC voltage drops below the V_{CC_STOP}, IC stops switching enter hiccup protection. Then VCC

voltage will be recharged up by the pull resistor from VIN to VCC. IC will restart after VCC is charged to V_{CC_START}. LA4100 repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Switching Frequency and Audible Noise Reduction

LA4100 is peak current control mode. IC switching frequency will decrease with load decreasing to achieve excellent light load efficiency. When LA4100 switching frequency is much higher than 20k, the switching frequency can be estimated by below formula in the DCM mode:

$$F_{SW} = \frac{2(V_{IN} - V_O)}{L * {I_{PK}}^2} * \frac{V_O * Io}{V_{IN}}$$

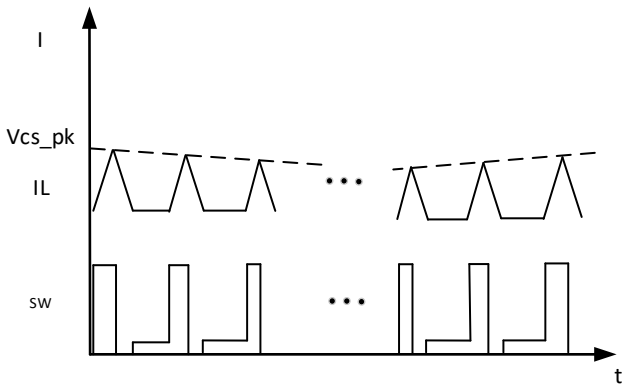
The LA4100 will gradually reduce the peak current to minimum 1/2.5 of the max peak current set by sense resistor when switching frequency drops to 20KHz. The inductor current can be greatly reduced in this condition and the load range of enter the audible noise will become smaller. After system frequency enter the audible noise range, the smaller inductor energy will reduce the noise cause by the inductor vibration.

Green Mode Operation

LA4100 switching frequency will decrease with load decreasing. As a result, LA4100 can achieve excellent light load efficiency. Different with traditional burst mode the LA4100 switching cycle can automatically decrease to 20ms maximum. As a result the light load ripple voltage and voltage overshoot has optimized.

EMI Reduction

LA4100 achieves the switching frequency jitter by modulate the V_{CS_PK}. By doing this EMI noise peak caused by the switching frequency noise will be greatly reduced sample the EMI design and reduce the solution cost.

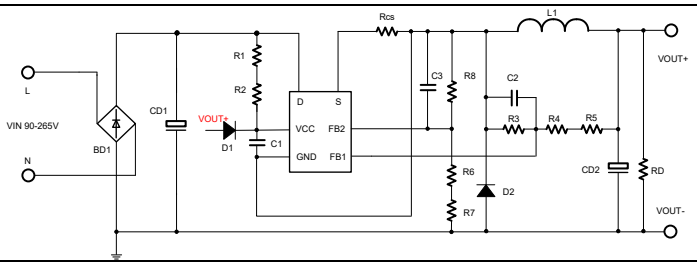
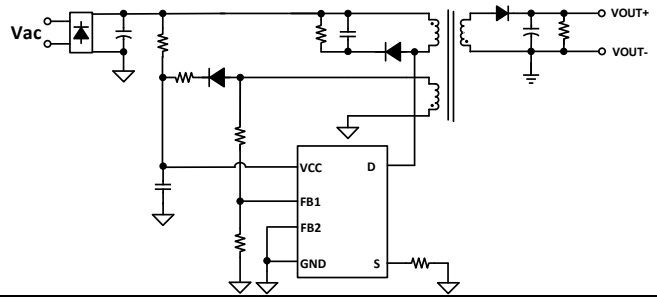


Frequency Spread Spectrum

Over Temperature Protection

LA4100 has built-in accurate over temperature protection. It monitors the MOSFET temperature and improves the system reliability. Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the MOSFET temperature exceeds 150°C, the entire chip shuts down. When MOSFET temperature drops below 150°C system will discharge and recharge VCC cap to achieve the thermal restart delay and restart the IC.

Application Information

Topology	Circuit Schematic	Feature
Non-isolated High-Side Buck		1. Non-isolated 2. Low Cost 3. Direct Feedback
Isolated PSR Flyback		1. Isolated 2. Low Cost 3. Indirect Feedback

Setting the FB1 Resistor

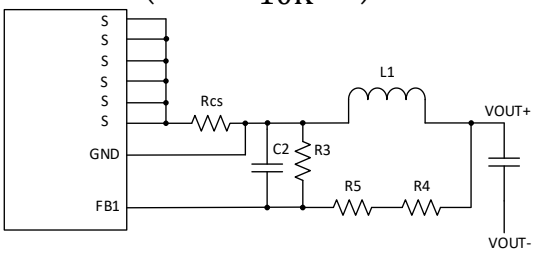
LA4100 output voltage can be set by the external resistor dividers on FB1 pin. Equation as below:

$$V_{OUT} = 2.05 * \left(1 + \frac{(R_4 + R_5)}{R_3}\right) - 0.7$$

While 0.7V is the forward voltage drop of the freewheeling diode.

Normally use a value around 10K for R3 resistor. To avoid the noise to the FB1 pin, recommend to use a 10pF/50V capacitor in parallel with R3 resistor. For this design example choose 10K for R3, 22K for R5, 47k for R4. Then the operating output voltage is:

$$V_O = 2.05 * \left(1 + \frac{22K + 47K}{10K}\right) - 0.7 = 15.5V$$

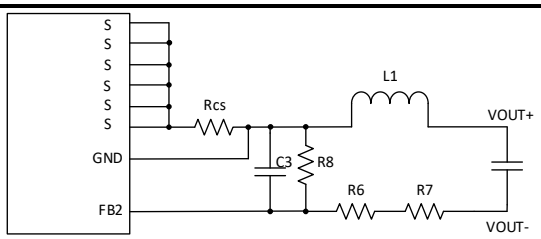


FB1 Feedback Network

Setting the FB2 Resistor

FB2 can be used to set the wake-up voltage under no-load condition. If FB2 wake-up threshold is not triggered within Toff max 20ms, then IC will work under 20ms typical switching cycle. If FB2 wake-up threshold is triggered within 20ms, LA4100 will wake up and start normal operating immediately to achieve fast loop response. If FB2 voltage is lower than -0.233V rno pulse will be allowed any more to avoid VOUT overshoot higher even if the off time is longer than the MAX off time 20ms. So in no-load output voltage max value is determined by below formula:

$$V_{O\_MAX} = 0.233 * (1 + \frac{R_6 + R_7}{R_8})$$



FB2 Feedback Network

Recommend to use smaller than 5.1K resistor for R8. Avoid the noise to the FB1 pin, recommend to use a 10pF/50V capacitor in parallel with R8 resistor. For this design example, choose 5.1K for R8, 180K for R6, 180K for R7. The no-load max output voltage will be:

$$V_{O\_MAX} = 0.233 * \left(1 + \frac{180K + 180K}{5.1K}\right) = 16.7V$$

To achieve small no-load power consumption, need to choose proper dummy resistor. The divided voltage on dummy resistor Rd recommend to below 30% of the FB2 set no-load output voltage:

$$V_{R8} = V_{IN} \frac{R_d}{R_1 + R_2 + R_d}$$

While V_{IN} is line voltage after rectified. When max voltage is 265V, in this design example

$$V_{Rd} = 265*1.414*\left({}^{47K}/_{(3000K + 3000K + 47K)}\right) = 2.91V < 16.7V * 30\%$$

Wake-up voltage is set by FB2. When FB2 below 0.179V IC will wake-up. In this design example:

$$V_O = 0.179 * \left(1 + \frac{180K + 180K}{5.1K}\right) = 12.8V$$

Setting the Max Output Current

Consider IC works in DCM to CCM critical mode under max output condition. So the max output current will be determined by below formula:

$$I_O = \frac{I_{PK}}{2}$$

While I_{PK} is the inductor peak current. I_{PK} is determined by Rcs with below formula:

$$I_{PK} = \frac{V_{CS\_PK}}{R_{CS}}$$

In this design example, choose Rcs=0.47Ω, I_O=0.3A.

Note need to choose 1% accuracy with good temperature coefficient resistor for Rcs to achieve good production and over temperature consistency.

Selecting the Inductor and Set the Switching Frequency

At full load condition, IC works in critical mode. In this case the switching frequency can be estimated by below formula:

$$F_{SW} = \frac{(V_{IN} - V_O)}{L * I_{PK}} * \frac{Vo}{V_{IN}}$$

While V_{IN} is line voltage after rectified. For example: 230VAC V_{IN}=230*1.414=325V. In this design example L_P=150uH, so the switching frequency under 230V is:

$$F_{SW} = \frac{(325 - 15.5) * 15.5}{150 * 2 * 325} \times 10^6 = 49.3K$$

Consider the EMI performance and PCB solution size. Recommend to set the switching frequency below 100KHz. Too high switching frequency will result in thermal and EMI issue. To low switching frequency will increase the solution size and increase the inductor and capacitor value.

Selecting the Startup Resistor and VCC Capacitor

LA4100 VCC start current is as small as 3.1uA typical. Choose an pull-up resistor with higher than 10μA will be enough. When design to achieve low no-load power consumption, choose a large pull-up resistor to reduce the input current. When design to achieve fast startup, choose a small pull-up resistor. Recommend not to choose Schottky diode due to the Schottky diode will have large leakage current at high temperature. If must use Schottky diode need choose smaller pull-up resistor to avoid startup failure at high temperature. Normally choose a value between 200K to 8MΩ for the pull-up resistor.
Choose 1μF to 4.7μF capacitor for VCC cap. Due to after IC starts switching VCC will consume more current and pull-up resistor may not be able to supply. VCC need to be supply by the VOUT via the external diode. If output capacitor is too big, need to choose a larger VCC cap to avoid VCC drop below V_{CC_STOP} before VOUT ramp up.
In this design example, choose 3MΩ for both R1 and R2 resistor.

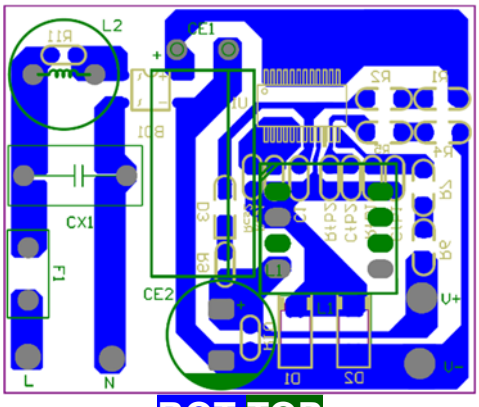
Selecting the Output Capcitor

Output capacitor is used to maintain the output voltage. The steady state ripple voltage can be calculated with below formula:

$$V_{OUT\_ripple} = \frac{I_{PK}}{8F_{SW} * C_{OUT}} + I_{PK} * R_{ESR}$$

Recommend to choose low ESR Aluminum electrolytic capacitor to reduce the output ripple voltage.
Due to the FB2 design, LA4100 has good transient performance. Doesn't need to use too large output capacitor to achieve the transient requirement. Under 1A load condition, 470μF output capacitor will be enough. The output capacitance can be reduced if the full load condition reduced.
In this design example, choose 100uF/25V for CD2.

PCB LAYOUT

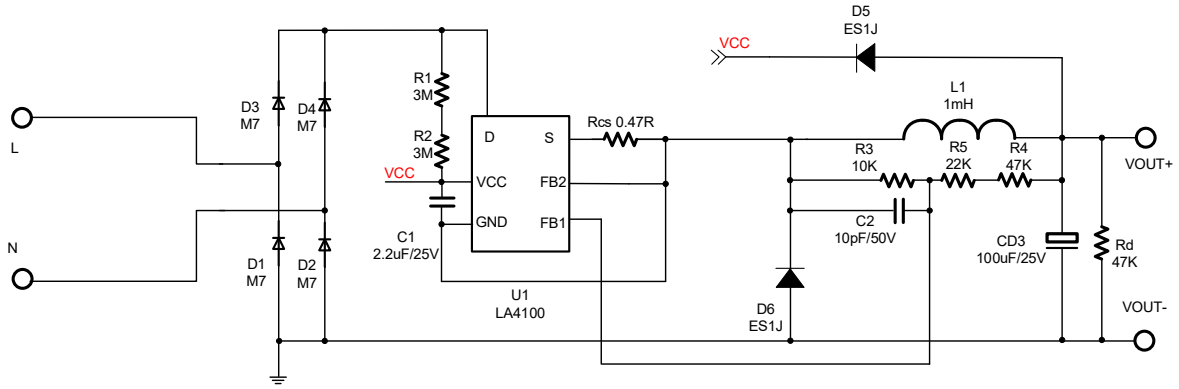


Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

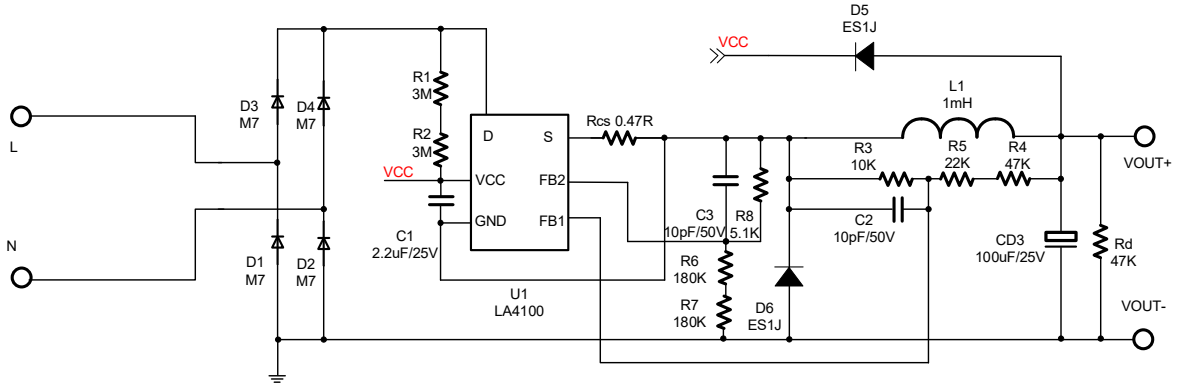
- High voltage- Low voltage trace distance need to wider than 1mm.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.

- Don’t put the heat sourcing device close to each other on the PCB to achieve good thermal performance. The heat sourcing device are: Rectifier bridge, LA4100, inductor, freewheeling diode.
- For double-sided PCB don’t do cross line on the power trace to achieve good EMI.
- Place the external feedback resistors as close to FB1 and FB2 as possible. The FB1 and FB2 resistor need to be placed always from the Drain node of LA4100.
- Use large copper area on LA4100 Drain to achieve good heat dissipation.

Typical Application Circuit



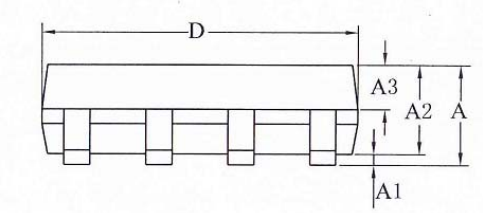
VOUT=15V, IOUT=0.3A without FB2 wakeup

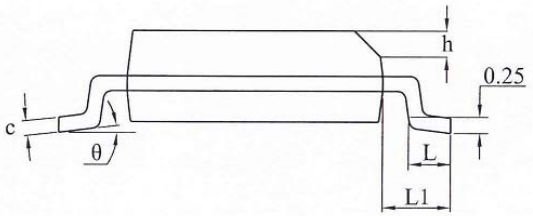


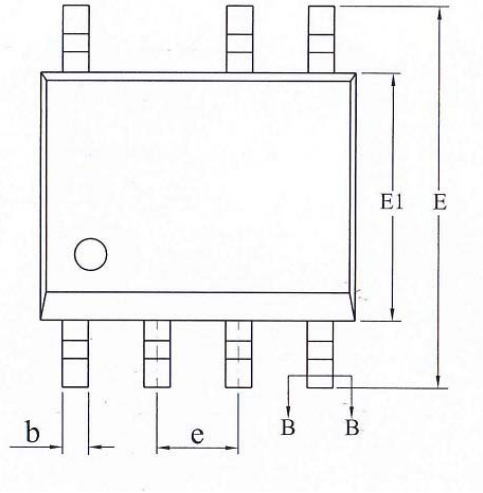
VOUT=15V, IOUT=0.3A with FB2 wakeup

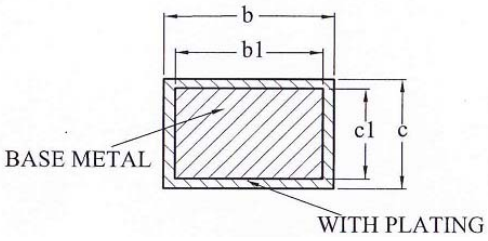
Detailed Package Outline Drawing:

Package type: SOP 7L









SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°