600V Half-Bridge Module

For Small Appliance Motor Drive Applications

LAS1M0261

Overview

LasSOP-10

LAS1M0261 is a half-bridge module designed for advanced appliance motor drive applications such as energy efficient fans and pumps. LASemi's technology offers an extremely compact, high performance half-bridge topology in an isolated package. The advanced IPM offers a combination of LASemi's low $R_{DS(on)}$ MOSFET technology and the industry benchmark half-bridge high voltage, rugged driver in a small LasSOP-10 package. The dedicated open-source pin from low side MOSFET is provided for current sensing. The input works with Schmitt-trigger and the logic voltage is compatible with 3.3V/5V/15V signal. The UVLO, deadtime and thermal shutdown are also provided.

Features

- Built-in high-performance 600V/3A FRMOSFET and >5us short circuit tolerance
- Integrated Bootstrap diode
- Robust at negative transient voltage; >2.5mm creep distance
- Gate drive supply range from 10 to 20V
- UVLO for both high side and low side
- Built-in dead time to avoid cross-conduction
- Thermal Shutdown (TSD) protection
- Over current detection
- FO/SD output for fault indication and shutdown function
- The low-profile, compact footprint SMT LasSOP-10 package offers extended creepage distances and allows heat sinking of both PowerFET through the PCB

Typical Application

- BLDC fan/pumps

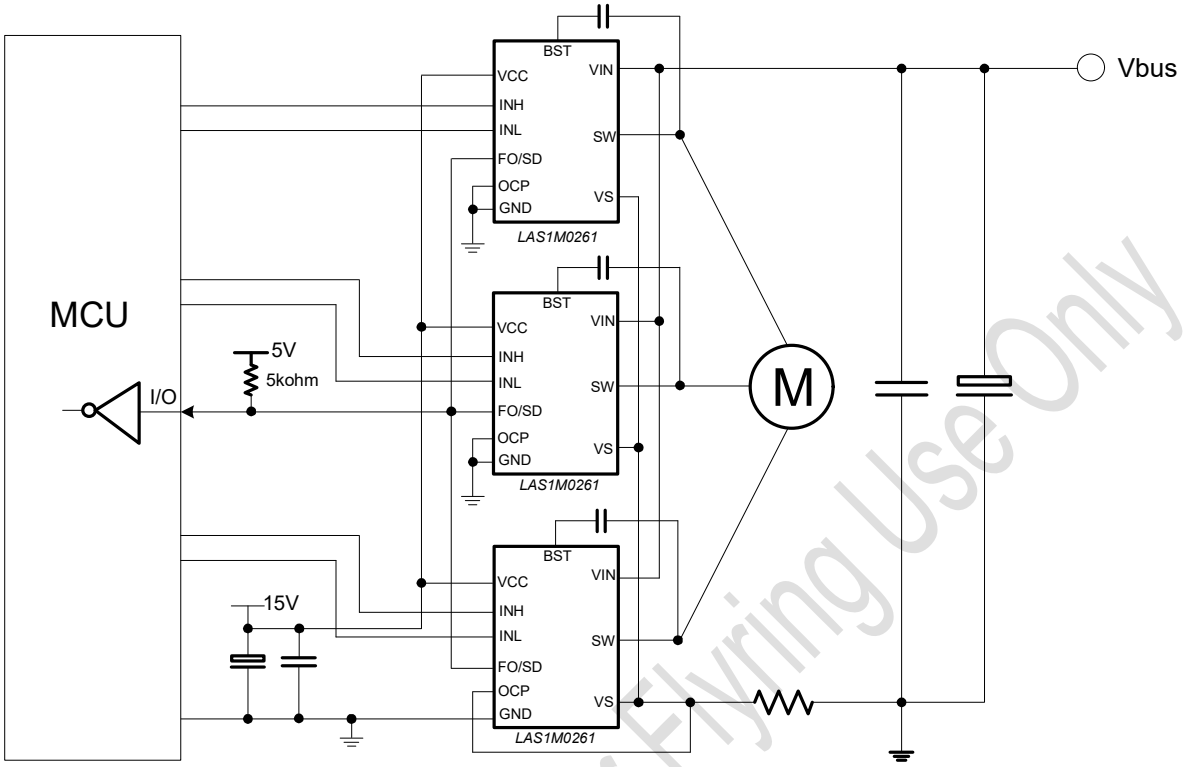


Figure 1 Single Shunt Resistor topology with over current protection function

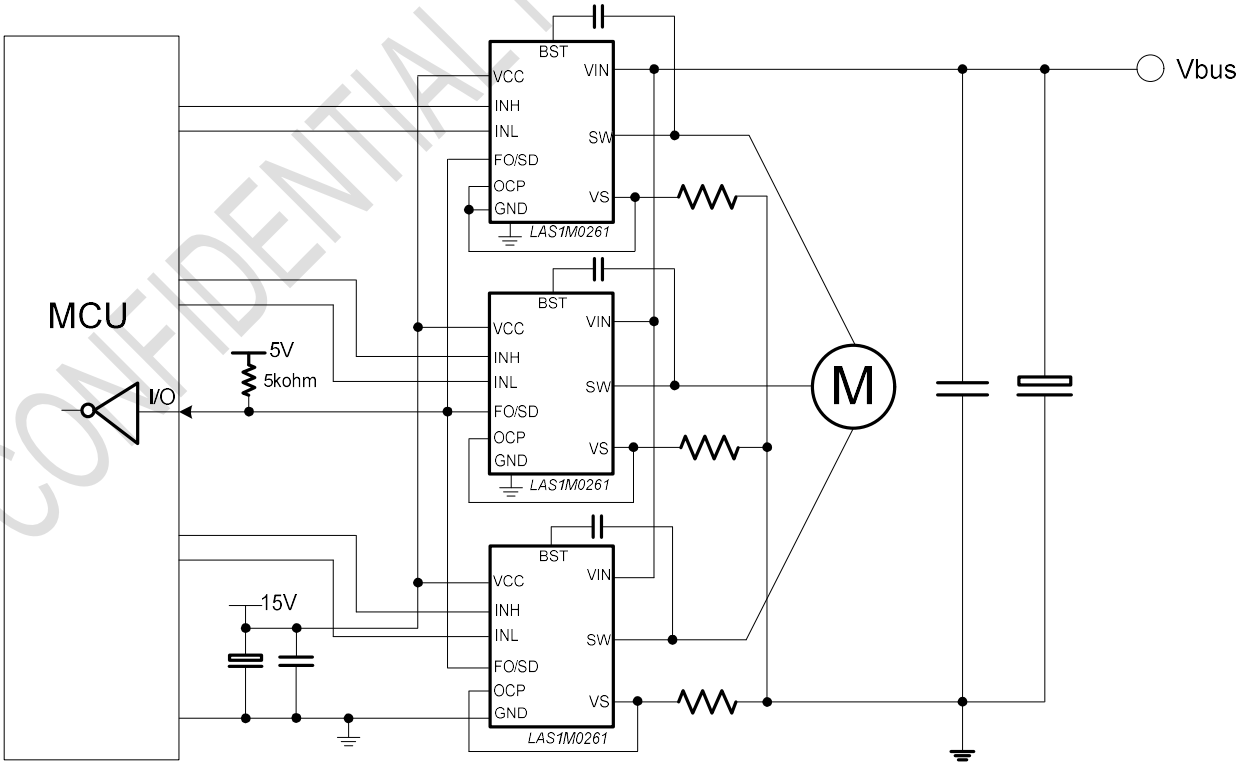
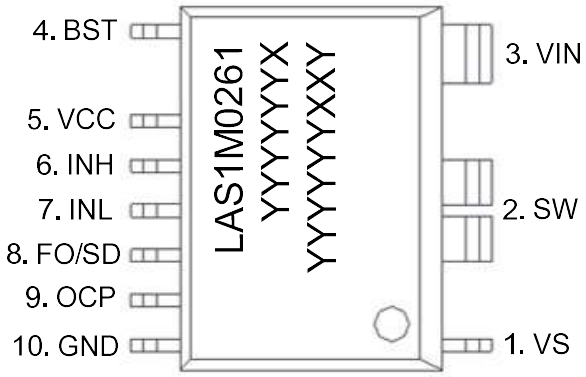


Figure 2 3-Shunt Resistors topology with individual over current protection

Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LAS1M0261	LasSOP-10	-40 to 125^{0}C	T/R 1500 pcs/roll	sales@latticeart.com

Pin Diagram

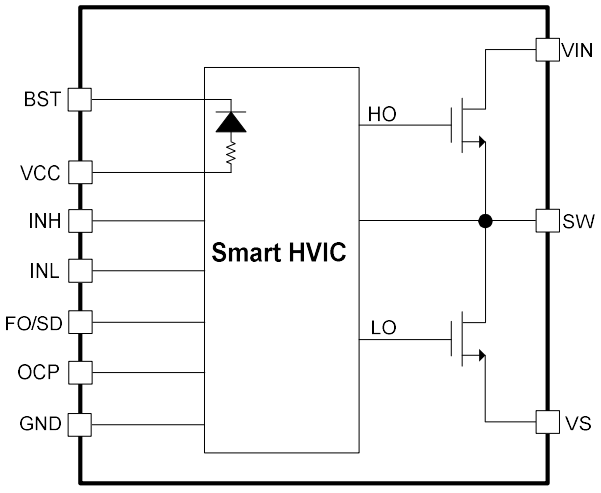


YYYYYY: IC Lot number
X: version
YYYYYY: MOS Code
XX: week number
Y: Year code

Pin Description

Pin No.	Symbol	Pin Description
1	VS	Open source for low side MOSFET
2	SW	SW phase output
3	VIN	DC bus
4	BST	High side floating supply
5	VCC	Power supply for low side
6	INH	High side gate driver input
7	INL	Low side gate driver input
8	FO/SD	Fault indicator and shutdown input
9	OCP	Over current detection; If NOT use, short OCP to GND
10	GND	Ground pin

Block Diagram



Absolute Maximum Ratings (note 1)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
VCC	Power supply voltage for low side	20	V
BST-SW	Power supply voltage for high side	20	V
VIN	DC bus	600	V
I_D	Each MOSFET current, continues, Tj<150^{o}C	1.5	A
I_{DM}	Each MOSFET pulse current<100us	3	A
HIN, LIN	Input logic voltage	20	V
FO/SD	Fault indicator and shutdown input	20	V
VS	Open source voltage	10	V
T_{STG}	Storage temperature	-55 to150	^{o}C
T_j	Junction temperature	-40 to +150	^{o}C
P_D	Total power dissipation	8.3	W

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
VCC	Power supply pin for low side	11 to 18	V
BST	High side floating supply voltage	SW+11 to SW+18	V
VIN	DC bus voltage	<500	V
HIN/LIN	Logic input voltage	VCC	V
F_{PWM}	PWM carrier frequency	<20	kHz

Electrical Characteristics

T_A=25^{0}C, unless otherwise specified.

Gate driver part

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{QVCC}	Quiescent VCC supply current	VCC=15V, HIN=LIN=0V,SW=0V	120	150	170	uA
I_{BST-SW}	Quiescent V_{BST-SW} supply current	V_{BST-SW}=15V, HIN=LIN=0V	15	30	45	uA
VCC_{ON}	VCC under-voltage rising threshold		8.3	9.1	9.9	V
VBS_{ON}	V_{BST-SW} under voltage rising threshold		8	8.5	9.4	V
VCC_{OFF}	VCC under-voltage falling threshold		7.5	8.1	8.8	V
VBS_{OFF}	VBS under-voltage falling threshold		7.5	7.8	8.5	V
VCC_{HYS}	UVLO hysteresis voltage			1		V
VBS_{HYS}	BST-SW UVLO hysteresis			0.7		V
I_{IN_LKG}	Logic “1” input bias current	HIN,LIN=5V		5		uA
I_{IN_SINK}	Logic “0” input bias current	HIN,LIN=0V			1	uA
V_{IL}	OFF threshold voltage	Logic low level			0.8	V
V_{IH}	ON threshold voltage	Logic high level	3			V
V_{OCP}	Over current protection threshold		0.38	0.43	0.48	V
V_{SD_OFF}	Shutdown threshold voltage				0.8	V
V_{SD_ON}	SD turn on threshold voltage		3			V
V_{FO}	Fault output open drain	V_{OCP}=0.6V, I_{FO}=5mA		0.5		V
V_{FO_Float}	FO floating voltage			4.8		V
R_{FO_PU}	Internal FO pull up resistor		500	680	800	kohm
DT	Dead time			100		ns
T_{FLT_IN}	Input filter			100		ns
MT	High side and low side delay match time				60	ns
T_{OTP}	Over temperature protection shutdown rising threshold			138		ºC
T_{OTP_HYS}	OTP hysteresis			28		ºC
R_{BSD}	Bootstrap diode resistance		70	100	130	ohm

Power MOS part

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	VCC=0V, I_D=500uA	600			V
I_{DSS}	Zero Gate voltage Drain Current	VCC=0V, V_{DS}=600V			1	uA
V_{SD}	Drain-source diode forward voltage	VCC=V_{BS}=10V I_D=2.5A		0.9		V
$R_{DS(ON)}$	Drain-source Turn-On Resistance	VCC=V_{BS}=15V VIN=5V, I_D=1.5A		3.2		ohm
Trr	Reverse recovery time	VIN=400V, VCC=V_{BST-SW}=12V， I_D=2A; Inductive Load, High-side and Low-side Switching		100		ns

Function Descriptions

1. Input and output True Table

HIN	LIN	OUTPUT	Description
0	0	Hi-Z	High side and low side OFF
0	1	0	Low side ON, High side OFF
1	0	VIN	High side ON, Low side OFF
1	1	Hi-Z	Forbidden input, High side and low side OFF
Open	Open	Hi-Z	Input internal pull-down resistor 1M ohm

2. Dynamic switching diagram

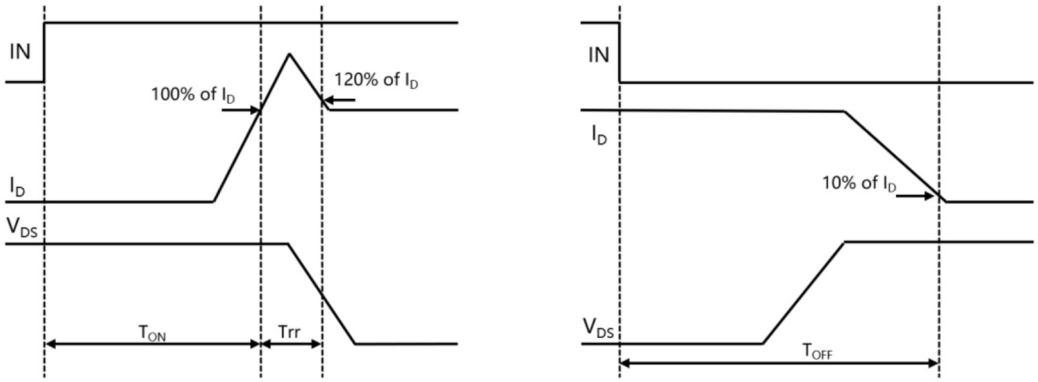


Figure 1 Dynamic switching diagram

3. Delay Match Time

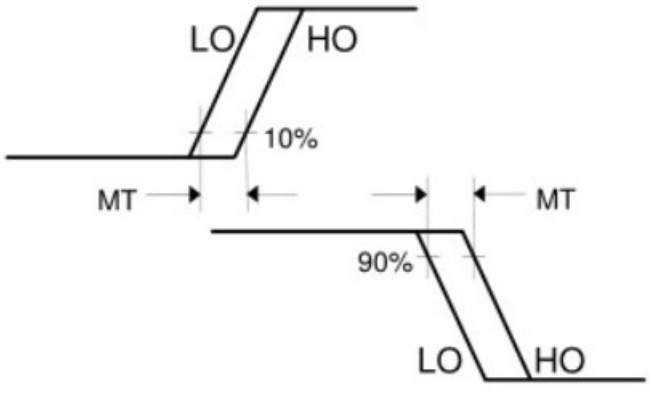


Figure 2 Delay match time

4. Thermal Shutdown (TSD)

The LAS1M0261 incorporates a thermal shutdown (TSD) circuit. Figure 3 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, a rise in ambient temperature at the device, etc.), the IC shuts down both high-side and low-side output transistors.

The TSD circuit in HVIC can monitor the power MOSFET with a relative accuracy since the compact module package makes the power device and HVIC closely placed.

When the temperature of HVIC exceeds the TSD operating temperature (T_{TSD},138°C), the TSD circuit is activated. When the temperature of the HVIC decreases to the TSD releasing Temperature(110°C) or less, the shutdown condition is released. The output transistors then resume operating according to input signals.

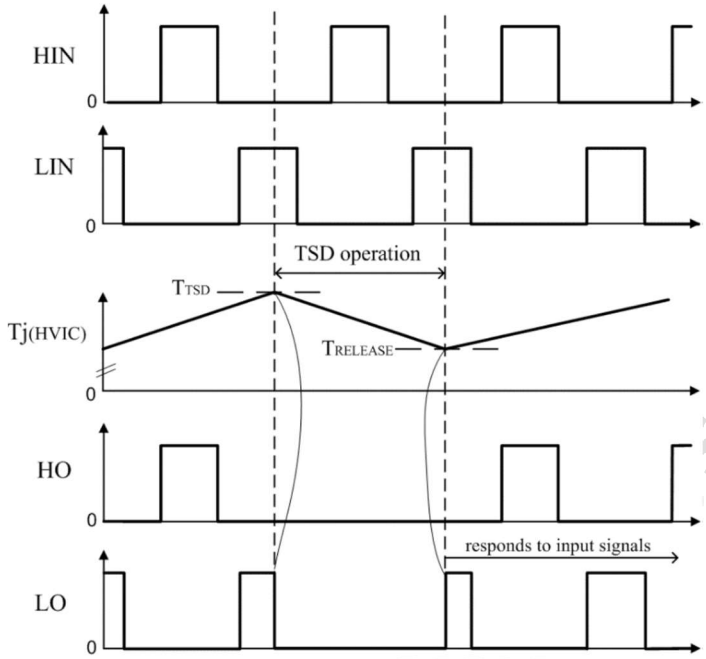


Figure 3 Thermal Shutdown Protection

5. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 4 shows operational waveforms of undervoltage lockout for low-side power supply (i.e., UVLO_VCC).

When the VCC pin voltage decreases to the logic operation stop voltage(8.0V) or less, the UVLO_VCC circuit in the corresponding phase gets activated and sets both of HO and LO signals to logic low. When the VCC pin voltage increases to the logic operation start voltage (9.0V) or more, the IC releases the UVLO_VCC operation. Then, the IC resumes the following transmissions: an LO signal according to the LIN pin input command; an HO signal according to the rising edge of the first HIN pin input command after the UVLO_VCC release.

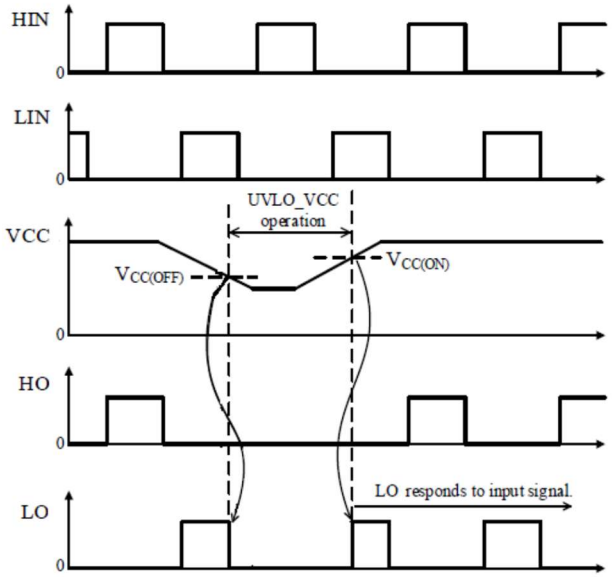


Figure 4 UVLO_VCC Operational Waveform

6. Undervoltage Lockout for High-side Power Supply (UVLO_BST)

Figure 5 shows operational waveforms of undervoltage lockout for high-side power supply (i.e., UVLO_BST).

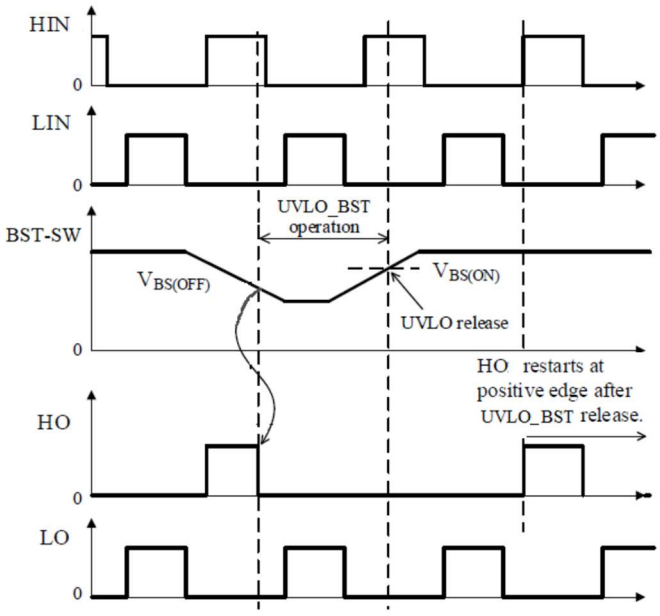


Figure 5 UVLO_BST Operational Waveform

When the voltage between the BST and SW pins decreases to the logic operation stop voltage(7.8V) or less, the UVLO_BST circuit in corresponding phase gets activated and sets an HO signal to logic low. When the voltage between BST and SW pins increases to the logic operation start voltage(8.4V) or more, the IC releases the UVLO_VB operation. Then, the HO signal becomes logic high at the rising edge of the first input command after the UVLO_VB release.

7. Over Current protection function

OCP pin detects current sensing resistor's voltage. When OCP pin's voltage exceeds

0.43V, LAS1M0261 will pull down FO/SD for 65us. As long as FO/SD stays low, HO and LO will not output driver signal no matter what HIN and LIN inputs are. If OCP function is not used, it is recommended that short OCP pin to GND.

8. FO/SD function

FO/SD is multiple function pin. This pin will indicate low voltage when LAS1M0261 enters a fault condition such as VCC UVLO, thermal shutdown, over current protection. Meanwhile FO/SD shutdown LAS1M0261's output when the pin is low.

9. PCB Design Guidelines

The LAS1M0261's VIN and SW wide-lead pin layout is configured to provided sufficient copper area for heat sinking. Figure 6 gives an example of the PCB layout.

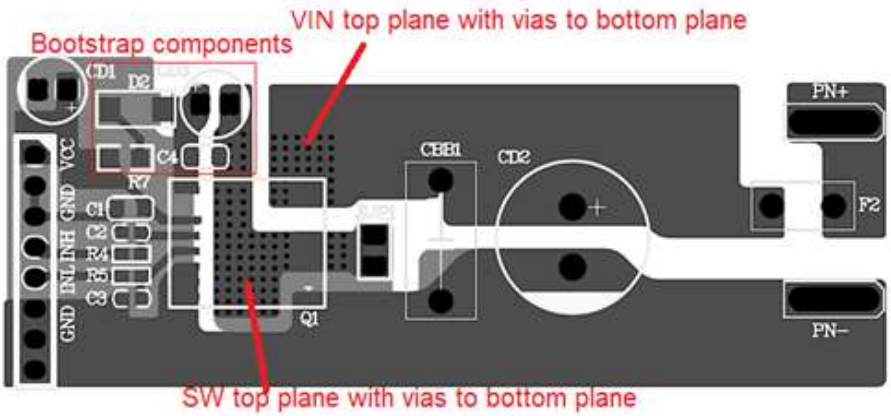
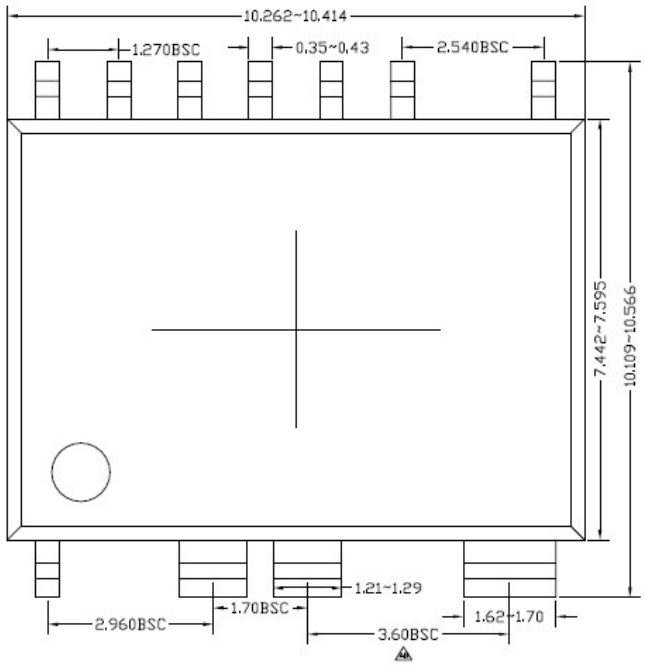
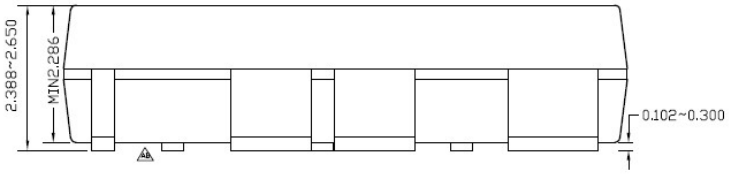


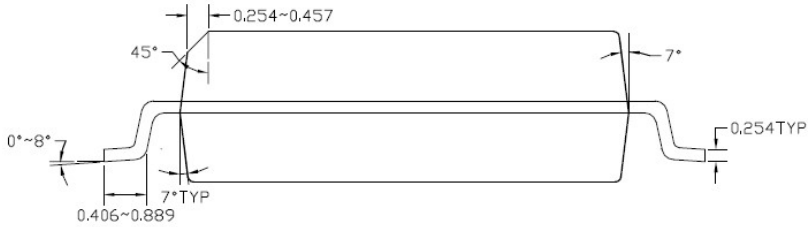
Figure 6 PCB Design example

Detail Package Outline Drawing

Package type: LasSOP10







1). LEADFRAME MATERIAL: COPPER
2). LEADFRAME THICKNESS: 0.203
3). FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.1 MM.
4). BOTH PACKAGE LENGTH AND WIDTH DO NOT INCLUDE MOLD FLASH.
5). CONTROLLING DIMENSION: MM
6). REFERENCE JEDEC MS-013, MS-012
7). THE SIZE LABEL OF THE LENGTH AND WIDTH IN THE DRAWING BELONG TO THE BOTTOM SIZE OF THE PACKAGE.