600V Half Bridge Gate driver

LA7101

Overview

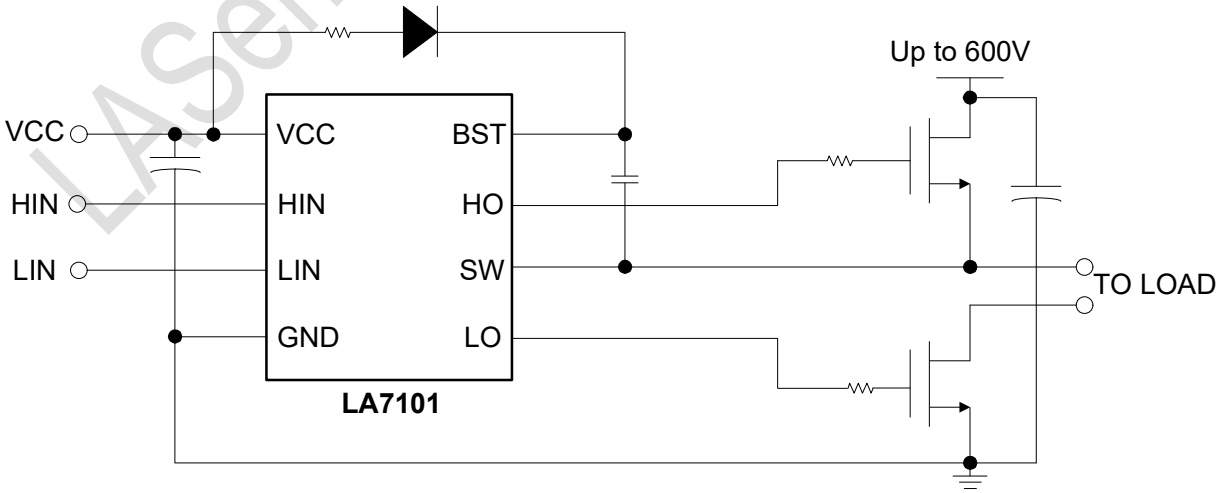
LA7101 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. he output drivers feature a high pulse current buffer stage designed for minimum river cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

SOP8

Features

- Floating channel designed for bootstrap operation; Fully operational to +600V; Tolerant to negative transient voltage dv/dt immune
- Gate drive supply range from 10 to 20V.
- UVLO for both high side and low side
- Built-in dead time to avoid cross-conduction; Matched propagation delay for both channels
- Available in SOP8 package

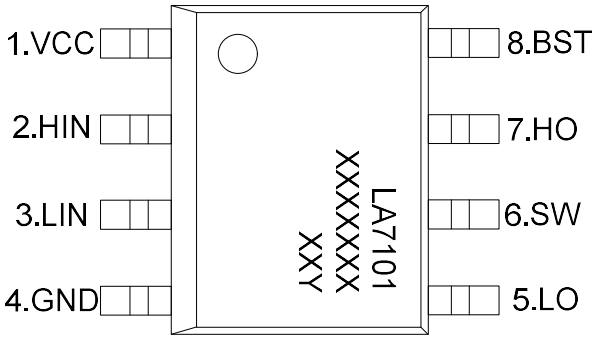
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA7101	SOP8	-40 to 150^{0}C	T/R 3000pcs/roll	sales@latticeart.com

Pin Diagram

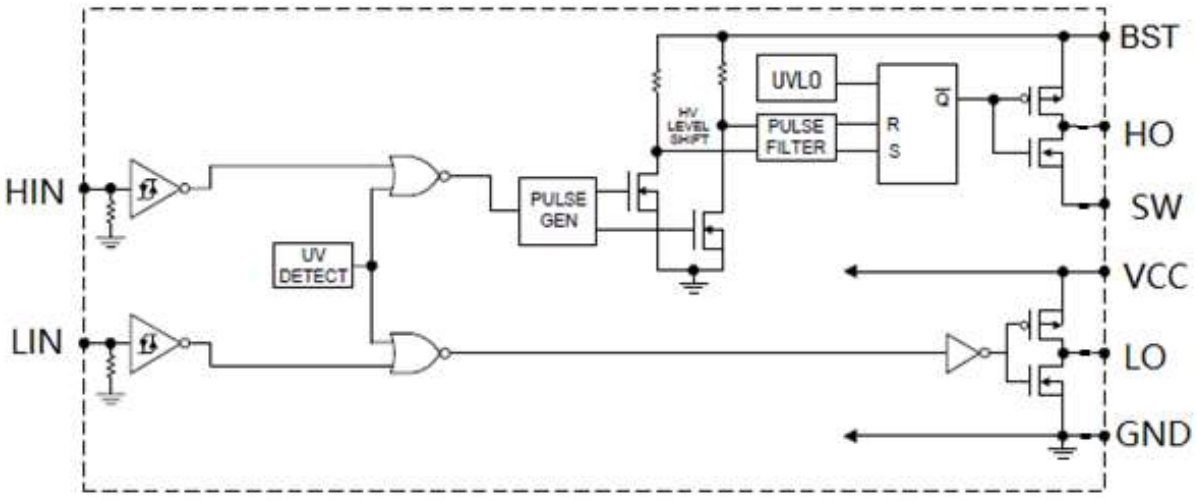


XXXXXX: Lot number
Last X: version
XX: week code
Y: Year code

Pin Description

Pin No.	Symbol	Pin Description
1	VCC	Power supply for low side and logic
2	HIN	Logic input for high side gate driver
3	LIN	Logic input for low side gate driver
4	GND	Ground pin
5	LO	Low side gate driver output
6	SW	SW phase output
7	HO	High side gate driver output
8	BST	High side floating supply

Block Diagram



Absolute Maximum Ratings (note 1)

Tj=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
BST	High side floating supply voltage	625	V
SW	High side floating supply offset voltage	BST-25	V
V_{HO}	High side floating output voltage	SW-0.3 to BST+0.3	V
VCC	Low side and logic supply voltage	25	V
V_{LO}	Low side output voltage	VCC+0.3	V
HIN, LIN	Input logic voltage	20	V
dV_{SW}/dt	Allowable offset supply voltage transient	50	V/ns
T_{STG}	Storage temperature	-55 to150	ºC
T_j	Junction temperature	-40 to +150	ºC
$R_{th(j-c)}$	Junction to case thermal resistance	200	ºC/W
P_D	Total power dissipation	0.625	W
T_L	Lead temperature(soldering, 10 seconds)	300	ºC
ESD	Human Body mode	2k	V

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
VCC	Power supply pin for low side	10 to 20	V
BST	High side floating supply voltage	SW+10 to SW+20	V
SW	High side floating supply offset voltage	<600	V
$V_{HO\&LO}$	Gate driver output voltage	VCC	V
HIN/LIN	Logic input voltage	<18	V
T_A	Ambient temperature	-40 to 125	ºC

Electrical Characteristics

Dynamic Electrical Characteristics

V_{BIAS}(VCC, V_{BS})=15, C_L=1000pF and T_A=25^{0}C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{ON}	Turn-on propagation delay	SW=0V		200	260	ns
T_{OFF}	Turn-on propagation delay	SW=600V		200	260	ns
T_{DT}	Dead Time			100		ns
T_r	Turn-on rise time			100	170	ns
T_f	Turn-off fall time			50	90	ns
MT	Delay matching, HS&LS turn-on/off				50	ns

Static Electrical Characteristics

VBIAS (VCC, VBS) = 15V and TA = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to GND. The VO and IO parameters are referenced to GND and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage	VCC=10V to 20V	3			V
V_{IL}	Logic “0” input voltage	VCC=10V to 20V			0.8	V
V_{OH}	High level output voltage, VBIAS-VO	I_o=0A			100	mV
V_{OL}	LO level output voltage, VBIAS-VO	I_o=0A			100	mV
I_{LK}	Offset supply leakage current	BST=SW=600V			10	uA
I_{QBS}	Quiescent V_{BST-SW} supply current	VIN = 0V or 5V	15	30	45	uA
I_{QVCC}	Quiescent VCC supply current	HIN=LIN=0V	65	95	125	uA
I_{IN_LKG}	Logic “1” input bias current	HIN,LIN=5V		5		uA
I_{IN_SINK}	Logic “0” input bias current	HIN,LIN=0V			1	uA
VCC_{ON}	VCC under-voltage rising threshold		8.5	9	9.7	V
VBS_{ON}	V_{BST-SW} under voltage rising threshold		7.8	8.4	9.2	V
VCC_{UVLO}	VCC under-voltage falling threshold		7.5	8	8.5	V
VBS_{UVLO}	VBS under-voltage falling threshold		7.5	7.8	8.5	V
VCC_{HYS}	UVLO hysteresis voltage		0.7	1	1.3	V
VBS_{HYS}	BST UVLO hysteresis voltage		0.4	0.6	0.8	V
I_{O+}	Output high short circuit pulse current	Vo=0V, VIN=5V, Pulse width<10us		210		mA
I_{O-}	Output low short circuit pulse	Vo=15V,		400		mA

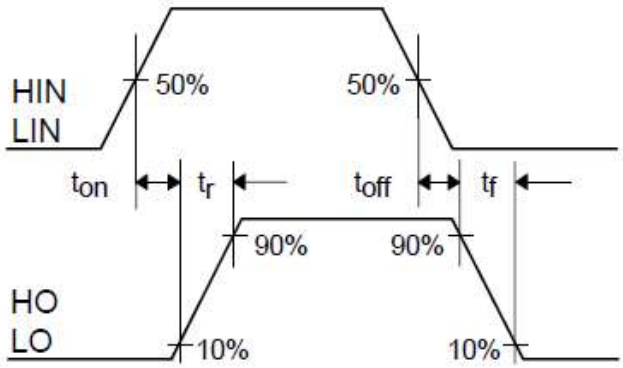
	current	VIN=5V, Pulse width<10us				

Function Descriptions

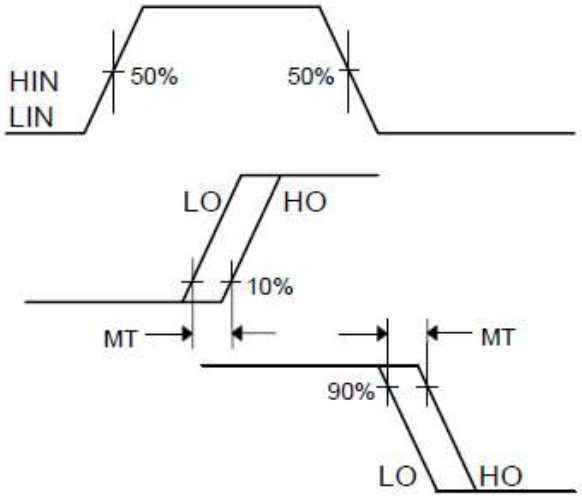
1. Input and output true table

HIN	LIN	OUTPUT	Description
0	0	Hi-Z	High side and low side OFF
0	1	0	Low side ON, High side OFF
1	0	VM	High side ON, Low side OFF
1	1	Hi-Z	Forbidden input, High side and low side OFF
Open	Open	Hi-Z	Input internal pull-down resistor 1M ohm

2. Dynamic switching diagram

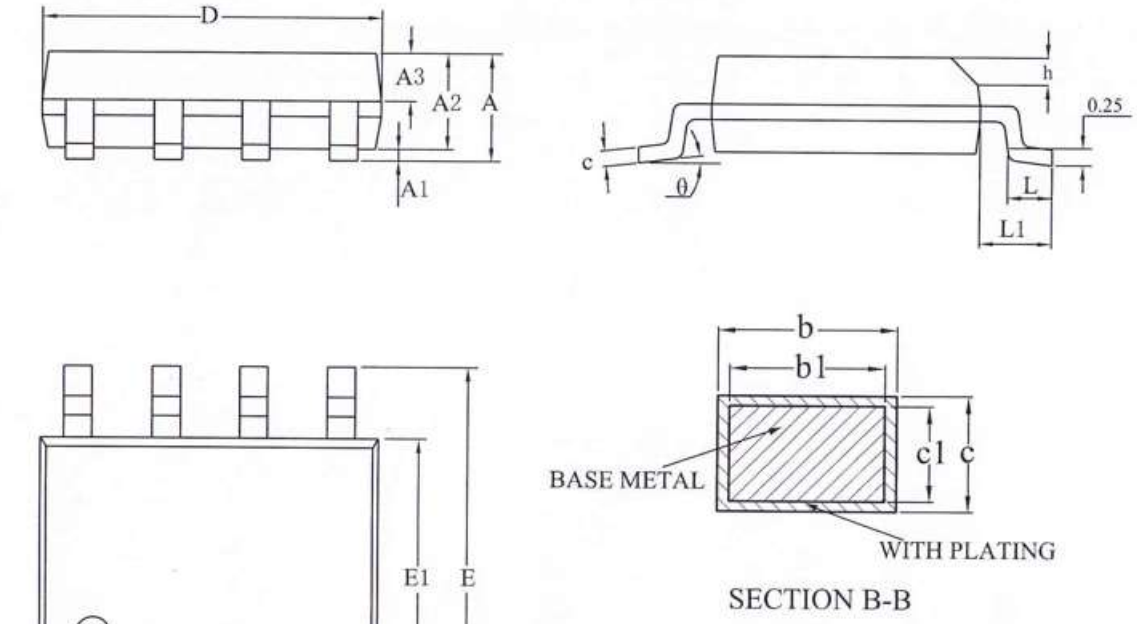


3. Delay Match Time



Detail Package Outline Drawing

SOP8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°