



#### **40V P-CHANNEL ENHANCEMENT MODE MOSFET**

### **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>A</sub> = +25°C
-40V	11mΩ @ V <sub>GS</sub> = -10V	-10.1A
-400	15mΩ @ V <sub>GS</sub> = -4.5V	-8.8A

## **Description & Applications**

This MOSFET is designed to meet the stringent requirements of Automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- DC-DC Converters
- Power Management Functions
- Analog Switch

## **Features and Benefits**

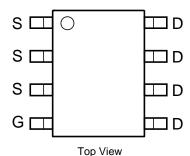
- 100% Unclamped Inductive Switch (UIS) Test in Production
- Low Input Capacitance
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DMP4015SSSQ is suitable for automotive applications requiring specific change control and is AEC-Q101 qualified, is PPAP capable, and is manufactured in IATF16949:2016 certified facilities.

### **Mechanical Data**

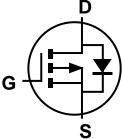
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.
  UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
  Solderable per MIL-STD-202, Method 208 <sup>23</sup>
- Weight: 0.074 grams (Approximate)











**Equivalent Circuit** 

### **Ordering Information** (Note 4)

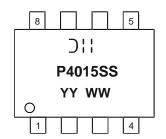
Part Number	Qualification	Case	Packaging
DMP4015SSSQ-13	Automotive	SO-8	2,500/Tape & Reel

Pin Configuration

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

# **Marking Information**



⊃;; = Manufacturer's Marking P4015SS = Product Type Marking Code YYWW = Date Code Marking YY = Year (ex: 19 = 2019) WW = Week (01 to 53)



# **Maximum Ratings** (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	$V_{DSS}$	-40	V		
Gate-Source Voltage			$V_{GSS}$	±25	V
Continuous Prais Current (Note 5) / 40/	Steady	$T_A = +25^{\circ}C$		-9.1	A
Continuous Drain Current (Note 5) V <sub>GS</sub> = -10V	State	$T_A = +70^{\circ}C$	- I <sub>D</sub>	-7.2	
Continuous Drain Current (Note 5) V <sub>GS</sub> = -4.5V	Steady	T <sub>A</sub> = +25°C	- I <sub>D</sub>	-7.8	A
Continuous Diain Current (Note 5) VGS = -4.5V	State	T <sub>A</sub> = +70°C		-6.2	
Continuous Drain Current (Note 6) V 40V	Steady T			-10.1	Α
Continuous Drain Current (Note 6) V <sub>GS</sub> = -10V	State	T <sub>A</sub> = +70°C	I <sub>D</sub>	-8	A
Continuous Drain Current (Note 6) \/- 45\/	Steady	$T_A = +25^{\circ}C$	· I <sub>D</sub>	-8.8	A
Continuous Drain Current (Note 6) V <sub>GS</sub> = -4.5V	State	$T_A = +70^{\circ}C$		-7	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I <sub>DM</sub>	-100	Α		
Avalanche Current (Note 7)			I <sub>AS</sub>	-22	Α
Avalanche Energy (Note 7)	E <sub>AS</sub>	242	mJ		

## **Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	$P_{D}$	1.45	W
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	88	°C/W
Total Power Dissipation (Note 6)	P <sub>D</sub>	1.82	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{ heta JA}$	70	°C/W
Thermal Resistance, Junction to Case (Note 6)	R <sub>θJC</sub>	7.6	°C/W
Operating and Storage Temperature Range	$T_{J}, T_{STG}$	-55 to +150	°C

# **Electrical Characteristics** (@ $T_A = \pm 25^{\circ}C$ , unless otherwise specified.)

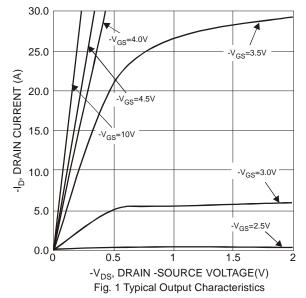
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-40	_	_	V	$V_{GS} = 0V, I_D = -250\mu A$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		_	-1	μΑ	$V_{DS} = -40V, V_{GS} = 0V$	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 25V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	-1.5	-2	-2.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	J		7	11	0	$V_{GS} = -10V, I_D = -9.8A$	
Static Diam-Source On-Resistance	R <sub>DS(ON)</sub>		9	15	mΩ	$V_{GS} = -4.5V$ , $I_D = -9.8A$	
Forward Transfer Admittance	Y <sub>fs</sub>		26		S	$V_{DS} = -20V, I_{D} = -9.8A$	
Diode Forward Voltage (Note 5)	$V_{SD}$	_	-0.7	-1	V	$V_{GS} = 0V, I_{S} = -1A$	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	C <sub>iss</sub>		4,234	_		V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V f = 1MHz	
Output Capacitance	Coss		1,036		pF		
Reverse Transfer Capacitance	C <sub>rss</sub>	_	526	_		I = IIVII IZ	
Gate Resistance	$R_{g}$		7.77		Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge	$Q_g$		47.5			$V_{DS} = -20V, V_{GS} = -5V$ $I_{D} = -9.8A$	
Gate-Source Charge	$Q_{gs}$		14.2	_	nC		
Gate-Drain Charge	$Q_{gd}$	_	13.5	_			
Turn-On Delay Time	t <sub>D(ON)</sub>	_	13.2	_		$V_{GS} = -10V, V_{DD} = -20V, R_g = 6\Omega,$	
Turn-On Rise Time	t <sub>R</sub>	_	10	_	ns		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	_	302.7		115	$I_D = -1A, R_L = 20\Omega$	
Turn-Off Fall Time	t <sub>F</sub>	_	137.9	_			

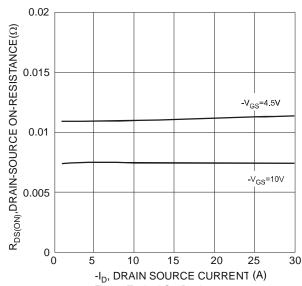
Notes:

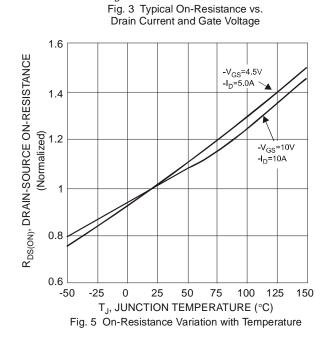
- 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout. 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
- 7. UIS in production with L = 1mH,  $T_J = +25$ °C.
- 8. Short duration pulse test used to minimize self-heating effect.
- 9. Guaranteed by design. Not subject to production testing.

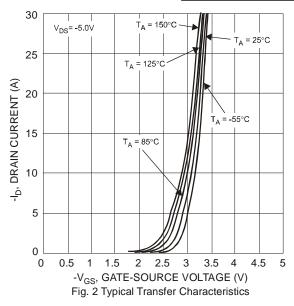


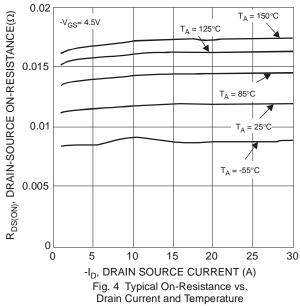






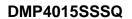






0.016 0.016 0.012 0.012 0.004 0.

Fig. 6 On-Resistance Variation with Temperature





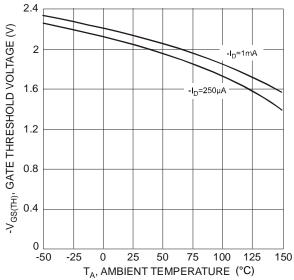
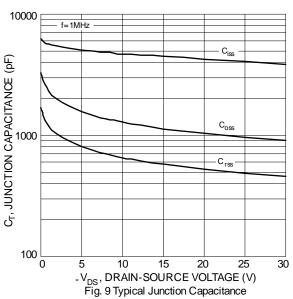
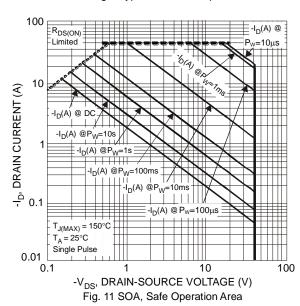
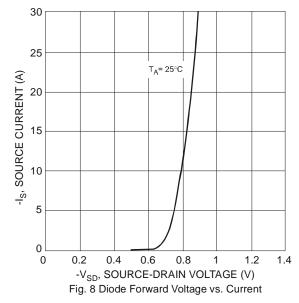
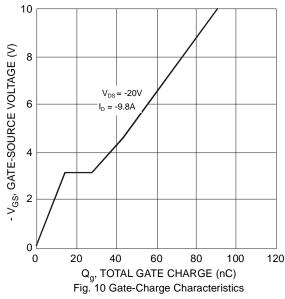


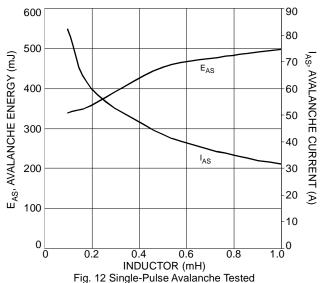
Fig. 7 Gate Threshold Variation vs. Ambient Temperature



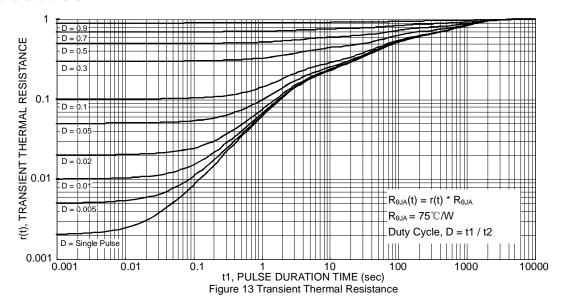










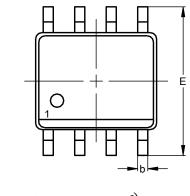


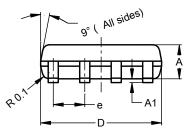


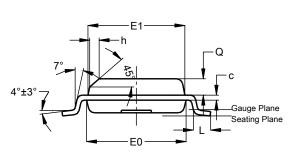
## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.





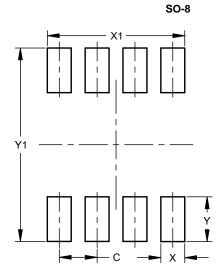




SO-8					
Dim	Min	Max	Тур		
Α	1.40	1.50	1.45		
<b>A1</b>	0.10	0.20	0.15		
b	0.30	0.50	0.40		
С	0.15	0.25	0.20		
D	4.85	4.95	4.90		
Е	5.90	6.10	6.00		
E1	3.80	3.90	3.85		
E0	3.85	3.95	3.90		
е			1.27		
h			0.35		
L	0.62	0.82	0.72		
Q	0.60	0.70	0.65		
All Dimensions in mm					

# Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)
С	1.27
X	0.802
X1	4.612
Y	1.505
V1	6.50



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