

June 1993 Revised February 2005

# 74VHC14 Hex Schmitt Inverter

#### **General Description**

The VHC14 is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC04 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals, thus providing greater noise margin than conventional inverters.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

#### **Features**

- High Speed:  $t_{PD}$  = 5.5 ns (typ) at  $V_{CC}$  = 5V
- $\blacksquare$  Low power dissipation: I\_CC = 2  $\mu$ A (Max) at T\_A = 25 °C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min)
- Power down protection is provided on all inputs
- Low noise: V<sub>OLP</sub> = 0.8V (Max)
- Pin and function compatible with 74HC14

#### **Ordering Code:**

Order Number	Package Number	Package Description					
74VHC14M (Note 1)	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow					
74VHC14MX_NL (Note 2)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow					
74VHC14SJ (Note 1)	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide					
74VHC14MTC (Note 1)	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74VHC14MTC_NL (Note 3)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74VHC14MTCX_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide					
74VHC14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide					

Pb-Free package per JEDEC J-STD-020B.

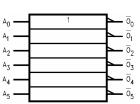
Note 1: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Note 2: "\_NL" indicates Pb-Free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

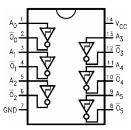
 $\textbf{Note 3: } \verb|`\_NL" indicates Pb-Free product (per JEDEC J-STD-020B).$ 

## Logic Symbol

#### IEEE/IEC



## **Connection Diagram**



## **Pin Descriptions**

Pin Names	Description				
A <sub>n</sub>	Inputs				
$\overline{O}_n$	Outputs				

## Truth Table

Α	0
L	Н
Н	L

#### **Absolute Maximum Ratings**(Note 4)

 $\begin{array}{lll} \mbox{Supply Voltage (V}_{\mbox{CC}}) & -0.5\mbox{V to } +7.0\mbox{V} \\ \mbox{DC Input Voltage (V}_{\mbox{IN}}) & -0.5\mbox{V to } +7.0\mbox{V} \\ \end{array}$ 

Storage Temperature ( $T_{STG}$ )  $-65^{\circ}C$  to  $+150^{\circ}C$ 

Lead Temperature (T<sub>L</sub>)

Soldering (10 seconds)

## Recommended Operating Conditions (Note 5)

Note 4: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The data book specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifica-

tions.

260°C

Note 5: Unused inputs must be held HIGH or LOW. They may not float.

#### **DC Electrical Characteristics**

Symbol	Parameter	V <sub>cc</sub>	T <sub>A</sub> = 25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions		
Syllibol		VCC	Min	Тур	Max	Min	Max	Units	Col	iditions	
$V_{P}$	Positive Threshold Voltage	3.0			2.20		2.20				
		4.5			3.15		3.15	V			
		5.5			3.85		3.85				
$V_N$	Negative Threshold Voltage	3.0	0.90			0.90					
		4.5	1.35			1.35		V			
		5.5	1.65			1.65					
$V_{H}$	Hysteresis Voltage	3.0	0.30		1.20	0.30	1.20				
		4.5	0.40		1.40	0.40	1.40	V			
		5.5	0.50		1.60	0.50	1.60				
V <sub>OH</sub>	HIGH Level Output Voltage	2.0	1.9	2.0		1.9			$V_{IN} = V_{IL}$		
		3.0	2.9	3.0		2.9		V		$I_{OH} = -50 \mu A$	
		4.5	4.4	4.5		4.4					
		3.0	2.58			2.48		V	1	$I_{OH} = -4 \text{ mA}$	
		4.5	3.94			3.80		v		$I_{OH} = -8 \text{ mA}$	
V <sub>OL</sub>	LOW Level Output Voltage	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH}$		
		3.0		0.0	0.1		0.1	V		$I_{OL} = 50 \mu A$	
		4.5		0.0	0.1		0.1				
		3.0			0.36		0.44	V	1	$I_{OL} = 4 \text{ mA}$	
		4.5			0.36		0.44	v		$I_{OL} = 8 \text{ mA}$	
I <sub>IN</sub>	Input Leakage Current	0-5.5			±0.1		±1.0	μΑ	V <sub>IN</sub> = 5.5V or GND		
Icc	Quiescent Supply Current	5.5			2.0		20.0	μΑ	$V_{IN} = V_{CC}$ or GND		

#### **Noise Characteristics**

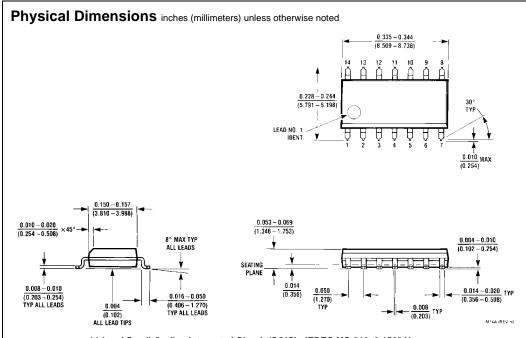
	<b>.</b> .	V	T <sub>A</sub> =	25°C	Unite	Conditions	
Symbol	Parameter	V <sub>CC</sub>	Тур	Limits	Units		
V <sub>OLP</sub> (Note 6)	Quiet Output Maximum Dynamic V <sub>OL</sub>	5.0	0.4	0.8	V	C <sub>L</sub> = 50 pF	
V <sub>OLV</sub> (Note 6)	Quiet Output Minimum Dynamic V <sub>OL</sub>	5.0	-0.4	-0.8	V	C <sub>L</sub> = 50 pF	
V <sub>IHD</sub> (Note 6)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	C <sub>L</sub> = 50 pF	
V <sub>ILD</sub> (Note 6)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	C <sub>L</sub> = 50 pF	

Note 6: Parameter guaranteed by design.

## **AC Electrical Characteristics**

Symbol	Parameter	v <sub>cc</sub>	T <sub>A</sub> = 25°C			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions
			Min	Тур	Max	Min	Max	Offics	Conditions
t <sub>PLH</sub>	Propagation Delay	$3.3 \pm 0.3$		8.3	12.8	1.0	15.0	ns	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Time			10.8	16.3	1.0	18.5		C <sub>L</sub> = 50 pF
		$5.0 \pm 0.5$		5.5	8.6	1.0	10.0	ns	C <sub>L</sub> = 15 pF
				7.0	10.6	1.0	12.0		C <sub>L</sub> = 50 pF
C <sub>IN</sub>	Input Capacitance			4	10		10	pF	V <sub>CC</sub> = Open
C <sub>PD</sub>	Power Dissipation Capacitance			21				pF	(Note 7)

Note 7: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC</sub> (Opr) = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/6 (per Gate)

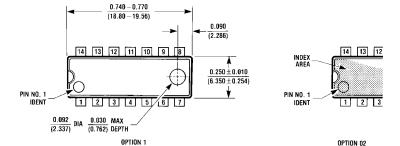


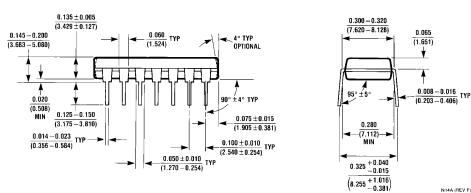
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 10.2±0.1 -A-1.1 TYP 5.01 TYP 5.3±0.1 9.27 TYP 7.8 0.2 C B A ALL LEAD TIPS PIN #1 IDENT. 1.27 TYP - 0.6 TYP LAND PATTERN RECOMMENDATION SEE DETAIL A ALL LEAD TIPS 1.8±0.1 -C-0.15±0.05 0.15-0.25 1.27 TYP DIMENSIONS ARE IN MILLIMETERS NOTES: 0.25 CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. 0.60±0.15 SEATING PLANE M14DRevB1 DETAIL A Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M14D

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 -A-7.72 4.16 6.4 4.4±0.1 -B-3.2 0.2 C B A 0.65 ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT. - SEE DETAIL A ALL LEAD TIPS 1.2 MAX - 0.90 +0.15 - 0.09-0.20 -C-- 0.10±0.05 0.19 - 0.30 **♦** 0.13 **№** A B**⑤** C**⑤** -12.00° TOP & BOTTOM R0.09 MIN-GAGE PLANE NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. 0.25 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. -1.00-R0.09 MIN MTC14RevC3 DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)





14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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