FEATURES

- VDD range: 2.7V to 5.5V
- Low Offset Voltage: 0.5mV (Typical)
- Low Drift: 0.65μV/° C(Typical)
- Low Noise
- Quiescent Current: 50μA
- Rail to Rail Input/Output
- MicroSize Packages: SOIC and TSSOP
- -40° C to 125° C Operation

APPLICATIONS

- Transducers
- Temperature Measurement
- Electronic Scales
- Medical instrumentation
- Handheld Test Equipment

GENERAL DESCRIPTION

The MT0324 are quad CMOS operational amplifiers that uses the proprietary auto-calibration technique to simultaneously provide very low offset voltage, near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 200mV beyond the rails, and rail-to-rail output that swings within 50mV of the rails, single or dual supplies as low as 2.7V(±1.35V) and up to 5.5V(±2.75V) can be used. These devices are optimized for low voltage, single supply operation.

The MT0324 offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity. The MT0324 is available in the 14-pin SOIC package, and specified for operation from -40° C to 125° C.

SIMPLIFIED SCHEMATIC

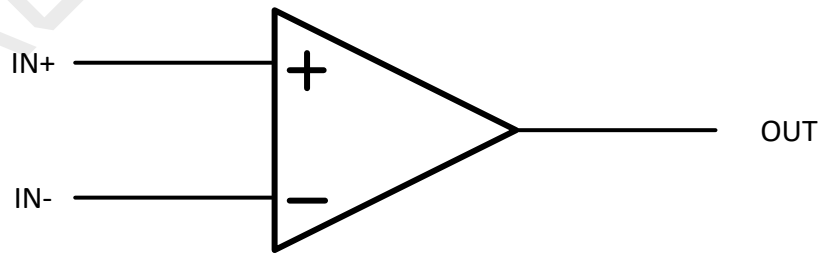


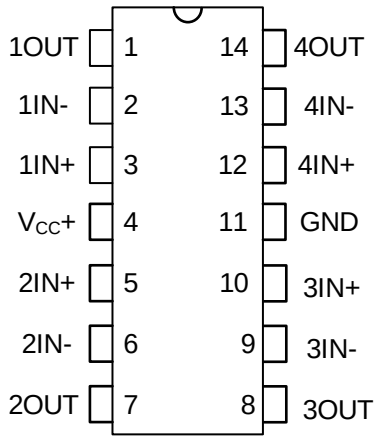
Figure 1. Simplified Schematic

ABSOLUTE MAXIMUM RATINGS (Note 1)

Thermal Resistance θ_{JC}.....130°C/W
Supply Voltage.....2.7 to 5.5V
Signal Input Terminals Voltage...-0.1 to (V+)+0.1V
Operating Junction Temperature.....125°C
Operating Temperature Range.....-40°C to 125°C
Storage Temperature .....-65°C to 150°C

PACKAGE/ORDER INFORMATION

TOP VIEW



Order Part Number	Package	Top Marking
MT0324	14-Pin SOIC 14-Pin TSSOP	MT0324CJ MT0324CG

DEVICE INFORMATION

Order Part Number	Top Marking	Package
MT0324	MT0324CJ	SOIC-14
	MT0324CG	TSSOP-14

PIN DESCRIPTION

Pin Name	Pin Number	Description
1OUT	1	Output 1
1IN-	2	Inverting input 1
1IN+	3	Noninverting input 1
V_{CC}+	4	Positive (highest) power supply
2IN+	5	Noninverting input 2

2IN-	6	Inverting input 2
2OUT	7	Output 2
3OUT	8	Output 3
3IN-	9	Inverting input 3
3IN+	10	Noninverting input 3
GND	11	Negative(lowest) power supply
4IN+	12	Noninverting input 4
4IN-	13	Inverting input 4
4OUT	14	Output 4

ELECTRICAL CHARACTERISTICS (Note 3)

(At T_A = 25°C, R_L=10kΩ connected to V_S/2 , and V_{OUT}=V_S/2,unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_S=±2.5V		0.5		mV
Input Offset Voltage Drift	T_A = -40°C to 125°C		0.65		μV/°C
Power Supply Rejection Ratio	V_S =2.7V to 5.5V T_A = -40°C to 125°C		88		dB
Input Bias Current	T_A = 25°C		1.7		pA
Input Offset Current			2.7		pA
Common-mode Voltage Range		(V-)-0.1		(V+)+0.1	V
Common-mode Rejection Ratio	(V-)-0.1<V_{CM}<(V+)+0.1 T_A = -40°C to 125°C		95		dB
Open Loop Voltage Gain	(V-)+100mV<V_O<(V+)-100mV, R_L=10kΩ T_A = -40°C to 125°C		101		dB
Gain-bandwidth product	C_L=100pF		1.7		MHz
Slew Rate	G=+1		1.3		V/μs
Specified Voltage Range		2.7		5.5	V
Quiescent Current	I_O=0A		50		μA
Operating Temperature Range		-40		125	°C
Storage Temperature Range		-65		150	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D)$ x (170°C/W).

Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

(At T_A = 25°C, V_S=5V, C_L=0pF, unless otherwise noted.)

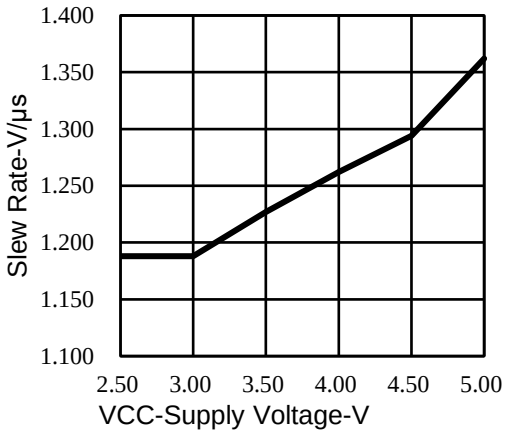


Figure 2. Slew Rate vs Supply Voltage

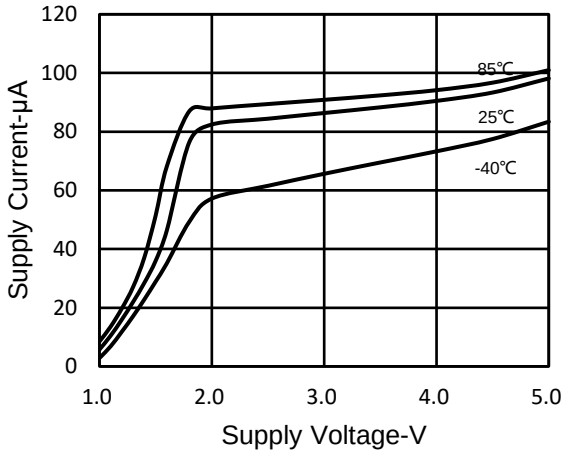


Figure 3. Supply Current vs Supply Voltage

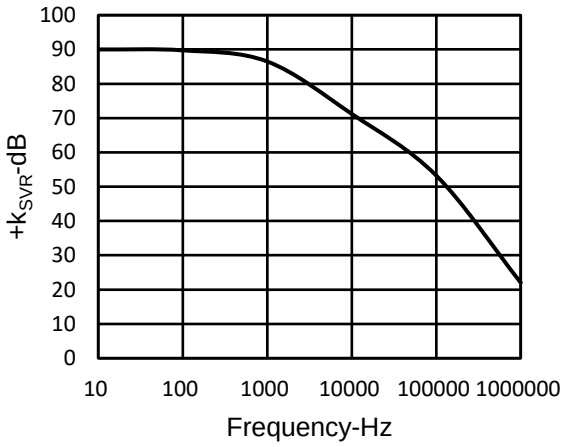


Figure 4. $+k_{SVR}$ vs Frequency

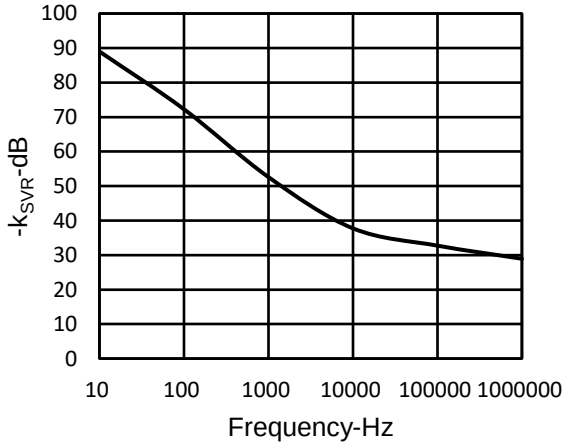


Figure 5. $-k_{SVR}$ vs Frequency

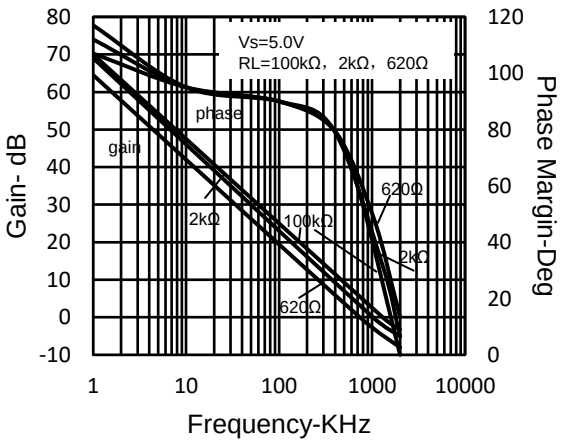


Figure 6. Frequency Response vs Resistive Load

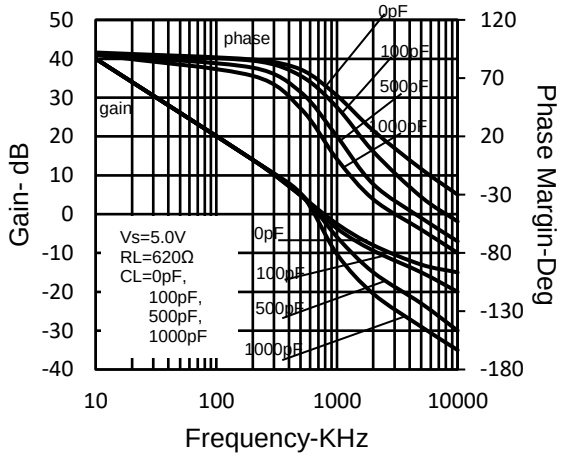


Figure 7. Frequency Response vs Capacitive Load

TYPICAL PERFORMANCE CHARACTERISTICS

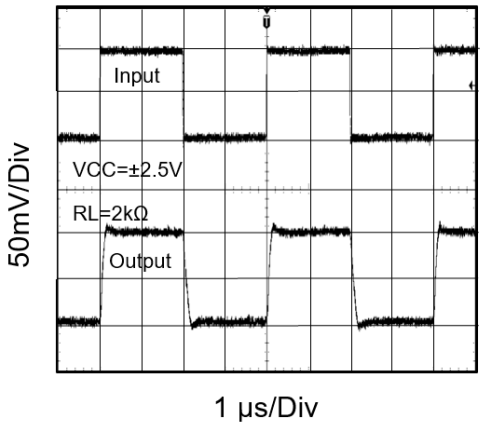


Figure 8. Noninverting Small-Signal Pulse Response

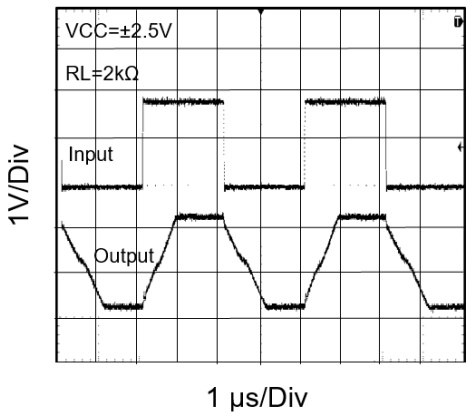


Figure 9. Noninverting Large-Signal Pulse Response

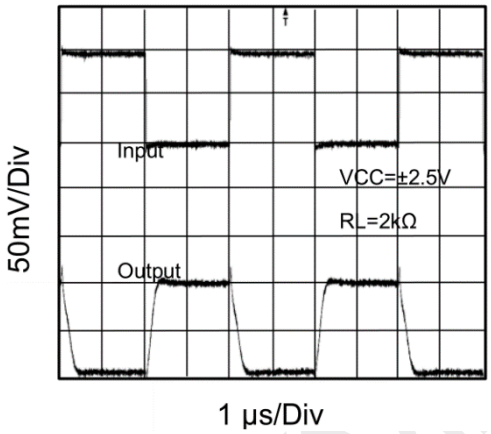


Figure 10. Inverting Small-Signal Pulse Response

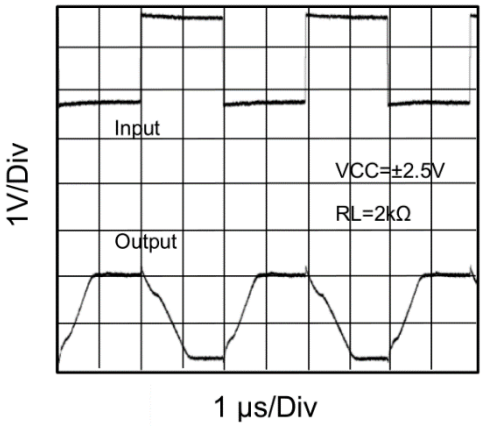


Figure 11. Inverting Large-Signal Pulse Response

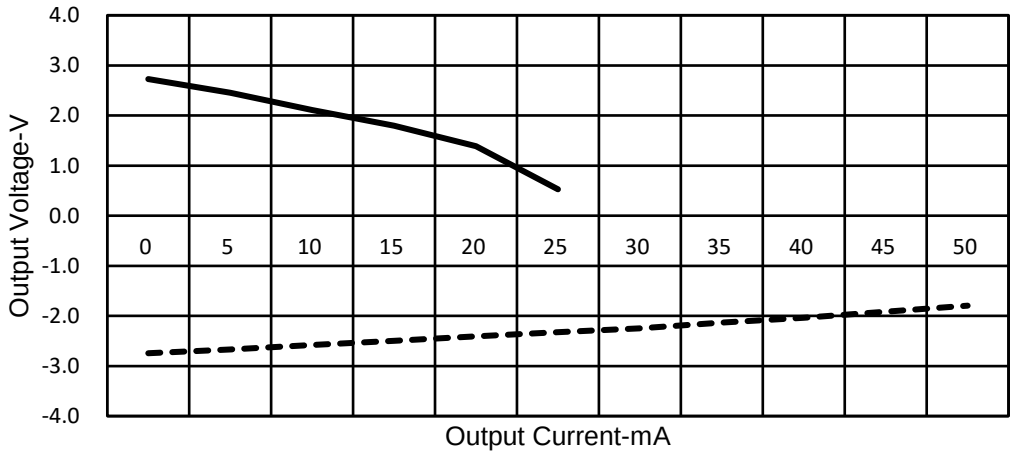


Figure 12. Output Voltage vs Output Current

FUNCTIONAL DESCRIPTION

Operating Voltage

The MT0324 devices are fully specified and ensured for operation from 2.7 V to 5.5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics graphs.

Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The MT0324 devices have a 1.7-MHz unity-gain bandwidth.

Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The MT0324 devices have a 1.32-V/μs slew rate. The MT0324 is characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ.

Device Functional Modes

The MT0324 device has a single functional mode. The device is powered on as long as the power supply voltage is between 2.7V(±1.35V) and 5.5V(±2.75V).

APPLICATIONS INFORMATION

The MT0324 is a unity-gain stable, precision operational amplifier with very low offset voltage drift; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1μF capacitors are adequate.

Typical Application

Figure 13 shows a simple circuit to convert a single-ended input into differential output. The MT0324 could be used to build this circuit. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 0.5 to 2 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$.

Detailed Design Procedure

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because MT0324 has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

Because the transfer function of $V_{OUT–}$ is heavily reliant on resistors (R1, R2, R3, and R4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

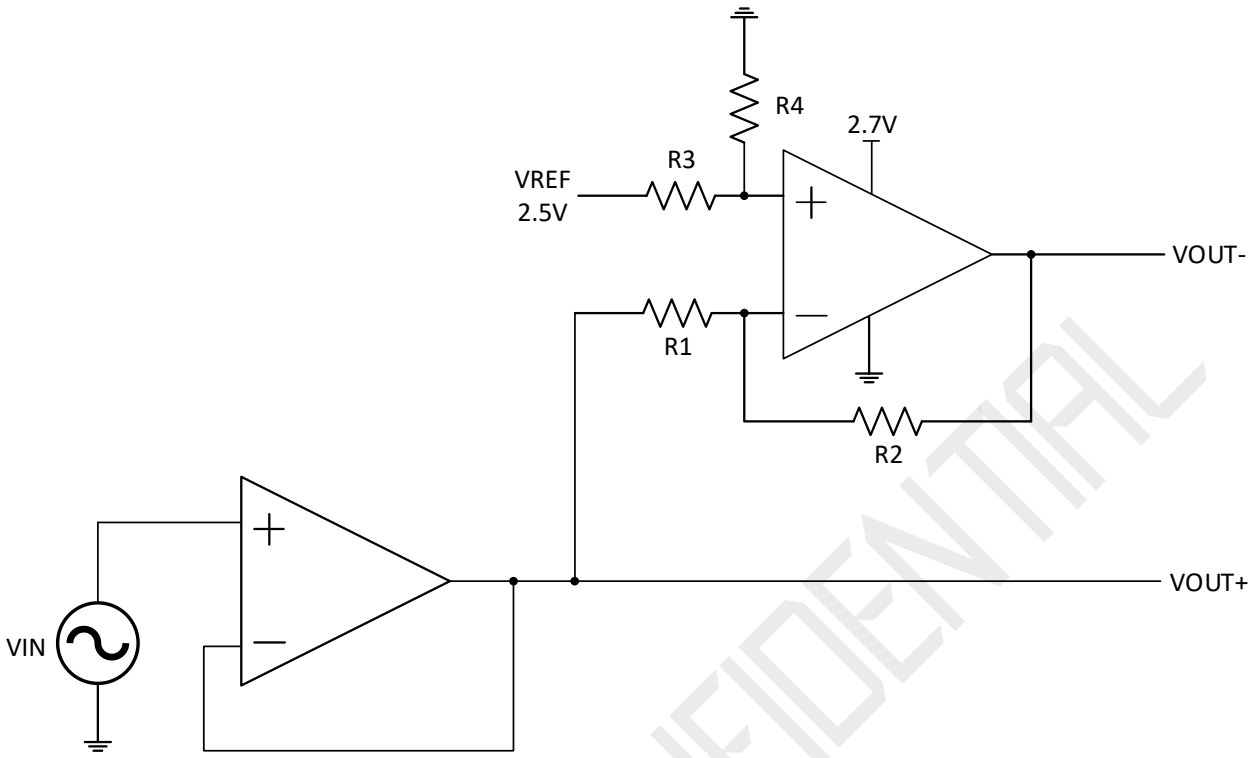
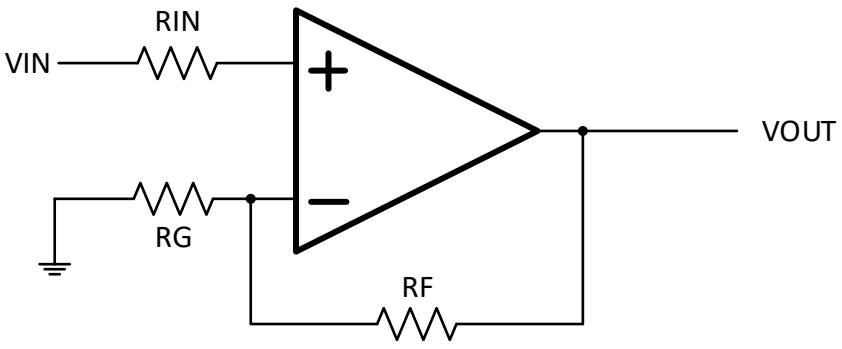


Figure 13. Schematic for Single-Ended Input to Differential Output Conversion

LAYOUT

Use good PCB layout practices for best operational performance of the device, including:

- Keep the length of input traces as short as possible.
- Run the input traces as far away from the supply lines as possible to reduce parasitic coupling.
- Place components close to device and to each other to reduce parasitic capacitance and parasitic errors.
- Use low-ESR, ceramic bypass capacitors to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Grounding for analog and digital portions of circuitry separately to suppresse the noise.



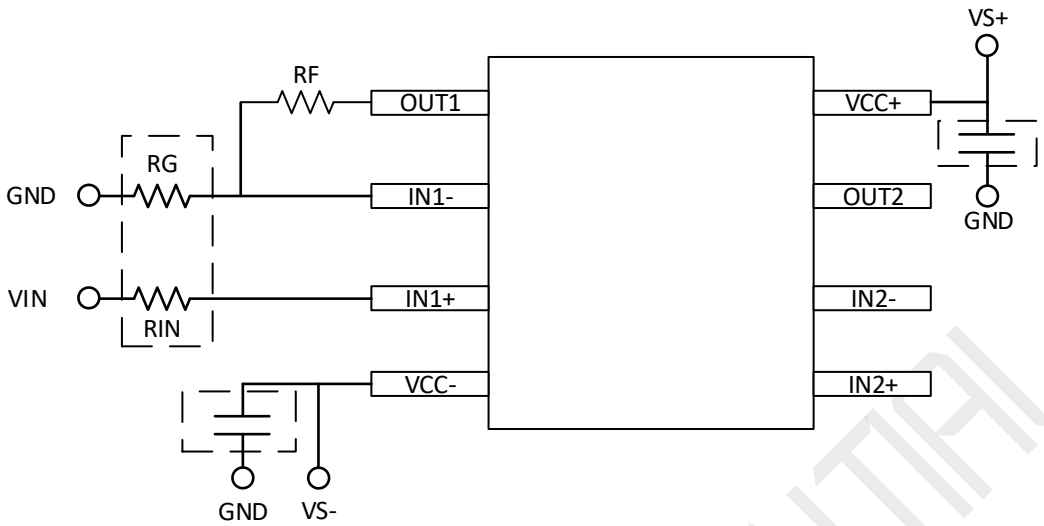
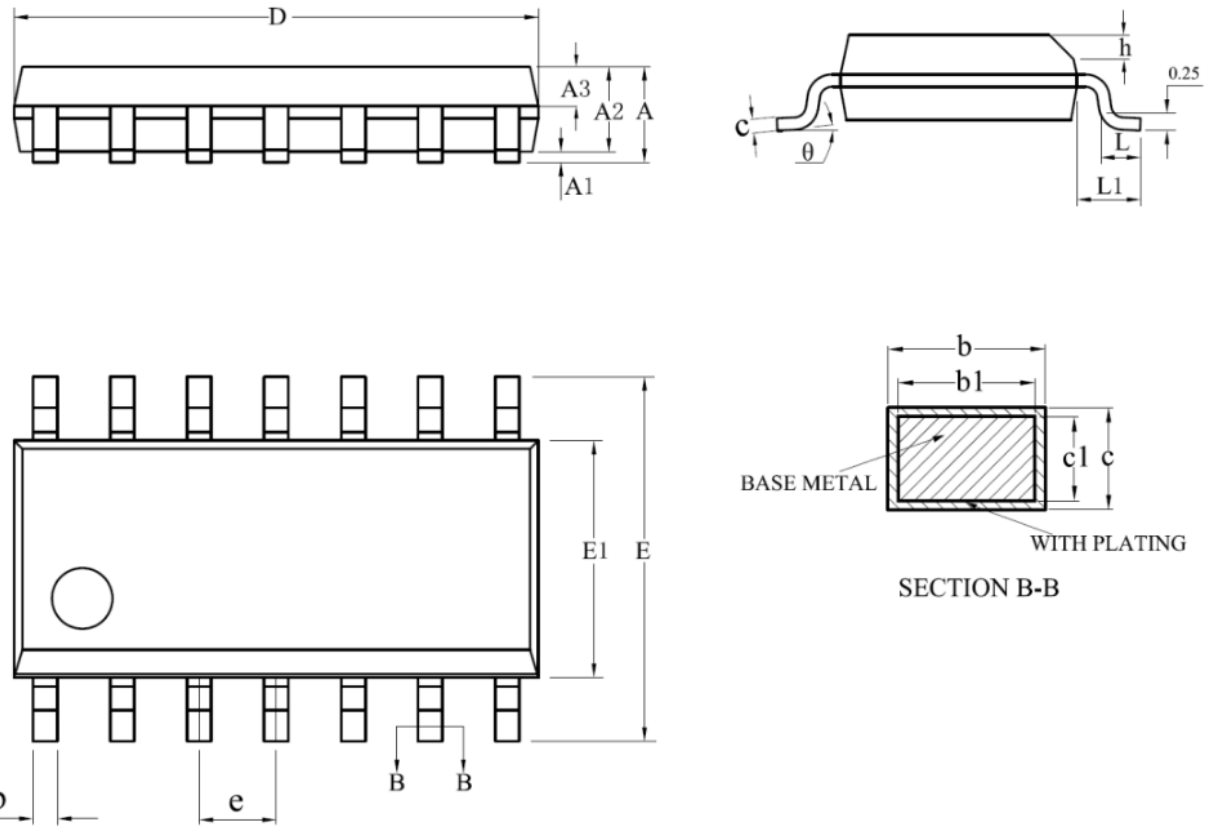


Figure 14. Operational Amplifier Schematic and Board Layout for Noninverting Configuration

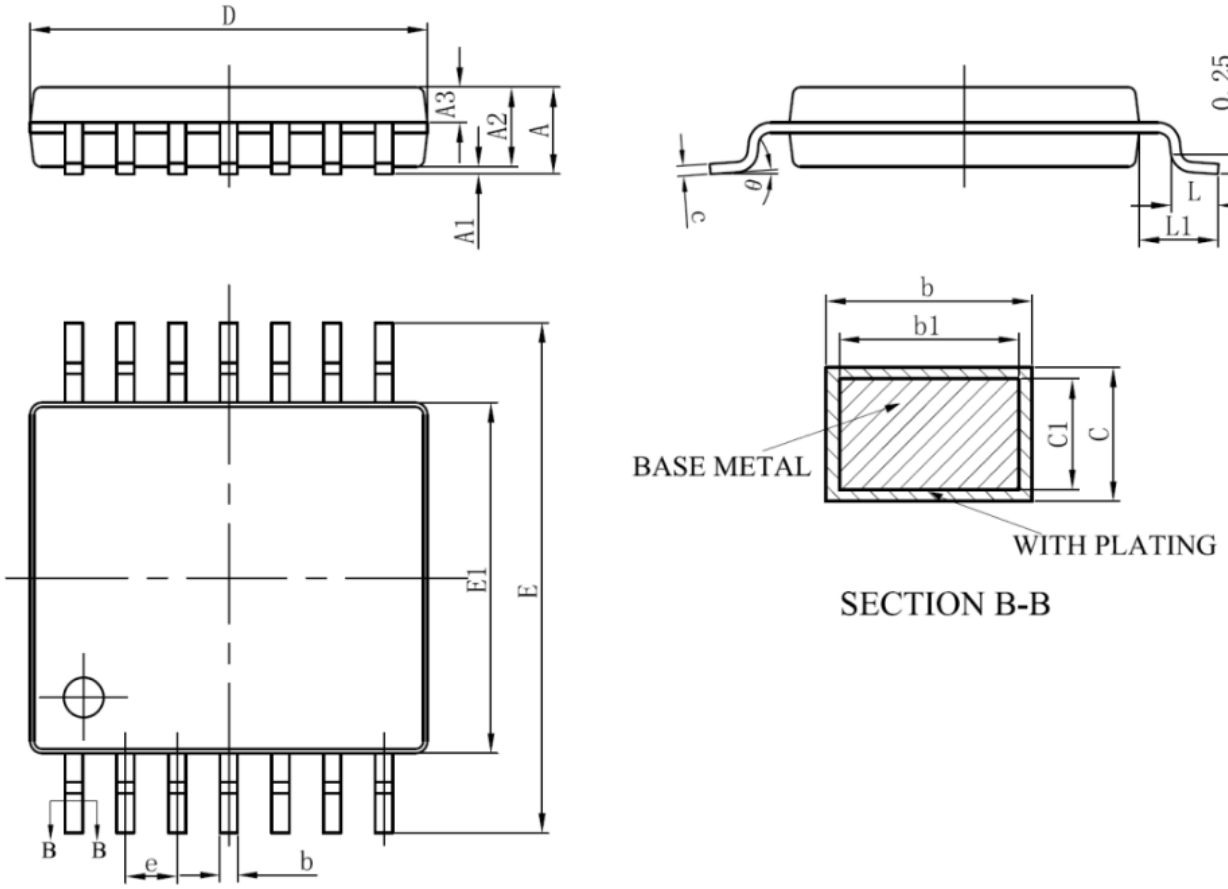
PACKAGE DESCRIPTION

SOIC-14



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.05	-	0.23
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

TSSOP-14



SYMBOL	millimeter		
	min	nom	max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	-	8°

NOTE:
1.All linear dimensions are in inches (millimeters).
2.This drawing is subject to change without notice.
3.Body length does not include mold flash,protrusions,or gate burrs.mold flash,protrusions,or gate burrs shall not exceed 0.006 (0.15) each side.
4.Body width does not include interlead flash.interlead flash shall not exceed 0.017 (0.43)each side.

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