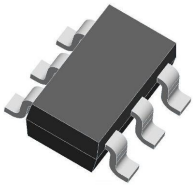
WS74199

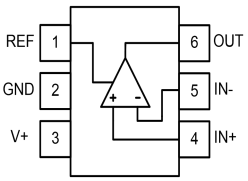
26-V, Bidirectional, Zero-Drift, Low- or High-Side,Voltage-Output,Current-Shunt Monitor

Http://www.willsemi.com

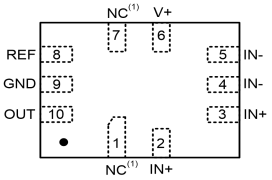


SOT363

QFN1418-10L



SOT363



QFN1418-10L

Pin configuration (Top view)

(1) NC denotes no internal connection. These pins can be left floating or connected to any voltage between GND and V+.

Descriptions

The WS74199 series of voltage-output, current-shunt monitors (also called current-sense amplifiers) are commonly used for over-current protection, precision-current measurement for system optimization, or in closed-loop feedback circuits. These devices operate from a single 2.7V to 26V power supply, drawing a maximum of 160 μA of supply current.

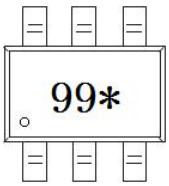
The WS74199 is available with MSL 3 Level in SOT363 and QFN1418-10L package. Standard products are Pb-Free and halogen-Free.

Applications

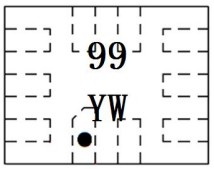
- Notebook Computers
- Qi-Compliant Wireless Charging Transmitters
- Telecom Equipment
- Power Management

Features

- Common Mode Range : -0.3 V ~ 26 V
- Offset Voltage (Enables Shunt Drops of 10-mV Full-Scale) : ±10 μV (type)
- Gain Error (Maximum Over Temperature) : ±1%
- 0.5-μV/°C Offset Drift (Maximum)
- 10-ppm/°C Gain Drift (Maximum)
- Choice of Gains:
  - -WS74199x1: 50 V/V
  - -WS74199x2: 100 V/V
  - -WS74199x3: 200 V/V
- Quiescent Current: 100 μA (Typical)
- Packages: 6-Pin SOT-363, 10-Pin QFN1418-10L



SOT363



QFN1418-10L

Marking

99 = Device code
*** = Year & week code**
Y = Year code
W = Week code

Order Information

Device	Package	Shipping
WS74199B-6/TR	SOT363	4000/Reel &Tape
WS74199Q-10/TR	QFN1418-10L	4000/Reel &Tape

Pin Descriptions (WS74199B-6/TR)

Pin Number	Symbol	Descriptions
1	REF	Reference voltage, 0 V to V+
2	GND	Ground
3	V+	Power supply, 2.7 V to 26 V
4	IN+	Connect to supply side of shunt resistor
5	IN-	Connect to load side of shunt resistor
6	OUT	Output voltage

Pin Descriptions (WS74199Q-10/TR)

Pin Number	Symbol	Descriptions
1, 7	NC	No internal connection
2, 3	IN+	Connect to supply side of shunt resistor.
4, 5	IN-	Connect to load side of shunt resistor
6	V+	Power supply, 2.7 V to 26 V
8	REF	Reference voltage, 0 V to V+
9	GND	Ground
10	OUT	Output voltage

Absolute maximum ratings

Parameter		MIN	MAX	UNIT
Supply Voltage			26	V
Analog inputs, V_{IN+}, V_{IN-}(2)	Differential (V_{IN+}) - (V_{IN-})	-12	12	V
	Common-mode(3)	GND - 0.3	26	
REF input		GND - 0.3	(V+) + 0.3	V
Output(3)		GND - 0.3	(V) + 0.3	V
Input current Into all pins(3)			5	mA
Operating temperature		-40	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		-65	150	°C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. V_{IN+} and V_{IN-} are the voltages at the IN+ and IN- pins, respectively.
3. Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5mA.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum level	Unit
HBM	Human Body Model ESD	JEDEC-EIA/JESD22-A114A	±1500	V
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	±250	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	±2000	V

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
V_{CM} Common-mode input voltage	-0.1	12	27	V
V_S Operating supply voltage (applied to V+)	2.7	5	27	V
T_A Operating free-air temperature	-40		125	°C

Thermal Information

THERMAL METRIC(1)	WS74199		UNIT
	SOT-363	QFN1418-10L	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	227.3	107.3	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	79.5	56.5	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	72.1	18.7	°C/W
ψ_{JT} Junction-to-top characterization parameter	3.6	1.1	°C/W
ψ_{JB} Junction-to-board characterization parameter	70.4	18.7	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Electronics Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, V_{SENSE} = V_{IN+} − V_{IN-}, and V_{REF} = V_S / 2, unless otherwise noted.

Parameter	Test Conditions	Min	Typ	Max	Unit
Input					
V_{CM} Common-mode input range	T_A = - 40°C to 125°C	-0.2		26	V
CMR Common-mode rejection	V_{IN+} = 0 V to 26 V, V_{SENSE} = 0 mV, T_A = - 40°C to 125°C	78	110		dB
V_{OS} Offset voltage, RTI(1)	V_{SENSE} = 0 mV		±10		μV
dV_{OS}/dT V_{OS} vs temperature	T_A = - 40°C to 125°C		0.1		μV/°C
PSR Power supply rejection	V_S = 2.7 V to 26 V, V_{IN+} = 26 V, V_{SENSE} = 0 mV	±72	±1		μV/V
I_B Input bias current	V_{IN+} = 26 V V_{SENSE} = 0 mV	27	40	55	μA
I_{OS} Input offset current	V_{SENSE} = 0 mV		±0.5		μA
Output					
G Gain	WS74199x1		50		V/V
	WS74199x2		100		
	WS74199x3		200		
Gain error	V_{ersion} A and B, V_{SENSE} = −5 mV to 5 mV, T_A = - 40°C to 125°C		±0.03%	±1%	
Gain error vs temperature	T_A = - 40°C to 125°C		10		ppm/°C
Maximum capacitive load	No sustained oscillation		1		nF
Voltage Output(2)					
Swing to V+ power-supply rail	R_L = 10 kΩ to GND,		17	25	mV
Swing to GND	R_L = 10 kΩ to V+,		17	25	mV
Frequency Response					
GBW Bandwidth	C_{LOAD} = 10 pF, WS74199x1		95		kHz
SR Slew rate			0.5		V/μs
Noise, RTI (1)					
Voltage noise density			35		nV/√Hz
Power Supply					
V_S Operating voltage range	T_A = - 40°C to 125°C	2.7		26	V
I_Q Quiescent current	V_{SENSE} = 0 mV		100	160	μA

Electronics Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, V_{SENSE} = V_{IN+} − V_{IN-}, and V_{REF} = V_S / 2, unless otherwise noted.

Temperature Range				
Specified range		-40	125	°C
Operating range		-40	125	°C
θ_{JA} Thermal resistance	SOT-363	250		°C/W
	QFN1418-10L	80		

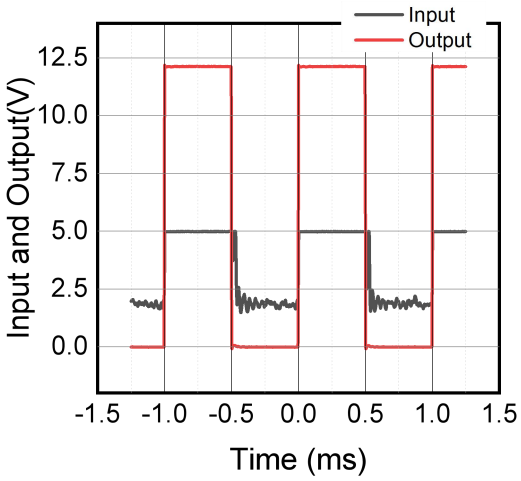
Note:

1. RTI = Referred-to-input.
2. See Typical Characteristic curve, Output Voltage Swing vs Output Current.R1

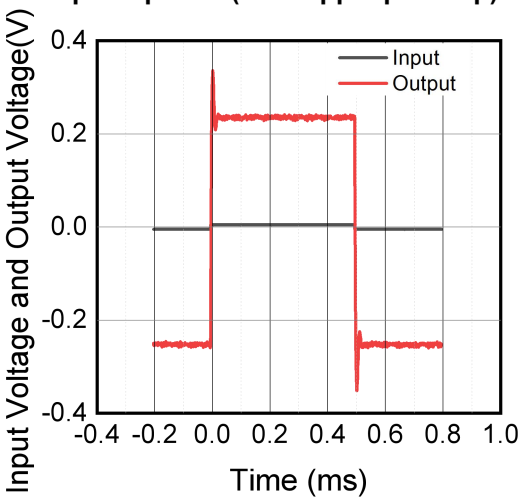
Typical Characteristics

T_A = 25°C, V_S = 5V, V_{IN+} = 12V, and V_{REF} = V_S / 2 (unless otherwise noted)

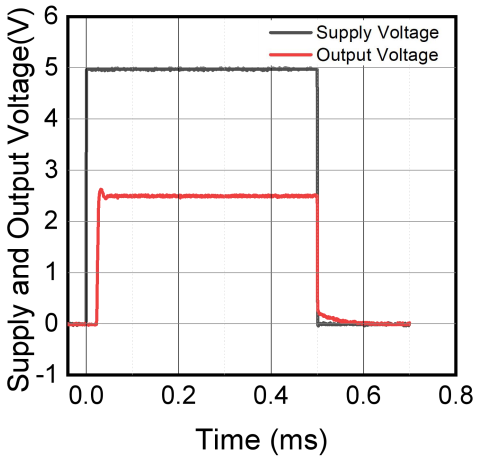
Noninverting Differential Input Overload



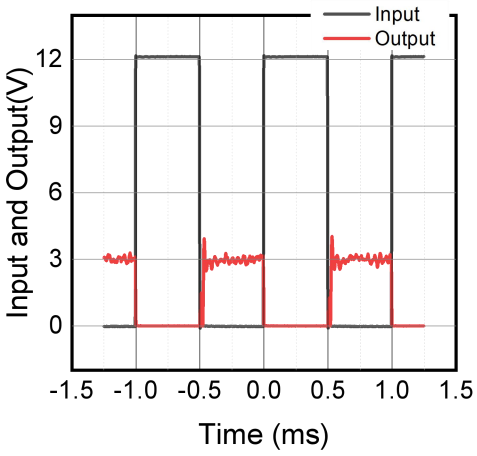
Step Response (10-mVpp Input Step)



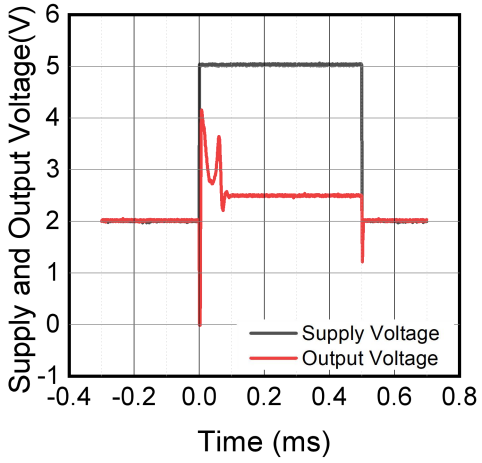
Start-Up Response



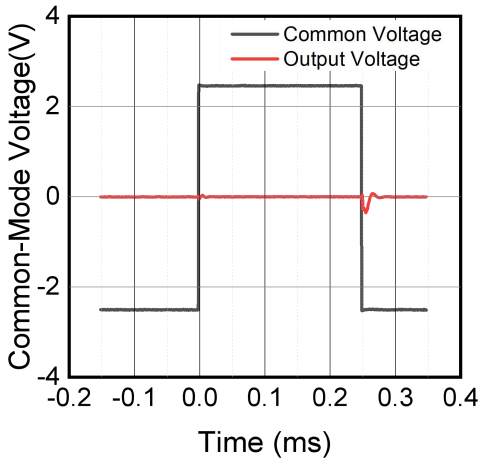
Inverting Differential Input Overload



Brownout Recovery



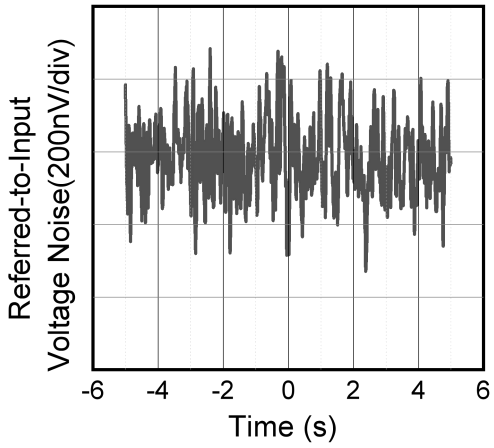
Common-Mode Voltage Transient Response



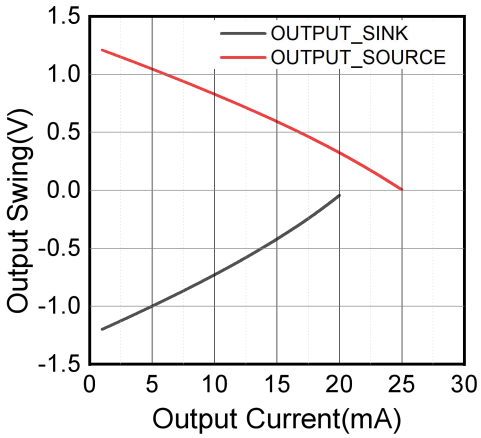
Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, V_{IN+} = 12V, and V_{REF} = V_S / 2 (unless otherwise noted)

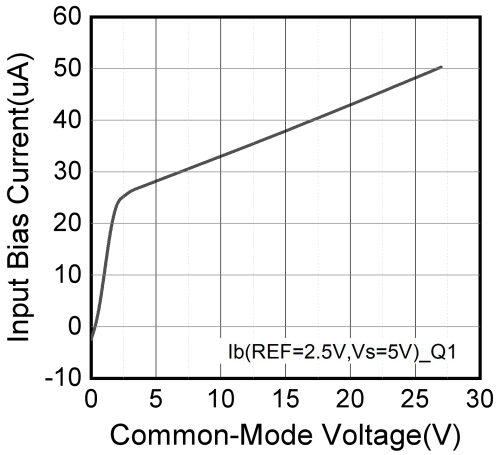
Referred-to-Input Voltage Noise



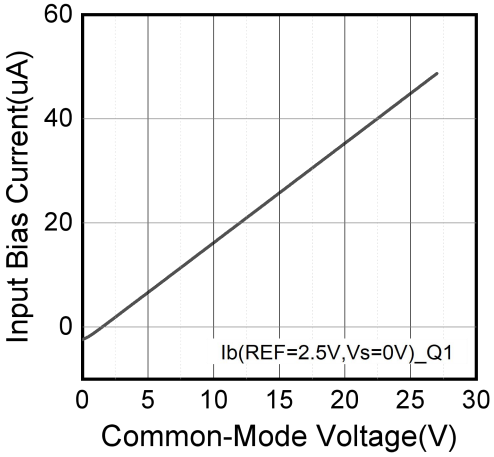
Output Voltage Swing vs Output Current(Vs=2.7V)



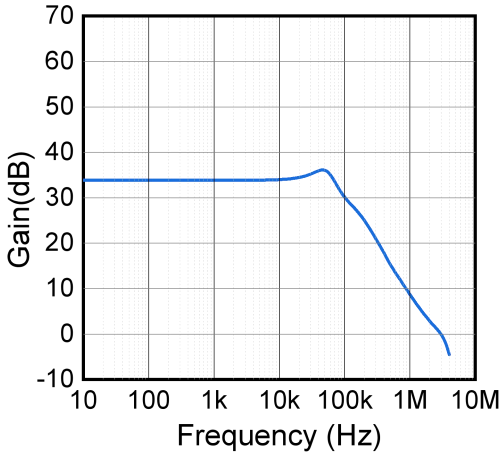
Input Bias Current vs Common-Mode Voltage(With Supply Voltage=5V)



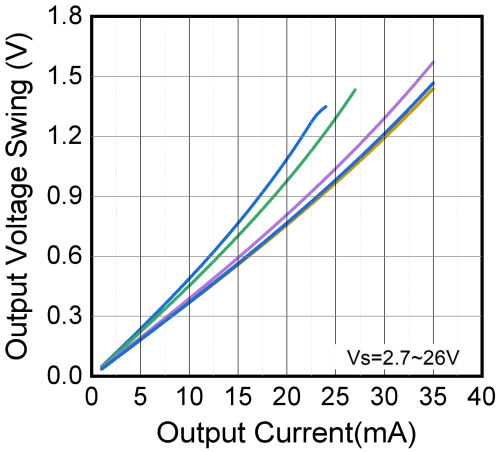
Input Bias Current vs Common-Mode Voltage(With Supply Voltage=0V)



Gain vs Frequency



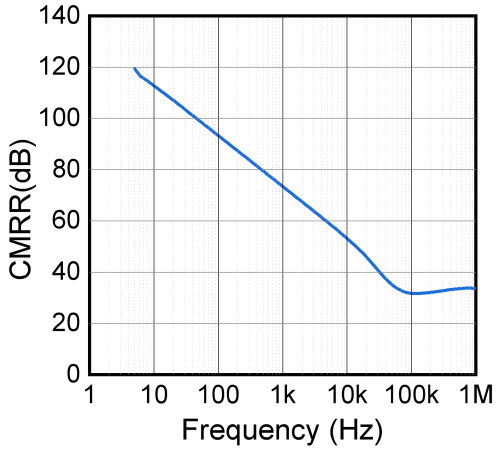
Output Voltage Swing vs Output Current(Vs=2.7~26V)



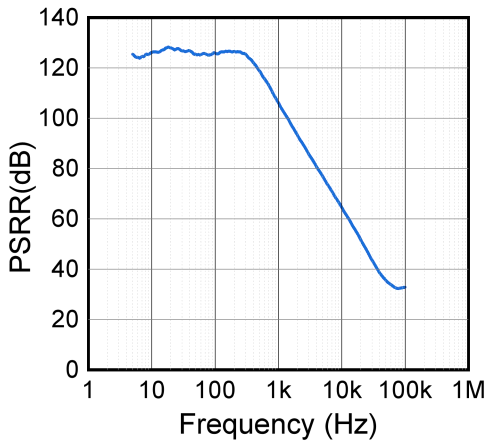
Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, V_{IN+} = 12V, and V_{REF} = V_S / 2 (unless otherwise noted)

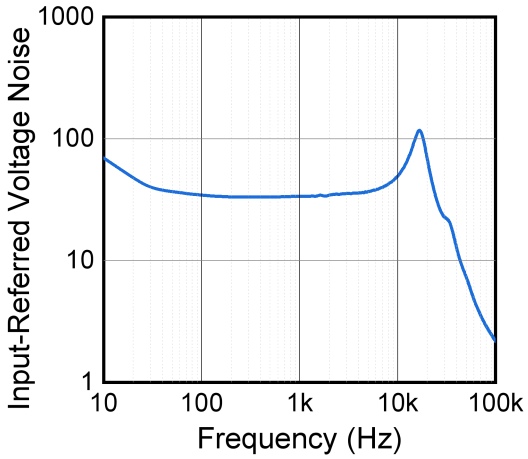
Common-Mode Rejection Ratio vs Frequency



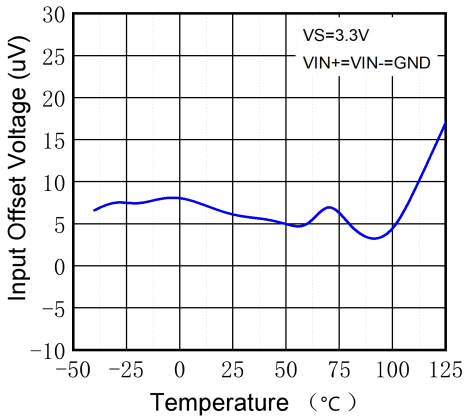
Power-Supply Rejection Ratio vs Frequency



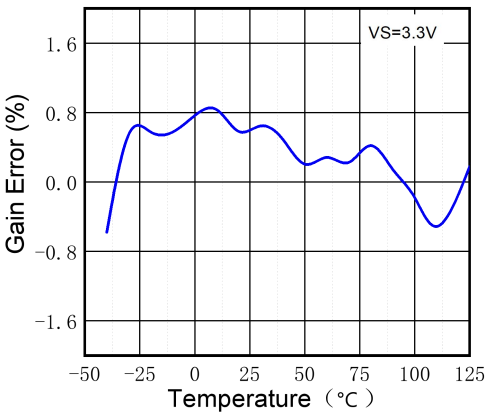
Input-Referred Voltage Noise vs Frequency



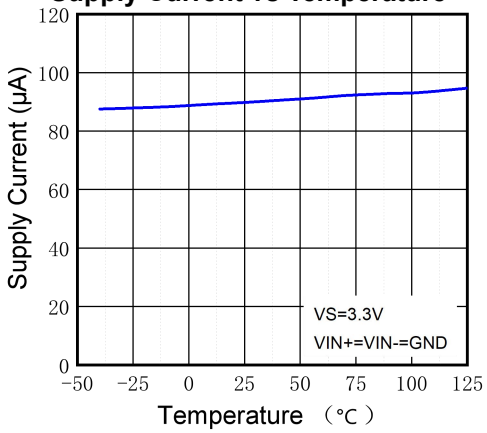
Input Offset Voltage vs Temperature



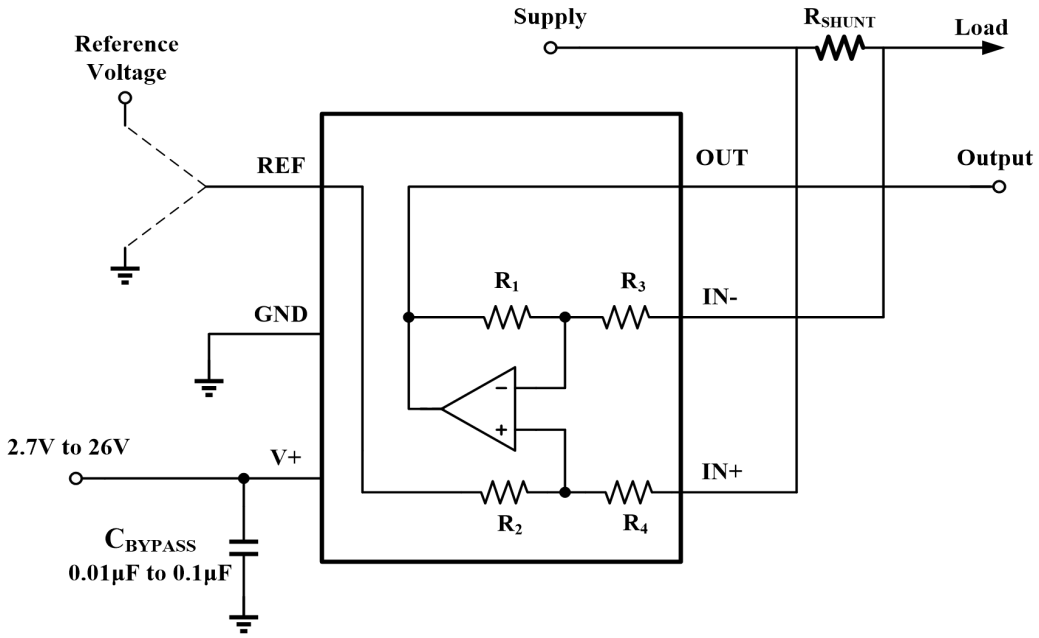
Gain Error vs Temperature



Supply Current vs Temperature



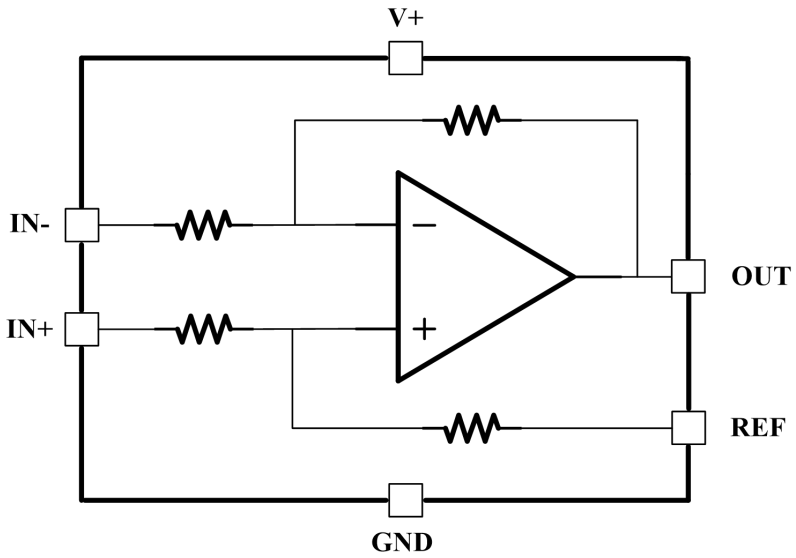
Simplified Schematic



The WS74199 is a 26-V common mode, zero-drift topology, current-sensing amplifier that can be used in both low-side and high-side configurations. The device is a specially-designed, current-sensing amplifier that is able to accurately measure voltages developed across a current-sensing resistor on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 150 µV with a maximum temperature contribution of 0.5 µV/℃ over the full temperature range of －40℃ to +125℃.

Functional Block Diagram



Basic Connections

Figure 1 shows the basic connections for the WS74199. The input pins, IN+ and IN–, must be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

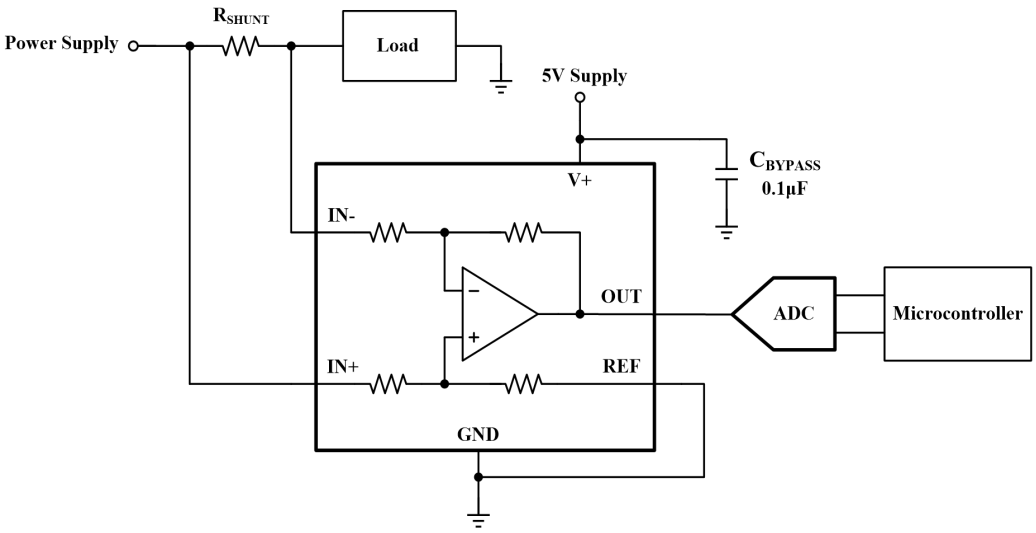


Figure 1. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

On the RSW package, two pins are provided for each input. These pins must be tied together (that is, tie IN+ to IN+ and tie IN– to IN–).

Selecting R_s

The zero-drift offset performance of the WS74199 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current shunt monitors typically require a full-scale range of 100 mV.

The WS74199 series gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, there are applications that must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower gain of 50 or 100 to accommodate larger shunt drops on the upper end of the scale. For instance, an WS74199A1 operating on a 3.3-V supply can easily handle a full-scale shunt drop of 60 mV, with only 150 µV of offset.

Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. Figure 2 shows a filter placed at the inputs pins.

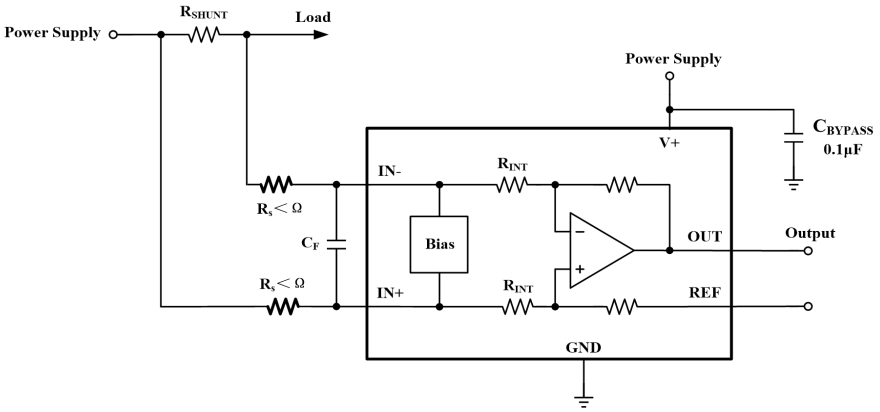


Figure 2. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be kept to 10 Ω (or less if possible) to reduce any affect to accuracy. The internal bias network shown in Figure 2 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R3 and R4 (or R_{INT} as shown in Figure 2). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is seen at the device input pins is given in Equation 1:

$$Gain\ \ Error\ \ Factor = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (1)$$

where:

- R_{INT} is the internal input resistor (R_3 and R_4).
- R_S is the external series resistance.

Device Functional Modes

With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as listed in Table 1. Each individual device gain error factor is listed in Table 2.

Table 1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
WS74199x1	50	20
WS74199x2	100	10
WS74199x3	200	5

Table 2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
WS74199x1	$\frac{20{,}000}{(17 \times R_S) + 20{,}000}$
WS74199x2	$\frac{10{,}000}{(9 \times R_S) + (10{,}000)}$
WS74199x3	$\frac{1000}{R_S + 1000}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on Equation 2:

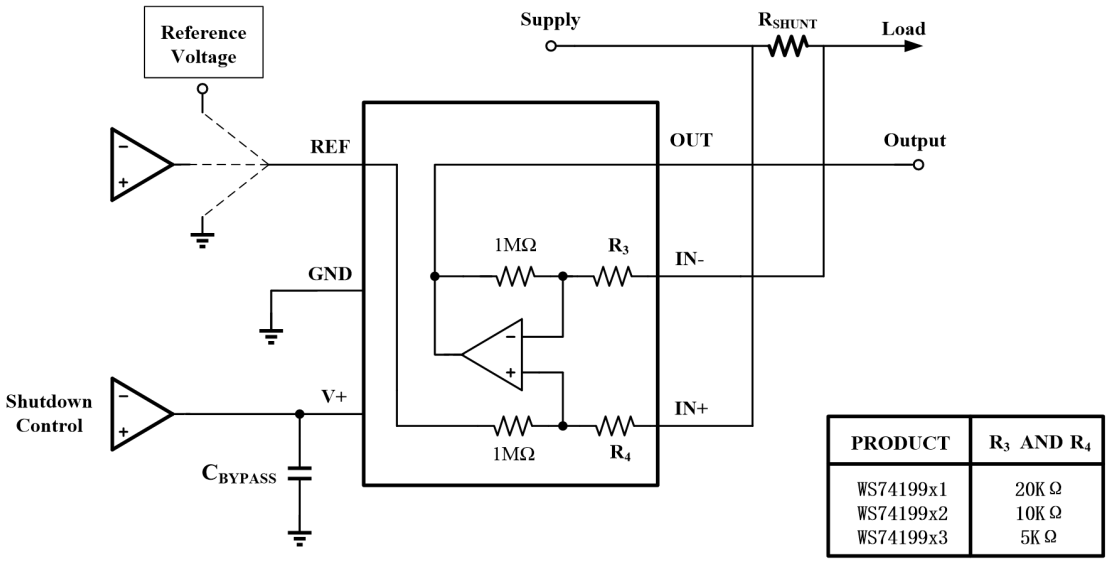
$$Gain\ Error\ (\%) = 100 - (100 \times Gain\ Error\ Factor) \quad (2)$$

For example, using an WS74199x2 and the corresponding gain error equation from Table 2, a series resistance of 10-Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 0.89% solely because of the external 10-Ω series resistors. Using an WS74199x1 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

Shutting Down the WS74199 Series

Although the WS74199 series does not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the WS74199. This gate or switch turns on and turns off the WS74199 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the WS74199 in shutdown mode shown in Figure 3.



NOTE: 1-MΩ paths from shunt inputs to reference and the WS74199 outputs.

Figure 3. Basic Circuit for Shutting Down the WS74199 With a Grounded Reference

There is typically slightly more than 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) from each input of the WS74199 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or operational amplifier is powered when the WS74199 is shut down, the calculation is direct; instead of assuming 1-MΩ to ground, however, assume 1-MΩ to the reference voltage. If the reference or operational amplifier is also shut down, some knowledge of the reference or operational amplifier output impedance under shutdown conditions is required. For instance, if the reference source functions as an open circuit when not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled WS74199 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage impressed across a 1-MΩ resistor.

NOTE

When the device is powered up, there is an additional, nearly constant, and well-matched 25 μA that flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

REF Input Impedance Effects

As with any difference amplifier, the WS74199 series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin must be buffered by an operational amplifier.

In systems where the WS74199 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 4 depicts a method of taking the output from the WS74199 by using the REF pin as a reference.

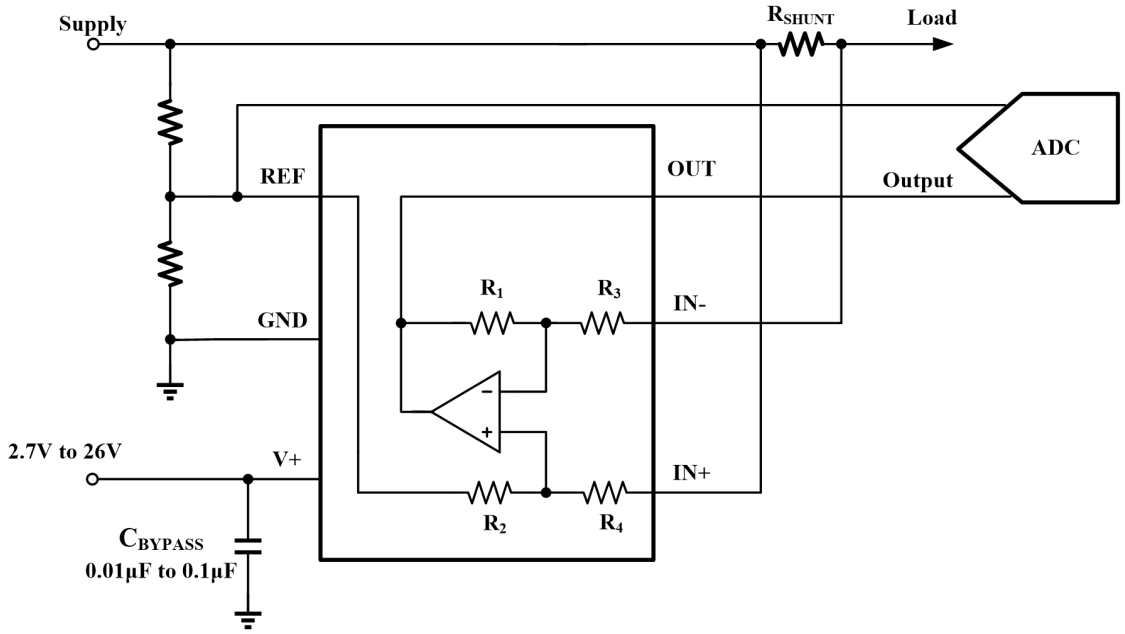


Figure 4. Sensing the WS74199 to Cancel Effects of Impedance on the REF Input

Using the WS74199 With Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the WS74199 series can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diode or Zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors (see Figure 5) as a working impedance for the Zener. Keeping these resistors as small as possible is preferable, most often approximately 10 Ω. Larger values can be used with an effect on gain as discussed in the *Input Filtering* section. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523. See *TIDA-00302 Transient Robustness for Current Shunt Monitor Design Guide*, TIDU473 for more information on transient robustness and current-shunt monitor input protection.

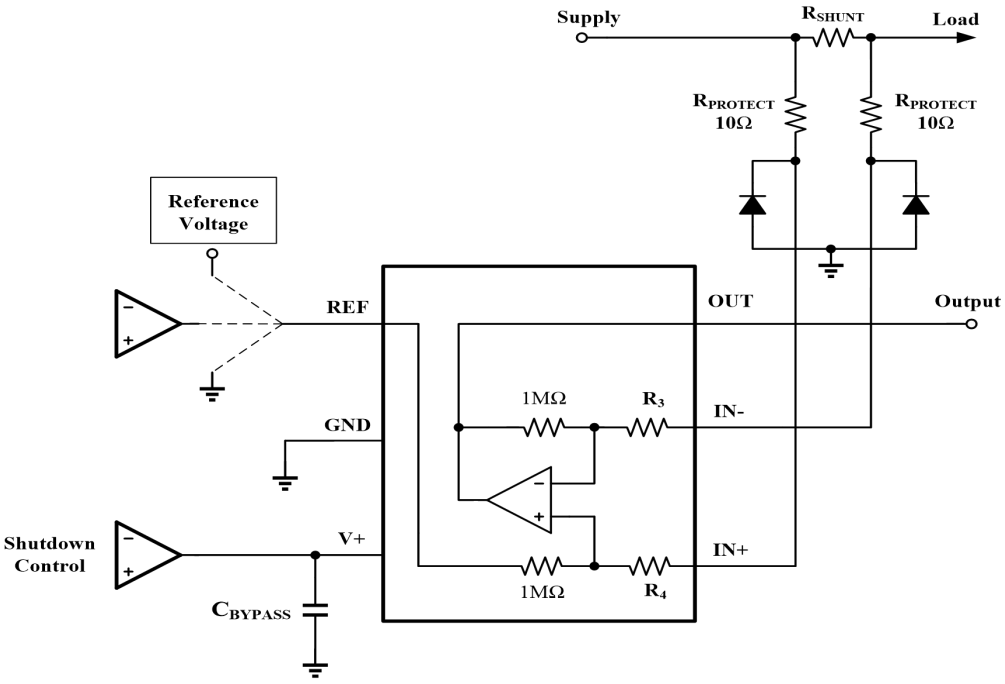


Figure 5. WS74199 Transient Protection Using Dual Zener Diodes

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is shown in Figure 6. In either of these examples, the total board area required by the WS74199 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

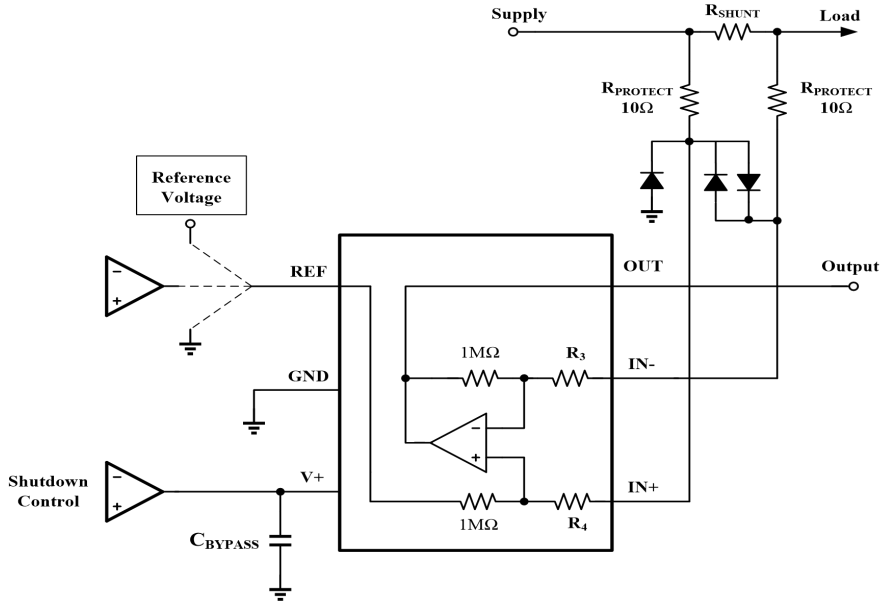


Figure 6. WS74199 Transient Protection Using a Single Transzorb and Input Clamps

Improving Transient Robustness

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins can cause damage to the internal ESD structures on version A devices. This potential damage is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Take care to ensure that external series input resistance does not significantly affect gain error accuracy. For accuracy purposes, keep the resistance under 10Ω if possible. Ferrite beads are recommended for this filter because of their inherently low dc ohmic value. Ferrite beads with less than 10 Ω of resistance at dc and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 μF and 0.1 μF to ensure adequate attenuation in the high-frequency region. This protection scheme is shown in Figure 7. Again, see *TIDA-00302 Transient Robustness for Current Shunt Monitor Design Guide*, TIDU473 for more information on transient robustness and current-shunt monitor input protection.

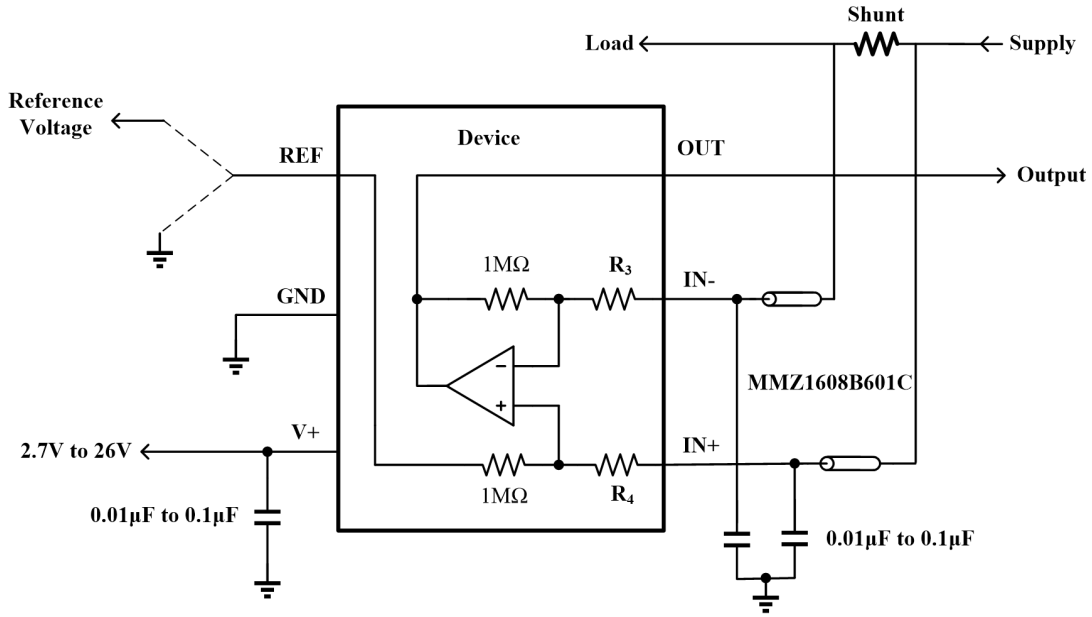


Figure 7. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B and C devices are now available with new ESD structures that are not susceptible to this latching condition. Version B and C devices are incapable of sustaining these damage-causing latched conditions so these devices do not have the same sensitivity to the transients that the version A devices have, thus making the version B and C devices a better fit for these applications.

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The WS74199 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

Design Requirements

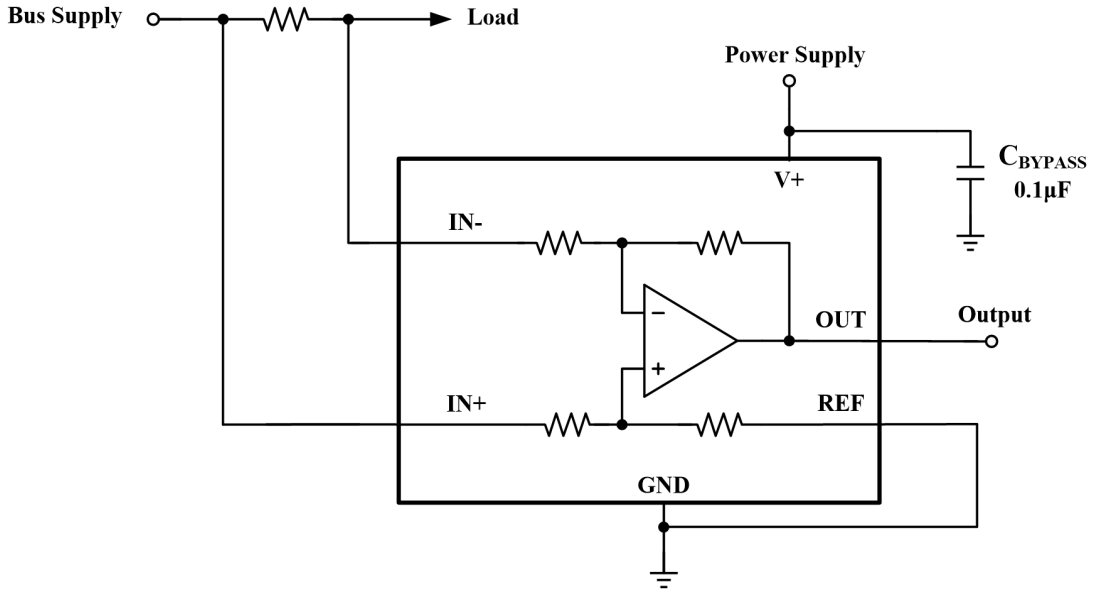


Figure 8. Unidirectional Application Schematic

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 8. When the input signal increases, the output voltage at the OUT pin increases.

Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output saturated low condition with no input signal when the

REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN- pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

Bidirectional Operation

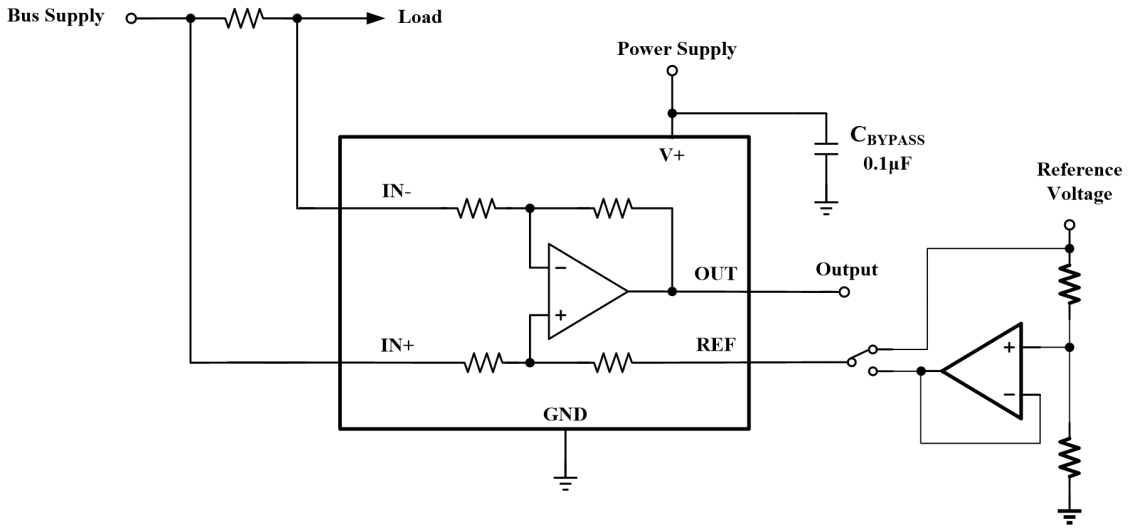


Figure 9. Bidirectional Application Schematic

Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin; see Figure 9. The voltage applied to REF (VREF) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above VREF for positive differential signals (relative to the IN– pin) and responds by decreasing below VREF for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, VREF is typically set at mid-scale for equal signal range in both current directions. In some cases, however, VREF is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

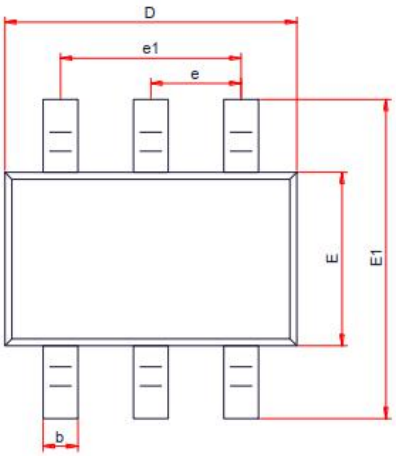
Power Supply Recommendations

The input circuitry of the WS74199 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V.

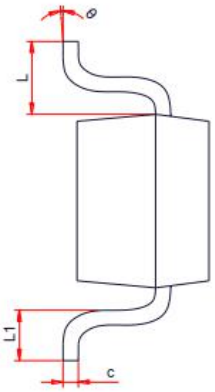
However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Also, the WS74199 can withstand the full input signal range up to 26 V range in the input pins, regardless of whether the device has power applied or not.

PACKAGE OUTLINE DIMENSIONS

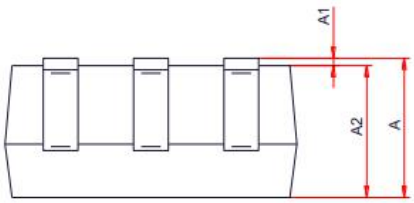
SOT-363



TOP VIEW



SIDE VIEW



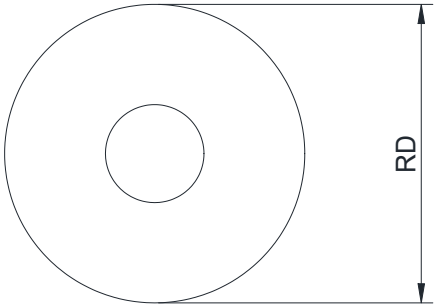
SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.80	0.95	1.10
A1	0.00	-	0.10
A2	0.80	0.90	1.00
b	0.10	-	0.35
c	0.08	-	0.25
D	1.80	2.00	2.20
E	1.15	1.25	1.35
E1	2.00	2.20	2.45
e	0.65 BSC		
e1	1.30 BSC		
L	0.30Ref		
L1	0.15	-	0.46
θ	0°	-	8°

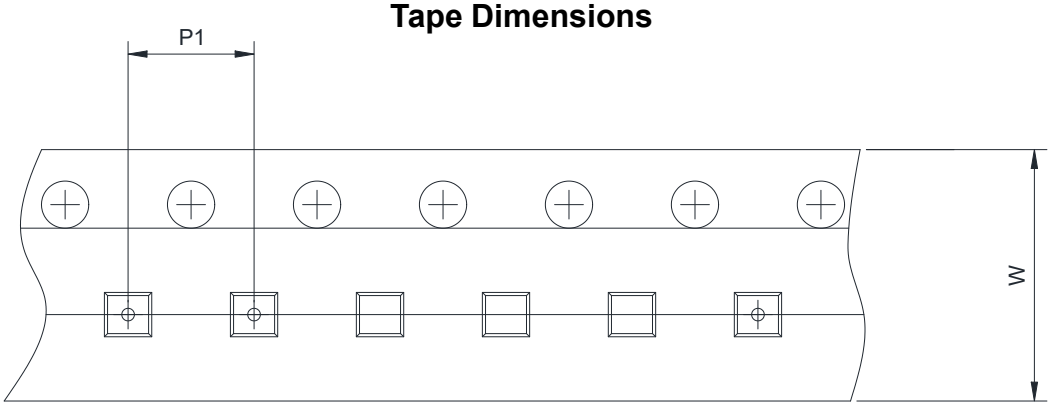
TAPE AND REEL INFORMATION

SOT-363

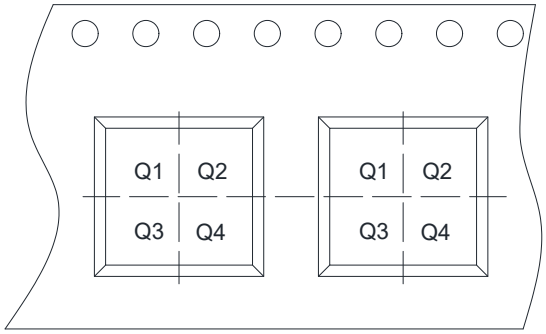
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape

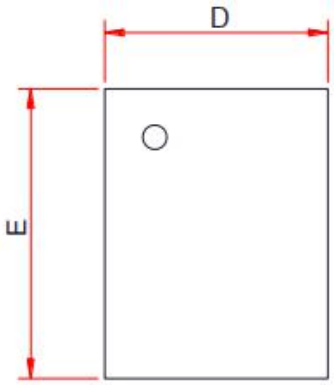


User Direction of Feed

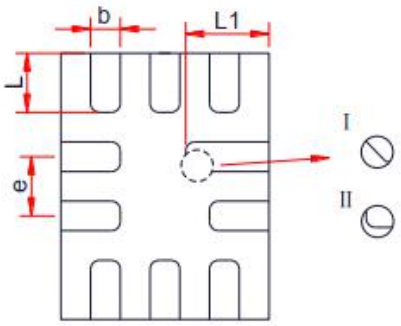
RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☐ Q2	☑ Q3	☐ Q4

PACKAGE OUTLINE DIMENSIONS

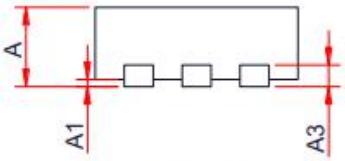
QFN1418-10L



TOP VIEW



BOTTOM VIEW



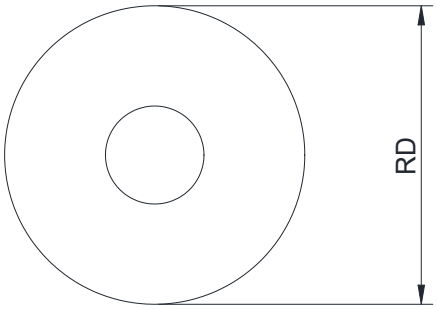
SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00	-	0.05
A3	0.15 Ref		
D	1.35	1.40	1.45
E	1.75	1.80	1.85
b	0.15	0.20	0.25
L	0.30	0.40	0.50
L1	0.40	0.50	0.60
e	0.40 BSC		

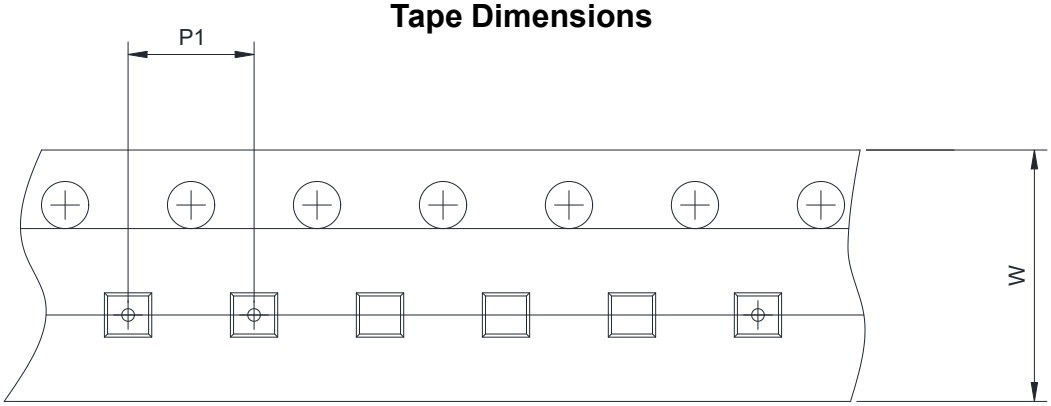
TAPE AND REEL INFORMATION

QFN1418-10L

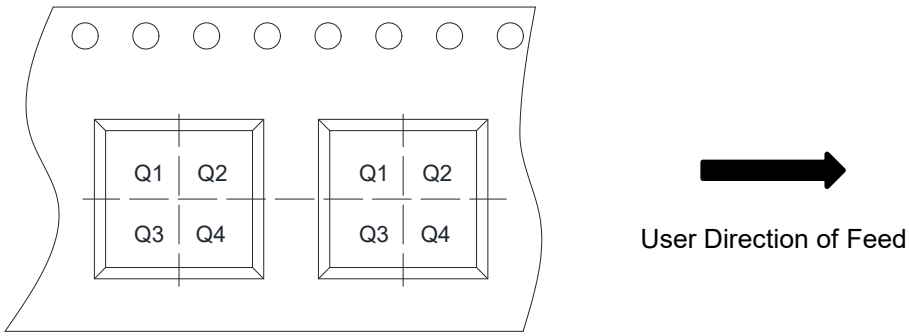
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
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