

WS72412
18MHz Rail-to-Rail Input Output CMOS Operational Amplifiers
[Http://www.willsemi.com](http://www.willsemi.com)
Descriptions

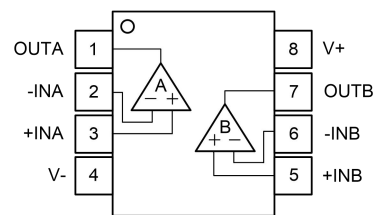
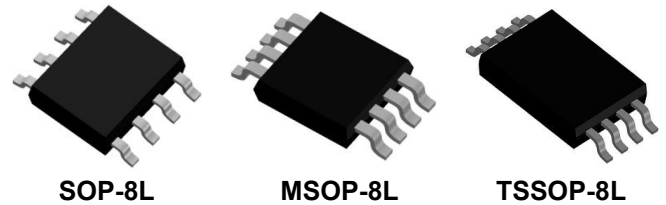
The WS72412 is a low power rail-to-rail input output operational amplifier featuring low current noise, high slew rate and wide signal bandwidth. The combination of low noise, low input bias currents, high speed and inside EMI filter make this amplifier useful in a wide variety of applications. Filters, integrators, photo-diode amplifiers, and high impedance sensors all benefit from this combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion of this device. Applications for this amplifier include power amplifier (PA) controls, laser diode control loops, portable and loop-powered instrumentation, audio amplification for portable devices, and ASIC input and output amplifiers. The WS72412 is dual channel version available in SOP-8L package , MSOP-8L and TSSOP-8L package.

Applications

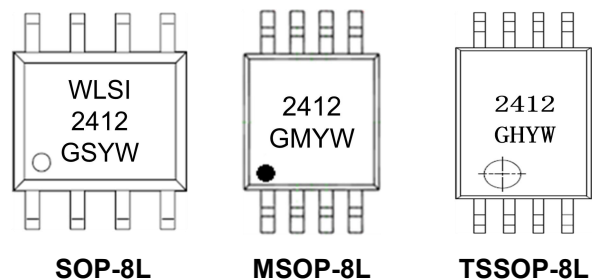
- Sensor Signal Conditioning
- Consumer Audio
- Multi-Pole Active Filters
- Communications
- Security
- Scanners

Features

- Gain-bandwidth Product : 18 MHz
- Low Noise : 8 nV/ $\sqrt{\text{Hz}}$ (f= 1kHz)
- Slew Rate : 9 V/ μs
- Offset Voltage : 2.5 mV (max)
- Supply Range : 2.2 V to 5.5 V
- Supply Current : 1.25 mA/ch
- High Output Current : 170 mA
- Low THD+N : -102dB
- Rail-to-Rail Input/Output Swing
- - 40°C to 125°C Operation Range
- Robust 8kV HBM and 400V MM and 2kV CDM



**SOP-8L/MSOP-8L/TSSOP-8L
Pin configuration (Top view)**


Marking

- 2412** = Device code
GS = Special code
GM = Special code
GH = Special code
Y = Year code
W = Week code

Order Information

Device	Package	Shipping
WS72412S-8/TR	SOP-8L	4000/Reel &Tape
WS72412M-8/TR	MSOP-8L	4000/Reel &Tape
WS72412H-8/TR	TSSOP-8L	4000/Reel &Tape

Pin Descriptions

Pin Number	Symbol	Descriptions
1	OUTA	Output of Amplifier A
2	-INA	Inverting input of Amplifier A
3	+INA	Non-inverting input of Amplifier A
4	V-	Negative supply
5	+INB	Non-inverting input of Amplifier B
6	-INB	Inverting input of Amplifier B
7	OUTB	Output of Amplifier B
8	V+	Positive supply

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage, ([V+] – [V-])	$V_S^{(2)}$	6	V
Input Differential Voltage	$V_{IDR}^{(3)}$	±6	V
Input Common Mode Voltage Range	V_{ICR}	(V-)-0.2 to (V+)+0.2	V
Output Short-Circuit Duration	t_{SO}	Unlimited	/
Operating Free-Air Temperature Range	T_A	-40 to 125	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Junction Temperature Range	T_J	150	°C
Lead Temperature Range	T_L	260	°C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values, except differential voltage are with respect to network terminal.
3. Differential voltages are at +IN with respect to -IN.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8 JEDEC-EIA/JESD22-A114A	±8000	V
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	±400	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	±2000	V

Electronics Characteristics

The *denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_{OUT} = V_S/2$, $R_{load} = 100\text{k}\Omega$, $C_{load} = 100\text{pF}$.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Input Offset Voltage	$V_{CM} = V_S/2$	-2.5	± 0.6	+2.5	mV
α_{VOS}	Input Offset Voltage Drift	-40°C to 125°C		2		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input Bias Current			10		pA
I_{OS}	Input Offset Current			10		pA
V_n	Input Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz		0.6		μV_{P-P}
e_n	Input Voltage Noise Density	$f = 1\text{kHz}$		8		$\text{nV}/\sqrt{\text{Hz}}$
CMRR	Common Mode Rejection Ratio	$V_{CM} = 1\text{V}$ to 3V	60	105		dB
V_{CM}	Common Mode Input Voltage Range		$(V_-) - 0.1$		$(V_+) + 0.1$	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.2\text{V}$ to 5.5V , $V_{CM} = 0\text{V}$	60	110		dB
A_{VOL}	Open Loop Large Signal Gain	$V_{OUT} = -2\text{V}$ to 2V , $R_{load} = 2\text{k}\Omega$	90	110		dB
V_{OH}	High Level Output Voltage	$R_{load} = 2\text{k}\Omega$		9		mV
		$R_{load} = 10\text{k}\Omega$		2		mV
V_{OL}	Low Level Output Voltage	$R_{load} = 2\text{k}\Omega$		8		mV
		$R_{load} = 10\text{k}\Omega$		2		mV
R_{OUT}	Closed-Loop Output Impedance	$G = 1$, $f = 1\text{MHz}$, $I_{OUT} = 0$		0.2		Ω
I_{SC}	Output Short-Circuit Current	Source Current		210		mA
		Sink Current		170		mA
V_S	Supply Voltage		2.2		5.5	V
I_Q	Quiescent Current per Amplifier	$V_S = 5\text{V}$		1.25	1.6	mA
PM	Phase Margin	$R_{load} = 1\text{k}\Omega$, $C_{load} = 60\text{pF}$		60		degrees
GM	Gain Margin	$R_{load} = 1\text{k}\Omega$, $C_{load} = 60\text{pF}$		8		dB
GBWP	Gain-Bandwidth Product	$f = 1\text{kHz}$		18		MHz
t_s	0.1% Settling Time	1.5 to 3.5V , Unity Gain		0.75		μs
SR	Slew Rate	$A_V = 1$, $R_{load} = 2\text{k}\Omega$, $C_{load} = 100\text{pF}$		9		$\text{V}/\mu\text{s}$
FPBW	Full Power Bandwidth	$2V_{P-P}$		400		kHz
THD+N	Total Harmonic Distortion and Noise	$f = 1\text{kHz}$, $A_V = 1$, $R_{load} = 2\text{k}\Omega$, $V_{OUT} = 1V_{PP}$		-102		dB
X_{talk}	Channel Separation	$f = 1\text{kHz}$, $R_L = 2\text{k}\Omega$		110		dB

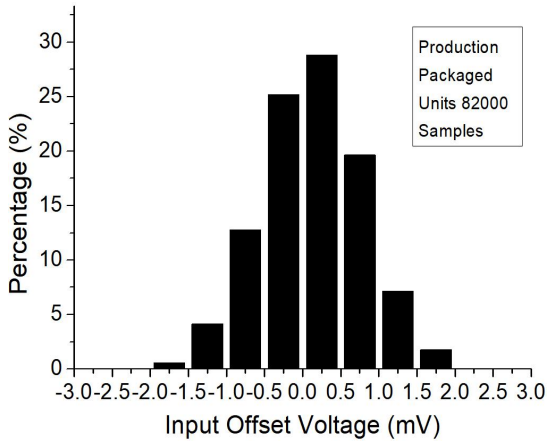
Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
2. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.
3. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.
4. Full power bandwidth is calculated from the slew rate $FPBW = SR/(\pi \cdot V_{P-P})$.

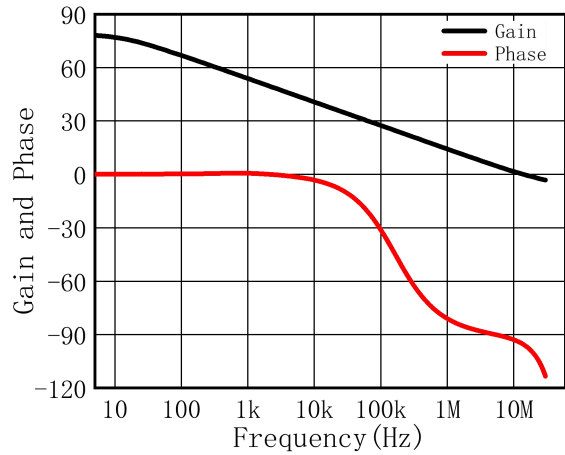
Typical Characteristics

$T_A=25^{\circ}\text{C}$, $V_S=\pm 2.5\text{V}$, $V_{CM}=0\text{V}$, unless otherwise noted.

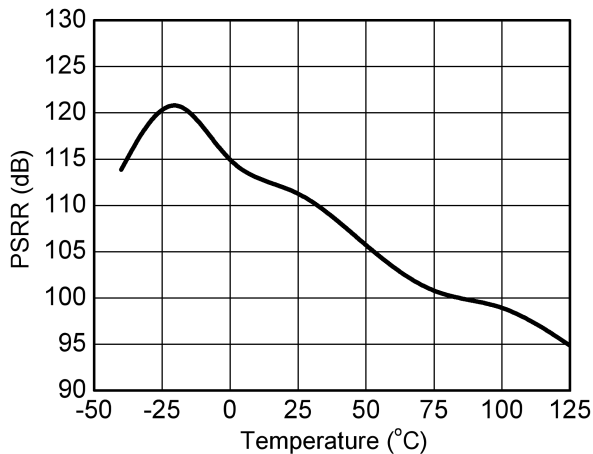
Offset Voltage Production Distribution



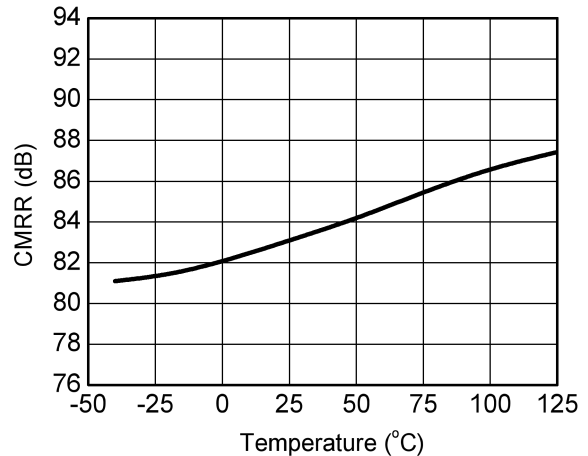
Open-Loop Gain and Phase



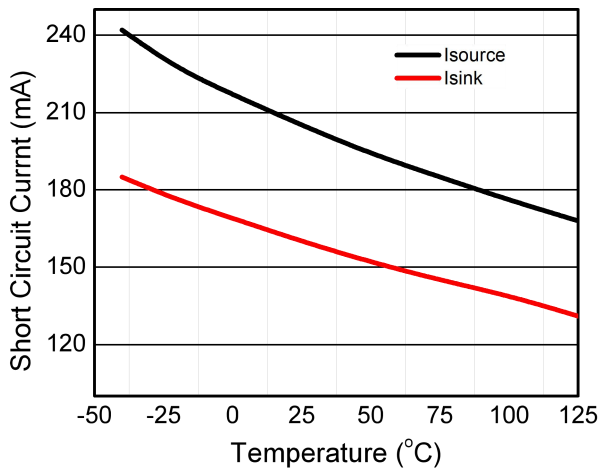
Power-Supply Rejection Ratio vs. Temperature



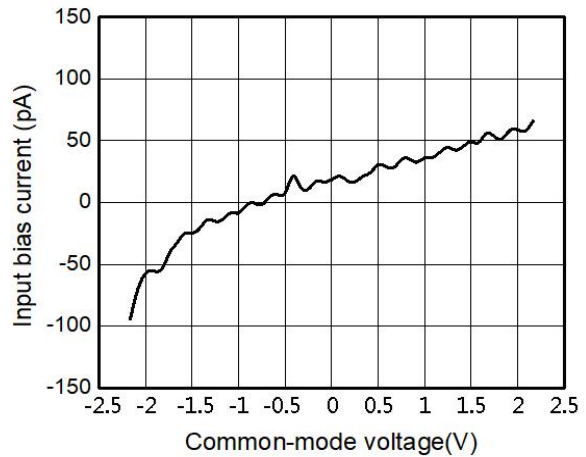
CMRR vs. Temperature



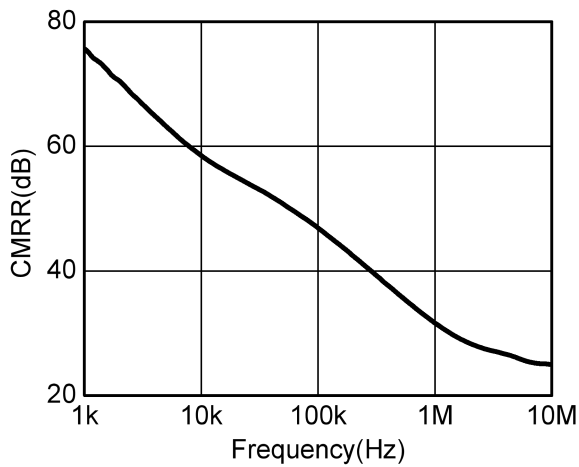
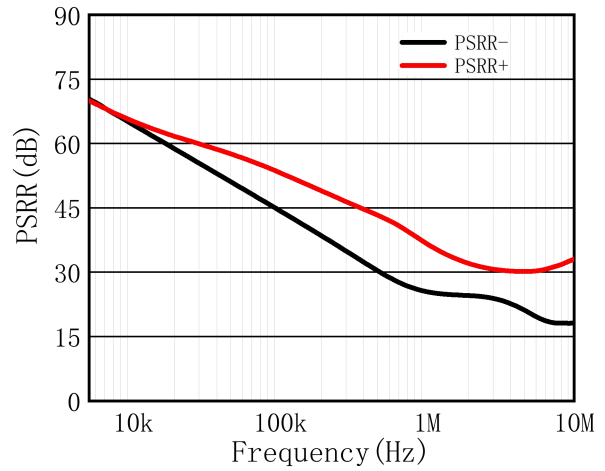
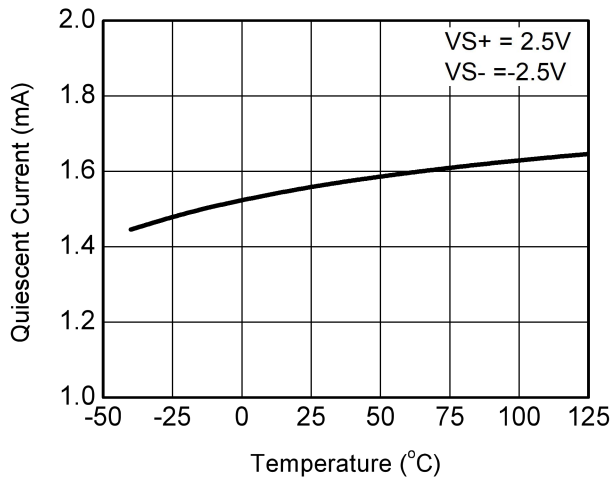
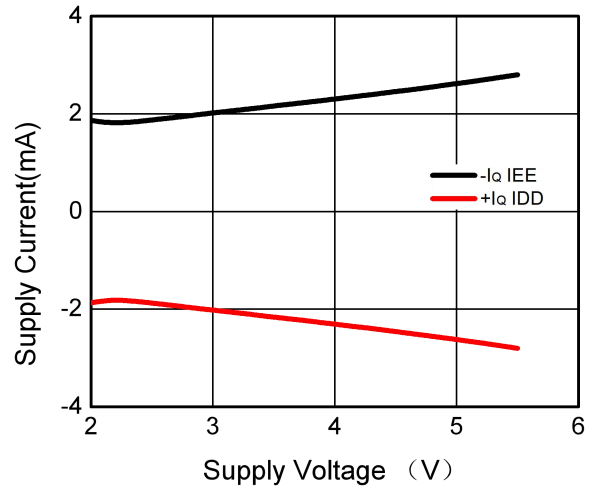
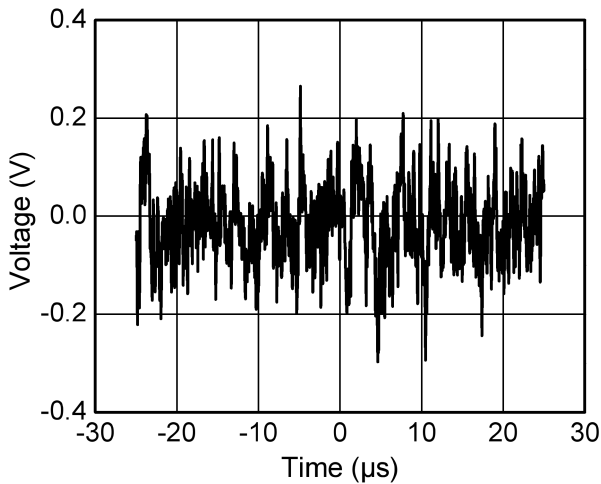
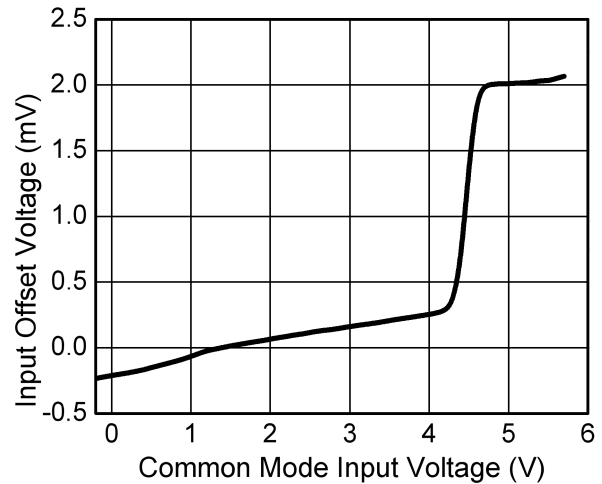
Short Circuit Current vs. Temperature



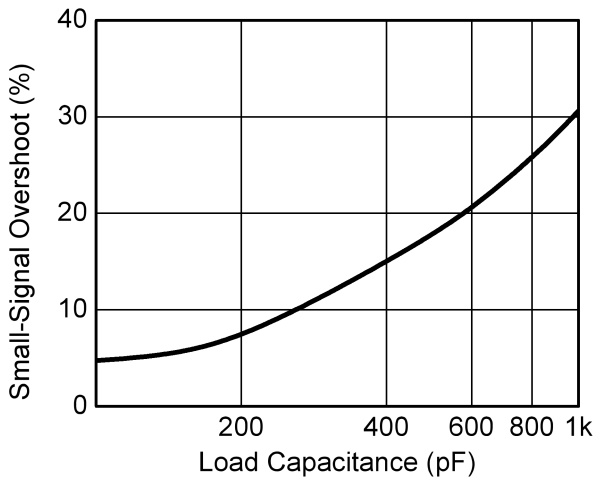
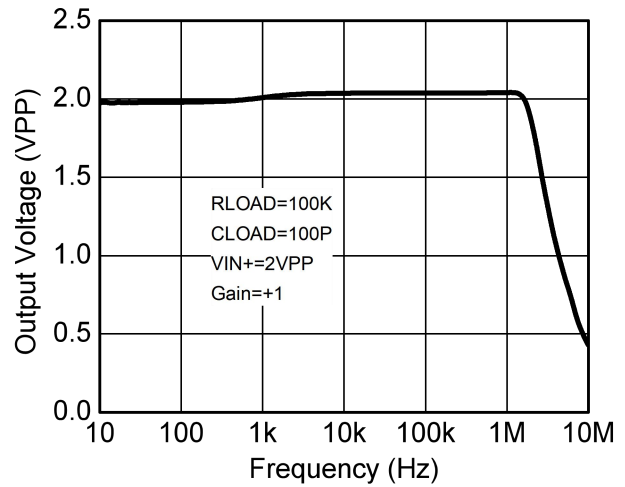
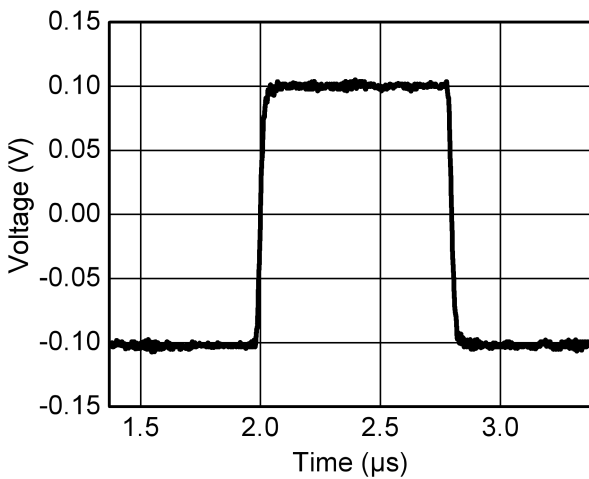
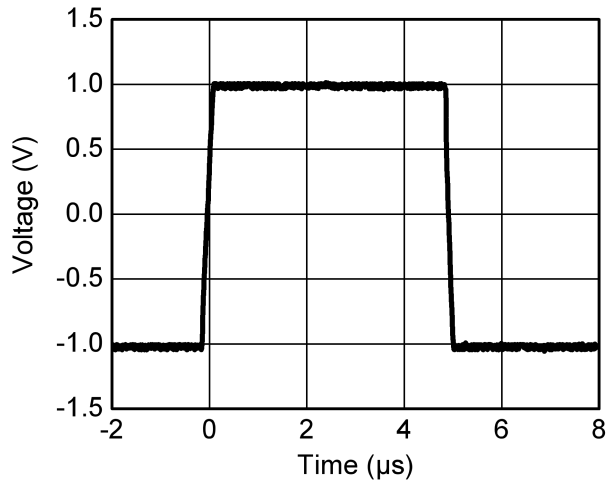
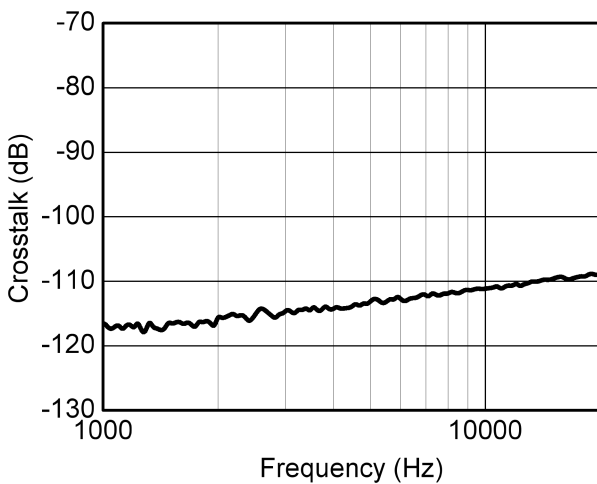
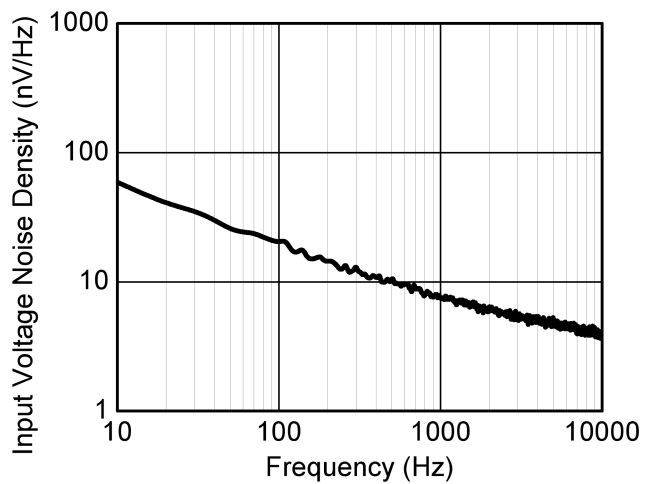
Input Bias Current vs. Input Common Mode Voltage



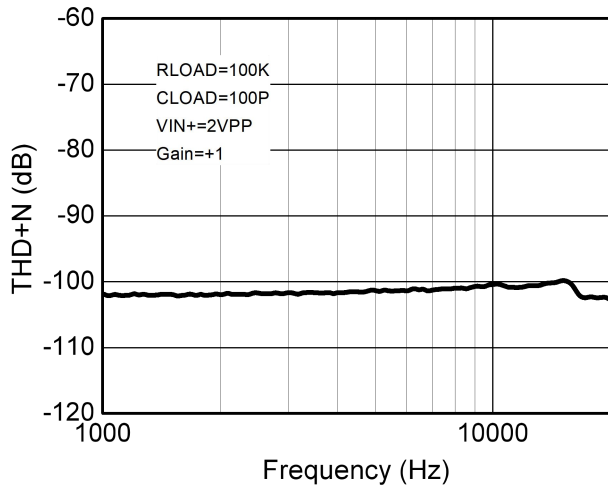
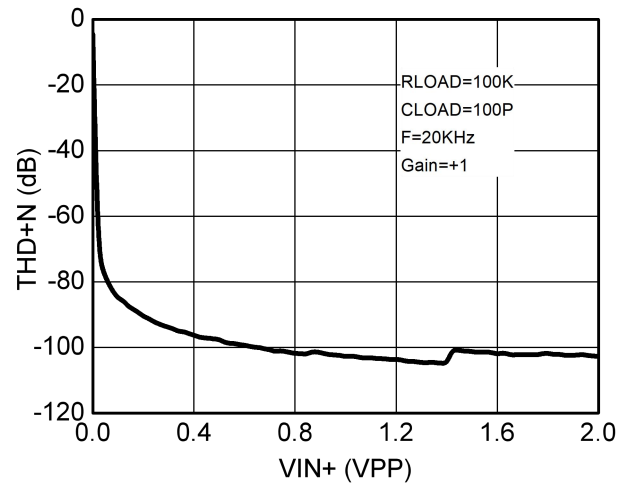
Typical Characteristics (continued)
 $T_A=25^\circ\text{C}$, $V_S=\pm 2.5\text{V}$, $V_{CM}=0\text{V}$, unless otherwise noted

CMRR vs. Frequency

Power-Supply Rejection Ratio vs. Frequency

Quiescent Current vs. Temperature

Quiescent Current vs. Supply Voltage

0.1 Hz TO 10 Hz Input Voltage Noise

Offset Voltage vs Common-Mode Voltage


Typical Characteristics (continued)
 $T_A=25^\circ\text{C}$, $V_S=\pm 2.5\text{V}$, $V_{CM}=0\text{V}$, unless otherwise noted

Small-Signal Overshoot vs. Load Capacitance

Closed-Loop Output Voltage Swing

Small-Signal Step Response, 100mV Step

Large-Scale Step Response, 2V Step

Crosstalk

Noise Density


Typical Characteristics (continued)
 $T_A=25^\circ\text{C}$, $V_S=\pm 2.5\text{V}$, $V_{CM}=0\text{V}$, unless otherwise noted

THD+N vs freq

THD+N vs Vin

Operation

The WS72412 series op amps can operate on a single-supply voltage (2.2 V to 5.5 V), or a split-supply voltage (± 1.1 V to ± 2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 μ F to 0.1 μ F). These amplifiers are fully specified from +2.2 V to +5.5 V and over the extended temperature range of -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

Input ESD Diode Protection

The WS72412 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 1 shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

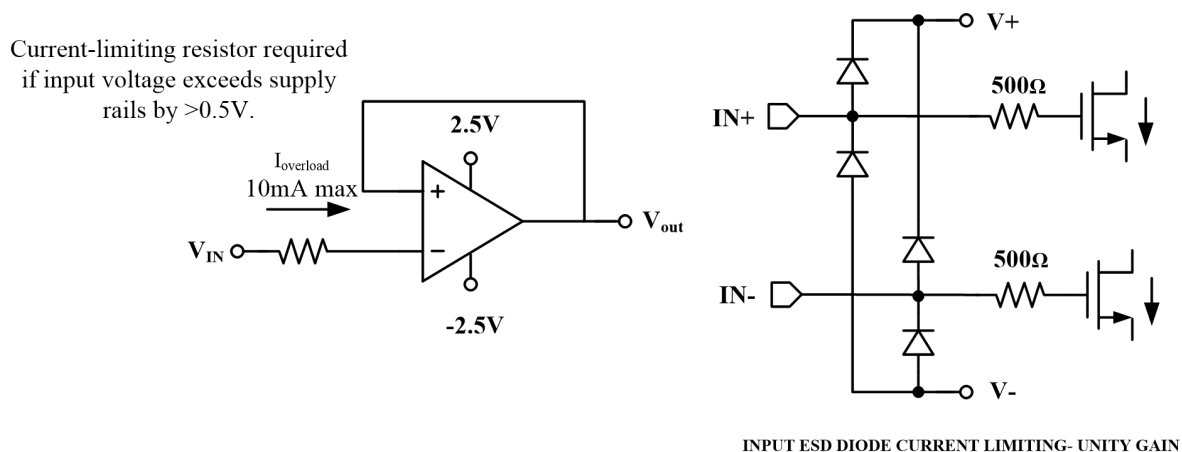


Figure1. Input ESD Diode

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12} \Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the WS72412 OPA's input bias current at $+27^{\circ}\text{C}$ ($\pm 3\text{pA}$, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

- a) Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op-amp (e.g., $V_{DD}/2$ or ground).

b) Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

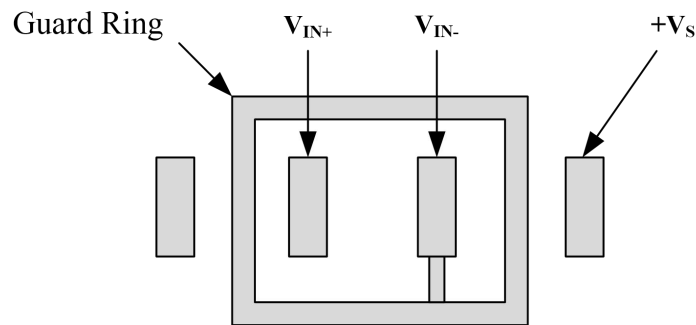


Figure 2 The Layout of Guard Ring

Power Supply Layout and Bypass

The WS72412 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., $0.01\mu\text{F}$ to $0.1\mu\text{F}$) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., $1\mu\text{F}$ or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PCB lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

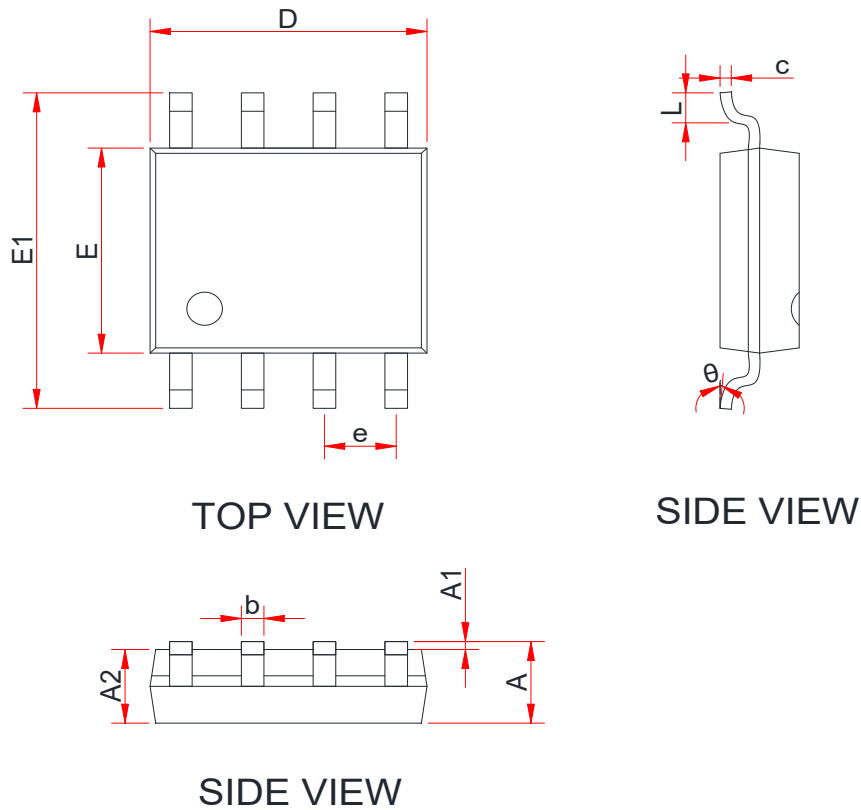
To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

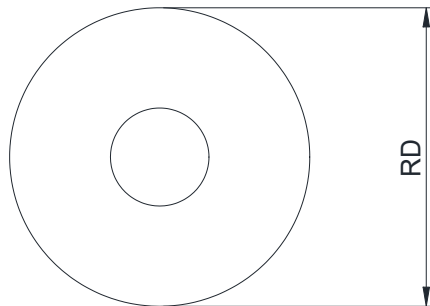
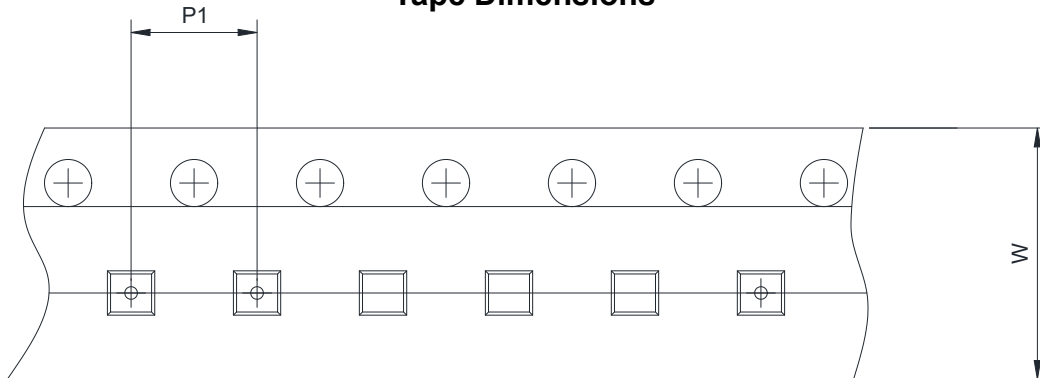
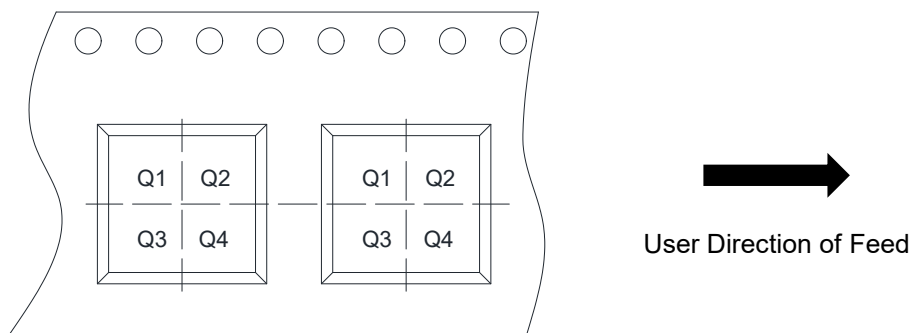
A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of

thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

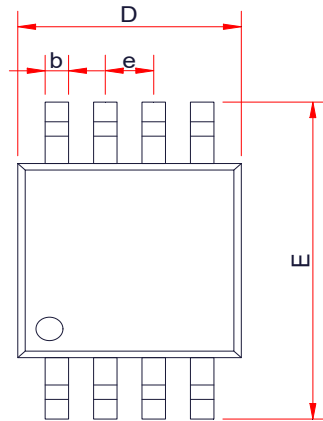
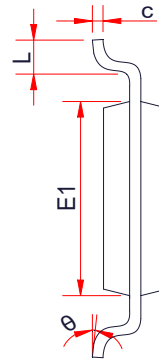
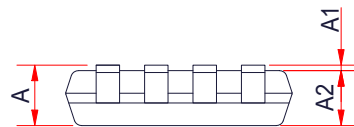
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

PACKAGE OUTLINE DIMENSIONS
SOP-8L


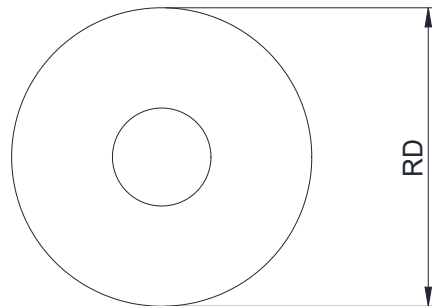
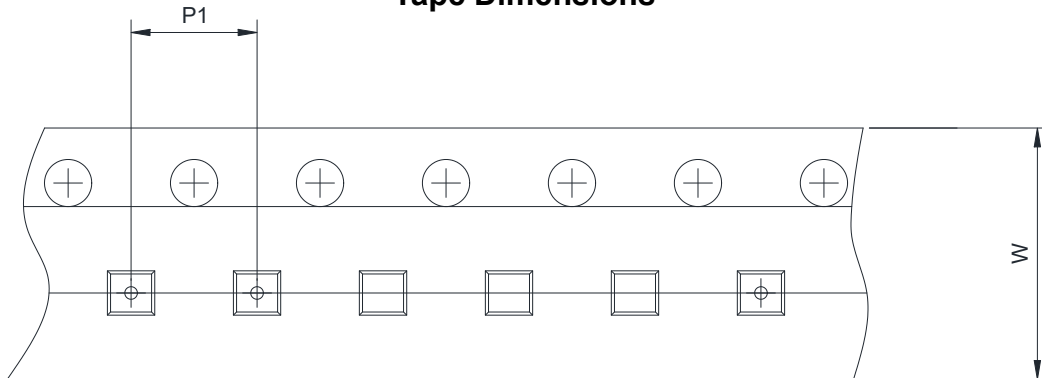
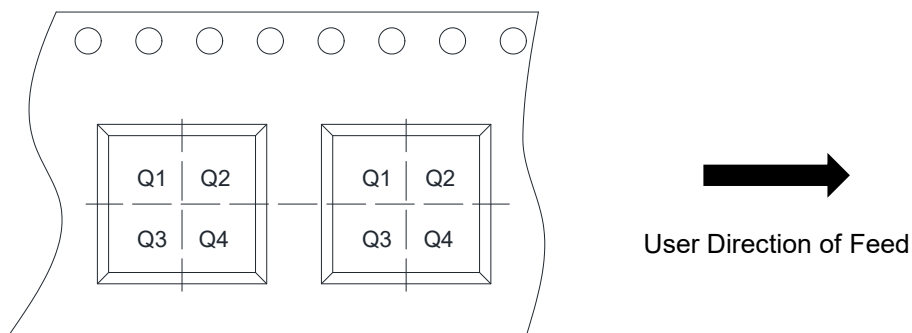
Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	1.35	1.55	1.75
A1	0.05	0.15	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.15	-	0.26
D	4.70	4.90	5.10
E	3.70	3.90	4.10
E1	5.80	6.00	6.20
e	1.27BSC		
L	0.40	-	1.27
θ	0°	-	8°

TAPE AND REEL INFORMATION
SOP-8L
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


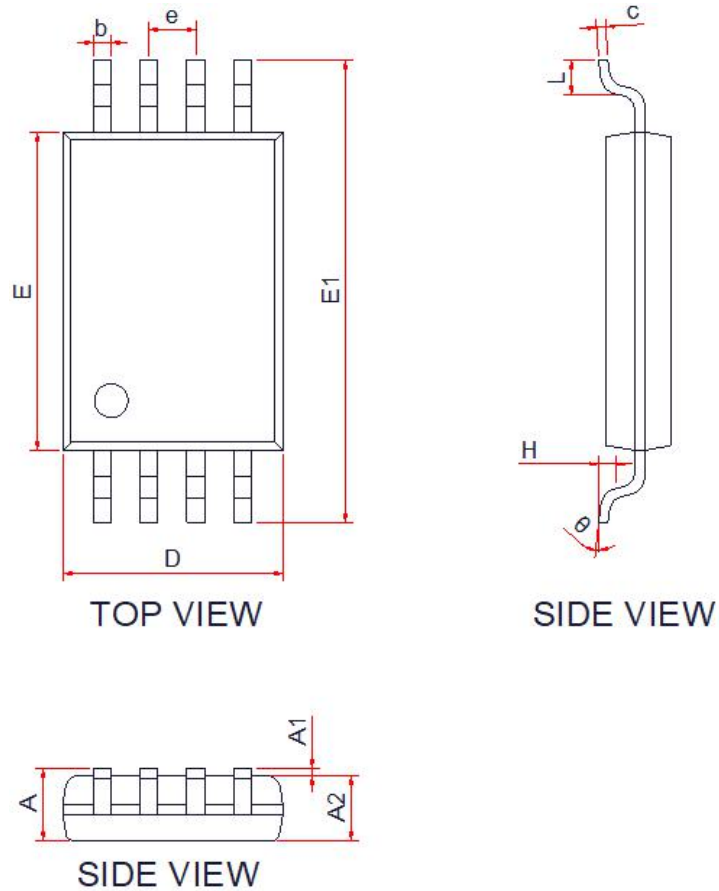
RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm	<input checked="" type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4

PACKAGE OUTLINE DIMENSIONS
MSOP-8L

TOP VIEW

SIDE VIEW

SIDE VIEW

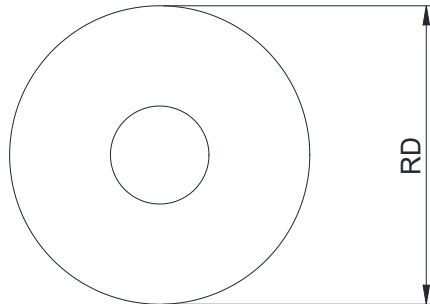
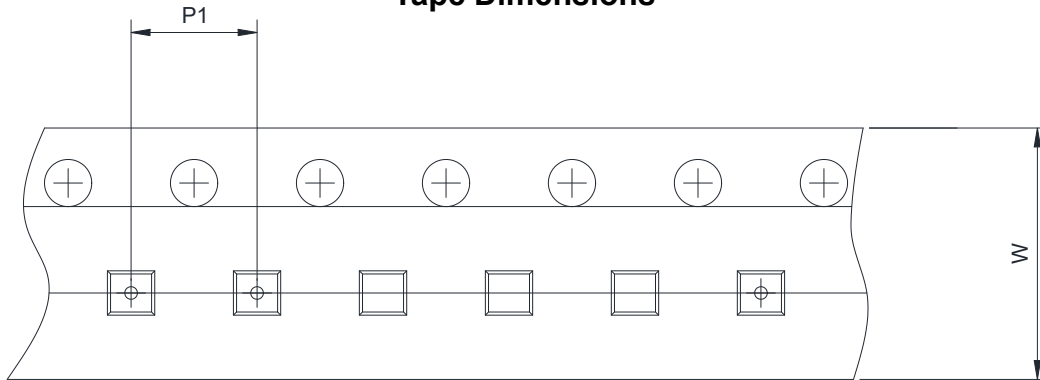
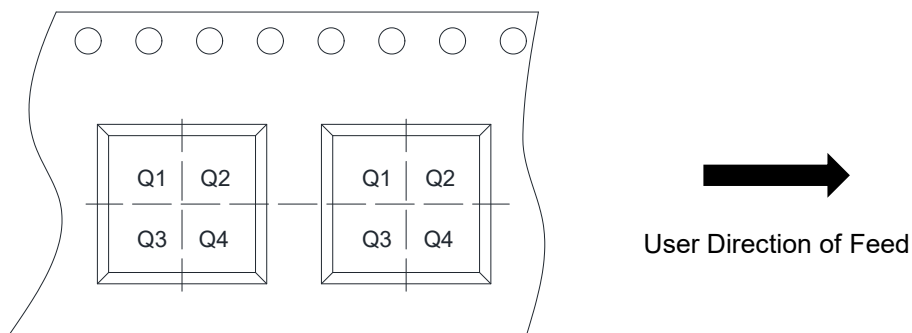
Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	-	-	1.10
A1	0.02	-	0.15
A2	0.75	0.80	0.95
b	0.25	-	0.38
c	0.09	-	0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	-	0.80
θ	0°	-	6°

TAPE AND REEL INFORMATION
MSOP-8L
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm	<input checked="" type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4

PACKAGE OUTLINE DIMENSIONS
TSSOP-8L


Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	2.90	3.00	3.10
E	4.30	4.40	4.50
E1	6.25	6.40	6.55
e	0.65 BSC		
L	0.45	-	0.75
θ	0°	-	8°

TAPE AND REEL INFORMATION
TSSOP-8L
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape


RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm	<input checked="" type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4