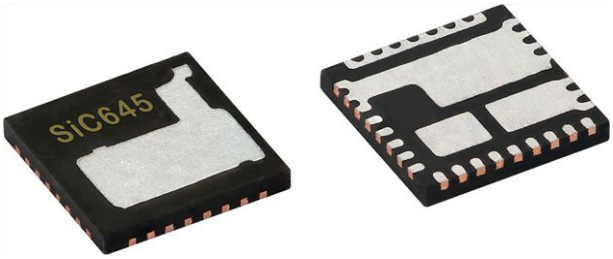
60 A VRPower® Smart Power Stage (SPS) Module with Integrated High Accuracy Current and Temperature Monitors



DESCRIPTION

The SiC645 is a smart VRPower® device that integrates a high side and low side MOSFET, a high performance driver with integrated bootstrap FET. The SiC645 offers high accuracy current and temperature monitors that can be fed back to the controller and doubler to complete a multiphase DC/DC system. They simplify design and increase performance by eliminating the DCR sensing network and associated thermal compensation. Light-load efficiency is supported via a dedicated left control pin. An industry leading thermally enhanced dual cooled, 5 mm x 5 mm PowerPAK® MLP package allows minimal overall PCB real estate and low profile construction.

The devices feature a 3.3 V (SiC645A) or 5 V (SiC645) compatible tri-state PWM input that, working together with multiphase PWM controllers, will provide a robustsolution in the event of abnormal operating conditions. The SiC645 also improves system performance and reliability with integrated fault protection of UVLO, over-temperature and over-current. An open-drain fault reporting pin simplifies the handshake between the smart VRPower device and multiphase controllers and can be used to disable the controller during start-up and fault conditions.

FEATURES

- Input range: 4.5 V to 18 V
- Supports 60 A DC current
- Compatible with 3.3 V (SiC645A) and 5 V (SiC645) tri-state PWM
- Down slope current sensing
- ± 3 % accuracy current monitor (I_{MON}) with REF_{IN} input
- 8 mV/°C temperature monitor with OT flag
- Dedicated low side FET control input
- Fault protection
  - High side FET short and over-current protection
  - Over-temperature protection
  - V_{CC} and V_{IN} under voltage lockout (UVLO)
- Open drain fault reporting output
- Up to 2 MHz switching frequency
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- High frequency and high efficiency VRM and VRD
- Core, graphic, and memory regulators for microprocessors
- High density VR for server, networking, and cloud computing
- POL DC/DC converters and video gaming consoles

TYPICAL APPLICATION DIAGRAM

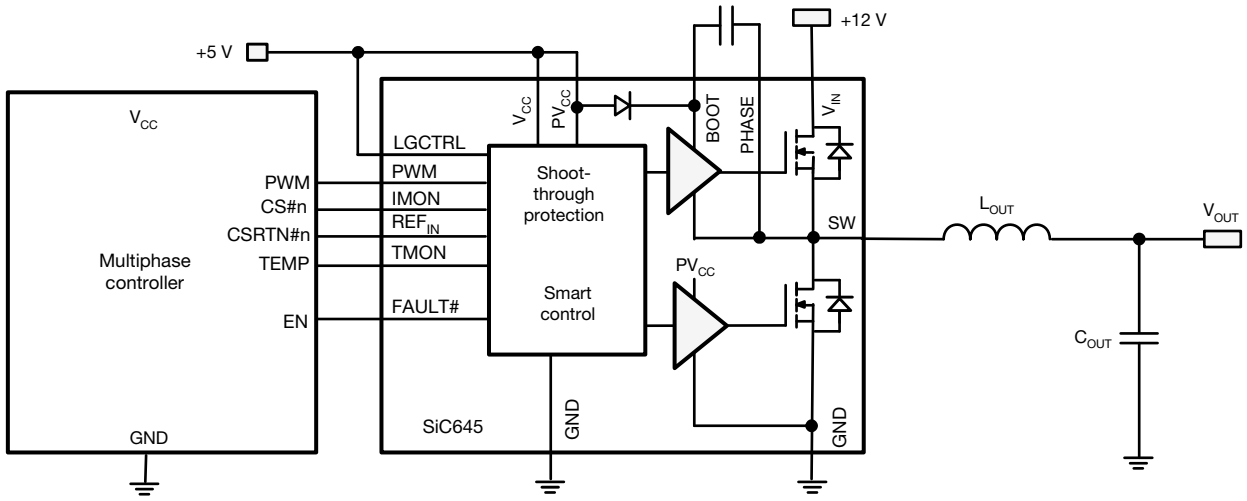


Fig. 1 - Typical Application Block Diagram

TYPICAL APPLICATION CIRCUIT WITH SiC645

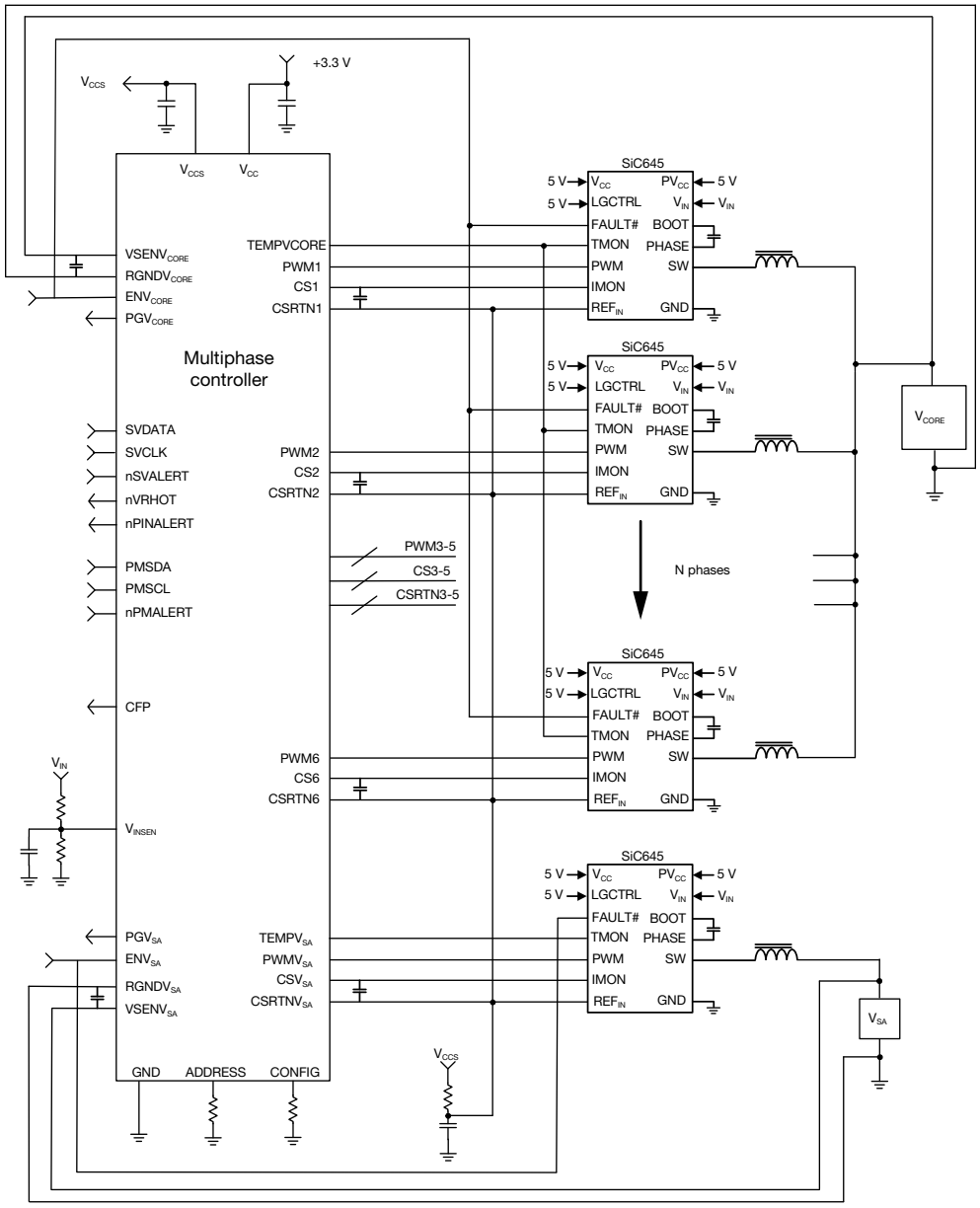


Fig. 2 - Typical Application Circuit

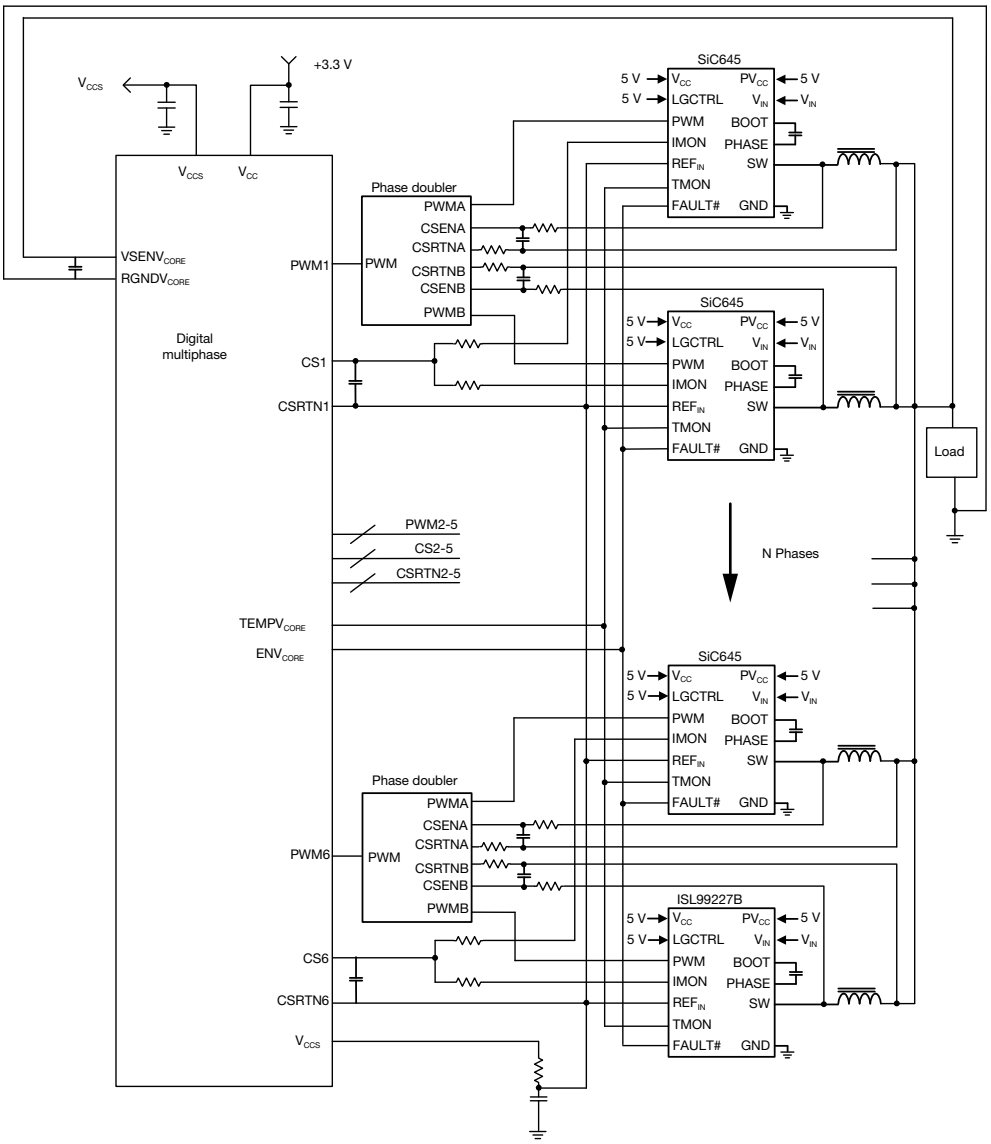


Fig. 3 - Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

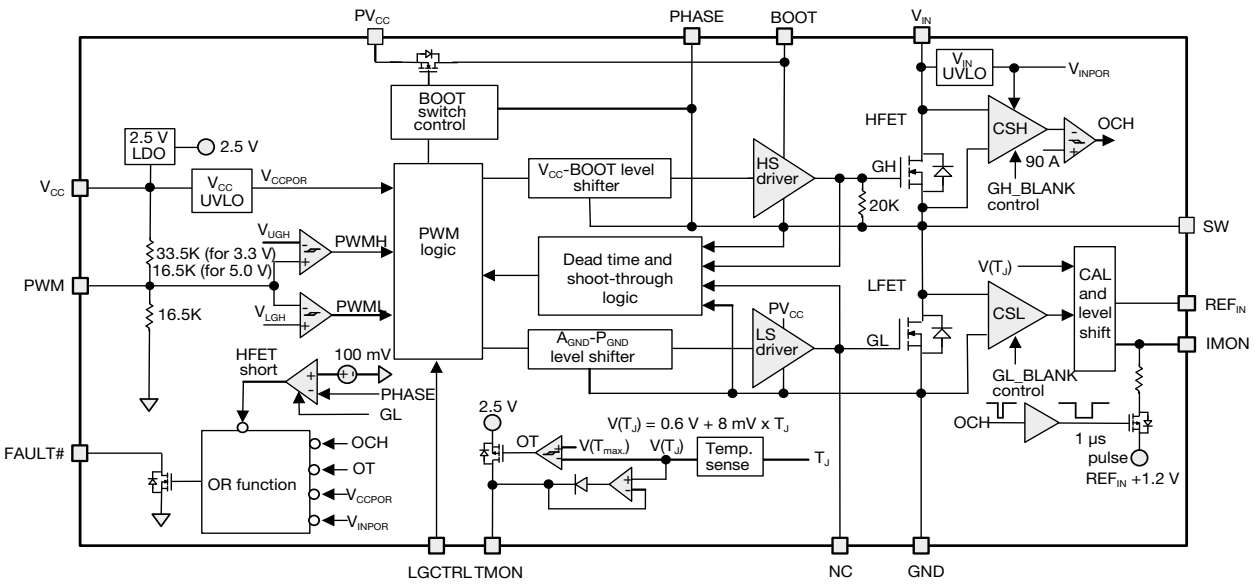


Fig. 4 - Functional Block Diagram

ORDERING INFORMATION				
PART NUMBER	**MARKING CODE**	**TEMPERATURE RANGE (°C)**	**PWM INPUT (V)**	**PACKAGE (RoHS-compliant)**
SiC645ADR-T1-GE3	45D	-40 to +85	3.3	Dual cooled PowerPAK MLP55-32L
SiC645ALR-T1-GE3	45L	-10 to +100	3.3	Dual cooled PowerPAK MLP55-32L
SiC645AER-T1-GE3	45E	-40 to +125	3.3	Dual cooled PowerPAK MLP55-32L
SiC645ER-T1-GE3	45E	-40 to +125	5	Dual cooled PowerPAK MLP55-32L

PINOUT CONFIGURATION

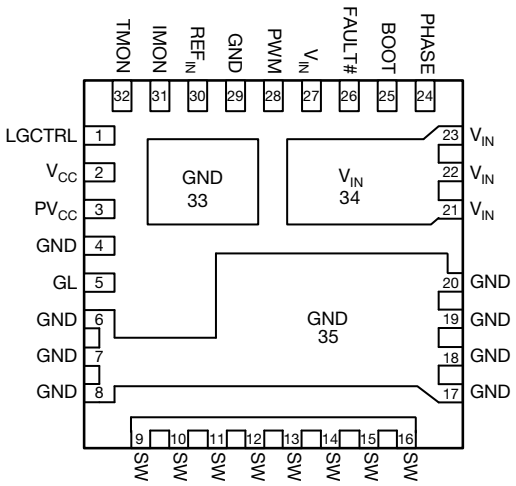


Fig. 5 - Pinout Configuration

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	LGCTRL	Lower gate control signal input. LO = GL LO (LFET off). HI = normal operation (GL and GH strictly obey PWM). This pin should be driven with a logic signal, or externally tied high if not required; it should not be left floating
2	V_{CC}	+5 V logic bias supply. Place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to GND
3	PV_{CC}	+5 V gate drive bias supply. Place a high quality low ESR ceramic capacitor (~1 µF/X7R) in close proximity from this pin to GND
4, 6, 7, 8, 17, 18, 19, 20, 29, 33, 35	GND	GND pins are internally connected. Pins 4 and 29 should be connected directly to the nearby GND paddles on package bottom. Fig. 15 shows GND paddles should be connected to the system GND plane with as many vias as possible to maximize thermal and electrical performance.
5	NC	No connect (This is a low side gate driver output (GL), optional to monitor for system debugging)
9, 10, 11, 12, 13, 14, 15, 16	SW	Switching junction node between HFET source and LFET drain. Connect directly to output inductor
21, 22, 23, 27, 34	V_{IN}	Input of power stage (to drain of HFET). Place at least 2 ceramic capacitors (10 µF or higher, X5R or X7R) in close proximity across V_{IN} and GND. Pin 27 should not be used for decoupling. For optimal performance, place as many vias as possible in the bottom side V_{IN} paddle
24	PHASE	Return of boot capacitor. Internally connected to SW node so no external routing required for SW connection
25	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (0.1 µF/X7R to 0.22 µF/X7R)i n close proximity across BOOT and PHASE pins
26	FAULT#	Open drain output pin. Any fault (over-current, over-temperature, shorted HFET, or POR / UVLO) will pull this pin to ground. This pin may be connected to the controller enable pin or used to signal a fault at the system level
28	PWM	PWM input of gate driver, compatible with 3.3 V and 5 V tri-state PWM signal
30	REF_{IN}	Input for external reference voltage for I_{MON} signal. This voltage should be between 0.8 V and 1.6 V. Connect REF_{IN} to the appropriate current sense input of the controller. Place a high quality low ESR ceramic capacitor (~ 0.1 µF) in close proximity from this pin to GND
31	I_{MON}	Current monitor output, referenced to REF_{IN}. I_{MON} will be pulled high (to REF_{IN} +1.2 V) to indicate an HFET shorted or over-current fault. Connect the I_{MON} output to the appropriate current sense input of the controller. No more than 56 pF capacitance can be directly connected across I_{MON} and REF_{IN} pins. With a 100 Ω series resistor, up to 470 pF may be used
32	T_{MON}	Temperature monitor output. For multiphase, the T_{MON} pins can be connected together as a common bus; the highest voltage (representing the highest temperature) will be sent to the PWM controller. T_{MON} will be pulled high (to 2.5 V) to indicate an over-temperature fault. No more than 250 pF total capacitance can be directly connected across T_{MON} and GND pins; with a series resistor, a higher capacitance load is allowed, such as 1 kΩ for 100 nF load

ABSOLUTE MAXIMUM RATINGS				
ELECTRICAL PARAMETER	**SYMBOL**	**CONDITIONS**	**LIMIT**	**UNIT**
Supply voltage	V_{CC}, PV_{CC}		-0.3 to +6	V
Input supply voltage	V_{IN}		-0.3 to +25	
PHASE, SW voltage	V_{PH-GND}, V_{SW-GND}	GND - 10 V, < 20 ns pulse width, 10 µJ	-0.3 to +25	
BOOT voltage	V_{BOOT_GND}		-0.3 to +36	
Other I/O pin voltage			-0.3 to V_{CC} + 0.3	
Maximum junction temperature (plastic package)			150	°C
Maximum storage temperature range			-65 to +150	
Lead (Pb)-free reflow profile			-	-

Note

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
Operating junction temperature range	-40	-	125	°C
Supply voltage (V_{CC}, PV_{CC})	-	5 ± 5 %	-	V
Input supply voltage (V_{IN})	4.5	-	18	

THERMAL INFORMATION		
THERMAL RESISTANCE	**θ_{JA} (°C/W)**	**θ_{JC} (°C/W)**
Dual cooled PowerPAK MLP55-32L (1)(2)(3)	10.7	1.6

Notes

(1) θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features

(2) For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside

(3) These ratings vary with PCB layout and operating condition, and limited by device temperature and thermal shutdown trip point

ELECTRICAL SPECIFICATIONS

(recommended operating conditions, unless otherwise noted. T_J = -40 °C to +125 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN. (1)	TYP.	MAX. (1)	
POWER RATING						
Maximum instant power dissipation		T_A = 25 °C, 150 A (2)	-	100	-	W
Maximum continuous power dissipation		T_A = 25 °C, θ_{JA} = 10 °C/W, T_J = 150 °C (2)	-	12.5	-	
THERMAL RESISTANCE						
Thermal resistance junction to PCB	θ_{JB}	(2)	-	5.2	-	°C/W
Thermal resistance junction to ambient	θ_{JA}	0 LFM (2)	-	10.7	-	
		400 LFM (2)	-	9.3	-	
V_{CC} SUPPLY CURRENT						
Logic standby current	IV_{CC}	PWM = open	-	4.75	-	mA
Gate drive standby current	IPV_{CC}	PWM = open	-	100	-	µA
Logic operational current	IV_{CC}	PWM = 300 kHz	-	4.75	-	mA
Gate drive operational current	IPV_{CC}	PWM = 300 kHz	-	15	-	
POWER-ON RESET AND ENABLE						
V_{CC} rising POR threshold			-	3.86	4.20 (3)	V
V_{CC} falling POR threshold			3.20 (3)	3.58	-	
V_{CC} POR hysteresis			-	280	-	mV
V_{CC} POR delay to operation			-	125	197 (3)	µs
V_{IN} rising POR threshold			-	4	4.2 (3)	V
V_{IN} falling POR threshold			3.4 (3)	3.5	-	
V_{IN} POR hysteresis			-	445	-	mV
3.3 V PWM INPUT (see "Timing Diagram")						
Sink impedance			-	33.5	-	kΩ
Source impedance			-	16.5	-	
Tri-state lower gate falling threshold		V_{CC} = 5 V	-	1.11	-	V
Tri-state lower gate rising threshold			-	0.87	-	
Tri-state upper gate rising threshold			-	2.13	-	
Tri-state upper gate falling threshold			-	1.95	-	
Tri-state shutdown window			1.3 (3)	-	1.8 (3)	
5 V PWM INPUT (see "Timing Diagram")						
Sink impedance			-	16.5	-	kΩ
Source impedance			-	16.5	-	
Tri-state lower gate falling threshold		V_{CC} = 5 V	-	1.51	-	V
Tri-state lower gate rising threshold			-	1.14	-	
Tri-state upper gate rising threshold			-	3.24	-	
Tri-state upper gate falling threshold			-	3.02	-	
Tri-state shutdown window			1.6 (3)	-	2.8 (3)	
SWITCHING TIME						
GH turn-on propagation delay	t_{PDHU}	GL low to GH high, see Fig. 6	-	8	-	ns
GH turn-off propagation delay	t_{PDLU}	PWM low to GH low, see Fig. 6	-	40	-	
GL turn-on propagation delay	t_{PDHL}	GH low to GL high, see Fig. 6	-	8	-	
GL turn-off propagation delay	t_{PDLL}	PWM high to GL low, see Fig. 6	-	23	-	
GL exit tri-state propagation delay	t_{PDTSL}	Tri-state to GL high), see Fig. 6	-	25	-	
GH exit tri-state propagation delay	t_{PDTSU}	Tri-state to GH high, see Fig. 6	-	35	-	
PWML tri-state shutdown hold-off time	t_{TSSHDL}	PWM low to GL low, see Fig. 6	-	40	-	
PWMH tri-state shutdown hold-off time	t_{TSSHDU}	PWM low to GH low, see Fig. 6	-	50	-	

ELECTRICAL SPECIFICATIONS

(recommended operating conditions, unless otherwise noted. T_J = -40 °C to +125 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN. (1)	TYP.	MAX. (1)	
CURRENT MONITOR						
$IREF_{IN}$ voltage range			0.8 (3)	1.2	1.6 (3)	V
I_{MON} current gain accuracy (V_{CC} = 5 V)		10 A, T_J = 90 °C	-	± 2	-	%
		≥ 10 A, T_J = 40 °C to 25 °C	-	± 3	-	
		≥ 10 A, T_J = 20 °C to 125 °C	-	± 4	-	
		≥ 10 A, T_J = 0 °C to 125 °C	-	± 5	-	
Downslope blanking time			-	160	-	ns
HFET over-current trip			-	90	-	A
I_{MON} to $IREF_{IN}$ at OCP			1.1 (3)	1.2	1.3 (3)	V
TEMPERATURE MONITOR						
Over-temperature rising threshold			-	140	-	°C
Over-temperature falling threshold			-	125	-	
Over-temperature hysteresis			-	15	-	
Temperature coefficient		T_J = 25 °C to 125 °C	-	8	-	mV/K
		T_J = -40 °C to +25 °C	-	8	-	
T_{MON} voltage at 25 °C temperature		V (T_J) = 0.6 V + (8 mV x T_J)	-	0.80	-	V
T_{MON}high at over-temperature			2.3 (3)	2.5	2.7 (3)	
FAULT PIN						
Output low voltage		5 mA	-	0.18	0.26	V
Leakage current			-	16	-	nA
BOOTSTRAP DIODE						
Forward voltage drop		5 mA	-	0.09	-	V
On-resistance	R_F		-	16	-	Ω
LGCTRL PIN						
Rising threshold		Logic high, (normal: obeys PWM)	-	1.29	1.6	V
Falling threshold		Logic low, (forces GL low; left off)	0,70 c	1.01	-	
MOSFETs						
High side MOSFET (HFET) $R_{DS(on)}$			-	3.6	-	mΩ
Low side MOSFET (LFET) $R_{DS(on)}$			-	0.76	-	

Notes

(1) Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design

(2) These ratings vary with PCB layout and operating condition, and limited by SPS temperature and thermal shutdown trip point

(3) Limits apply across the operating temperature range

TIMING DIAGRAM

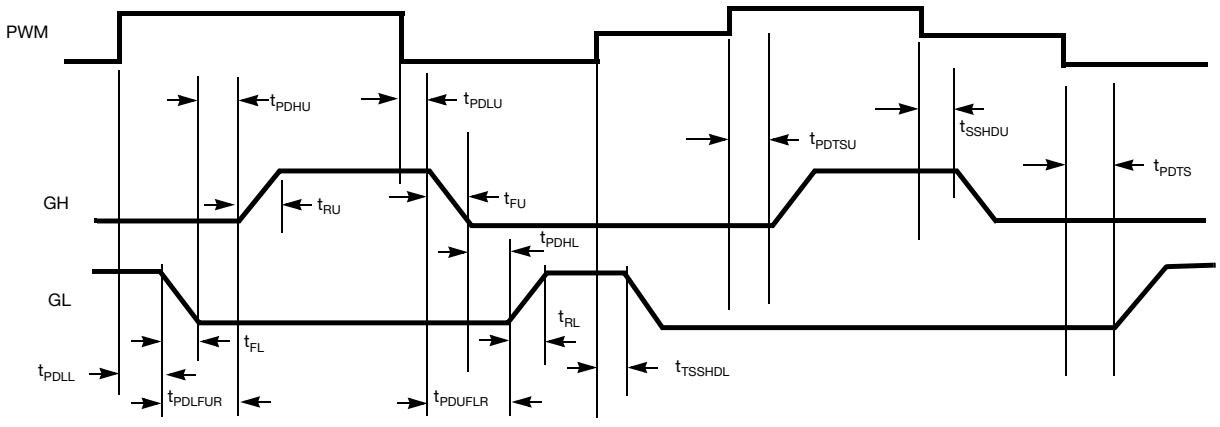


Fig. 6 - Timing Diagram

TYPICAL CHARACTERISTICS (P_{VCC} = 5 V, T_A = 25 °C, unless otherwise stated)

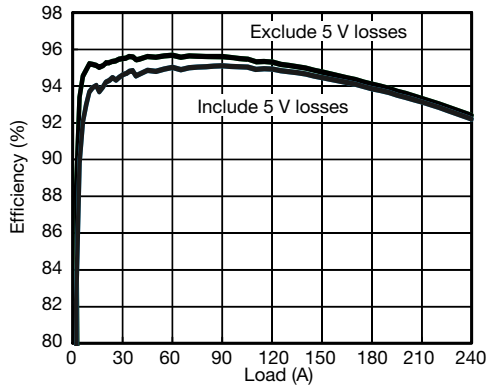


Fig. 7 - 1.8 V V_{OUT} Power Stage Efficiency (V_{IN} = 12 V, f_{SW} = 500 kHz; L_{OUT} = 0.18 µH/0.17mΩ/FP1008-180-R; Auto-Phase Enabled in 6-Phase Operation)

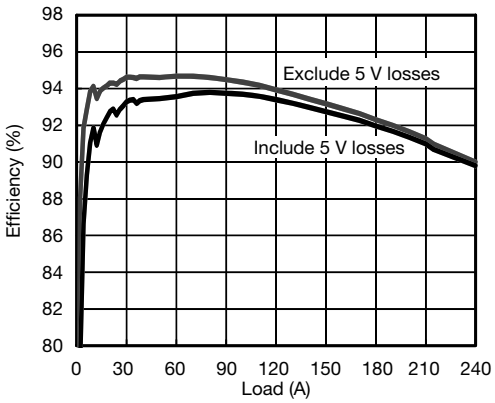


Fig. 10 - 1.2 V Power Stage Efficiency (V_{IN} = 12 V, f_{SW} = 500 kHz; L_{OUT} = 0.18 µH/0.17mΩ/FP1008-180-R; Auto-Phase Enabled in 6-Phase Operation)

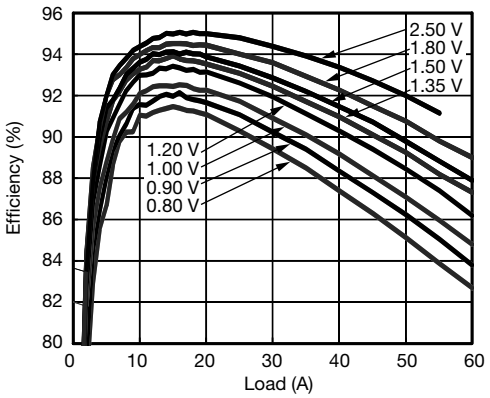


Fig. 8 - Power Stage Efficiency (V_{IN} = 12 V, f_{SW} = 500 kHz; L_{OUT} = 0.18 µH/0.17mΩ/FP1008-180-R

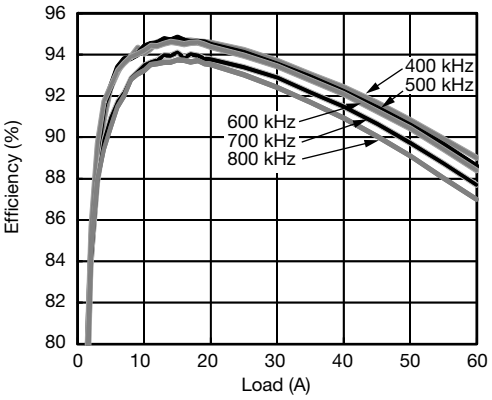


Fig. 11 - Power Stage Efficiency (V_{IN} = 12 V, f_{SW} = 500 kHz; L_{OUT} = 0.18 µH/0.17mΩ/FP1008-180-R

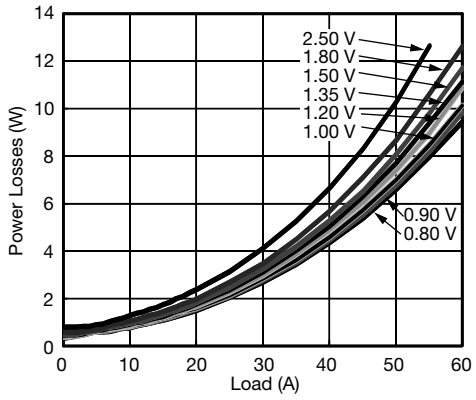


Fig. 9 - Power Dissipation (V_{IN} = 12 V, f_{SW} = 500 kHz; L_{OUT} = 0.18 µH/0.17mΩ/FP1008-180-R

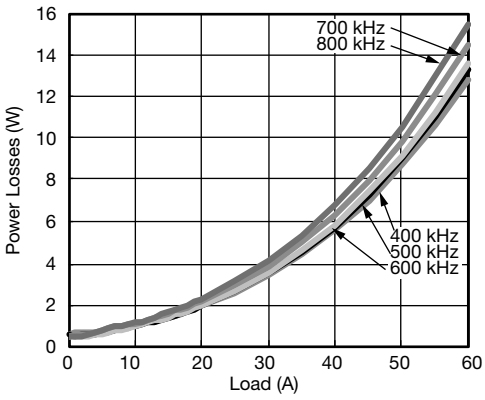


Fig. 12 - Power Dissipation (V_{IN} = 12 V, f_{SW} = 500 kHz; L_{OUT} = 0.18 µH/0.17mΩ/FP1008-180-R

DETAILED OPERATIONAL DESCRIPTION

The SiC645 is an optimized driver and power stage solution for high density synchronous DC/DC power conversion. It includes high performance GH and GL drivers, a NFET controlled to function as a bootstrap diode, and MOSFET pair optimized for high switching frequency buck voltage regulators. It also includes advanced power management features.

1. Accurate current and thermal reporting outputs
2. Fault protections of HFET over-current, HFET short, over-temperature, V_{CC} UVLO, and V_{IN} UVLO

Power-On Reset (POR)

During initial start-up, the V_{CC} voltage rise is monitored. Once the rising V_{CC} voltage exceeds 3.86 V (typical) for 125 µs, then normal operation of the driver is enabled. The PWM signals are passed through to the gate drivers, the T_{MON} output is valid, and the I_{MON} output starts at zero, and becomes valid on the first GL signal. If V_{CC} drops below the falling threshold of 3.58 V (typical), operation of the driver is disabled. The PV_{CC} voltage is not monitored as it should to be from the same supply as V_{CC}.

V_{IN} POR is also monitored. When both V_{CC} and V_{IN} reach above their POR trip points, it enables HFET over-current protection.

Both V_{CC} and V_{IN} POR are gated to the FAULT# pin, which goes high once both V_{CC} and V_{IN} are above their POR levels and no other faults occur.

Shoot-Through Protection

Prior to POR, the undervoltage protection function is activated and both GH and GL are held active low (HFET and LFET off). After POR (the rising thresholds; see electrical specifications), and 125 µs delay, the PWM and LGCTRL signals are used to control both high side and low-side MOSFETs, as shown in Table 1.

SiC645's dead time control is optimized for high efficiency and guarantees that simultaneous conduction of both FETs cannot occur.

Should the driver have no bias voltage applied (either V_{CC} or PV_{CC} missing) and be unable to actively hold the MOSFETs off, an integrated 20 kΩ resistor from the upper MOSFET gate to source will aid in keeping the HFET device in its off state. This can be especially critical in applications where the input voltage rises prior to the SiC645 V_{CC} and PV_{CC} supplies.

TABLE 1 - GH AND GL OPERATION TRUTH TABLE

PWM	LGCTRL	GH	GL	HFET, LFET	COMMENT
Tri-state	X	0	0	Both off	-
0	1	0	1	LFET on	Normal
1	1	1	0	HFET on	Normal
0	0	0	0	LFET off	GL low
1	0	1	0	HFET on	Normal

Tri-State PWM Input

The SiC645A supports a 3.3 V PWM tri-level input, compatible with Vishay's digital multiphase controllers as well as other control IC's utilizing 3.3 V PWM logic. Use the SiC645 for 5 V PWM logic. Should the pin be pulled into and remain in the tri-state window for a set hold off time (~ 25 ns), the driver will force both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.

This feature is utilized by Vishay PWM controllers as a method of forcing both MOSFETs off. Should the PWM input be left floating, the pin will be pulled into the tri-state window internally and thus force both MOSFETs to a safe off state.

Although the PWM input can sustain a voltage as high as V_{CC}, the SiC645 is not compatible with a controller that actively drives its mid-level in tri-state higher than 1.7 V.

Bootstrap Function

The SiC645 features an internal NFET that is controlled to function as a bootstrap diode. A high quality ceramic capacitor should be placed in close proximity across the BOOT and PHASE pins. The bootstrap capacitor can range between 0.1 µF to 0.22 µF (0402 to 0603 and X5R to X7R) for normal buck switching applications.

Current Monitoring

LFET current is monitored and a signal proportional to that current is output on the I_{MON} pin (relative to the REF_{IN} pin). The I_{MON} and REF_{IN} pins should be connected to the appropriate current sense input pin of the controller. This method does not require external R_{SENSE} or DCR sensing of inductor current.

Fig. 13 depicts the low side current sense concept and demonstrates how the accuracy will be defined. After the falling edge of PWM, there are two delays; one that represents the expected propagation delay from PWM to GH/SW, and a second blanking delay to allow time for the transition to settle; typical total time is ~ 350 ns. The I_{MON} output approximates the actual I_L waveform shown within the tolerance band.

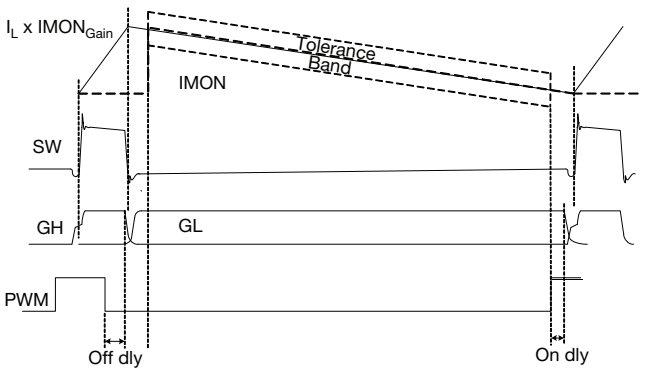


Fig. 13 - LFET Current Sample Diagram

The HFET current is not monitored in the same way, so no valid measured current is available while PWM is high (and the short delays before and after). During this time, the I_{MON} will output the last valid LFET current before the sampling stopped. On start-up after POR, the I_{MON} will output zero (relative to REF_{IN}, which represents zero current) until the switching begins, and then the current can be properly measured.

The high side FET current is separately monitored for OC conditions; see the “over-current protection” section.

Over-Current Protection

Fig. 14 shows the timing diagram of an over-current fault. There is a comparator monitoring the HFET current while it is on (GH high; also requires V_{IN} POR above its trip point). If the current is higher than 90 A (typical; not user-programmable), then an OC fault is detected. The GH will be forced low, even if PWM is still high; this effectively shortens the PWM (and GH) pulse width, to limit the current. The I_{MON} pin is pulled up to REF_{IN} +1.2 V, which will be detected by the controller as an over-current fault. The controller is then expected to force PWM to tri-state (which gates off both FETs) or low state (turns on LFET), either of which signals the SPS that the fault has been acknowledged. This starts a ~ 1 µs fault clear delay. The I_{MON} flag is released after the delay. The driver will then respond to PWM inputs normally.

Note that if the controller does NOT acknowledge, the I_{MON} flag will stay high indefinitely, which will also hold GH low.

If OC is detected, the FAULT# pin is also pulled low; the timing on the FAULT# pin will follow that of the I_{MON} pin.

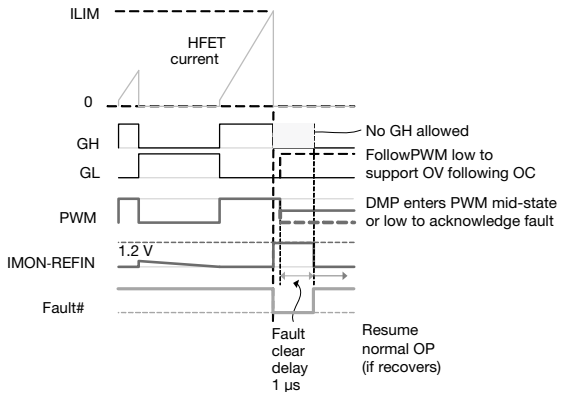


Fig. 14 - Over-current Fault Timing Diagram

Shorted HFET Protection

In the case of a shorted HFET, the SW node will have excessive positive voltage present even when the LFET is turned on. The SiC645 monitors the SW node during periods when the LFET is on (GL is high), and should that voltage exceed 100 mV (typical), the HFET short fault is declared. The SiC645 will pull the I_{MON} pin high, and the FAULT# will be pulled low. But the fault will be latched; V_{CC} POR is needed to reset it. GH will be gated low (ignore PWM = high), but the SiC645 will still respond to PWM tri-state and logic low.

Thermal Monitoring

The SiC645 monitors its internal temperature and provides a signal proportional to that temperature on the T_{MON} pin. T_{MON} has a voltage of 600 mV at 0 °C and reflects temperature at 8 mV/°C. The T_{MON} output is valid 125 µs after V_{CC} POR.

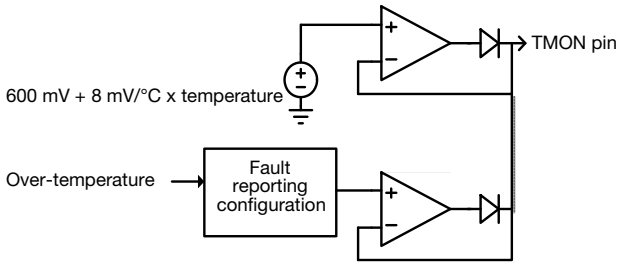


Fig. 15 - Over-Temperature Fault

Fig. 15 shows a simplified functional representation. The top section includes the sensor and the output buffer. The bottom section includes the protection sensing, that will pull the output high. The T_{MON} pin is configured internally such that a user can tie multiple pins together externally and the resulting T_{MON} bus will assume the voltage of the highest contributor (representing the highest temperature).

Thermal Protection

If the internal temperature exceeds the over-temperature trip point (+140 °C typical), the T_{MON} pin is pulled high (to ~2.5 V), and the FAULT# pin is pulled low. No other action is taken on-chip. Both the T_{MON} and FAULT# pins will remain in the fault mode, until the junction temperature drops below +125 °C typical; at that point, the T_{MON} and FAULT# pins resume normal operation; the DMP can detect that the fault condition has gone away, and decide what to do next.

FAULT Reporting

Over-current and shorted HFET detections will pull the I_{MON} pin to a high (fault) level, such that the DMP should quickly recognize it as out of the normal range. Over-temperature detection will pull the T_{MON} pin to a high (fault) level, such that the PWM controller should quickly recognize it as out of the normal range.

All of the above faults, plus the V_{CC} and V_{IN} POR (UVLO) conditions, will also pull down the FAULT# pin. This can be used by the controller (or system) as fault detection, and can also be used to disable the controller, through its enable pin.

The fault reporting and respective SPS response are summarized in Table 2.

TABLE 2 - FAULT REPORTING SUMMARY				
FAULT EVENT	I_{MON}	T_{MON}	FAULT#	RESPONSE
OC	High	n/a	Low	GH gated off. The controller should acknowledge and force its PWM to tri-state to keep both HFET and LFET off. The fault is cleared ~ 1 µs after PWM enters tri-state, otherwise, it stays asserted. (if system OVP occurs, the controller may sen PWM to turn on LEFT)
Shorted HFET	I_{MON} latched high	n/a	FAULT# latched low	GH gated off, until fault latch is cleared by V_{CC} POR. GL follows PWM.
OT	n/a	High	Low	GH and GL follow PWM.
V_{CC} UVLO	I_{MON} - REF_{IN} = 0 V	T_{MON} not valid	Low	Switching stops while in UVLO. Once above V_{CC} POR after 125 µs: GH and GL follow PWM; the FAULT# is released; T_{MON} is valid; I_{MON} - REF_{IN} is valid after GL first goes low.
V_{IN} UVLO	OC not valid	n/a	Low	GH and GL follow PWM.

PCB LAYOUT CONSIDERATIONS

Proper PCB layout will reduce noise coupling to other circuits, improve thermal performance, and maximize the efficiency. The following is meant to lead to an optimized layout:

- Place multiple 10 µF or greater ceramic capacitors directly at device between V_{IN} and P_{GND} as indicated in Fig. 16 This is the most critical decoupling and reduced parasitic inductance in the power switching loop. This will reduce overall electrical stress on the device as well as reduce coupling to other circuits. Best practice is to place the decoupling capacitors on the same PCB side as the device.
  For a design with tight space requirements, these decoupling capacitors can be placed under the device, i.e., bottom layer, as shown in Fig. 18
- Connect GND to the system GND plane with a large via array as close to the GND pins as design rules allow. This improves thermal and electrical performance.
- Place PV_{CC}, V_{CC} and BOOT-PHASE decoupling capacitors at the IC pins as shown in Fig. 16.
- Note that the SW plane connecting the SiC645 and inductor must carry full load current and will create resistive loss if not sized properly. However, it is also a very noisy node that should not be oversized or routed close to any sensitive signals. Best practice is to place the inductor as close to the device as possible and thus minimizing the required area for the SW connection. If one must choose a long route of either the V_{OUT} side of the inductor or the SW side, choose the quiet V_{OUT} side. Best practice is to locate the SiC645 as close to the final load as possible and thus avoid noisy or lossy routes to the load.
- The I_{MON} and IREF network and their vias should not sit on the top of the V_{IN} plane, a keep out area is recommended, as shown in Fig. 18.
- The PCB is the best thermal heatsink material than any top side cooling materials. The PCB always has enough vias to connect V_{IN} and GND planes. Insufficient vias will yield lower efficiency and very poor thermal performance.

Fig. 17 and Fig. 18 show a multiphase PCB layout example.

PCB LAYOUT FOR MINIMIZING CURRENT LOOPS

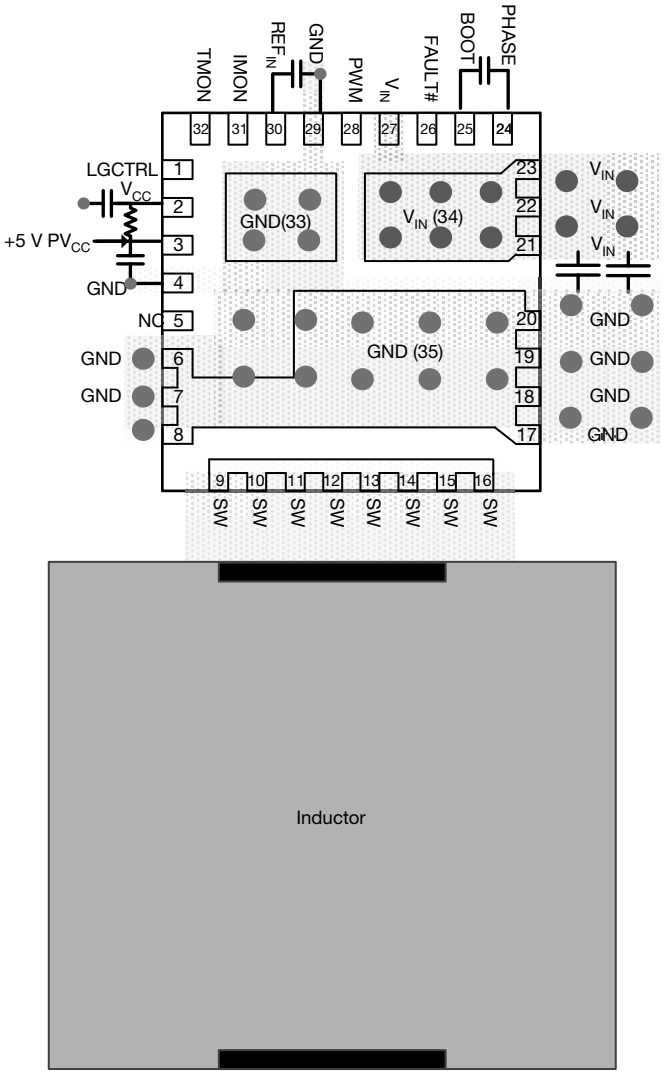


Fig. 16 - Single-Phase PCB Layout for Minimizing Current Loops

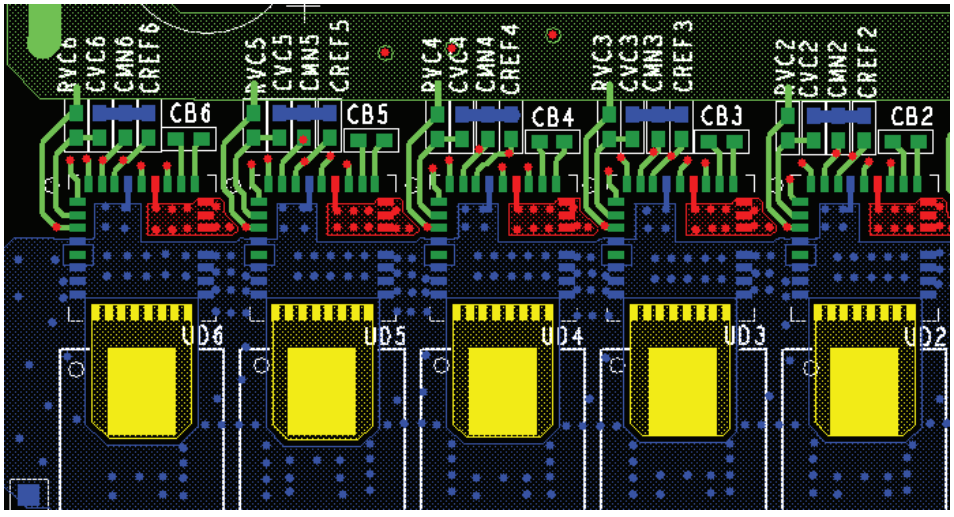


Fig. 17 - Multi-Phase PCB Layout Example Top Layer

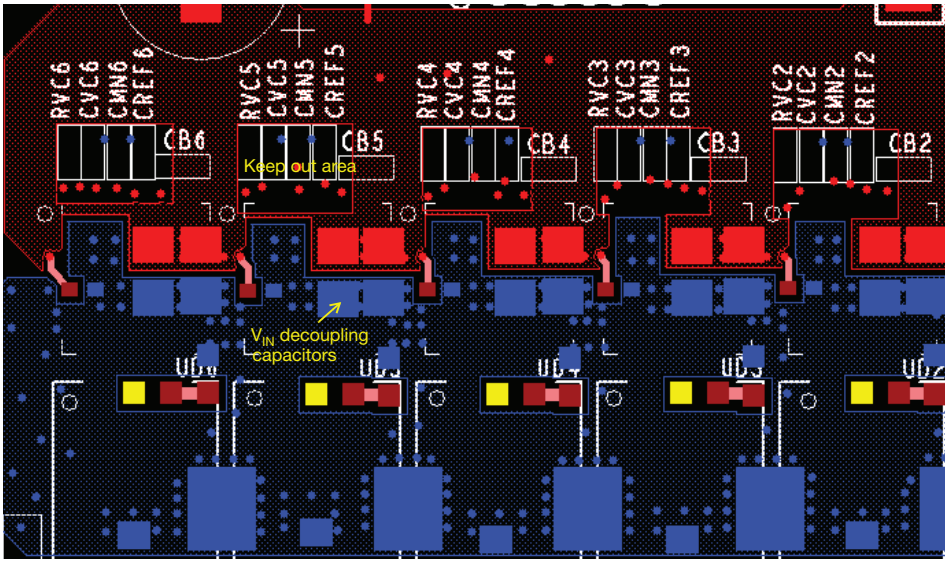


Fig. 18 - Multi-Phase PCB Layout Example Bottom Layer

PRODUCT SUMMARY		
Part number	SiC645	SiC645A
Description	60 A smart power stage, 4.5 V_{IN} to 18 V_{IN}, 5 V PWM with diode emulation mode	60 A smart power stage, 4.5 V_{IN} to 18 V_{IN}, 3.3 V PWM with diode emulation mode
Input voltage min. (V)	4.5	4.5
Input voltage max. (V)	18	18
Continuous current rating max. (A)	60	60
Switch frequency max. (kHz)	2000	2000
Enable (yes / no)	No	No
Monitoring features	I_{MON}, T_{MON}	I_{MON}, T_{MON}
Protection	UVLO, OCP, OTP, HS-short	UVLO, OCP, OTP, HS-short
Light load mode	Diode emulation	Diode emulation
Pulse-width modulation (V)	5	3.3
Package type	PowerPAK MLP55-32L double cooling	PowerPAK MLP55-32L double cooling
Package size (W, L, H) (mm)	5.0 x 5.0 x 0.60	5.0 x 5.0 x 0.60
Status code	2	2
Product type	VRPower (DrMOS)	VRPower (DrMOS)
Applications	Computer, industrial, networking	Computer, industrial, networking

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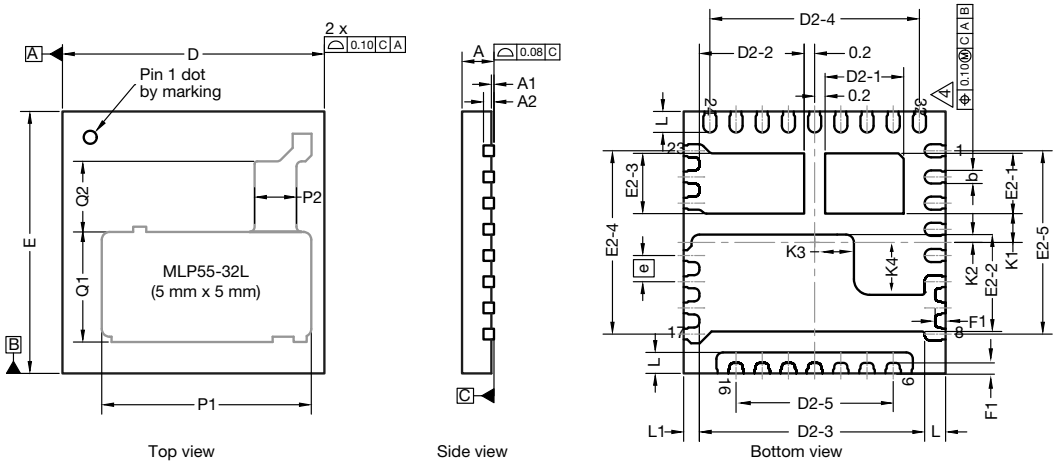
For technical questions, contact: powerictechsupport@vishay.com

PowerPAK® MLP55-32 Double Cooling Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (3)	0.56	0.61	0.66	0.022	0.024	0.026
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (2)	0.20	0.25	0.30	0.008	0.010	0.012
D		5.00 BSC			0.196 BSC	
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.95	2.00	2.05	0.077	0.079	0.081
D2-3	4.25	4.30	4.35	0.167	0.169	0.171
D2-4		4.00 BSC			0.157 BSC	
D2-5		3.50 BSC			0.138 BSC	
e		0.50 BSC			0.020 BSC	
E		5.00 BSC			0.197 BSC	
E2-1	1.10	1.15	1.20	0.043	0.045	0.047
E2-2	1.80	1.85	1.90	0.071	0.073	0.075
E2-3	1.10	1.15	1.20	0.043	0.045	0.047
E2-4		3.50 BSC			0.138 BSC	
E2-5		3.50 BSC			0.138 BSC	
F1	0.15	0.20	0.25	0.006	0.008	0.010
K1		0.55 ref.			0.022 ref.	
K2		0.15 ref.			0.006 ref.	
K3		0.75 ref.			0.030 ref.	
K4		1.00 ref.			0.039 ref.	
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.25	0.30	0.35	0.010	0.012	0.014
P1	3.95	4.00	4.05	0.1555	0.1575	0.1595
P2	0.75	-	1.15	0.030	-	0.045
Q1	2.05	2.10	2.15	0.081	0.083	0.085
Q2	1.30	1.35	1.40	0.051	0.053	0.055
N (1)		31			31	

ECN: T20-0103-Rev. B, 23-Mar-2020
DWG: 6054

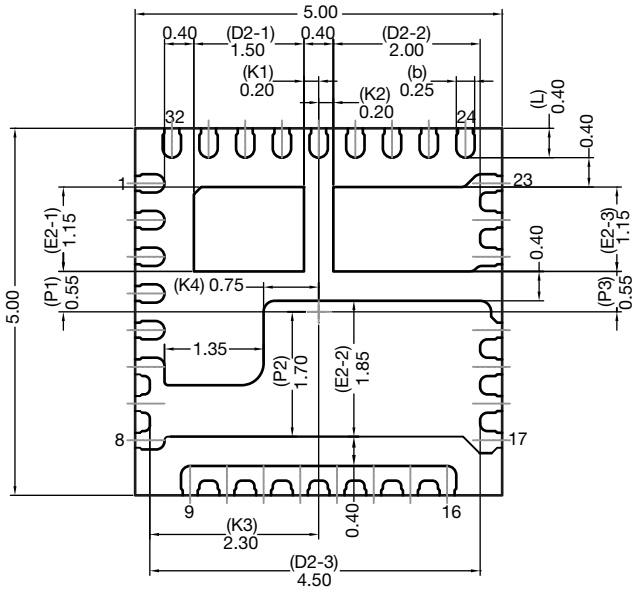
Notes

- Use millimeters as the primary measurement
- Dimensioning and tolerances conform to ASME Y14.5M-1994
- The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- Exact shape and size of this feature is optional
- Package warpage max. 0.08 mm

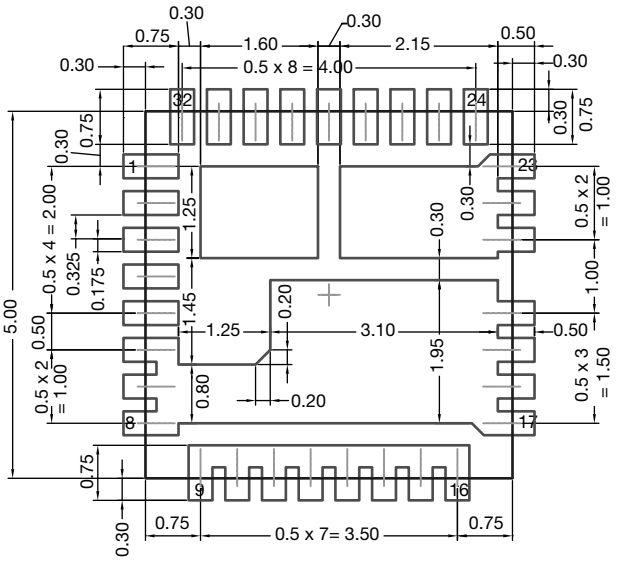
(1) N is the number of terminals. Nd1 and Nd3 is the number of terminals in y-direction. Nd2 and Nd4 is the number of terminals in x-direction
(2) Dimensions b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
(3) Applied only for terminals

Recommended Land Pattern PowerPAK® MLP55-32L

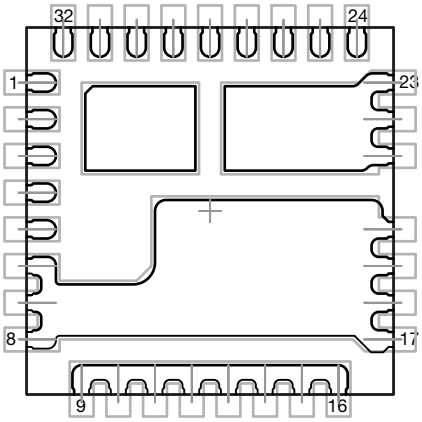
Component for MLP55-32L
Top side transparent view
(no bottom view)



Land pattern for MLP55-32L



Component and land pattern
for MLP55-32L



Component for MLP55-32L

Land pattern for MLP55-32L

All dimensions are in millimeters

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