# XC9248 Series

ETR05022-008

## 18V Driver Transistor Built-In Synchronous Step-Down DC/DC Converter

## ■GENERAL DESCRIPTION

The XC9248 series is 18V bootstrap synchronous step-down DC/DC converter with built-in Nch-Nch driver transistors. With an input voltage range from 4.5V to 18V and a maximum output current of 2.2A, the series is suitable for digital home appliance power supplies and can be used with small ceramic capacitors.

The series has a 0.8V reference voltage, and using externally connected resistors, the output voltage can be set freely from 1.0V to 12V.

The control method is synchronous PWM (Source/ Sink). The soft start time is internally set to 2.8ms (TYP.), also can be adjusted using external capacitor.

With UVLO (Under Voltage Lock Out) function, the internal driver transistors are forced OFF when input voltage falls down below 3.8V (TYP.).

The series includes over current protection, $V_{OUT}$ short-circuit protection, Lx short-circuit protection, $V_{OUT}$ overvoltage protection and thermal shutdown.

## ■APPLICATIONS

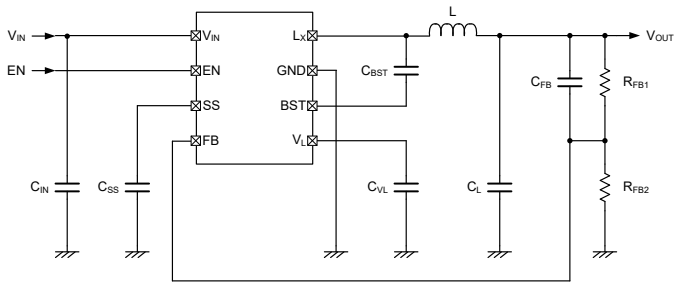
- ●Digital home appliance
- ●Office automation equipment
- ●Note PCs / Tablet PCs
- ●Car accessories power supplies

## ■FEATURES

| | | |
|---|---|---|
| Input Voltage | : | 4.5V ~ 18V |
| Output Voltage | : | 1.0V ~ 12V ($V_{FB}$=0.8V±1.5%) (*1) |
| Output Current | : | 2.2A |
| Efficiency | : | 93.8% (*1) @$V_{IN}$=12V,$V_{OUT}$=5V, $I_{OUT}$=700mA |
| Oscillation Frequency | : | 500kHz |
| Maximum Duty Cycle | : | 79% |
| Soft-Start Time | : | Fixed 2.8ms, set by external capacitor |
| Protection Circuit | : | UVLO |
| | | High side over current protection |
| | | Low side over current protection |
| | | $V_{OUT}$ Short-circuit Protection |
| | | $L_X$ Short-circuit Protection |
| | | $V_{OUT}$ Over voltage protection |
| | | Thermal shutdown |
| Package | : | SOP-8FD |
| Environmentally Friendly | : | EU RoHS Compliant, Pb Free |

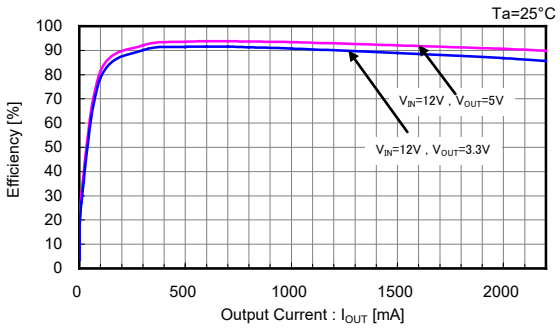
(*1) Performance depends on external components and wiring on the PCB.

## ■TYPICAL APPLICATION CIRCUIT

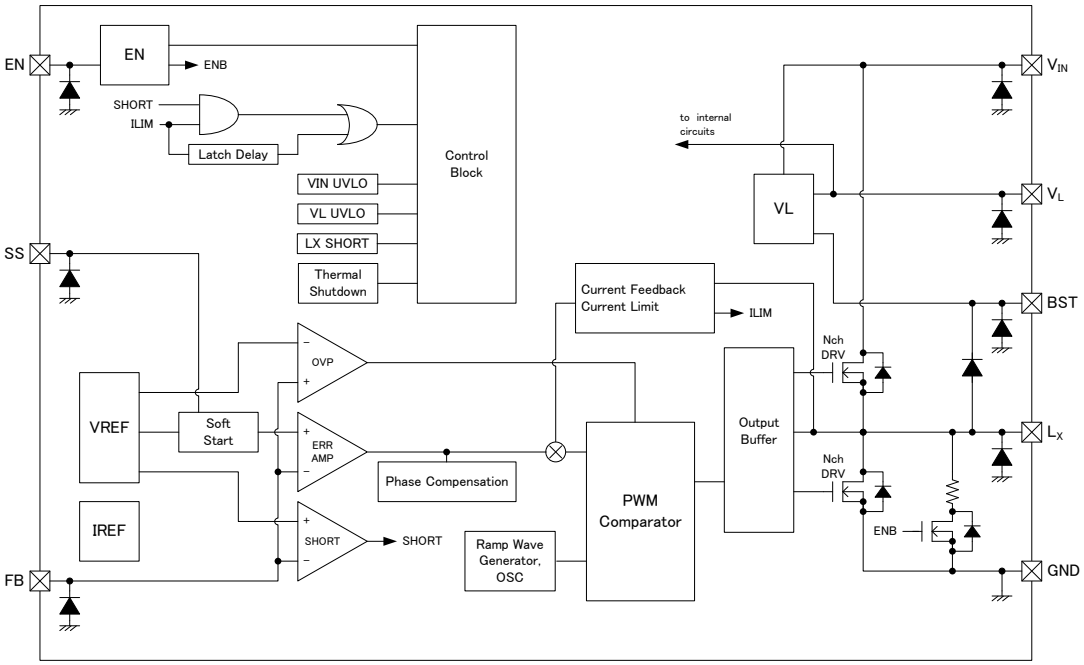



## ■TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs. Output Current



## ■BLOCK DIAGRAM




* Internal diodes include an ESD protection diode and a parasitic diode.

## ■PRODUCT CLASSIFICATION

### ●Ordering Information

XC9248①②③④⑤⑥-⑦

| DESIGNATOR | ITEM | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | TYPE | A | Refer to Selection Guide |
| | | B | |
| ②③ | FB Voltage | 08 | FB voltage is fixed in 0.8V |
| ④ | Oscillation Frequency | 5 | 500kHz |
| ⑤⑥-⑦ (*1) | Package | QR-G | SOP-8FD (1,000pcs/Reel) |

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

### ●Selection Guide

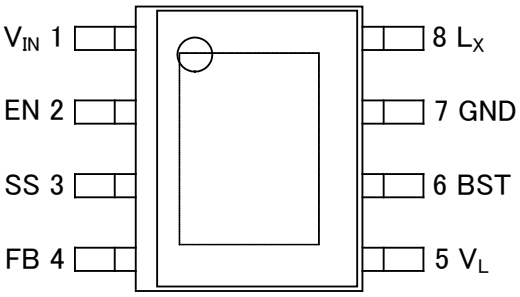
| TYPE | CURRENT LIMITER | LATCH FOR CURRENT LIMITER | LATCH FOR $V_{OUT}$-SHORT | LATCH FOR $L_X$-SHORT (*2) |
|---|---|---|---|---|
| A | YES | YES (*1) | YES | YES |
| B | YES | NO | NO | YES |

| TYPE | ENABLE | UVLO | $C_L$ AUTO-DISCHARGE | THERMAL SHUTDOWN |
|---|---|---|---|---|
| A | YES | YES | YES | YES |
| B | YES | YES | YES | YES |

(*1) The over-current protection latch is an integral latch type.

(*2) To prevent an extremely large rush current from flowing in the event that Lx is short-circuited, both the A & B types have an Lx short protection latch function.

## ■PIN CONFIGURATION




SOP-8FD
(TOP VIEW)

*The dissipation pad for the SOP-8FD package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No.7) pin.

## ■PIN ASSIGNMENT

| PIN NUMBER | PIN NAME | FUNCTIONS |
|---|---|---|
| 1 | $V_{IN}$ | Power Input |
| 2 | EN | Enable |
| 3 | SS | External Soft-start |
| 4 | FB | FB Voltage Monitor |
| 5 | $V_L$ | Internal Regulator Output |
| 6 | BST | Pre Driver Supply |
| 7 | GND | Ground |
| 8 | $L_X$ | Switching Output |

## ■FUNCTION

| PIN NAME | SIGNAL | STATUS |
|---|---|---|
| EN | L | Stand-by |
| | H | Active |
| | OPEN | Undefined State (*1) |

(*1) On the XC9248 series, causes unspecified behavior and thus is prohibited.

## ■ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| $V_{IN}$ Pin Voltage | | $V_{IN}$ | -0.3 ~ 20 | V |
| EN Pin Voltage | | $V_{EN}$ | -0.3 ~ 20 | V |
| $L_X$ Pin Voltage | | $V_{LX}$ | -0.3 ~ $V_{IN}$ + 0.3 or 20 (*1) | V |
| BST Pin Voltage | | $V_{BST}$ | $V_L$ - 0.3 ~ $V_L$ + 20<br>$V_{LX}$ - 0.3 ~ $V_{LX}$ + 5.5 | V |
| $V_L$ Pin Voltage | | $V_{VL}$ | -0.3 ~ $V_{IN}$ + 0.3 or 5.5 (*2) | V |
| FB Pin Voltage | | $V_{FB}$ | -0.3 ~ 5.5 | V |
| SS Pin Voltage | | $V_{SS}$ | -0.3 ~ 5.5 | V |
| $L_X$ Pin Current | | $I_{LX}$ | ±5 | A |
| $V_L$ Pin Current | | $I_{VL}$ | 85 | mA |
| Power Dissipation (Ta=25℃) | SOP-8FD | Pd | 300 | mW |
| | | | 1500 (40mm x 40mm Standard board) (*3) | |
| | | | 2500 (JESD51-7 board)(*3) | |
| Operating Ambient Temperature | | Topr | -40 ~ 105 | °C |
| Storage Temperature | | Tstg | -50 ~ 125 | °C |

All voltages are described based on the ground voltage.

(*1) The maximum value should be either $V_{IN}$+0.3V or 20V in the lowest.

(*2) The maximum value should be either $V_{IN}$+0.3V or 5.5V in the lowest.

(*3) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

# ■ELECTRICAL CHARACTERISTICS

XC9248 Series

Ta=25℃

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{IN}$ | When connected to external components<br>$V_{IN}$ ≦7V: Setup $V_{OUT}$=3.3V<br>$V_{IN}$ >7V: Setup $V_{OUT}$=5V | 4.5 | - | 18 | V | ① |
| FB Voltage | $V_{FB}$ | $V_{FB}$=Sweep (0.812V→0.788V), $V_{SS}$=OPEN | 0.788 | 0.800 | 0.812 | V | ② |
| FB Voltage Temperature Characteristics | VFB/ (VFB･ΔTopr) | -40℃≦Topr≦105℃ | | ±40 | | ppm/℃ | ② |
| Maximum Output Current | $I_{OUTMAX}$ | When connected to external components | 2.2(*1) | - | - | A | ① |
| Supply Current | $I_q$ | $V_{IN}$=$V_{EN}$=18V, $V_{FB}$=0.9V | - | 0.76 | 1.10 | mA | ③ |
| Stand-by Current | $I_{STB}$ | $V_{IN}$=18V, $V_{EN}$=0V, $V_{FB}$=OPEN | - | 38 | 51 | μA | ③ |
| Oscillation Frequency | $f_{OSC}$ | $V_{FB}$=0.7V, $V_{SS}$=OPEN | 450 | 500 | 550 | kHz | ② |
| Maximum Duty Cycle | $D_{max}$ | $V_{FB}$=0.7V, $V_{SS}$=OPEN | 74 | 79 | - | % | ② |
| UVLO Detection Voltage | $V_{UVLOD}$ | $V_{IN}$=Sweep (4.5V→3.5V) , $V_{EN}$=2V, $V_{FB}$=0.9V<br>Voltage when $V_L$ pin changes from<br>"H" level to "L" level (*2) | 3.50 | 3.80 | 4.45 | V | ④ |
| UVLO Release Voltage | $V_{UVLOR}$ | $V_{IN}$=Sweep (3.5V→4.5V), $V_{EN}$=2V, $V_{FB}$=0.9V<br>Voltage when $V_L$ pin changes from<br>"L" level to "H" level (*2) | 3.55 | 3.90 | 4.50 | V | ④ |
| Low side Current Limit | $I_{LIMLS}$ | $V_{OUT}$=4.5V (Forced), Bottom point of $L_X$ pin current | 2.1 | - | - | A | ⑦ |
| Integral Latch Time (Type A) | $t_{LAT}$ | $V_{FB}$=0.9V, $I_{LX}$ = $I_{LIMLS}$<br>Time until SS pin changes from<br>"H" level to "L" level (*2) | 0.4 | 1.1 | 1.8 | ms | ⑤ |
| Internal Soft-start Time | $t_{SS}$ | $V_{IN}$=12V, $V_{EN}$=2V, $V_{FB}$=0.72V, $V_{SS}$=OPEN<br>Time until $L_X$ pin oscillates | - | 2.8 | - | ms | ② |
| SS Terminal Current | $I_{SS}$ | $V_{SS}$=0V, $V_{LX}$=$V_{FB}$=OPEN | 2 | 4 | 6 | μA | ⑥ |
| SS Threshold Voltage | $V_{SSTH}$ | $V_{FB}$=0.72V, $V_{SS}$=OPEN<br>Voltage when $L_X$ pin oscillates | 1.2 | 1.8 | 2.4 | V | ② |
| OVP Detection Voltage | $V_{OVPD}$ | $V_{FB}$=Sweep (0.788V→1.2V), $V_{SS}$=OPEN | - | 0.9 | 1.2 | V | ② |
| Efficiency | EFFI (*3) | Setup $V_{OUT}$=5V, $I_{OUT}$=0.7A<br>When connected to external components | - | 93.8 | - | % | ⑧ |
| Lx SW "H" ON Resistance | $R_{LXH}$ | | - | 0.12(*4) | - | Ω | - |
| Lx SW "L" ON Resistance | $R_{LXL}$ | | - | 0.12(*4) | - | Ω | - |
| EN "H" Voltage | $V_{ENH}$ | $V_{IN}$=12V, $V_{FB}$=0.9V, $V_{EN}$=Sweep (0.2V→1.4V)<br>Voltage when $V_L$ pin changes from<br>"L" level to "H" level (*2) | 1.4 | - | 18 | V | ④ |
| EN "L" Voltage | $V_{ENL}$ | $V_{IN}$=12V, $V_{FB}$=0.9V, $V_{EN}$=Sweep (1.4V→0.2V)<br>Voltage when $V_L$ pin changes from<br>"H" level to "L" level (*2) | GND | - | 0.2 | V | ④ |
| LX "L" Current | $I_{LXL}$ | $V_{IN}$=18V , $V_{EN}$=$V_{LX}$=0V , $V_{FB}$=$V_{SS}$=OPEN | -1 | 0 | - | μA | ⑥ |
| EN "H" Current | $I_{ENH}$ | $V_{IN}$=$V_{EN}$=18V , $V_{LX}$=$V_{FB}$=$V_{SS}$=OPEN | - | 16 | 21 | μA | ⑥ |
| EN "L" Current | $I_{ENL}$ | $V_{IN}$=18V , $V_{EN}$=0V , $V_{LX}$=$V_{FB}$=$V_{SS}$=OPEN | -0.1 | - | 0.1 | μA | ⑥ |
| FB "H" Current | $I_{FBH}$ | $V_{IN}$=18V , $V_{EN}$=0V , $V_{FB}$=5V , $V_{LX}$=$V_{SS}$=OPEN | -0.1 | - | 0.1 | μA | ⑥ |
| FB "L" Current | $I_{FBL}$ | $V_{IN}$=18V , $V_{EN}$=$V_{FB}$=0V , $V_{LX}$=$V_{SS}$=OPEN | -0.1 | - | 0.1 | μA | ⑥ |
| Thermal Shutdown Temperature | $T_{TSD}$ | | - | 150 | - | ℃ | - |
| Hysteresis Width | $T_{HYS}$ | | - | 25 | - | ℃ | - |
| $C_L$ Discharge Resistance | $R_{DCHG}$ | $V_{IN}$=12V , $V_{EN}$=0V , $V_{LX}$=2V , $V_{FB}$=$V_{SS}$=OPEN | - | 300 | - | Ω | ⑥ |
| $C_L$ Discharge Current | $I_{DCHG}$ | $V_{IN}$=12V , $V_{EN}$=0V , $V_{LX}$=12V , $V_{FB}$=$V_{SS}$=OPEN | - | 9 | - | mA | ⑥ |

Unless otherwise stated, $V_{IN}$=$V_{EN}$=12V

(*1) Mount conditions affect heat dissipation. Maximum output current is not guaranteed when Thermal Shutdown starts to operate earlier.

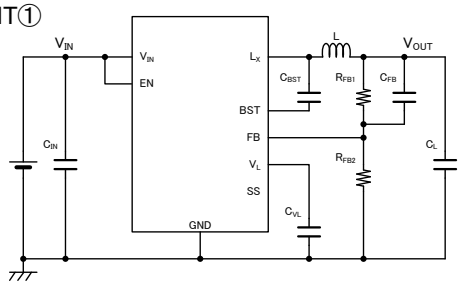
(*2) "H"=4.3V~5V, "L"=-0.1V~0.1V

(*3) EFFI = {[(output voltage)×(output current)]÷[(input voltage)×(input current)]}×100

(*4) Design value

# ■TEST CIRCUITS

## CIRCUIT①

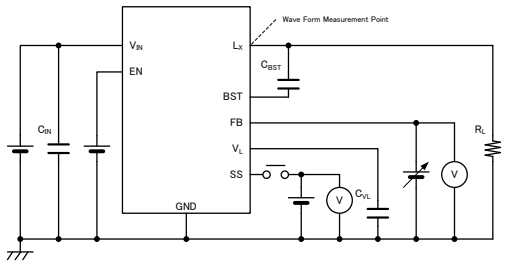



$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)
$C_{BST}$ : 0.1 $\mu$ F(ceramic)
$C_L$ : 22 $\mu$ F 2parallel(ceramic)

Setup $V_{OUT}$ = 3.3V
L : 6.8 $\mu$ H
$R_{FB1}$ : 47k Ω
$R_{FB2}$ : 15k Ω
$C_{FB}$ : 470pF

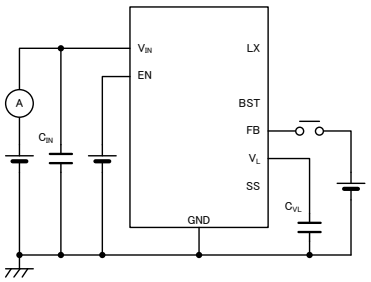
Setup $V_{OUT}$ = 5V
L : 6.8 $\mu$ H
$R_{FB1}$ : 43k Ω
$R_{FB2}$ : 8.2k Ω
$C_{FB}$ : 470pF

## CIRCUIT②



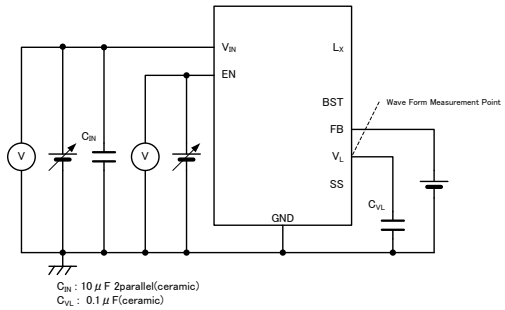

$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)
$C_{BST}$ : 0.1 $\mu$ F(ceramic)
$R_L$ : 300 Ω

## CIRCUIT③



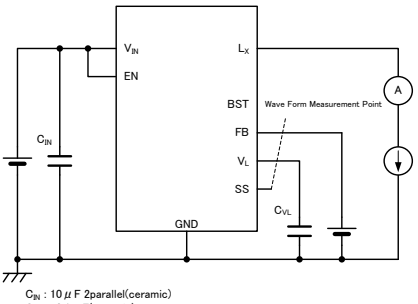

$C_{IN}$ : 1 $\mu$ F(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)

## CIRCUIT④



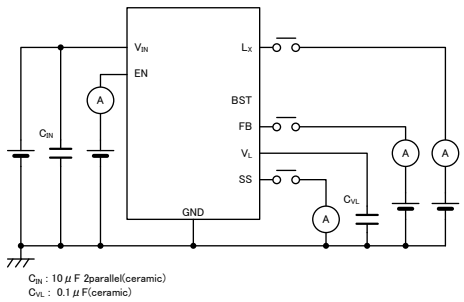

$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)

## CIRCUIT⑤



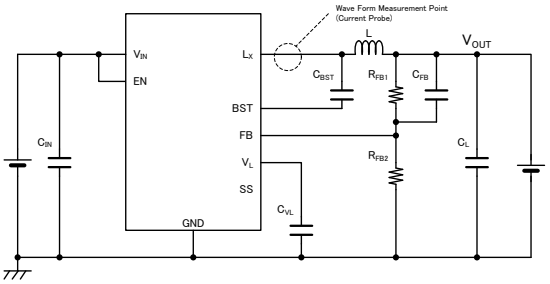

$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)

## CIRCUIT⑥




$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)

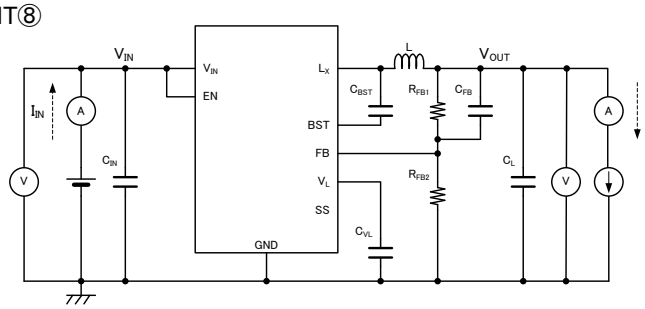
## CIRCUIT⑦




$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)
$C_{BST}$ : 0.1 $\mu$ F(ceramic)
$C_L$ : 22 $\mu$ F 2parallel(ceramic)

L : 6.8 $\mu$ H
$R_{FB1}$ : 43k Ω
$R_{FB2}$ : 8.2k Ω
$C_{FB}$ : 470pF

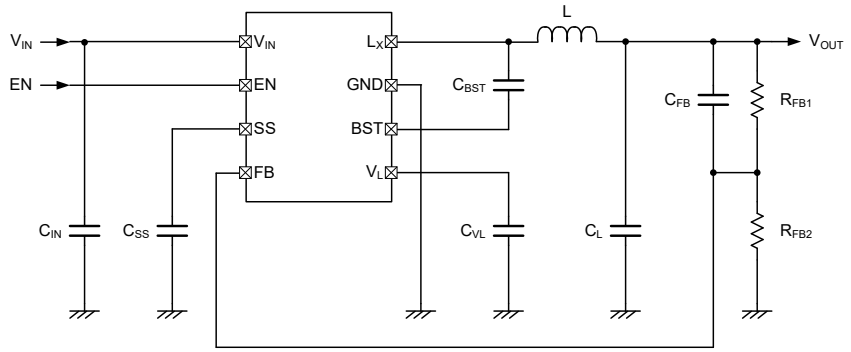
## CIRCUIT⑧




$C_{IN}$ : 10 $\mu$ F 2parallel(ceramic)
$C_{VL}$ : 0.1 $\mu$ F(ceramic)
$C_{BST}$ : 0.1 $\mu$ F(ceramic)
$C_L$ : 22 $\mu$ F 2parallel(ceramic)

L : 6.8 $\mu$ H
$R_{FB1}$ : 43k Ω
$R_{FB2}$ : 8.2k Ω
$C_{FB}$ : 470pF

# ■TYPICAL APPLICATION CIRCUIT




【Typical Examples】

| | MANUFACTURER | PART NUMBER | VALUE |
|---|---|---|---|
| L | TDK | CLF10040T100N | 10 μH |
| | TDK | CLF7045T6R8N | 6.8 μH |
| | TAIYO YUDEN | NR6045T4R5M | 4.5 μH |
| | TAIYO YUDEN | NR6028T2R2N | 2.2 μH |
| $C_{IN}$ (*1) | TDK | C2012X5R1E106K | 10 μF/25V 2parallel |
| | | C3216X7R1E106K | 10 μF/25V 2parallel |
| $C_L$ (*1) | TDK | C2012X5R1A226M | 22 μF/10V 2parallel |
| | | C3216X5R1E226M | 22 μF/25V 2parallel |
| | | C3225X7R1C226M | 22 μF/16V 2parallel |
| | | C4532X7R1E226M | 22 μF/25V 2parallel |
| $C_{SS}$ | | | 0.1 μF (*2)/10V |
| $C_{BST}$ | | | 0.1 μF/10V |
| $C_{VL}$ | | | 0.1 μF/10V |

(*1) Select components appropriate to the usage conditions (ambient temperature, input & output voltage).

(*2) For the capacitance value, please refer to P.8 < External soft-start setting >.

<Coil current setting >

For stable operation by current feedback control, the XC9248 series is optimum when the peak-to-peak current (Ipk) in the coil is set approximately between 0.5A to 1A. The Ipk value can be calculated by using the following equation:

$$Ipk\ [A] = (V_{IN} - V_{OUT}) \times V_{OUT} / V_{IN} / 0.5 / L\ [\mu H]$$

L : Coil Inductance

【Examples】

| $V_{IN}$ [V] | $V_{OUT}$ [V] | L [μH] | Ipk [A] |
|---|---|---|---|
| 5.0 | 1.0 | 2.2 | 0.73 |
| 5.0 | 2.5 | 3.3 | 0.76 |
| 12.0 | 3.3 | 6.8 | 0.70 |
| 12.0 | 5.0 | 6.8 | 0.86 |
| 18.0 | 5.0 | 10.0 | 0.72 |
| 18.0 | 12.0 | 10.0 | 0.80 |

## ■TYPICAL APPLICATION CIRCUIT (Continued)

<$V_{OUT}$ setting>

The output voltage can be set by connecting external dividing resistors. The output voltage is determined by the values of $R_{FB1}$ and $R_{FB2}$ as given in the equation below. The total of $R_{FB1}$ and $R_{FB2}$ should be less than 150kΩ. Output voltage range can be set freely from 1.0V to 12V with a 0.8V reference voltage.

$$V_{OUT}=0.8\times(R_{FB1}+R_{FB2})/R_{FB2}$$

Adjust the value of the phase compensation speed-up capacitor $C_{FB}$ so that $f_{zfp}=1 / (2 \times \pi \times C_{FB} \times R_{FB1})$ is about 7kHz. Adjustments are required from 5kHz to 50kHz depending on the application, value of inductance (L), and value of load capacitance ($C_L$).

【Examples】

$R_{FB1}=47k\Omega$, $R_{FB2}=15k\Omega$, $V_{OUT}=0.8V\times(47k\Omega+15k\Omega) /15k\Omega =3.3V$
$C_{FB}=470pF$, $fzfb=1/(2\times\pi\times470pF\times47k\Omega)=7.2kHz$

< Minimum $V_{OUT}$ >

The Minimum $V_{OUT}$ is set by MINDUTY. The MINDUTY changes by the external inductance(L).
For the L value, please choose the optimal value – see P.7 <Coil current setting>. The Minimum $V_{OUT}$ can be calculated by using the following equation:

$$V_{OUT}= V_{IN} \times MINDUTY / 100$$

【L vs. MINDUTY】

| L [μH] | MINDUTY [%] |
|---|---|
| 2.2 | 18 |
| 3.3 | 20 |
| 4.7 | 21 |
| 6.8 | 21 |
| 10 | 22 |

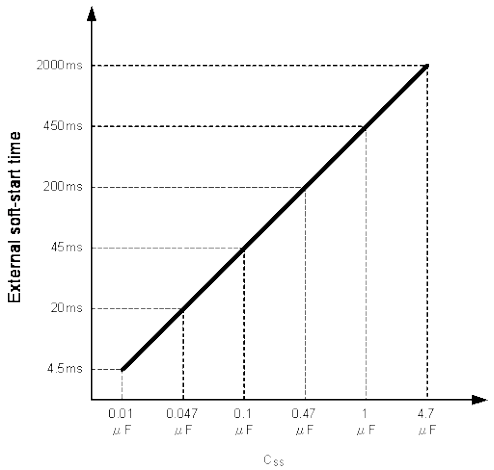
<External soft-start setting>

A capacitor can be connected to the SS pin to set a time longer than the internal soft-start time voluntarily.
By setting the EN pin to the $V_{ENH}$ voltage or higher, a current $I_{SS}$=4 μA (TYP.) flows to the SS pin and charges the capacitor.
When the SS pin voltage attains the SS threshold voltage $V_{SSTH}$=1.8V (TYP.), the output voltage reaches about 90% of the set voltage.
External soft-start can be calculated by using the following equation:

$$External\ soft\text{-}start\ time=V_{SSTH} \times C_{SS} / I_{SS}$$

【Examples】

$C_{SS}=0.1\mu F$, External soft-start time=1.8V × 0.1 μF / 4 μA × 1000=45ms



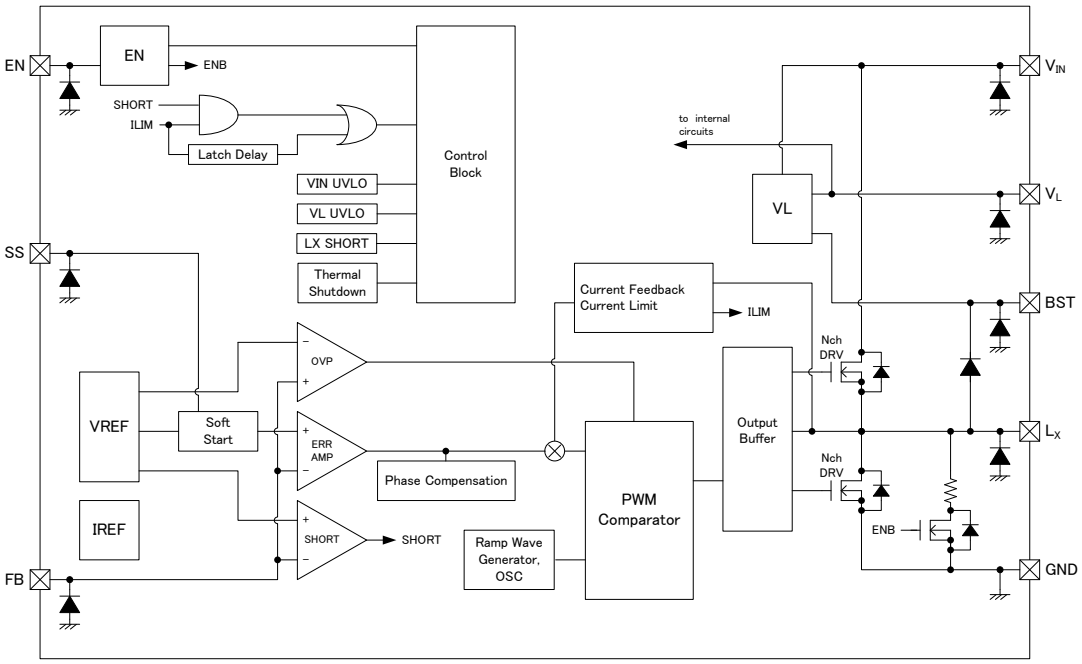
# ■OPERATIONAL EXPLANATION

The XC9248 series consists of a reference voltage source, an internal reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, Nch MOS driver transistor, current limiter circuit, UVLO, short protection circuit, thermal shutdown circuit, over voltage protection and others. (See the block diagram below.)

By using the error amplifier, the FB pin voltage is compared with the internal reference voltage. The signal is input into the PWM comparator to determine the on time of switching. The signal from the error amplifier is compared with the ramp wave from the ramp wave circuit, and the resulting output is delivered to the output buffer circuit to provide on-time of the duty cycle at the LX pin. This process is continuously performed to ensure stable output voltage.

The current feedback circuit monitors the Nch MOS driver transistor current for each switching operation, and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when using a low ESR capacitor such as ceramic, which results in ensuring stable output voltage.

XC9248 Series




<Reference Voltage Source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Ramp Wave Circuit>

The ramp wave circuit determines switching frequency. The frequency is fixed 500kHz internally. Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage. When a voltage lower than the reference voltage is fed back, the output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier output are fixed internally to deliver an optimized signal to the mixer. The error amplifier output signal optimized in the mixer is modulated with the current feedback signal. This signal is delivered to the PWM comparator.

## ■OPERATIONAL EXPLANATION (Continued)

<Current limiting>

The current limiting circuit of the XC9248 series monitors the current that flows through the Low side and High side Nch MOS driver Tr, and when over-current is detected, the current limiting function activates.

① Low side driver current limiting

The current in the Low side driver Tr. is detected to equivalently monitor the bottom value of the coil current.
The Low side driver current limiting function prohibits the High side driver Tr. from turning on in an over-current state where the bottom value of the coil current is higher than the Low side driver current limit value $I_{LIMLS}$.
Control to lower the switching frequency $f_{OSC}$ is also performed. When the over-current state is released, normal operation resumes.

② High side driver current limiting + Low side driver current limiting

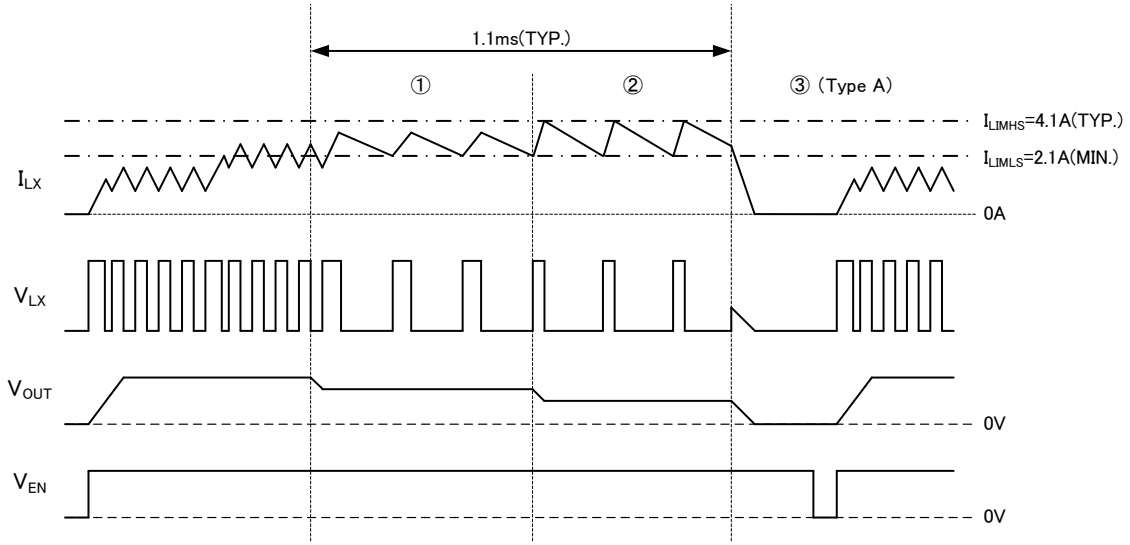
The current in the High side driver Tr. is detected to equivalently monitor the peak value of the coil current.
The High side driver current limiting function forcibly turns off the High side driver Tr. when the peak value of the coil current reaches the High side driver current limit value $I_{LIMHS}$. $I_{LIMLS} < I_{LIMHS}$ is set inside the IC, and therefore the Low side driver current limiting function of ① above also detects the over-current state at this time. When the over-current state is released, normal operation resumes.

③ Over-current latch (Type A)

Type A turns off the High side and Low side driver transistors when state ① or ② continues for 1.1 ms (TYP.). The $L_X$ pin is in the $C_L$ discharged state, and is latch-stopped at the GND level (0V).
The latch-stopped state only stops the pulse output from the $L_x$ pin; the internal circuitry of the IC continues to operate.
To restart after latch-stopping, L level and then H level must be input into the EN pin, or $V_{IN}$ pin re-input must be performed (after lowering the voltage below the UVLO detection voltage) to resume operation by soft start.
The over-current latch function may occasionally be released from the current limit detection state by the effects of ambient noise, and it may also happen that the latch time becomes longer or latching does not take place due to board conditions. For this reason, place the input capacitor as close as possible to the IC.

Type B is an automatic recovery type that performs the operation of ① or ② until the over-current state is released.

Low side driver current limit value $I_{LIMLS}$=2.1A (MIN.)
High side driver current limit value $I_{LIMHS}$=4.1A (TYP.)



# ■OPERATIONAL EXPLANATION (Continued)

<Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function monitors chip temperature. The thermal shutdown circuit starts operating and the Nch MOS driver transistor will be turned off when the chip's temperature reaches 150℃. The $L_X$ pin enters the $C_L$ discharged state and stops functioning at GND level (0V). When the temperature drops to 125℃ or less after shutting of the current flow, the IC performs the soft-start function to initiate output startup operation.

<UVLO Circuit>

When the $V_{IN}$ voltage becomes 3.8V (TYP.) or lower, the Nch MOS driver transistor is forced OFF. The $L_X$ pin enters the $C_L$ discharged state and stops functioning at GND level (0V). When the $V_{IN}$ voltage becomes 3.9V (TYP.) or higher, switching operation takes place. By releasing the UVLO function, the IC performs the soft-start function to initiate output startup operation. The soft-start function operates even when the $V_{IN}$ voltage falls momentarily below the UVLO detect voltage. The UVLO circuit does not cause a complete shutdown of the IC, but causes pulse output to be suspended; therefore, the internal circuitry remains in operation.

<Bootstrap method>

An Nch MOS driver Tr. is used for the High side driver, and a voltage higher than the $V_{IN}$ voltage is needed to turn the driver on. For that purpose, the bootstrap method is used to generate a voltage higher than the $V_{IN}$ voltage. The $C_{BST}$ capacitance is connected between BST and LX, and because the $V_{LX}$ voltage is lower than the 4.6V (TYP.) $V_L$ voltage that is the internal power supply, $C_{BST}$ is charged from $V_L$.

<$V_{OUT}$ short-circuit protection>

With the A type, when the output voltage $V_{OUT}$ is shorted to GND or is near a shorted state (the FB voltage is 1/2 or lower), and a current over the current limit flows to the High side or Low side driver Tr., a $V_{OUT}$ short circuit is detected and the High side and Low side driver Trs. are immediately turned off and latched. The $L_X$ pin enters the $C_L$ discharged state and stops functioning at GND level (0V). Once in the latched state, operation is resumed by either turning the IC off and restarting with the EN pin, or by re-input into the $V_{IN}$ pin (the voltage is lowered below the under-voltage lockout detection voltage once).

<$L_X$ short-circuit protection>

If the event that the $L_X$ pin shorts to GND, $L_X$ short-circuit protection activates for protection from over-current due to rush current and to protect the IC.

If the $L_X$ pin shorts to GND, High side current limiting will activate due to rush current when the High side driver Tr. turns on. The High side driver Tr. turn offs, and the Low side driver Tr. turns on at the same time. At this time, if Low side current limiting did not activate, an $L_X$ short-circuit is detected, and the Low side driver is turned off and latched at the same time as the High side driver Tr. Once in the latched state, operation is resumed by either turning the IC off and restarting with the EN pin, or by re-input into the $V_{IN}$ pin (the voltage is lowered below the under-voltage lockout detection voltage once).

<$V_{OUT}$ over-voltage protection>

To minimize output voltage overshoot, $V_{OUT}$ over-voltage protection activates when $V_{OUT}$ overshoot occurs due to the output resistance changing from a heavy load to a light load or otherwise. When $V_{OUT}$ overshoot occurs and the FB voltage that senses $V_{OUT}$ rises to 0.9V (TYP.) or more, the High side driver Tr. is immediately turned off and the Low side driver Tr. is turned on to prevent $V_{OUT}$ overshoot. When the FB voltage falls to 0.8V (TYP.) or less due to hysteresis, the High side driver Tr. turns on at the next clock cycle.

## ■OPERATIONAL EXPLANATION (Continued)

<$C_L$ high-speed discharge function>

When L level is input into the EN pin and the IC enters the standby state, the charge on the output capacitor $C_L$ can be discharged at high speed with the Nch MOS switch Tr. incorporated between $L_X$ and GND. This enables the prevention of application malfunctioning due to $C_L$ charge remaining when the IC stops.

The $C_L$ discharge time can be calculated from the equation below. Note that the equation varies depending on the set voltage $V_{OUT(E)}$.

(1) Equation when the set voltage $V_{OUT(E)}$ is 1V to 4V.

The $C_L$ discharge time is determined by $C_L$ and $R_{DCHG}$. If the time constant of $C_L$ and $R_{DCHG}$ is $\tau$ ($\tau = C_L \times R_{DCHG}$), the output voltage discharge time can be calculated by using the following equation:

$$V = V_{OUT(E)} \times e^{-t/\tau} \quad \text{or} \quad t = \tau \ln ( V_{OUT(E)} / V )$$

V : Output voltage after discharge
$V_{OUT(E)}$ : Output voltage
t : Discharge time
$\tau$ $C_L \times R_{DCHG}$

(2) Equation when the set voltage $V_{OUT(E)}$ is 4.1V to 12V.

The $C_L$ discharge time is determined by constant current until $V_{OUT(E)}$ is 4 V. When 4V or less, it is determined by $C_L$ and $R_{DCHG}$ as in (1). If $\tau$ ($\tau = C_L \times R_{DCHG}$) is the time constant of $C_L$ and $R_{DCHG}$ and the $C_L$ discharge current is $I_{DCHG}$, the discharge time of the output voltage can be calculated by using the following equation:

$$t = \tau \ln ( 4 / V ) + C_L \times (V_{OUT(E)} - 4) / I_{DCHG}$$

V : Output voltage after discharge
$V_{OUT(E)}$ : Output voltage,
t: Discharge time
$\tau$ $C_L \times R_{DCHG}$
$I_{DCHG}$ : $C_L$ : Discharge time

# ■NOTE ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and typical standard circuit examples of each component when carefully considering which components to select. Be especially careful of the capacitor characteristics and use B characteristics (JIS standard) or X7R, X5R (EIA standard) ceramic capacitors.

3. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current.
Please wire the input capacitor ($C_{IN}$) and the output capacitor ($C_L$) as close to the IC as possible.

4. This IC monitors Peak to Peak current in the coil by means of a Low side driver current limiting circuit and a High side driver current limiting circuit. The Peak to Peak current varies depending on the difference between the input voltage and the output voltage as well as the L value of the coil and thus, in some cases, current limiting may activate too frequently and cause operation to become unstable or the current may not reach the maximum output current.

5. With the A type, when a sharp load fluctuation occurs, the $V_{OUT}$ voltage drop is conveyed directly to the FB pin through $C_{FB}$, and short-circuit protection may activate at a voltage higher than 1/2 the $V_{OUT}$ voltage.

6. The $V_L$ pin is the output of the internal regulator for operation of the DC/DC control block. For stable operation, always connect an external capacitor $C_{VL}$ to the $V_L$ pin. Do not use the $V_L$ pin for external power supply, as it has been optimized as a local power supply.

7. With this IC, operation may become unstable at the minimum operating voltage or less.

8. Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.

9. Torex places an importance on improving our products and their reliability.
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

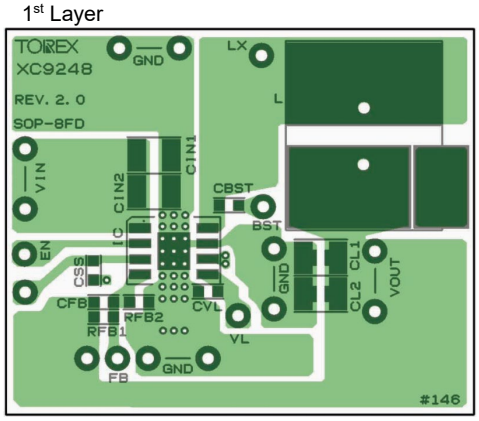
## ■NOTE ON USE (Continued)

10. Instructions for pattern layouts

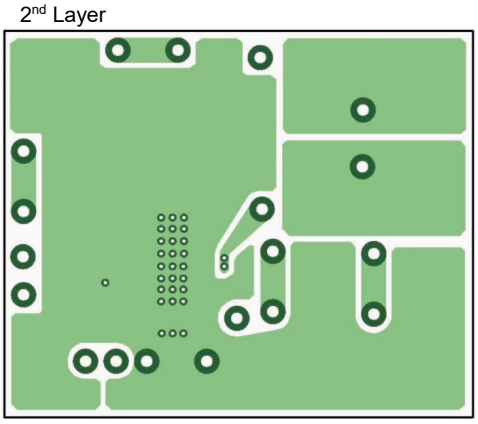
(1) In order to stabilize $V_{IN}$ voltage level, we recommend that a by-pass capacitor ($C_{IN}$) be connected as close as possible to the $V_{IN}$ and GND pins.
(2) Please mount each external component as close to the IC as possible.
(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.
(4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.
(5) Internal driver transistors bring on heat because of the output current ($I_{OUT}$) and ON resistance of the Nch MOS driver transistors.

<Reference Pattern Layout>

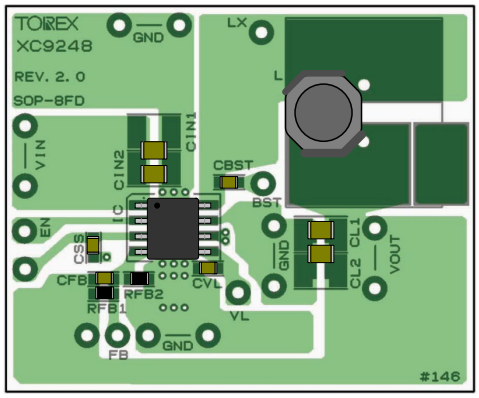
1st Layer




2nd Layer



PCB mounted

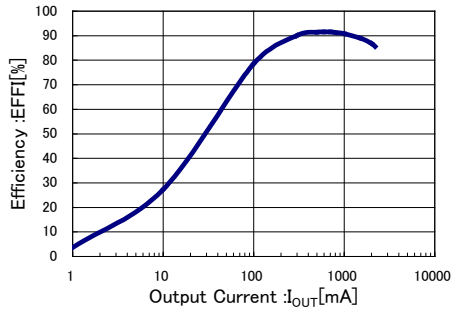


# ■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output current

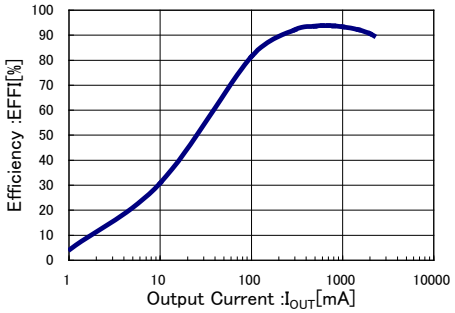
XC9248($V_{IN}$=12V , $V_{OUT}$=3.3V)

L=6.8μF(CLF7045T6R8N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



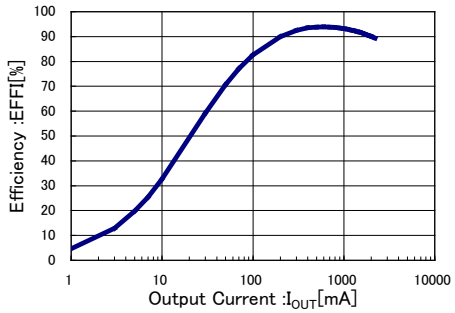

XC9248($V_{IN}$=12V , $V_{OUT}$=5V)

L=6.8μF(CLF7045T6R8N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



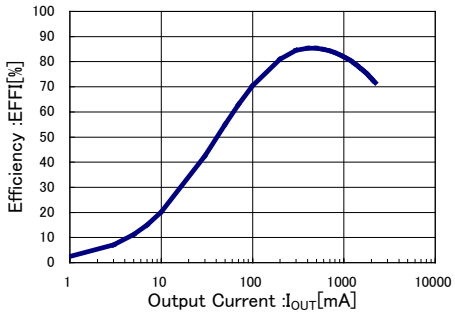

XC9248($V_{IN}$=9V , $V_{OUT}$=4V)

L=4.5μF(NR6045T4R5M)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)




XC9248($V_{IN}$=5V , $V_{OUT}$=1V)

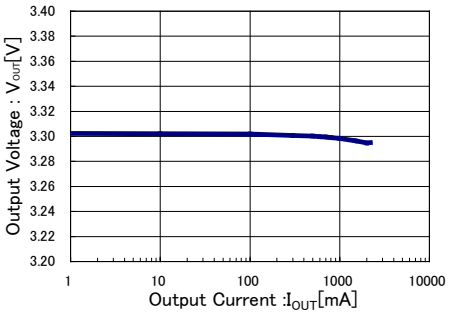
L=2.2μF(NR6028T2R2N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)




(2) Output Voltage vs. Output Currnt

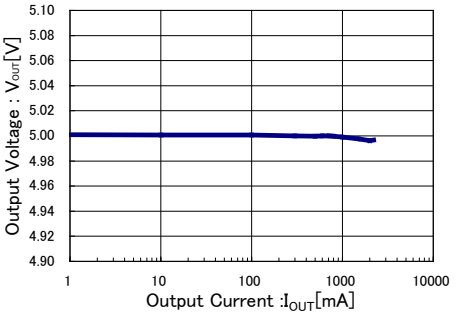
XC9248($V_{IN}$=12V , $V_{OUT}$=3.3V)

L=6.8μF(CLF7045T6R8N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



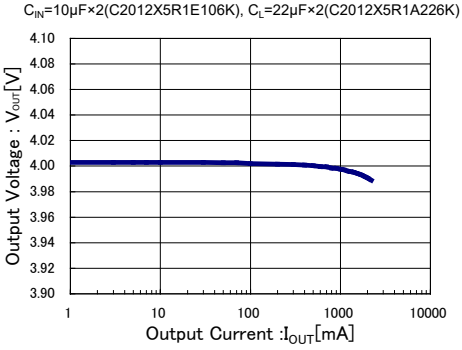

XC9248($V_{IN}$=12V , $V_{OUT}$=5V)

L=6.8μF(CLF7045T6R8N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



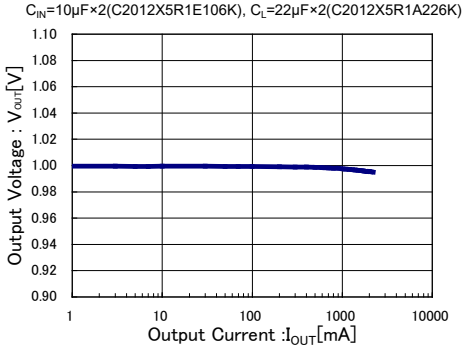

XC9248($V_{IN}$=9V , $V_{OUT}$=4V)

L=4.5μF(NR6045T4R5M)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)




XC9248($V_{IN}$=5V , $V_{OUT}$=1V)

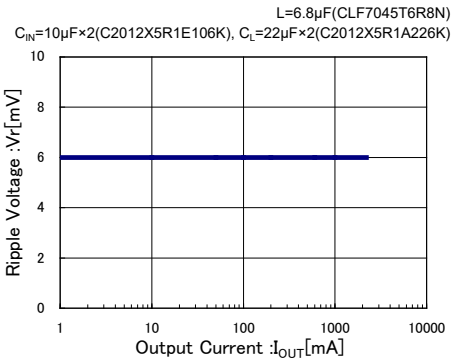
L=2.2μF(NR6028T2R2N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



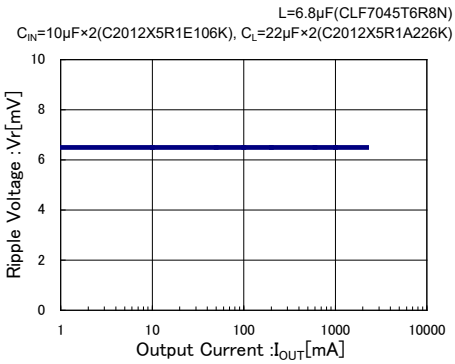
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(3) Ripple Voltage vs. Output Current

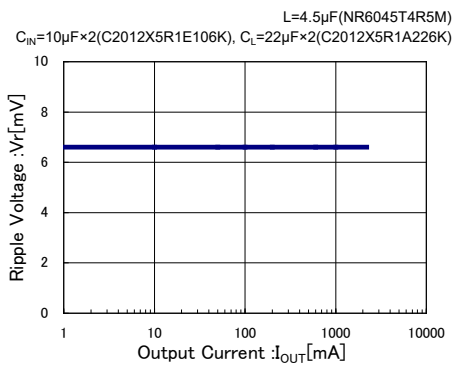
XC9248($V_{IN}$=12V , $V_{OUT}$=3.3V)



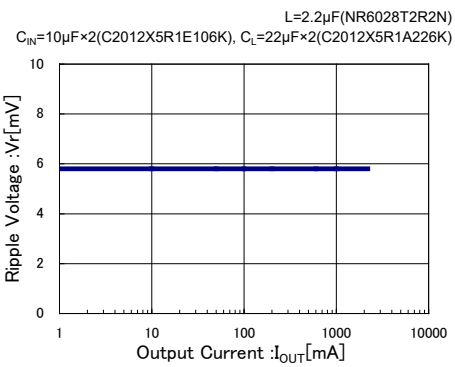

XC9248($V_{IN}$=12V , $V_{OUT}$=5V)




XC9248(VIN=9V , VOUT=4V)

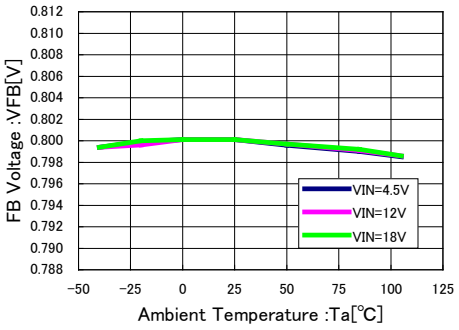



XC9248(VIN=5V , VOUT=1V)



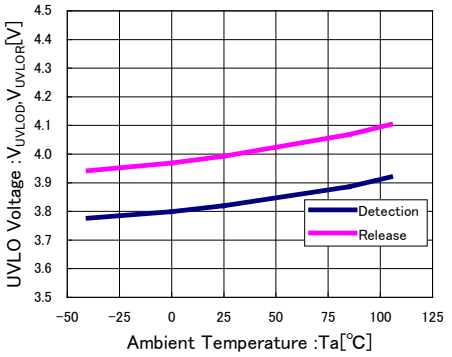

(4) FB Voltage vs. Ambient Temperature

XC9248



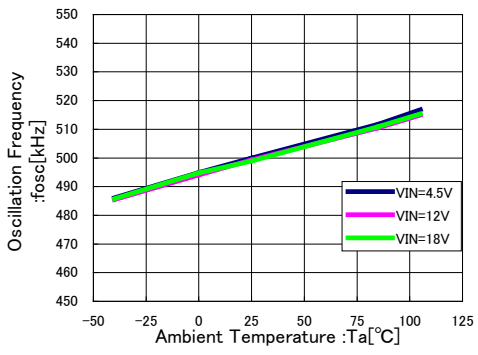

(5) UVLO Voltage vs. Ambient Temperature

XC9248



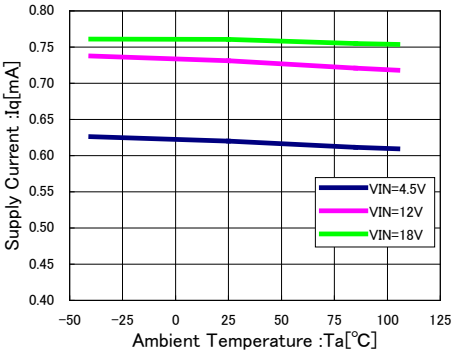

(6) Oscillation Frequency vs. Ambient Temperature

XC9248



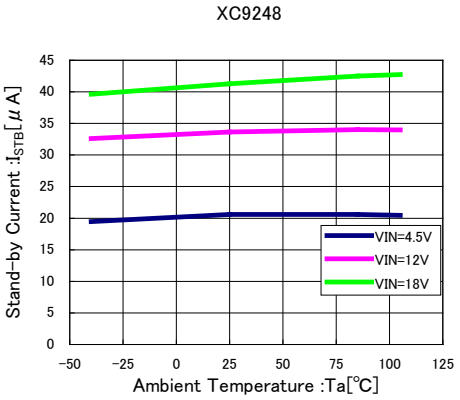

(7) Supply Current vs. Ambient Temperature

XC9248

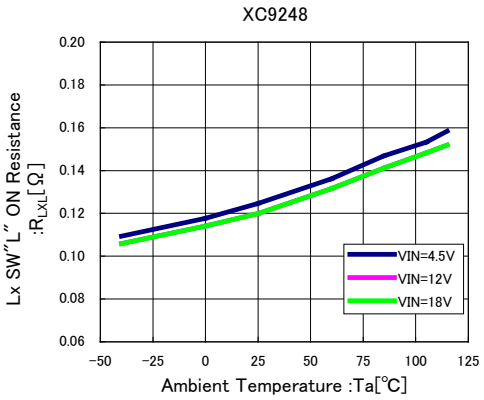


# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

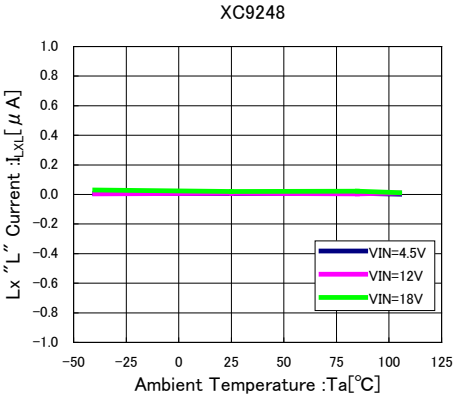
(8) Stand-by Current vs. Ambient Temperature



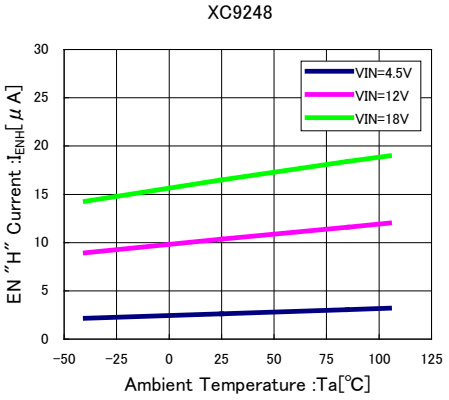

(9) Lx SW"L" ON Resistance vs. Ambient Temperature



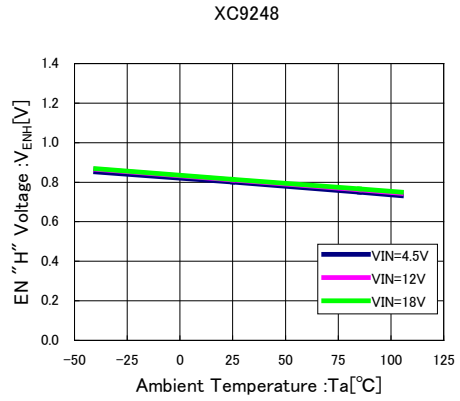

(10) Lx "L" Current vs. Ambient Temperature



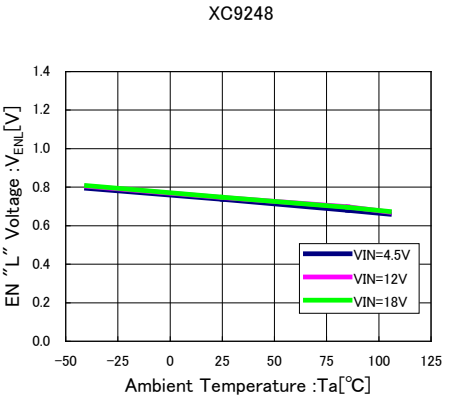

(11) EN "H" Current vs. Ambient Temperature



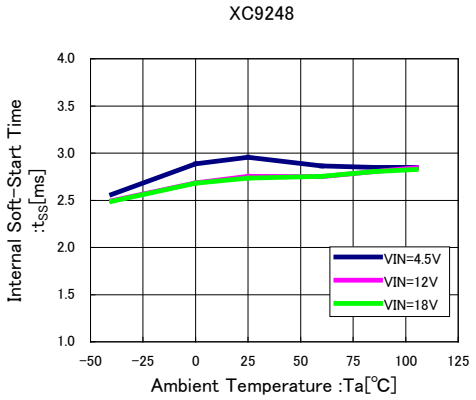

(12) EN "H" Voltage vs. Ambient Temperature



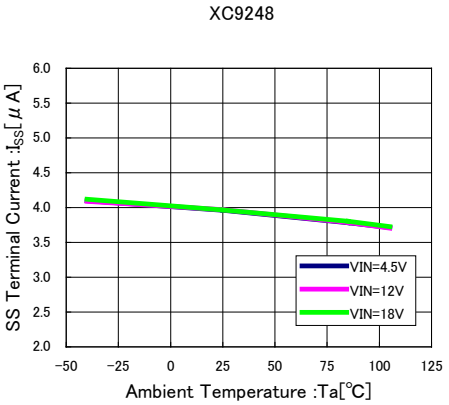

(13) EN "L" Voltage vs. Ambient Temperature




(14) Internal Soft-Start Time vs. Ambient Temperature



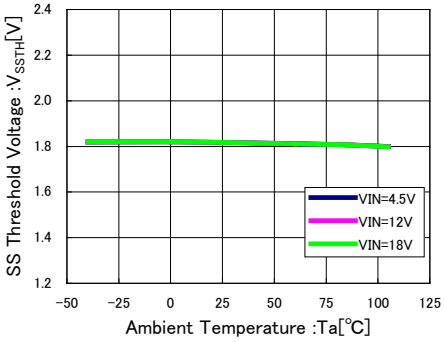

(15) SS Terminal Current vs. Ambient Temperature



# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

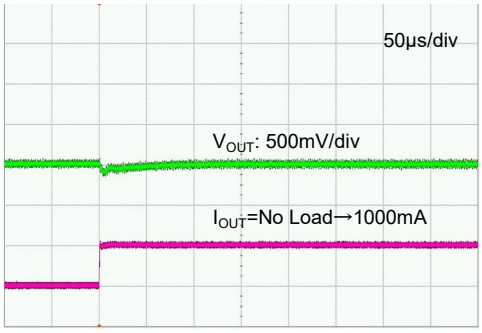
(16) SS Threshold Voltage vs. Ambient Temperature

XC9248

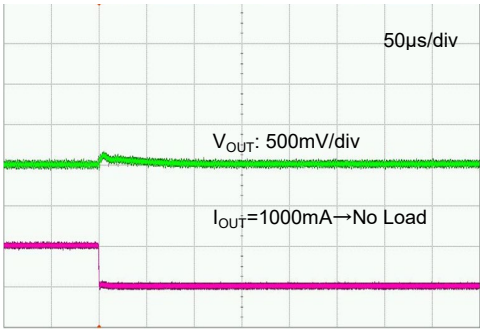



(17) Load Transient Response

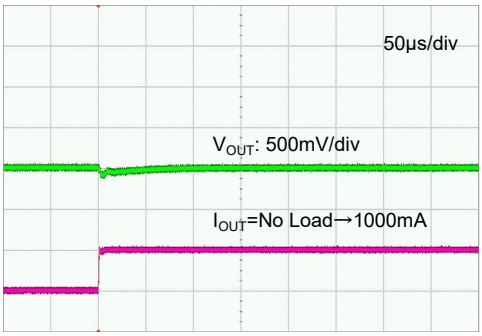
XC9248
$V_{IN}$=12V, $V_{OUT}$=3.3V, $I_{OUT}$=No Load→1000mA
L=6.8μF(CLF7045T6R8N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



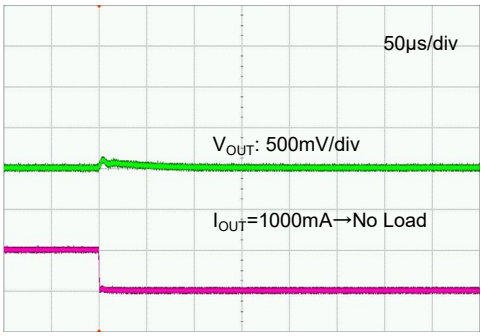

XC9248
$V_{IN}$=12V, $V_{OUT}$=3.3V, $I_{OUT}$=1000mA→No Load
L=6.8μF(CLF7045T6R8N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



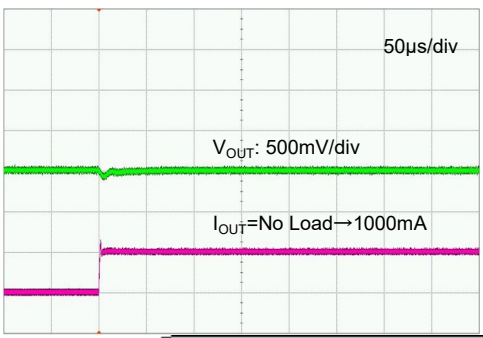

XC9248
$V_{IN}$=9V, $V_{OUT}$=4V, $I_{OUT}$=No Load→1000mA
L=4.5μF(NR6045T4R5M)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



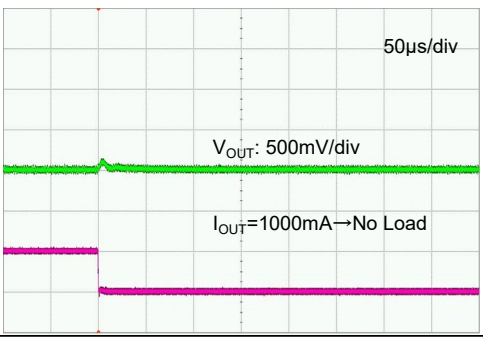

XC9248
$V_{IN}$=9V, $V_{OUT}$=4V, $I_{OUT}$=1000mA→No Load
L=4.5μF(NR6045T4R5M)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)




XC9248
$V_{IN}$=5V, $V_{OUT}$=1V, $I_{OUT}$=No Load→1000mA
L=2.2μF(NR6028T2R2N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)




XC9248
$V_{IN}$=5V, $V_{OUT}$=1V, $I_{OUT}$=1000mA→No Load
L=2.2μF(NR6028T2R2N)
$C_{IN}$=10μF×2(C2012X5R1E106K), $C_L$=22μF×2(C2012X5R1A226K)



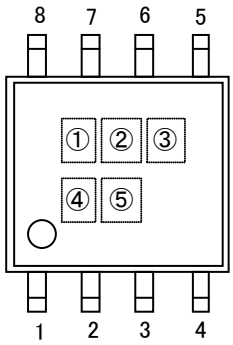
# ■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

| PACKAGE | OUTLINE / LAND PATTERN | THERMAL CHARACTERISTICS | |
|---|---|---|---|
| SOP-8FD | SOP-8FD PKG | Standard Board | SOP-8FD Power Dissipation |
| | | JESD51-7 Board | |

## ■MARKING RULE

SOP−8FD




① represents products series

| MARK | PRODUCT SERIES |
|---|---|
| B | XC9248******-G |

② represents products type

| MARK | PRODUCT SERIES |
|---|---|
| A | XC9248A*****-G |
| B | XC9248B*****-G |

③ represents FB voltage and oscillation frequency

| MARK | VOLTAGE (V) | OSCILLATION FREQUENCY | PRODUCT SERIES |
|---|---|---|---|
| 5 | 0.8 | 500kHz | XC9248*085**-G |

④⑤ represents production lot number
01～09、0A～0Z、11～9Z、A1～A9、AA～AZ、B1～ZZ in order.
(G, I, J, O, Q, W excluded)
* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9. 

TOREX SEMICONDUCTOR LTD.