

## 85mΩ High Function Power Switch

## ■ GENERAL DESCRIPTION

The XC8108 series is a P-channel MOSFET power switch IC with a low ON resistance. A current limit, reverse current prevention (prevents reverse current from  $V_{OUT}$  to  $V_{IN}$ ), soft start, thermal shutdown, and an under voltage lockout (UVLO) are incorporated as protective functions. A flag function monitors the power switch status. The flag output has N-channel open drain structure, and outputs Low level signal while over-current or overheating is detected, or while the reverse current prevention is operated.

A variable current limiting function is integrated, allowing the current limit value to be set, using an external resistor. The voltage level which is fed to CE pin determines the status of XC8108. The logic level of CE pin is selectable between either one of active high or active low.

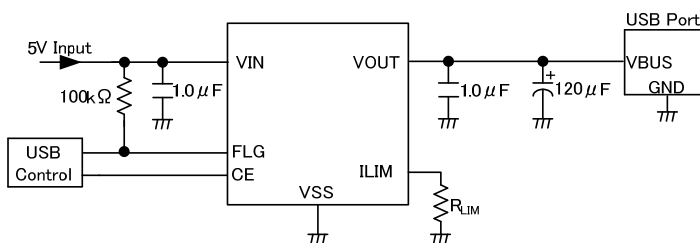
## ■ APPLICATIONS

- Set Top Boxes
- Digital TVs
- PCs
- USB Ports/USB Hubs
- HDMI

## ■ FEATURES

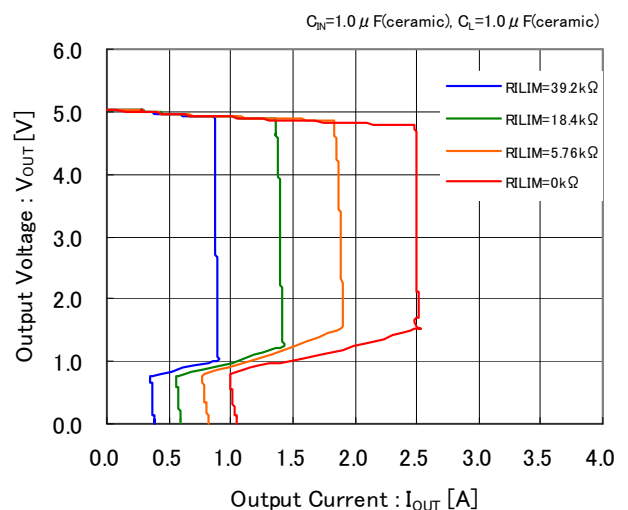
Input Voltage	: 2.5V~5.5V
Maximum Output Current	: 2A
ON Resistance	: 85mΩ@ $V_{IN}=5.0V$ (TYP.)
Supply Current	: 40 $\mu A$ @ $V_{IN}=5.0V$
Stand-by Current	: 0.1 $\mu A$ (TYP.)
Flag Delay Time	: 7.5ms (TYP.)
	* At over-current detection
	: 4ms (TYP.)
	* At reverse voltage detection
Protection Circuit	: Reverse Current Prevention
	: 0.9A~2.4A(TYP.)
	Thermal Shutdown
	Under Voltage Lockout(UVLO)
	Soft-start
Functions	: Flag Output
	CE Pin Input Logic Selectable
Current Limit Response Time	: 2 $\mu s$ (TYP.) *Reference value
Operating Ambient Temperature	: -40°C~+105°C
Packages	: USP-6C
Environmentally Friendly	: EU RoHS Compliant, Pb Free

## ■ TYPICAL APPLICATION CIRCUIT

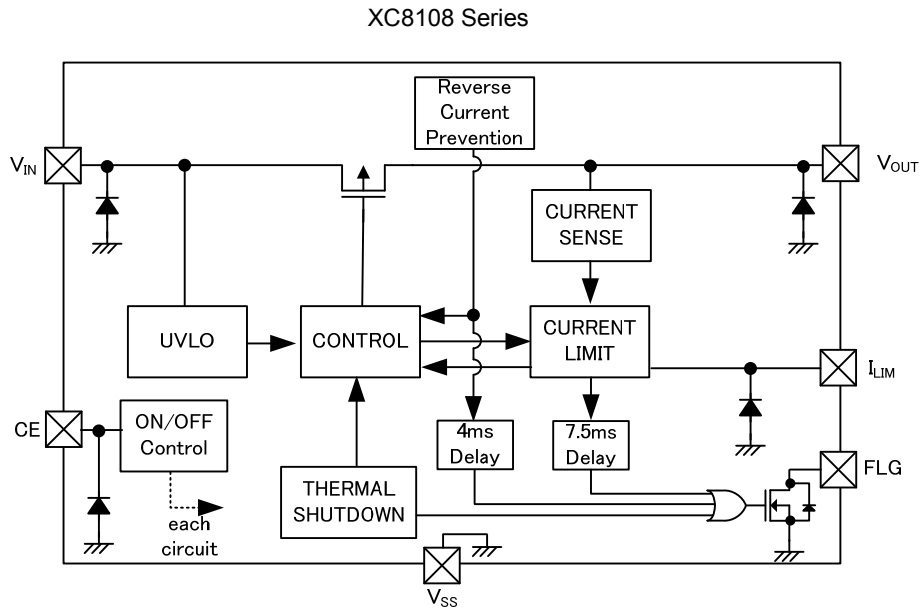


## ■ TYPICAL PERFORMANCE CHARACTERISTICS

XC8108xC20ER



## ■ BLOCK DIAGRAM



\* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

## ■ PRODUCT CLASSIFICATION

### ● Ordering Information

XC8108①②③④⑤⑥-⑦

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	CE Logic	A	Refer to Selection Guide
		B	
②	Protection Circuits Type	C	
		D	
③④	Maximum Output Current	20	2.0A (Adjustable current limit range: 900mA~2400mA)
⑤⑥-⑦ (*1)	Package (Order Unit)	ER-G	USP-6C (3,000pcs/Reel)

(\*1) The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

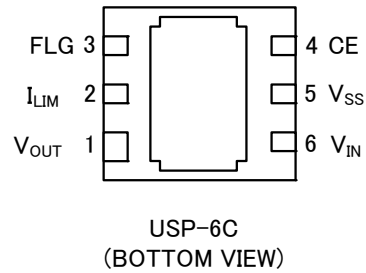
### ● Selection Guide

TYPE	CE LOGIC SELECTABLE	SOFT-START	CURRENT LIMIT ADJUSTABLE
AC	Active High	Yes	Yes
AD	Active High	Yes	Yes
BC	Active Low	Yes	Yes
BD	Active Low	Yes	Yes

TYPE	UVLO	FLG OUTPUT	REVERSE CURRENT PREVENTION
AC	Yes	Yes	Yes
AD	Yes	Yes	Yes
BC	Yes	Yes	Yes
BD	Yes	Yes	Yes

TYPE	THERMAL SHUT DOWN	LATCH PROTECTION
AC	Yes	No
AD	Yes	Yes
BC	Yes	No
BD	Yes	Yes

## ■ PIN CONFIGURATION



\* The dissipation pad for the USP-6C packages should be solder-plated for mounting strength and heat dissipation. Please refer to the reference mount pattern and metal masking. The dissipation pad should be connected to the  $V_{SS}$  (No. 5) pin.

## ■ PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
USP-6C		
1	$V_{OUT}$	Output
2	$I_{LIM}$	Current Limit Adjustment
3	FLG	Fault Report
4	CE	ON/OFF Control
5	$V_{SS}$	Ground
6	$V_{IN}$	Power Input

## ■ FUNCTION

TYPE	PIN NAME	SIGNAL	STATUS
A	CE	H	Active
		L	Stand-by
		OPEN	Undefined State (*1)
B		H	Stand-by
		L	Active
		OPEN	Undefined State (*1)

\* Avoid leaving the CE pin open; set to any fixed voltage.

## ■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V <sub>IN</sub>	-0.3~+6.0	V
Output Voltage		V <sub>OUT</sub>	-0.3~+6.0	V
Output Current		I <sub>OUT</sub>	2.8	A
CE Input Voltage		V <sub>CE</sub>	-0.3~+6.0	V
FLG Pin Voltage		V <sub>FLG</sub>	-0.3~+6.0	V
FLG Pin Current		I <sub>FLG</sub>	15	mA
I <sub>LIM</sub> Pin Voltage		V <sub>LIM</sub>	-0.3~+6.0	V
I <sub>LIM</sub> Pin Current		I <sub>LIM</sub>	±1	mA
Power Dissipation	USP-6C	Pd	120	mW
			1000 (40mm x 40mm Standard board) <sup>(*)2</sup>	
			1250 (JEDEC board) <sup>(*)2</sup>	
Operating Ambient Temperature		Topr	-40~+105	°C
Storage Temperature		Tstg	-55~+125	°C

\* All voltages are described based on the V<sub>SS</sub>.

(\*)1 Use with I<sub>OUT</sub> less than Pd/(V<sub>IN</sub>-V<sub>OUT</sub>).

(\*)2 This is a reference data taken by using the test board. Please see the power dissipation page for the mounting condition.

## ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V <sub>IN</sub>	-	2.5	-	5.5	V	①
On Resistance	R <sub>ON</sub>	V <sub>IN</sub> =3.3V, I <sub>OUT</sub> =1.0A	-	100	110	mΩ	①
		V <sub>IN</sub> =5.0V, I <sub>OUT</sub> =1.0A	-	85	104	mΩ	
Supply Current	I <sub>SS</sub>	V <sub>OUT</sub> =OPEN	-	40	75	μA	②
Stand-by Current	I <sub>STBY</sub>	V <sub>IN</sub> =5.5V, V <sub>OUT</sub> =OPEN V <sub>CE</sub> =V <sub>SS</sub> (XC8108A series) V <sub>CE</sub> =V <sub>IN</sub> (XC8108B series)	-	0.01	1.0	μA	②
Switch Leakage Current	I <sub>LEAK</sub>	V <sub>IN</sub> =5.5V, V <sub>OUT</sub> =0V V <sub>CE</sub> =V <sub>SS</sub> (XC8108A series) V <sub>CE</sub> =V <sub>IN</sub> (XC8108B series)	-	0.01	1.0	μA	②
Current Limit	I <sub>LIMIT</sub>	V <sub>OUT</sub> =V <sub>IN</sub> -0.3V I <sub>LIMIT</sub> shorted to V <sub>SS</sub>	2.16	2.40	2.64	A	①
		V <sub>OUT</sub> =V <sub>IN</sub> -0.3V R <sub>LIMIT</sub> =18.4kΩ	1.16	1.34	1.52		
Short-Circuit Current	I <sub>SHORT</sub>	V <sub>OUT</sub> =0V I <sub>LIMIT</sub> shorted to V <sub>SS</sub>	-	1.20	-	A	①
		V <sub>OUT</sub> =0V R <sub>LIMIT</sub> =18.4kΩ	-	0.67	-		
Current Limit Circuit Response Time <sup>(*)</sup>	t <sub>CLR</sub>	V <sub>IN</sub> =5.0V, V <sub>OUT</sub> : OPEN→0V Measure from V <sub>OUT</sub> =0V to when current falls below a certain I <sub>LIMIT</sub> value	-	2.0	-	μs	①
CE "H" Level Voltage	V <sub>CEH</sub>	V <sub>IN</sub> =5.5V, XC8108A series	1.5	-	5.5	V	①
		V <sub>IN</sub> =5.5V, XC8108B series	-	-	0.8		
CE "L" Level Voltage	V <sub>CEL</sub>	V <sub>IN</sub> =5.5V, XC8108A series	-	-	0.8	V	①
		V <sub>IN</sub> =5.5V, XC8108B series	1.5	-	5.5		
CE "H" Level Current	I <sub>CEH</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =5.5V	-0.1	-	0.1	μA	①
CE "L" Level Current	I <sub>CEL</sub>	V <sub>IN</sub> =5.5V, V <sub>CE</sub> =0V	-0.1	-	0.1	μA	①
UVLO Detected Voltage	V <sub>UVLOD</sub>	V <sub>IN</sub> : 2.2V→1.7V	1.8	1.9	2.0	V	①
UVLO Released Voltage	V <sub>UVLOR</sub>	V <sub>IN</sub> : 1.7V→2.2V	1.9	2.0	2.1	V	①
UVLO Hysteresis	V <sub>UHYS</sub>	-	-	0.1	-	V	①

**NOTE:**

Unless otherwise stated, V<sub>IN</sub>=5.0V, I<sub>OUT</sub>=1mA, I<sub>LIMIT</sub>=V<sub>SS</sub>, V<sub>CE</sub>=V<sub>IN</sub> (XC8108A series) or V<sub>CE</sub>=V<sub>SS</sub> (XC8108B series)

<sup>(\*)</sup> Design reference value. This parameter is provided only for reference.

## ■ ELECTRICAL CHARACTERISTICS (Continued)

Ta=25°C

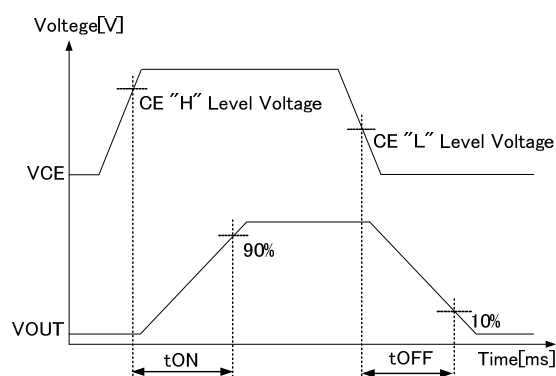
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
turn-on time	t <sub>ON</sub>	R <sub>LOAD</sub> =10Ω, V <sub>CE</sub> =0V→2.2V	-	0.60	1.00	ms	①
turn-off time	t <sub>OFF</sub>	R <sub>LOAD</sub> =10Ω, V <sub>CE</sub> =2.2V→0V	-	0.08	0.13	ms	①
FLG output FET On-resistance	R <sub>FLG</sub>	I <sub>FLG</sub> =10mA, V <sub>OUT</sub> =5.5V	-	15	20	Ω	③
FLG output FET Leakage Current	I <sub>FOFF</sub>	V <sub>IN</sub> =5.5V, V <sub>FLG</sub> =5.5V, V <sub>OUT</sub> =OPEN	-	0.01	0.1	μA	③
FLG delay time	t <sub>FD1</sub>	over-current condition	6.5	7.5	8.5	ms	①
	t <sub>FD2</sub>	reverse-voltage condition	2.7	4.0	4.7	ms	①
Reverse Current	I <sub>REV</sub>	V <sub>IN</sub> =0V, V <sub>OUT</sub> =5.5V V <sub>CE</sub> =5.0V (XC8108A series) V <sub>CE</sub> =V <sub>SS</sub> (XC8108B series)	-	0.1	1.0	μA	①
Reverse Current Prevention Detect Voltage	V <sub>REV_D</sub>	V <sub>IN</sub> : 5.0V→4.7V V <sub>OUT</sub> =5.0V	-	140	-	mV	①
Thermal Shutdown Detect Temperature	T <sub>TSD</sub>	Junction Temperature	-	150	-	°C	①
Thermal Shutdown Release Temperature	T <sub>TSR</sub>	Junction Temperature	-	130	-	°C	①
Thermal Shutdown Hysteresis Width	T <sub>HYS</sub>	Junction Temperature	-	20	-	°C	①

NOTE:

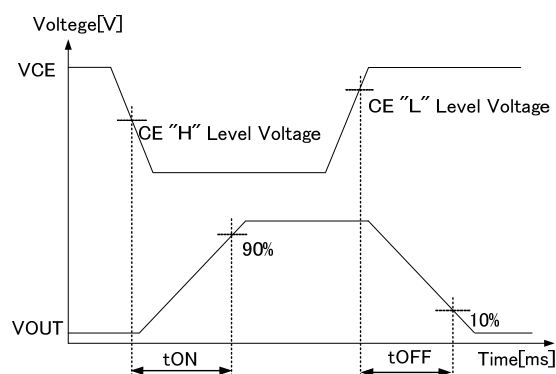
Unless otherwise stated, V<sub>IN</sub>=5.0V, I<sub>OUT</sub>=1mA, I<sub>LIM</sub>=V<sub>SS</sub>, V<sub>CE</sub>=V<sub>IN</sub> (XC8108A series) or V<sub>CE</sub>=V<sub>SS</sub> (XC8108B series)

## ■ TIMING CHART

● turn-on time, turn-off time



XC8108 Series, Type A

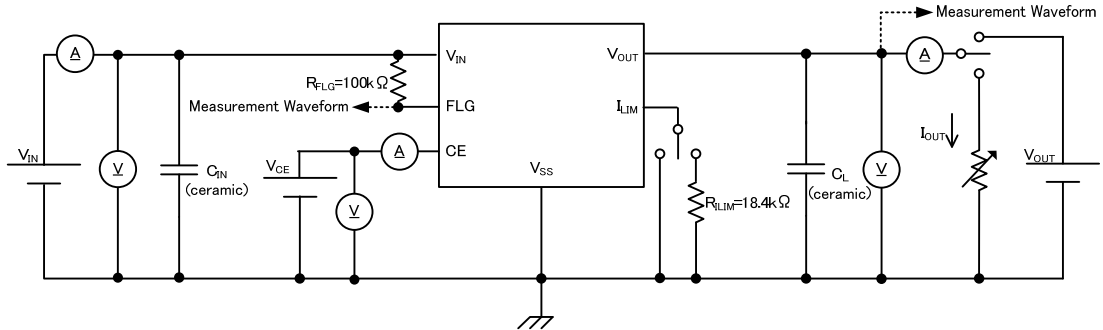


XC8108 Series, Type B

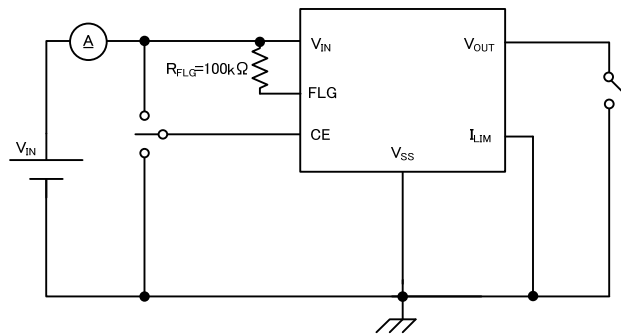
## TEST CIRCUITS

$C_{IN}=1.0\ \mu F$ ,  $C_L=1.0\ \mu F$

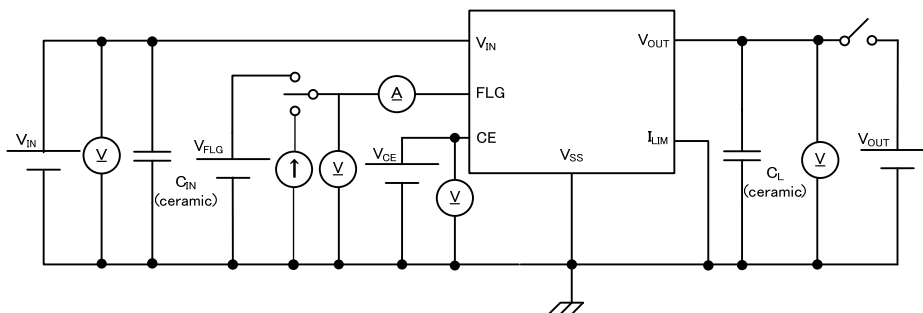
### 1) CIRCUIT①



### 2) CIRCUIT②



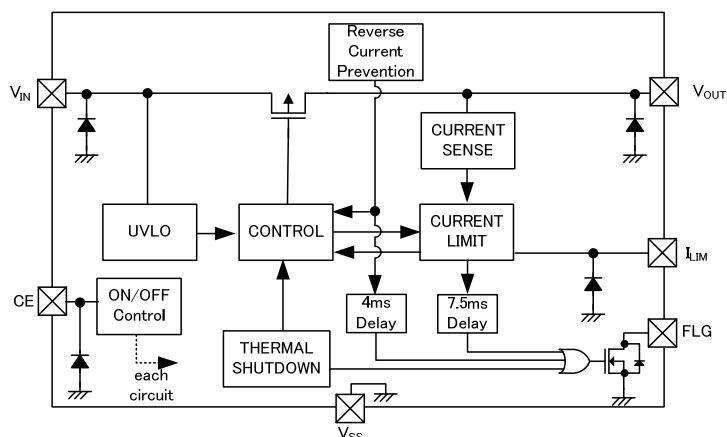
### 3) CIRCUIT③





## ■ OPERATIONAL EXPLANATION

The XC8108 series is a P-channel MOSFET power switch IC. The XC8108 series consists of a CE circuit, UVLO circuit, thermal shutdown circuit, current limiter circuit, reverse current prevention circuit, control block and others. The gate voltage of the power switch transistor is controlled with control block. The current limiter circuit and reverse current prevention circuit will operate based on the output voltage and output current. (See the BLOCK DIAGRAM below)



BLOCK DIAGRAM (XC8108 Series)

### <CE Pin>

The voltage level which is fed to CE pin controls the status of this IC. If either “H” level or “L” level which is defined as the electrical specification is fed to CE pin, then XC8108 can operate in standard manner. However, if the middle voltage which is neither “H” level nor “L” level is fed to CE pin, the consumption current will increase due to the shoot-through current at internal circuits. Also if CE pin is open, the status of XC8108 cannot be fixed and the behavior will be unstable.

### <Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function is built in. When the internal junction temperature reaches the temperature limit, the thermal shutdown circuit operates and the power switch transistor will turn OFF. The IC resumes its operation when the thermal shutdown function is released and the IC’s operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature. When the thermal shutdown circuit detects higher junction temperature than the detect temperature, the voltage level of FLG pin is low level. When the thermal shutdown circuit detects lower junction temperature than the release temperature, the thermal shutdown function is released and the voltage level of FLG pin is high level.

### <Under Voltage Lockout (UVLO) >

When the  $V_{IN}$  pin voltage goes down to lower voltage than UVLO detected voltage, the power switch transistor turns OFF by UVLO function in order to prevent false output caused by unstable operation of the internal circuitry. When the  $V_{IN}$  pin voltage goes up to higher voltage than UVLO released voltage, the UVLO function is released and the power switch transistor can turn ON.

### <Soft-start Function>

The soft-start circuit can reduce the in-rush current charged on the output capacitor when IC starts up. Additionally, due to the reduction of the in-rush current, the circuit can reduce the fluctuation of the input voltage as well. The soft-start time is optimized internally and defined as turn-on time. (TYP: 0.6ms)

## OPERATIONAL EXPLANATION (Continued)

### <Current limiter, short-circuit protection>

When the output current reaches the current limit value, the constant current limit circuit activates and as a result, the output voltage goes down.

If the short circuit comes at the V<sub>OUT</sub> pin, the output current is limited to the current which is specified as the short-circuit current value. If the over-current state lasts for 7.5ms (TYP.), the FLG pin changes to Low level output.

Two types are available for the current limiter circuit: an auto recovery type (product type C) and a latch off type (product type D). After the current limiter circuit activates and the FLG pin outputs low level, the operation is different between these two types.

The auto recovery type continuously limits the output current by the current limit value. When the over-current status finishes and the status of that the output current is less than the current limit value continues for 7.5ms (TYP.) or more, the voltage of FLG pin goes up “H” level again.

The latch off type turns off the power switch transistor after the FLG pin outputs Low level. The off state is maintained regardless of whether the over-current state is released.

Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

### <Current limit external adjustment function>

By connecting a resistor to the current limit external adjustment pin (I<sub>LIM</sub> pin), the current limit can be set to any value. By the following equation, the current limit value can be set to any value within a range of 900mA to 2400mA. When the I<sub>LIM</sub> pin is open, the switch transistor is forcibly turned off.

$$R_{LIM}(k\Omega) = 57207 / I_{LIMIT(T)}(mA) - 24.32(k\Omega)$$

R<sub>LIM</sub>: External resistance value    I<sub>LIMIT(T)</sub>: Current limit set value

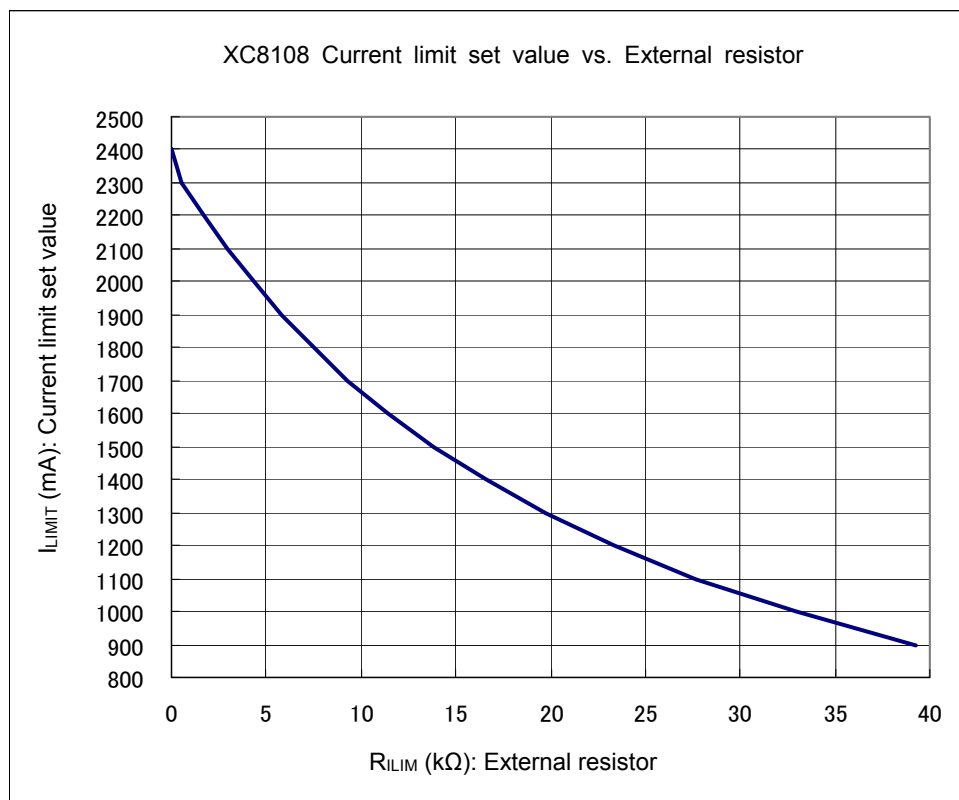
Table1. Current limit set value

I <sub>LIMIT(T)</sub> (mA)	R <sub>LIM</sub> (kΩ)	E96 External resistance value (kΩ)	Current limit value when use E96 external resistance (mA)
900	39.24	39.2	901
1000	32.89	33.2	995
1100	27.69	28.0	1093
1200	23.35	23.2	1204
1300	19.69	19.6	1303
1400	16.54	16.5	1401
1500	13.82	13.7	1505
1600	11.43	11.5	1597
1700	9.33	9.31	1701
1800	7.46	7.5	1798
1900	5.79	5.76	1902
2000	4.28	4.32	1997
2100	2.92	2.94	2099
2200	1.68	1.69	2199
2300	0.55	0.549	2300
2400	I <sub>LIM</sub> shorted to V <sub>SS</sub>		2400

## ■ OPERATIONAL EXPLANATION (Continued)

<Current limit external adjustment function> (Continued)

Fig1. Current limit set value



<Reverse current prevention>

An internal circuit is built in that prevents reverse current from the V<sub>OUT</sub> pin to the V<sub>IN</sub> pin.

When the difference between input voltage and V<sub>OUT</sub> pin voltage is higher than the detect voltage set internally, the reverse current prevention circuit activates, and the power switch transistor turns off, then the reverse current from the V<sub>OUT</sub> pin to the V<sub>IN</sub> pin is reduced to 0.1 μA (TYP.).

If the reverse-voltage state lasts for 4ms (TYP.), the FLG pin changes to Low level output.

Two types are available for the reverse current prevention circuit: the auto recovery type (product type C) and the latch off type (product type D). After the reverse current prevention circuit activates and the FLG pin outputs low level, the operation is different between these two types.

On the auto recovery type, when the output voltage drops below the input voltage, the reverse current prevention circuit stops immediately, and the power switch transistor turns on again. If the output voltage remains lower than the input voltage for 4ms (TYP.), the FLG pin returns to High level output.

On the latch off type, the power switch transistor remains in the off state even if the reverse voltage state is released. Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

## ■ OPERATIONAL EXPLANATION (Continued)

### <Flag function>

The flag circuit is built in which monitors the state of the power switch.

The FLG pin outputs Low level when the reverse current prevention function is operating. A resistance of 10kΩ to 100kΩ is recommended for the FLG pin pull-up resistance.

### Auto recovery type (product type C)

Protective function	FLG pin Low level output	Return to FLG pin High level output
Current limiter	7.5ms after over-current detection	7.5ms after over-current release
Reverse current prevention	4.0ms after reverse voltage detection	4.0ms after reverse voltage release
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released

### Latch off type (product type D)

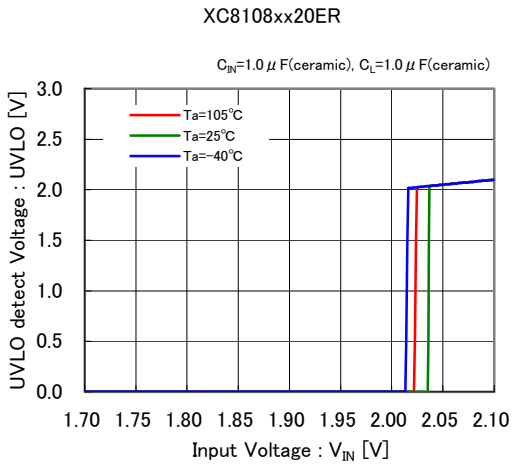
Protective function	FLG pin Low level output	Return to FLG pin High level output
Current limiter	7.5ms after over-current detection	When latch operation is released
Reverse current prevention	4.0ms after reverse voltage detection	When latch operation is released
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released

## ■ NOTES ON USE

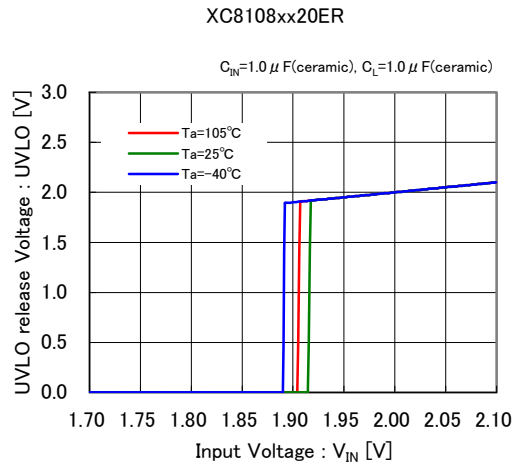
1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.
2. Where wiring impedance is high, operations may become unstable due to noise depending on output current.  
Please keep the resistance low between  $V_{IN}$  and  $V_{SS}$  wiring in particular.
3. Please place the input capacitor ( $C_{IN}$ ) and the output capacitor ( $C_L$ ) as close to the IC as possible.  
For the input or output capacitor, a capacitance of  $1.0 \mu F$  or higher is recommended.
4. When the voltage which is higher than the maximum input voltage is fed to the  $V_{IN}$  pin, and  $V_{OUT}$  is shorted to the  $V_{SS}$  level, in this case the short circuit may cause a fatal impact to operation for the IC. Please use within the operational voltage range.
5. The current limit value can be adjusted by external resistor ( $R_{LIM}$ ). The characteristic of the resistor influence the current limit value, please choose the resistor with small tolerance and temperature coefficient.
6. 80% of current limit set value is the recommended value of maximum output current.
7. Torex places an importance on improving our products and its reliability.  
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

## TYPICAL PERFORMANCE CHARACTERISTICS

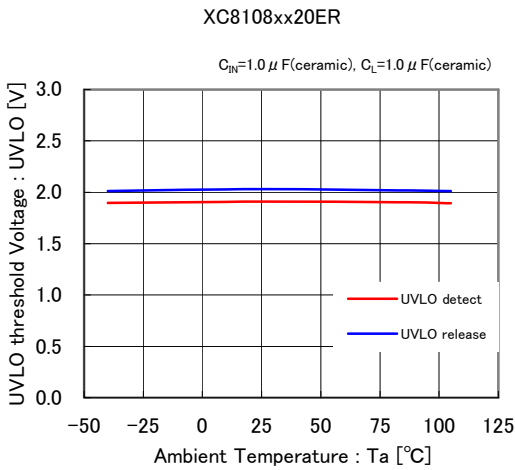
(1) UVLO detect Voltage vs. Input Voltage



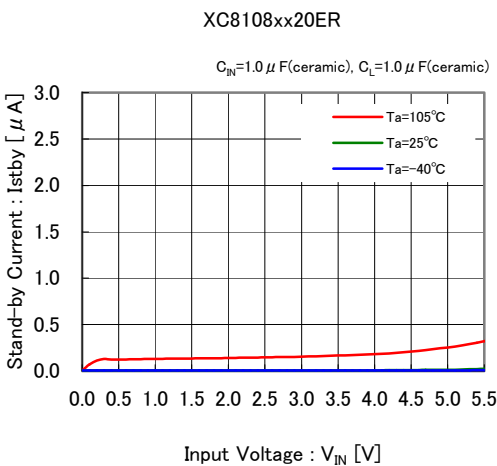
(2) UVLO release Voltage vs. Input Voltage



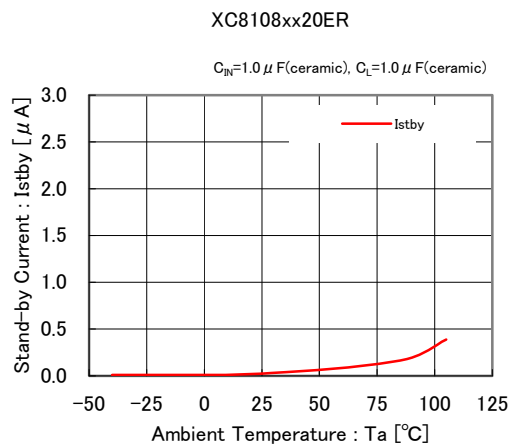
(3) UVLO threshold Voltage vs. Ambient Temperature



(4) Stand-by Current vs. Input Voltage

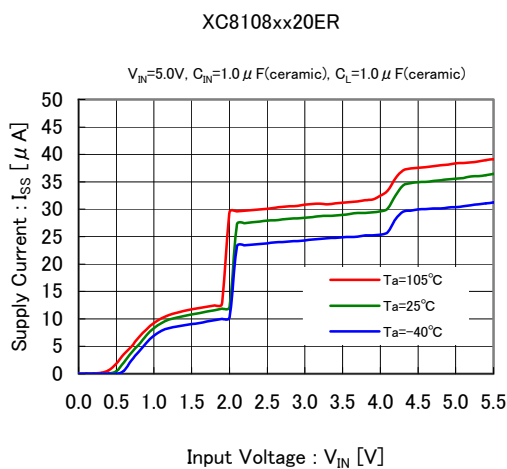


(5) Stand-by Current vs. Ambient Temperature

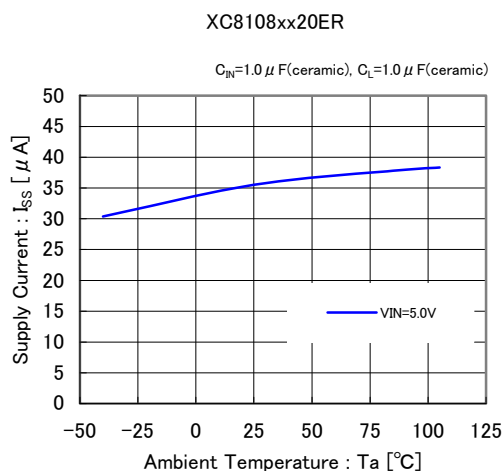


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

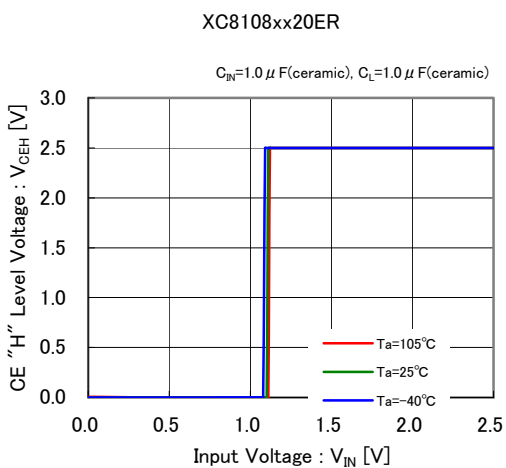
(6) Supply Current vs. Input Voltage (sweep up)



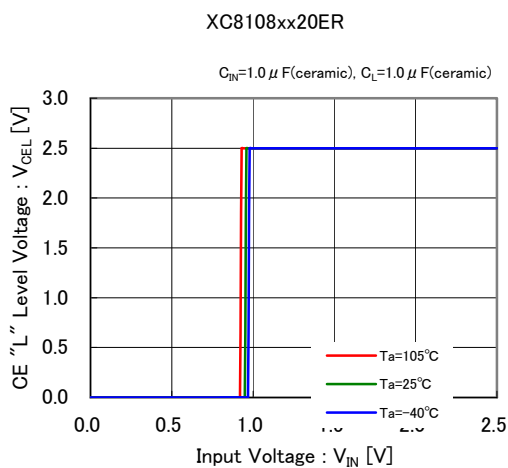
(7) Supply Current vs. Ambient Temperature



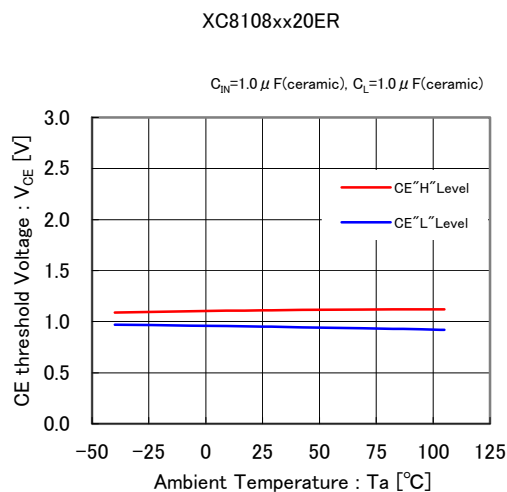
(8) CE "H" Level Voltage vs. Input Voltage



(9) CE "L" Level Voltage vs. Input Voltage

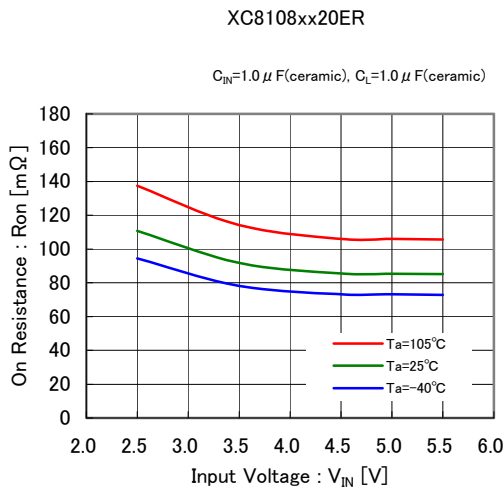


(10) CE threshold Voltage vs. Ambient Temperature

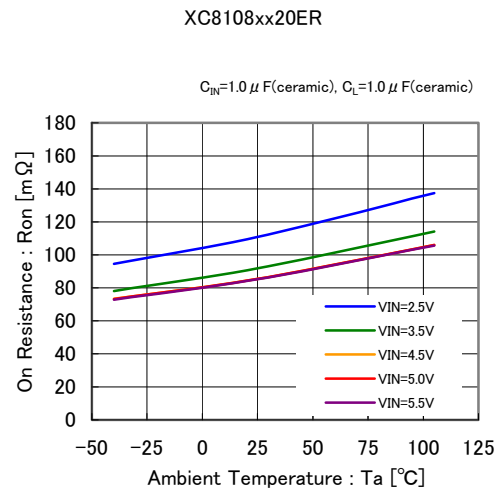


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

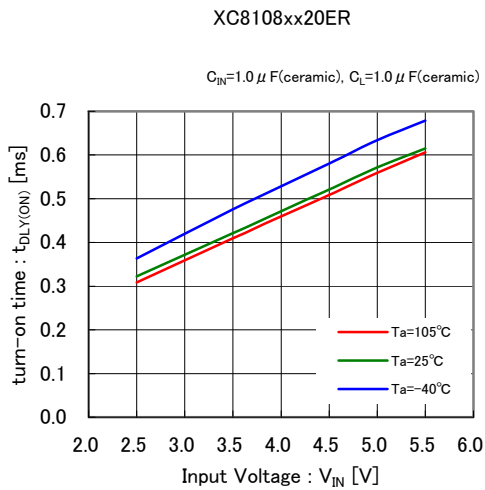
(11) On Resistance vs. Input Voltage



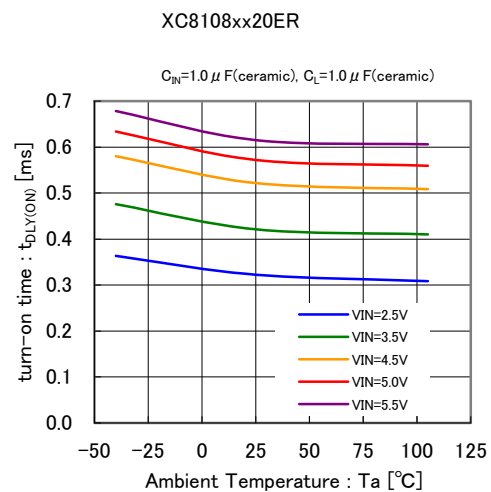
(12) On Resistance vs. Ambient Temperature



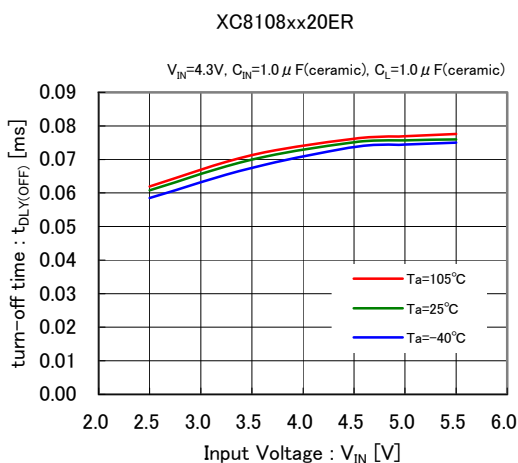
(13) turn-on time vs. Input Voltage



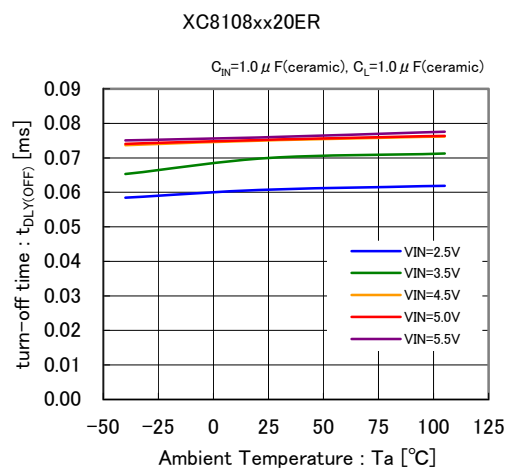
(14) turn-on time vs. Ambient Temperature



(15) turn-off time vs. Input Voltage



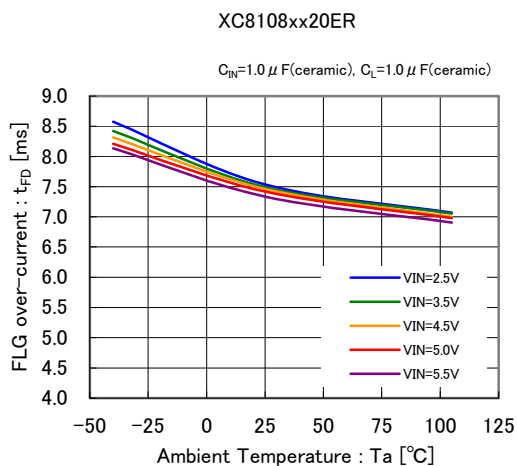
(16) turn-off time vs. Ambient Temperature



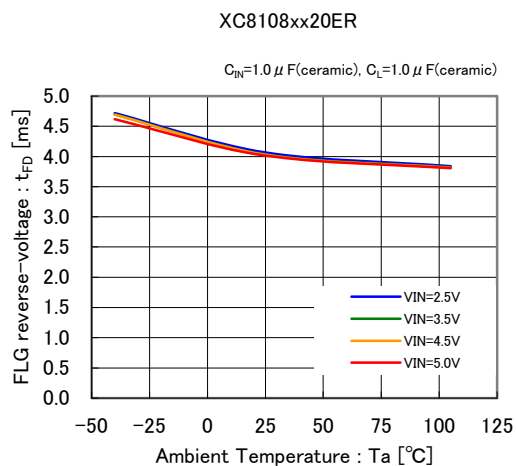


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

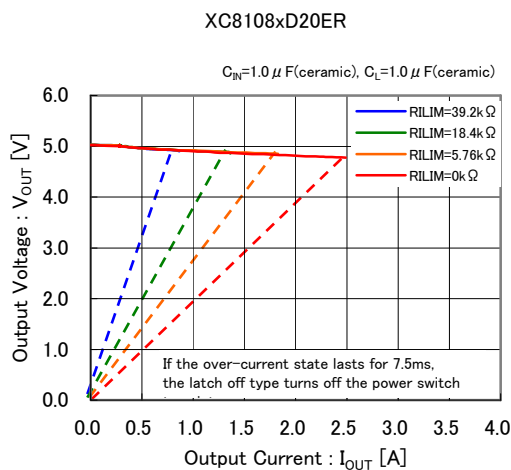
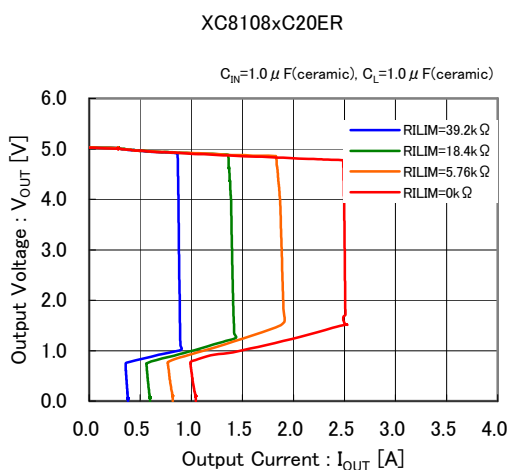
(17) FLG delay time over-current vs. Ambient Temperature



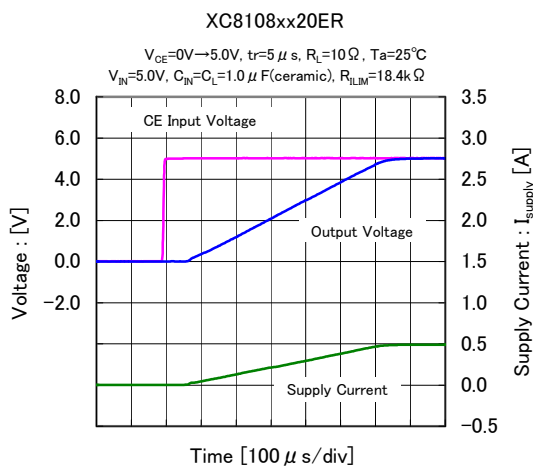
(18) FLG delay time reverse-voltage vs. Ambient Temperature



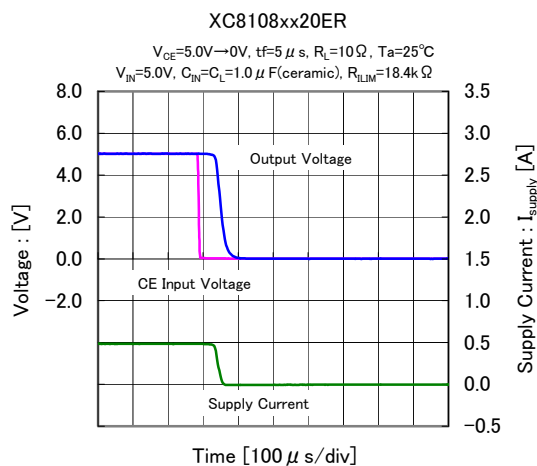
(19) Output Voltage vs. Output Current



(20) turn-on Delay vs. Rise Time ( $C_L=1.0 \mu F$ )

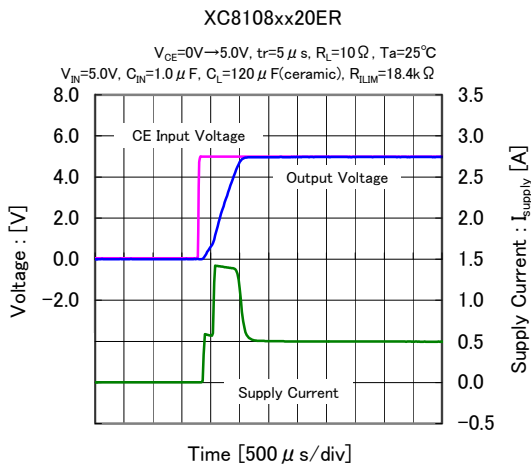


(21) turn-off Delay vs. Fall Time ( $C_L=1.0 \mu F$ )

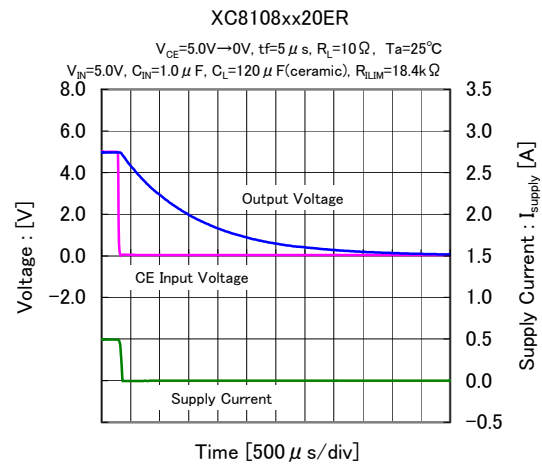


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

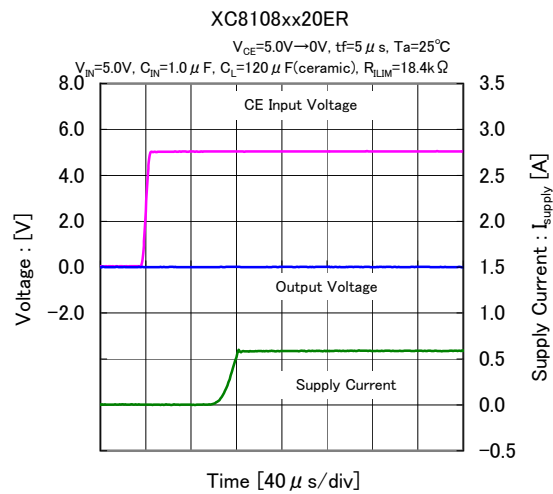
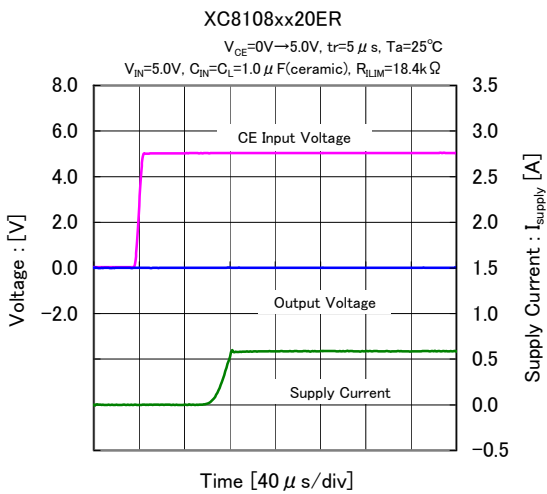
(22) turn-on Delay vs. Rise Time ( $C_L=120\ \mu\text{F}$ )



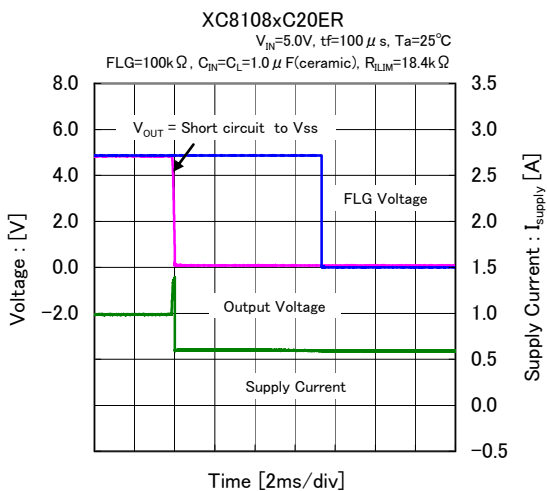
(23) turn-off Delay vs. Fall Time ( $C_L=120\ \mu\text{F}$ )



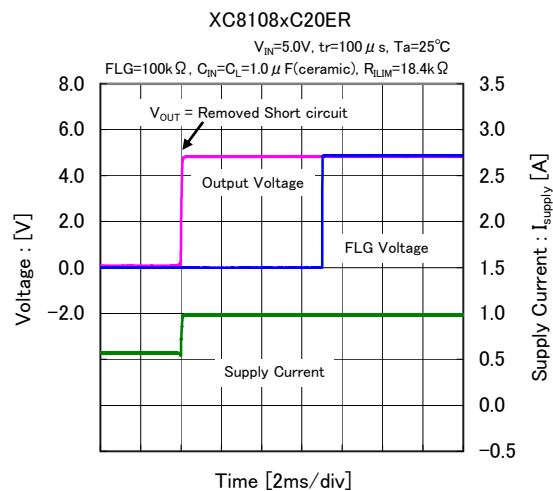
(24) Short Circuit Current, Device Enabled Into Short



(25) Short-Circuit Transient Response ( $V_{OUT}=5.0\ \Omega \rightarrow \text{short}$ ,  $C_L=1.0\ \mu\text{F}$ )

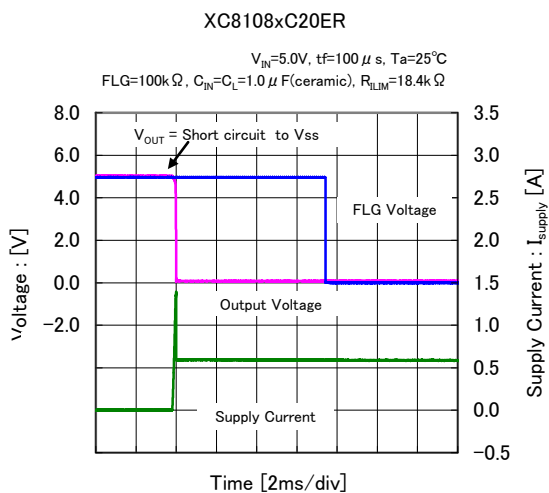


(26) Short-Circuit Transient Response ( $V_{OUT}=\text{short} \rightarrow 5.0\ \Omega$ ,  $C_L=1.0\ \mu\text{F}$ )

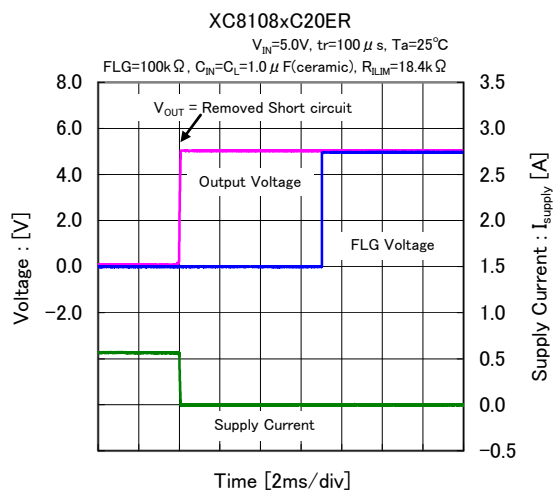


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

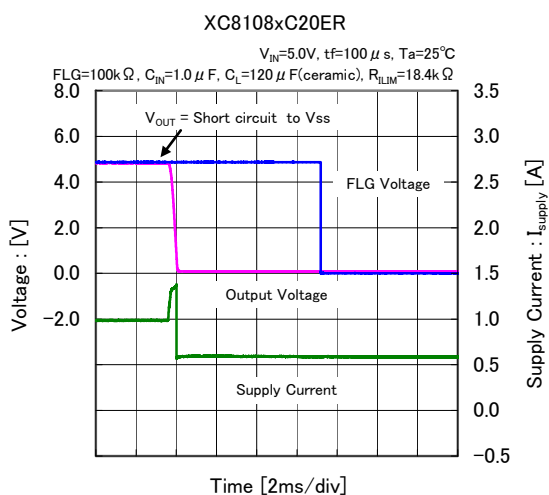
(27) Short-Circuit Transient Response  
( $V_{OUT}$ =open→short,  $C_L=1.0\mu F$ )



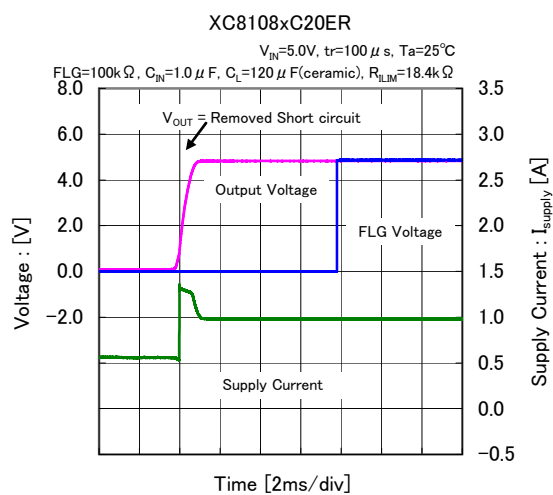
(28) Short-Circuit Transient Response  
( $V_{OUT}$ =short→open,  $C_L=1.0\mu F$ )



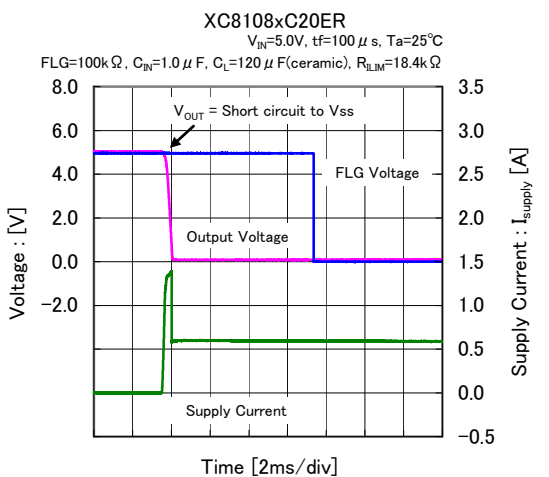
(29) Short-Circuit Transient Response  
( $V_{OUT}=5.0\Omega$ →short,  $C_L=120\mu F$ )



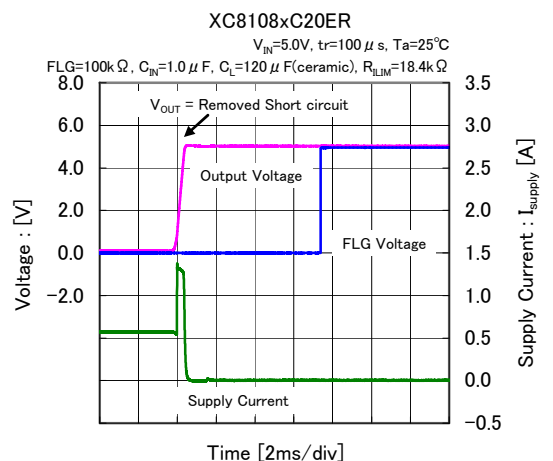
(30) Short-Circuit Transient Response  
( $V_{OUT}$ =short→5.0 $\Omega$ ,  $C_L=120\mu F$ )



(31) Short-Circuit Transient Response  
( $V_{OUT}$ =open→short,  $C_L=120\mu F$ )

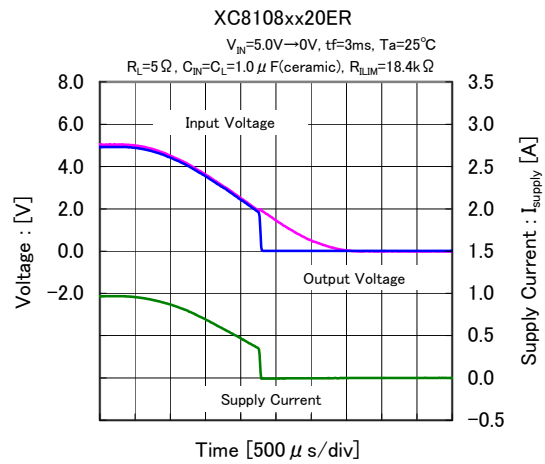
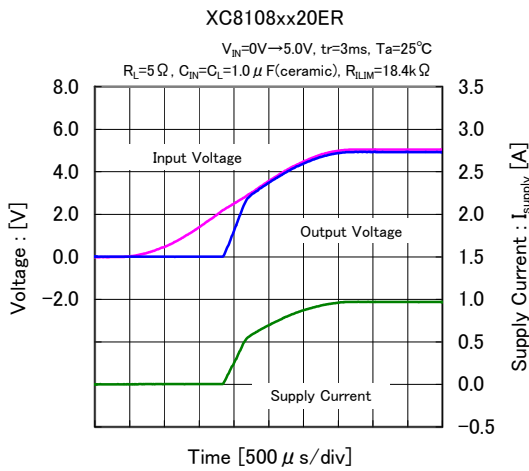


(32) Short-Circuit Transient Response  
( $V_{OUT}$ =short→open,  $C_L=120\mu F$ )

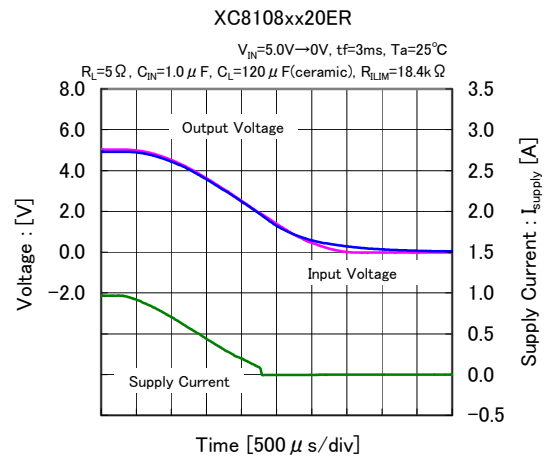
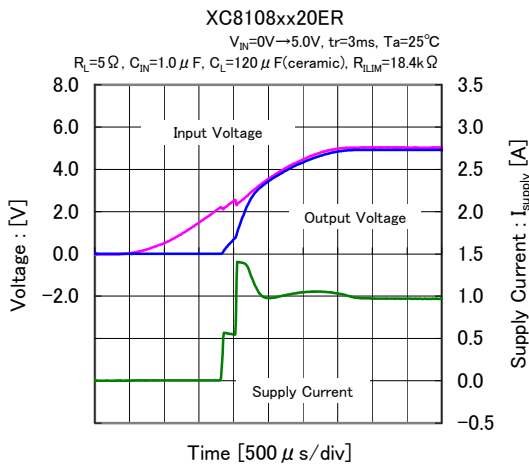


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

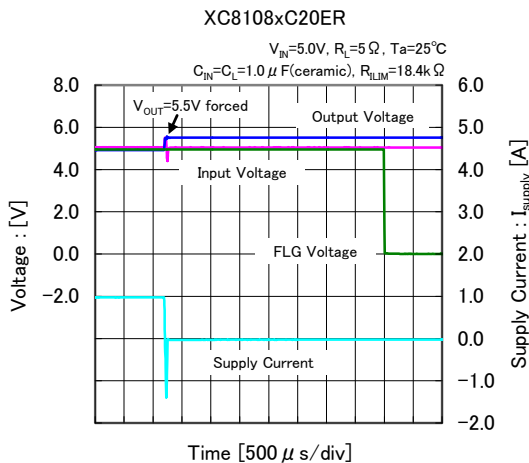
(33) UVLO Transient Response ( $C_L=1.0 \mu\text{F}$ )



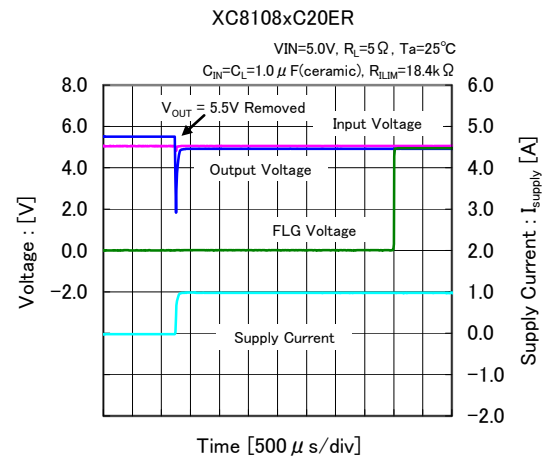
(34) UVLO Transient Response ( $C_L=120 \mu\text{F}$ )



(35) Reverse Voltage Detected Voltage ( $C_L=1.0 \mu\text{F}$ )

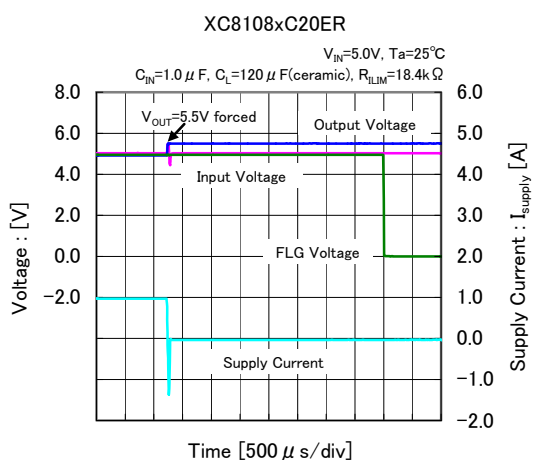


(36) Reverse Voltage Released Voltage ( $C_L=1.0 \mu\text{F}$ )

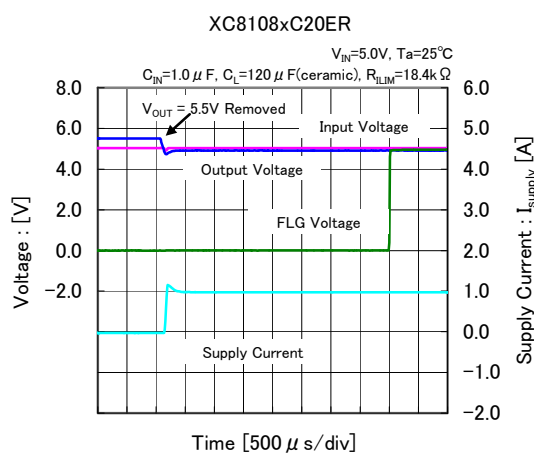


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

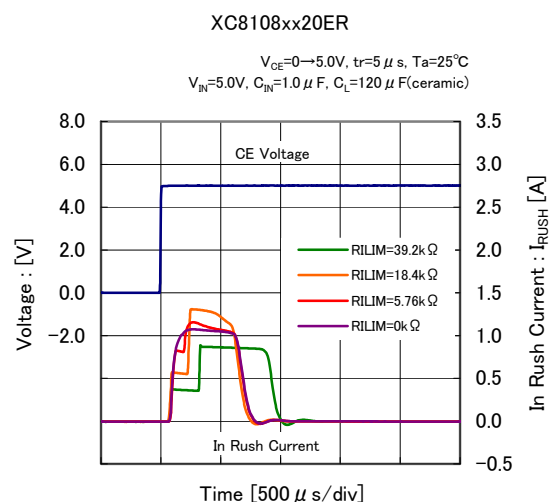
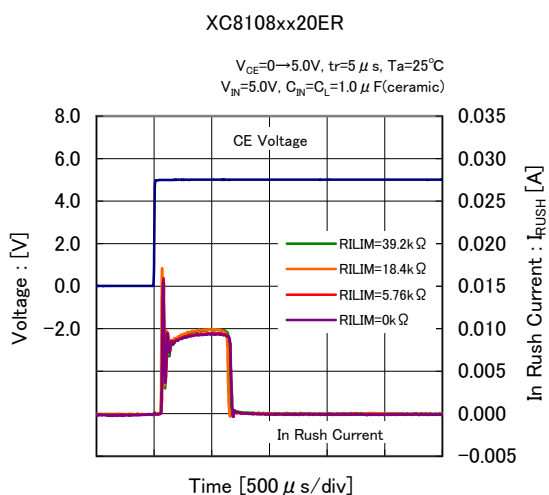
(37) Reverse Voltage Detected Voltage ( $C_L=120\ \mu\text{F}$ )



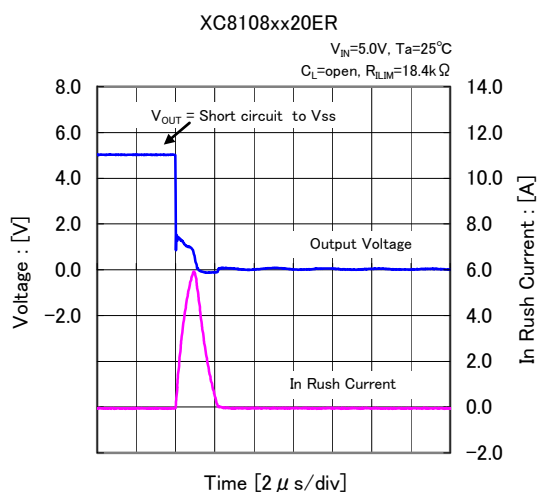
(38) Reverse Voltage Released Voltage ( $C_L=120\ \mu\text{F}$ )



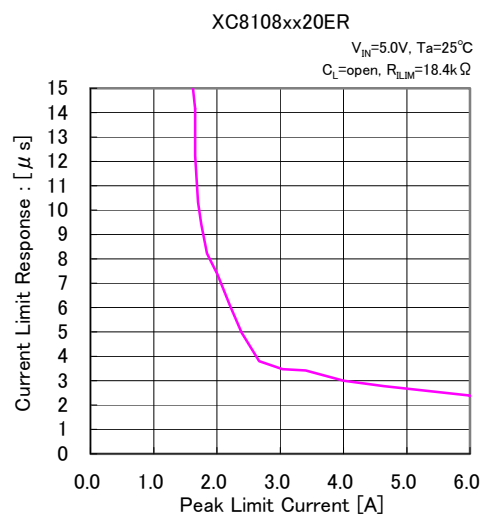
(39) CE Transient Response



(40) Short Applied

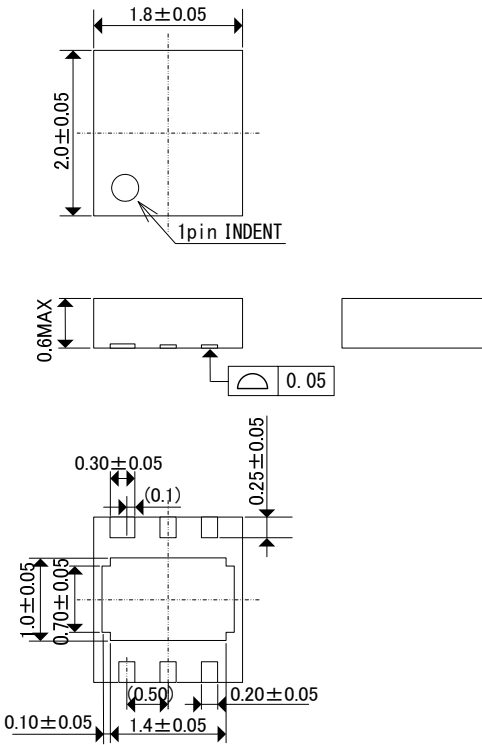


(41) Current Limit adapted time

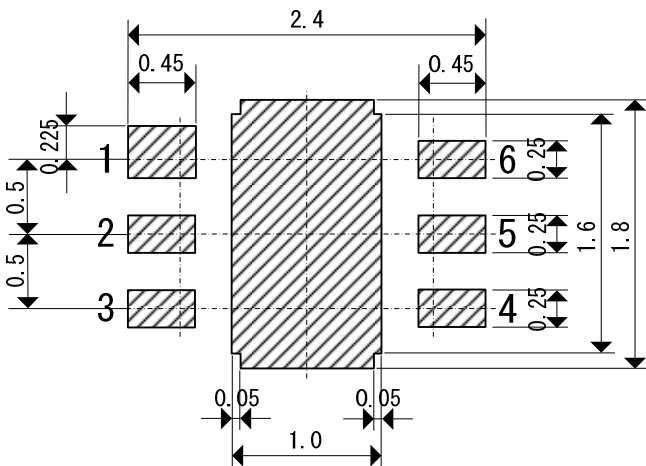


## PACKAGING INFORMATION

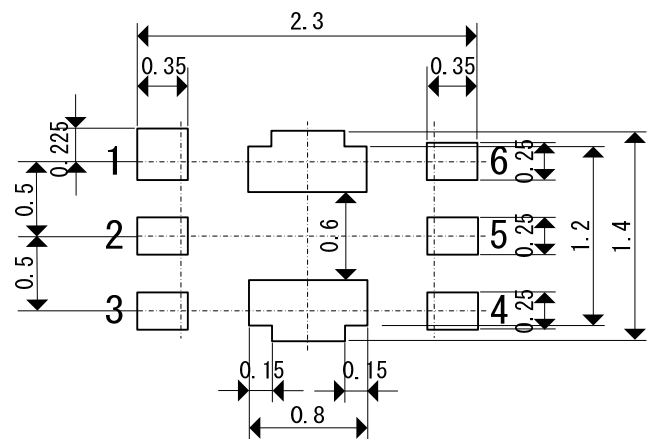
● USP-6C (unit:mm)



● USP-6C Reference Pattern Layout (unit: mm)



● USP-6C Reference Metal Mask Design (unit: mm)



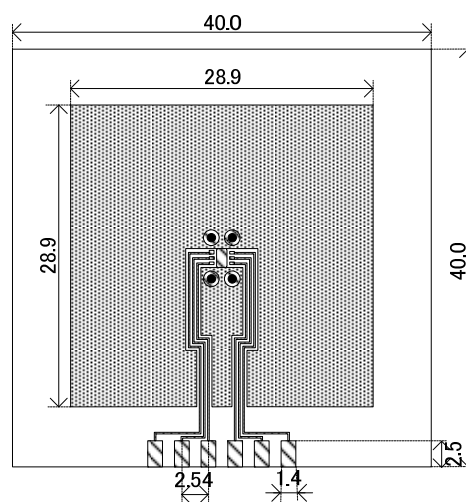
## ■ PACKAGING INFORMATION (Continued)

### ● USP-6C Power Dissipation (40mm x 40mm Standard board)

Power dissipation data for the USP-6C is shown in this page.  
The value of power dissipation varies with the mount board conditions.  
Please use this data as the reference data taken in the following condition.

#### 1. Measurement Condition

- Condition : Mount on a board
- Ambient : Natural convection
- Soldering : Lead (Pb) free
- Board : Dimensions 40 x 40 mm  
(1600 mm<sup>2</sup> in one side)
- Copper (Cu) traces occupy 50% of the board area in top and back faces
- Package heat-sink is tied to the copper traces
- Material : Glass Epoxy (FR-4)
- Thickness : 1.6mm
- Through-hole : 4 x 0.8 Diameter

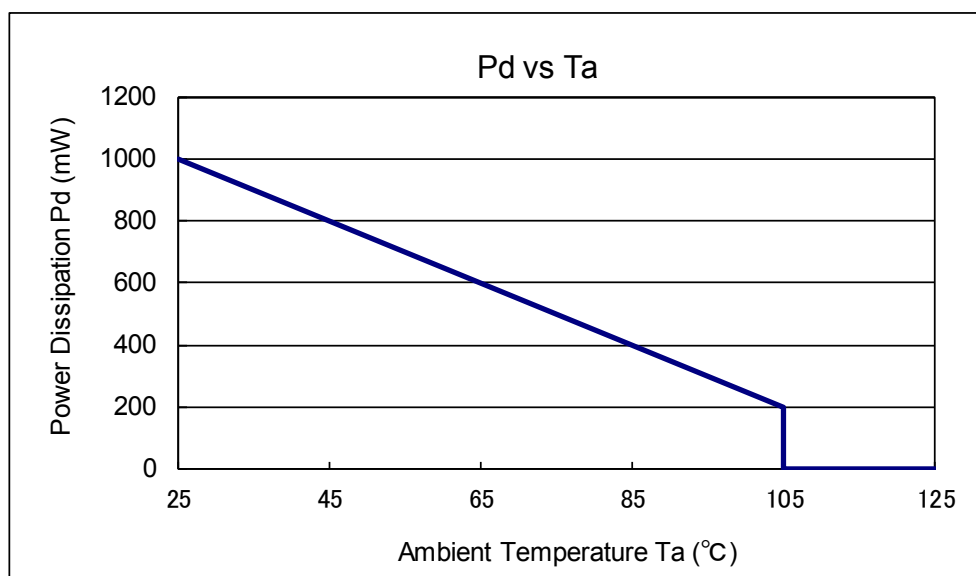


Evaluation Board (Unit : mm)

#### 2. Power Dissipation vs. Ambient Temperature

Board Mount ( $T_j$  max = 125°C)

Ambient Temperature (°C)	Power Dissipation Pd (mW)	Thermal Resistance (°C/W)
25	1000	100.00
105	200	



## PACKAGING INFORMATION (Continued)

### ● USP-6C Power Dissipation (JEDEC board)

Power dissipation data for the USP-6C is shown in this page.

The value of power dissipation varies with the mount board conditions.

Please use this data as one of reference data taken in the described condition.

#### 1. Measurement Condition (Reference data)

Condition : Mount on a board

Ambient : Natural convection

Soldering : Lead (Pb) free

Board : The board using 4 copper layer.

(76.2mm×114.3mm - - Area: about 8700mm<sup>2</sup>)

1st layer : No copper foil (Signal layer)

2nd layer : 70mm×70mm\_Connected to heat-sink.

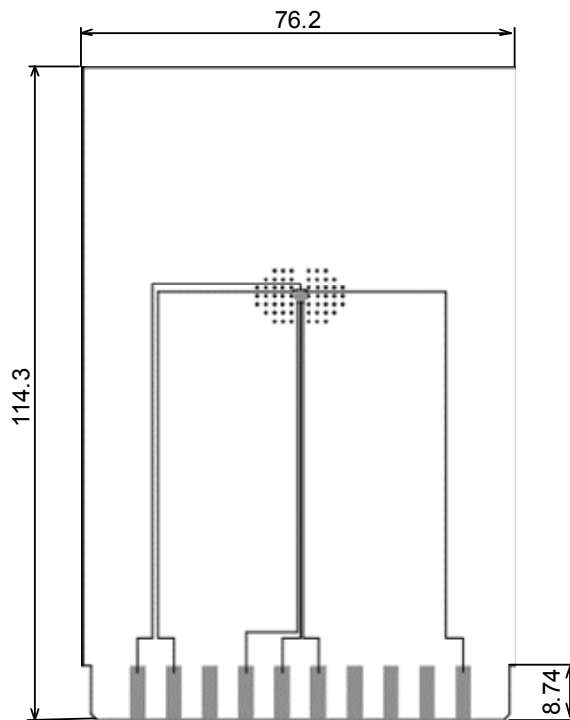
3rd layer : 70mm×70mm\_Connected to heat-sink.

4th layer : No copper foil (Signal layer)

Material : Glass Epoxy (FR-4)

Thickness : 1.6mm

Through-hole : φ0.2mm x 60pcs

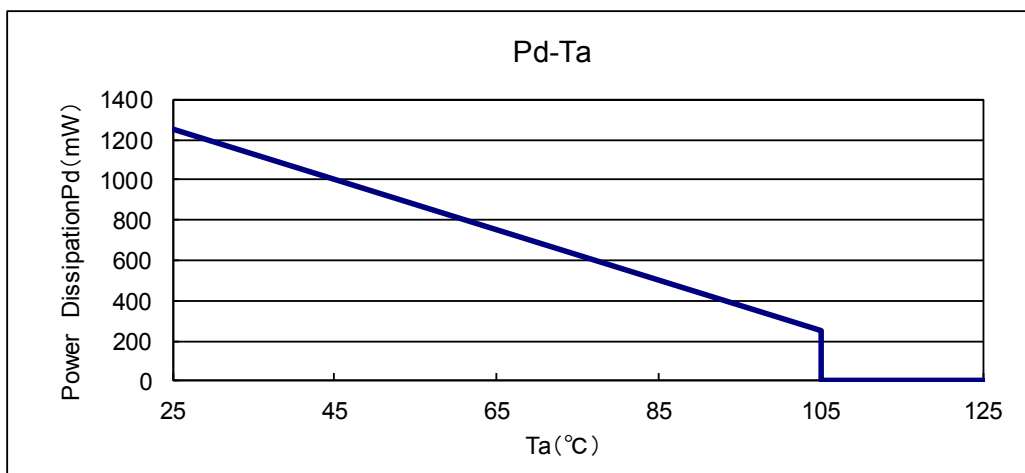


Evaluation Board (Unit: mm)

#### 2. Power Dissipation vs. Ambient temperature

Board Mount(Tjmax = 125°C)

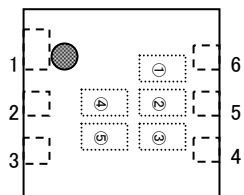
Ambient Temperature (°C)	Power Dissipation Pd (mW)	$\theta_{ja}$ (°C/W)
25	1250	80.00
105	250	





## MARKING RULE

USP-6C



① represents products series

MARK	PRODUCT SERIES
Z	XC8108*****-G

② represents product type

MARK	CE LOGIC	PROTECTION CIRCUIT TYPE	PRODUCT
1	Active High	Auto-recovery	XC8108AC****-G
2	Active High	Latch-off	XC8108AD****-G
3	Active Low	Auto-recovery	XC8108BC****-G
4	Active Low	Latch-off	XC8108BD****-G

③ represents maximum output current

MARK	CURRENT (A)	PRODUCT SERIES
5	2.0	XC8108**20**-G

④⑤ represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.

(G, I, J, O, Q, W excluded)

\* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.
3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.
4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.
5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.
6. Our products are not designed to be Radiation-resistant.
7. Please use the product listed in this datasheet within the specified ranges.
8. We assume no responsibility for damage or loss due to abnormal use.
9. All rights reserved. No part of this datasheet may be copied or reproduced unless agreed by Torex Semiconductor Ltd in writing in advance.

TOREX SEMICONDUCTOR LTD.