XC6118 Series

ETR02013-005

Voltage Detector with Separated Sense Pin & Delay Capacitor Pin

■GENERAL DESCRIPTION

The XC6118 series is a low power consumption voltage detector with high accuracy detection, manufactured using CMOS process and laser trimming technologies.
Since the sense pin is separated from the power supply pin, it allows the IC to monitor the other power supply.
The XC6118 can maintain the state of detection even when voltage of the monitored power supply drops to 0V.
Moreover, a release delay time can be adjusted by the external capacitor connected to the Cd pin.
The V_{OUT} pin is available in both CMOS and N-channel open drain output configurations.

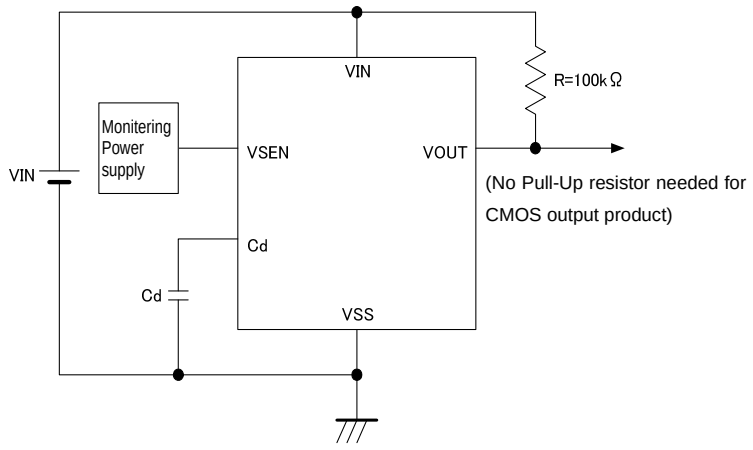
■APPLICATIONS

- ●Microprocessor reset circuitry
- ●Charge voltage monitors
- ●Memory battery back-up switch circuits
- ●Power failure detection circuits

■FEATURES

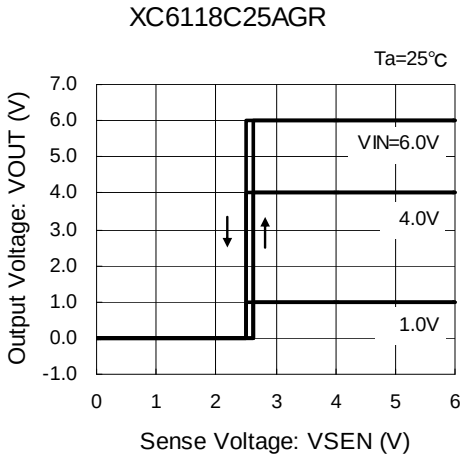
High Accuracy	:±2%(Detect Voltage≧1.5V) ±30mV(Detect Voltage＜1.5V)
Low Power Consumption	: 0.4μA TYP. (Detect, V_{IN}=1.0V) 0.8μA TYP. (Release, V_{IN}=1.0V)
Detect Voltage Range	: 0.8V～5.0V (0.1V increments)
Operating Voltage Range	: 1.0V～6.0V
Temperature Characteristics	: ±100ppm/℃ TYP.
Output Configuration	: CMOS, N-channel open drain
Pin Function	: Power supply separation Release delay time adjustable
Operating Ambient Temperature	: -40℃～+85℃
Packages	: USP-4, SOT-25
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

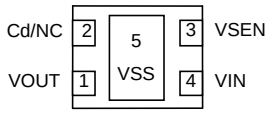


■TYPICAL PERFORMANCE CHARACTERISTICS

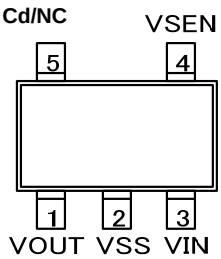
●Output Voltage vs. Sense Voltage



■PIN CONFIGURATION



USP-4
（BOTTOM VIEW）



SOT-25
（TOP VIEW）

* In the XC6118xxxA/B series, the dissipation pad should not be short-circuited with other pins.
* In the XC6118xxxC/D series, when the dissipation pad is short-circuited with other pins, connect it to the NC pin (No.2) pin before use.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
USP-4	SOT-25		
1	1	V_{OUT}	Output (Detect ”L”)
2	5	Cd	Delay Capacitance (*1)
2	5	NC	No Connection
3	4	V_{SEN}	Sense
4	3	V_{IN}	Input
5	2	V_{SS}	Ground (*2)

NOTE:
*1: With the VSS pin of the USP-4 package, a tab on the backside is used as the pin No.5.
*2: In the case of selecting no built-in delay capacitance pin type, the delay capacitance (Cd) pin will be used as the NC.

■PRODUCT CLASSIFICATION

●Ordering Information

XC6118①②③④⑤⑥−⑦(*1)

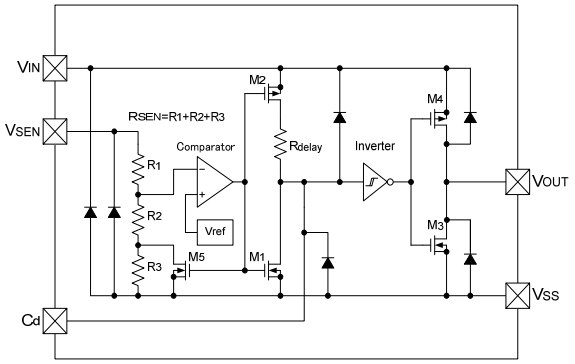
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage	08~50	e.g. 18 → 1.8V
④	Options	A	Built-in delay capacitance pin, hysteresis 5% (TYP.)(Standard*)
		B	Built-in delay capacitance pin, hysteresis less than 1%(Standard*)
		C	No built-in delay capacitance pin, hysteresis 5% (TYP.) (Semi-custom)
		D	No built-in delay capacitance pin, hysteresis less than 1% (Semi-custom)
⑤⑥-⑦	Packages (Order Unit)	GR-G	USP-4 (3,000/Reel)
		MR-G	SOT-25 (3,000/Reel)

*When delay function isn’t used, open the delay capacitance pin before use.

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully RoHS compliant.

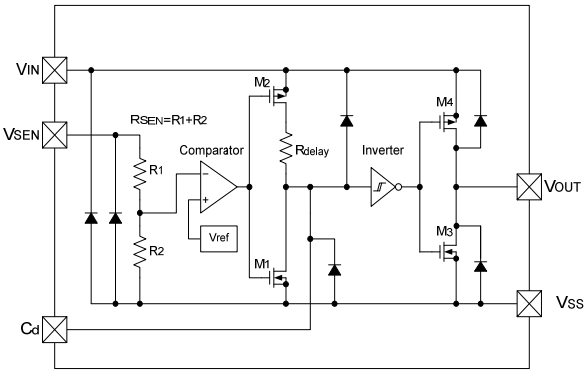
■BLOCK DIAGRAMS

(1) XC6118CxxA



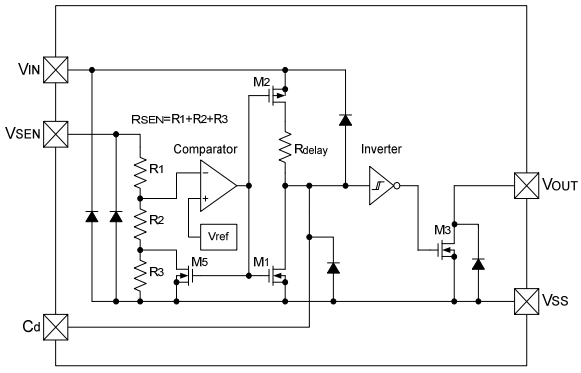
*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6118CxxC (semi-custom).

(2) XC6118CxxB



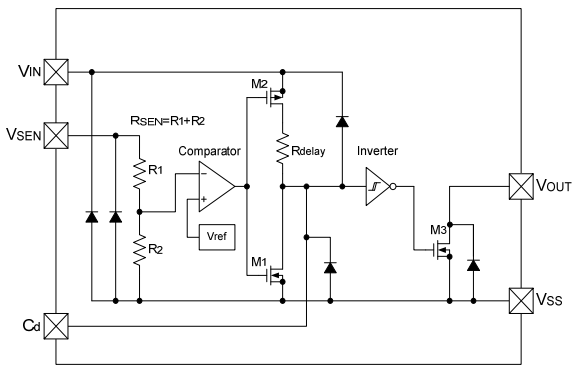
*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6118CxxD (semi-custom).

(3) XC6118NxxA



*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6118NxxC (semi-custom).

(4) XC6118NxxB



*The delay capacitance pin (Cd) is not connected to the circuit in the block diagram of XC6118NxxD (semi-custom).

* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

■ABSOLUTE MAXIMUM RATINGS

●XC6118xxxA/B

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS}-0.3～7.0	V
Output Current		I_{OUT}	10	mA
Output Voltage	XC6118C (*1)	V_{OUT}	V_{SS}-0.3～V_{IN}+0.3	V
	XC6118N (*2)		V_{SS}-0.3～7.0	
Sense Pin Voltage		V_{SEN}	V_{SS}-0.3～7.0	V
Delay Capacitance Pin Voltage		V_{CD}	V_{SS}-0.3～V_{IN}+0.3	V
Delay Capacitance Pin Current		I_{CD}	5.0	mA
Power Dissipation	USP-4	Pd	120	mW
	SOT-25		250	
Operating Ambient Temperature		Ta	-40～+85	°C
Storage Temperature		Tstg	-55～+125	°C

●XC6118xxxC/D

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS}-0.3～7.0	V
Output Current		I_{OUT}	10	mA
Output Voltage	XC6118C (*1)	V_{OUT}	V_{SS}-0.3～V_{IN}+0.3	V
	XC6118N (*2)		V_{SS}-0.3～7.0	
Sense Pin Voltage		V_{SEN}	V_{SS}-0.3～7.0	V
Power Dissipation	USP-4	Pd	120	mW
	SOT-25		250	
Operating Ambient Temperature		Ta	-40～+85	°C
Storage Temperature		Tstg	-55～+125	°C

NOTE:

*1: CMOS output

*2: N-ch open drain output

■ELECTRICAL CHARACTERISTICS

●XC6118xxxA

Ta=25℃

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Operating Voltage		V_{IN}	$V_{DF(T)}$=0.8～5.0V (*1)	1.0		6.0	V	-
Detect Voltage		V_{DF}	V_{IN}=1.0～6.0V		E-1		V	①
Hysteresis Width		V_{HYS}	V_{IN}=1.0～6.0V		E-2		V	①
Detect Voltage Line Regulation		$\Delta V_{DF}/(\Delta V_{IN} \cdot V_{DF})$	V_{IN}=1.0～6.0V		±0.1		%/V	①
Supply Current 1 (*2)		I_{SS1}	$V_{SEN}=V_{DF} \times 0.9$ V_{IN}=1.0V V_{IN}=6.0V		0.4 0.4	1.0 1.0	μA	②
Supply Current 2 (*2)		I_{SS2}	$V_{SEN}=V_{DF} \times 1.1$ V_{IN}=1.0V V_{IN}=6.0V		0.8 0.9	1.6 1.8	μA	②
Output Current (*3)		I_{OUT1}	V_{SEN}=0V, V_{DS}=0.5V(Nch) V_{IN}=1.0V V_{IN}=2.0V V_{IN}=3.0V V_{IN}=4.0V V_{IN}=5.0V V_{IN}=6.0V	0.1 0.8 1.2 1.6 1.8 1.9	0.7 1.6 2.0 2.3 2.4 2.5		mA	③
		I_{OUT2}	V_{SEN}=6.0V, V_{DS}=0.5V(Pch) V_{IN}=1.0V V_{IN}=6.0V		-0.30 -1.00	-0.08 -0.70	mA	④
Leakage Current	CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{SEN}=0V, V_{OUT}=0V, Cd: Open		-0.20		μA	③
	N-ch Open Drain Output		V_{IN}=6.0V, V_{SEN}=6.0V, V_{OUT}=6.0V, Cd: Open		0.20	0.40		
Temperature Characteristics		$\Delta V_{DF}/(\Delta T_{opr} \cdot V_{DF})$	-40℃≦T_{opr}≦85℃		±100		ppm/℃	①
Sense Resistance (*4)		R_{SEN}	V_{SEN}=5.0V V_{IN}=0V		E-4		MΩ	⑤
Delay Resistance (*5)		R_{DELAY}	V_{SEN}=6.0V V_{IN}=5.0V Cd=0V	1.6	2.0	2.4	MΩ	⑥
Delay capacitance pin Sink Current		I_{CD}	Cd=0.5V, V_{IN}=1.0V		200		μA	⑥
Delay Capacitance Pin Threshold Voltage		V_{TCD}	V_{SEN}=6.0V V_{IN}=1.0V V_{SEN}=6.0V V_{IN}=6.0V	0.4 2.9	0.5 3.0	0.6 3.1	V	⑦
Undefined Operation (*6)		V_{UNS}	V_{IN}=V_{SEN}=0～1.0V		0.3	0.4	V	⑧
Detect Delay Time (*7)		t_{DF0}	V_{IN}=6.0V, V_{SEN}=6.0V→0V Cd: Open		30	230	μs	⑨
Release Delay Time (*8)		t_{DR0}	V_{IN}=6.0V, V_{SEN}=0V→6.0V Cd: Open		30	200	μs	⑨

NOTE:

*1: $V_{DF(T)}$: Nominal detect voltage

*2: Current to the sense resistor is not included.

*3: I_{OUT2} is applied only to the XC6118C series (CMOS output).

*4: It is calculated from the voltage value and the current value of the V_{SEN}.

*5: It is calculated from the voltage value of the V_{IN} and the current value of the Cd.

*6: Maximum V_{OUT} voltage when V_{IN} is changed from 0V to 1.0V under connecting the V_{IN} pin to the V_{SEN} pin. This value is effective only to the XC6118C series (CMOS output).

*7: Delay time from the time of V_{SEN}=V_{DF} to the time of V_{OUT}= 0.6V when the V_{SEN} falls.

*8: Delay time from the time of V_{IN}= V_{DF} +V_{HYS} to the time of V_{OUT} = 5.4V when the V_{SEN} rises.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC6118xxxB

Ta=25℃

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Operating Voltage		V_{IN}	$V_{DF(T)}$=0.8～5.0V (*1)	1.0		6.0	V	-
Detect Voltage		V_{DF}	V_{IN}=1.0～6.0V		E-1		V	①
Hysteresis Width		V_{HYS}	V_{IN}=1.0～6.0V		E-3		V	①
Detect Voltage Line Regulation		$\Delta V_{DF}/(\Delta V_{IN} \cdot V_{DF})$	V_{IN}=1.0～6.0V		±0.1		%/V	①
Supply Current 1 (*2)		I_{SS1}	$V_{SEN}=V_{DF} \times 0.9$ V_{IN}=1.0V V_{IN}=6.0V		0.4 0.4	1.0 1.0	μA	②
Supply Current 2 (*2)		I_{SS2}	$V_{SEN}=V_{DF} \times 1.1$ V_{IN}=1.0V V_{IN}=6.0V		0.8 0.9	1.6 1.8	μA	②
Output Current (*3)		I_{OUT1}	V_{SEN}=0V V_{DS}=0.5V(Nch) V_{IN}=1.0V V_{IN}=2.0V V_{IN}=3.0V V_{IN}=4.0V V_{IN}=5.0V V_{IN}=6.0V	 0.1 0.8 1.2 1.6 1.8 1.9	 0.7 1.6 2.0 2.3 2.4 2.5		mA	③
		I_{OUT2}	V_{SEN}=6.0V V_{DS}=0.5V(Pch) V_{IN}=1.0V V_{IN}=6.0V		-0.30 -1.00	-0.08 -0.70	mA	④
Leakage Current	CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{SEN}=0V, V_{OUT}=0V, Cd: Open		-0.20		μA	③
	N-ch Open Drain Output		V_{IN}=6.0V, V_{SEN}=6.0V, V_{OUT}=6.0V, Cd: Open		0.20	0.40		
Temperature Characteristics		$\Delta V_{DF}/(\Delta T_{opr} \cdot V_{DF})$	-40℃≦T_{opr}≦85℃		±100		ppm/℃	①
Sense Resistance (*4)		R_{SEN}	V_{SEN}=5.0V V_{IN}=0V		E-4		MΩ	⑤
Delay Resistance (*5)		R_{DELAY}	V_{SEN}=6.0V V_{IN}=5.0V Cd=0V	1.6	2.0	2.4	MΩ	⑥
Delay capacitance pin Sink Current		I_{CD}	Cd=0.5V, V_{IN}=1.0V		200		μA	⑥
Delay Capacitance Pin Threshold Voltage		V_{TCD}	V_{SEN}=6.0V V_{IN}=1.0V V_{SEN}=6.0V V_{IN}=6.0V	0.4 2.9	0.5 3.0	0.6 3.1	V	⑦
Undefined Operation (*6)		V_{UNS}	$V_{IN}=V_{SEN}$=0～1.0V		0.3	0.4	V	⑧
Detect Delay Time (*7)		t_{DF0}	V_{IN}=6.0V, V_{SEN}=6.0V→0V Cd: Open		30	230	μs	⑨
Release Delay Time (*8)		t_{DR0}	V_{IN}=6.0V, V_{SEN}=0V→6.0V Cd: Open		30	200	μs	⑨

NOTE:

*1: $V_{DF(T)}$: Nominal detect voltage

*2: Current to the sense resistor is not included.

*3: I_{OUT2} is applied only to the XC6118C series (CMOS output).

*4: It is calculated from the voltage value and the current value of the V_{SEN}.

*5: It is calculated from the voltage value of the V_{IN} and the current value of the Cd.

*6: Maximum V_{OUT} voltage when V_{IN} is changed from 0V to 1.0V under connecting the V_{IN} pin to the V_{SEN} pin. This value is effective only to the XC6118C series (CMOS output).

*7: Delay time from the time of $V_{SEN}=V_{DF}$ to the time of V_{OUT}= 0.6V when the V_{SEN} falls.

*8: Delay time from the time of $V_{IN}= V_{DF} +V_{HYS}$ to the time of V_{OUT}= 5.4V when the V_{SEN} rises.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC6118xxxC

Ta=25℃

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Operating Voltage		V_{IN}	$V_{DF(T)}$=0.8～5.0V (*1)	1.0		6.0	V	-
Detect Voltage		V_{DF}	V_{IN}=1.0～6.0V		E-1		V	①
Hysteresis Width		V_{HYS}	V_{IN}=1.0～6.0V		E-2		V	①
Detect Voltage Line Regulation		$\Delta V_{DF}/(\Delta V_{IN} \cdot V_{DF})$	V_{IN}=1.0～6.0V		±0.1		%/V	①
Supply Current 1 (*2)		I_{SS1}	$V_{SEN}=V_{DF} \times 0.9$ V_{IN}=1.0V V_{IN}=6.0V		0.4 0.4	1.0 1.0	μA	②
Supply Current 2 (*2)		I_{SS2}	$V_{SEN}=V_{DF} \times 1.1$ V_{IN}=1.0V V_{IN}=6.0V		0.8 0.9	1.6 1.8	μA	②
Output Current (*3)		I_{OUT1}	V_{SEN}=0V V_{DS}=0.5V(Nch) V_{IN}=1.0V V_{IN}=2.0V V_{IN}=3.0V V_{IN}=4.0V V_{IN}=5.0V V_{IN}=6.0V	 0.1 0.8 1.2 1.6 1.8 1.9	 0.7 1.6 2.0 2.3 2.4 2.5		mA	③
		I_{OUT2}	V_{SEN}=6.0V V_{DS}=0.5V(Pch) V_{IN}=1.0V V_{IN}=6.0V		-0.30 -1.00	-0.08 -0.70	mA	④
Leakage Current	CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{SEN}=0V, V_{OUT}=0V		-0.20		μA	③
	Nch Open Drain Output		V_{IN}=6.0V, V_{SEN}=6.0V, V_{OUT}=6.0V		0.20	0.40		
Temperature Characteristics		$\Delta V_{DF}/(\Delta T_{opr} \cdot V_{DF})$	-40°C≦ T_{opr} ≦85°C		±100		ppm/°C	①
Sense Resistance (*4)		R_{SEN}	V_{SEN}=5.0V V_{IN}=0V		E-4		MΩ	⑤
Undefined Operation (*5)		V_{UNS}	$V_{IN}=V_{SEN}$=0～1.0V		0.3	0.4	V	⑦
Detect Delay Time (*6)		t_{DF0}	V_{IN}=6.0V, V_{SEN}=6.0→0V		30	230	μs	⑨
Release Delay Time (*7)		t_{DR0}	V_{IN}=6.0V, V_{SEN}=0→6.0V		30	200	μs	⑨

NOTE:

*1: $V_{DF(T)}$: Nominal detect voltage

*2: Current to the sense resistor is not included.

*3: I_{OUT2} is applied only to the XC6118C series (CMOS output).

*4: It is calculated from the voltage value and the current value of the V_{SEN}.

*5: Maximum V_{OUT} voltage when V_{IN} is changed from 0V to 1.0V under connecting the V_{IN} pin to the V_{SEN} pin. This value is effective only to the XC6118C series (CMOS output).

*6: Delay time from the time of $V_{SEN}=V_{DF}$ to the time of V_{OUT}= 0.6V when the V_{SEN} falls.

*7: Delay time from the time of $V_{IN}= V_{DF} +V_{HYS}$ to the time of V_{OUT}= 5.4V when the V_{SEN} rises.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC6118xxxD

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Operating Voltage	V_{IN}	$V_{DF(T)}$=0.8～5.0V (*1)	1.0		6.0	V	-
Detect Voltage	V_{DF}	V_{IN}=1.0～6.0V		E-1		V	①
Hysteresis Width	V_{HYS}	V_{IN}=1.0～6.0V		E-3		V	①
Detect Voltage Line Regulation	$\Delta V_{DF}/(\Delta V_{IN} \cdot V_{DF})$	V_{IN}=1.0～6.0V		±0.1		%/V	①
Supply Current 1 (*2)	I_{SS1}	$V_{SEN}=V_{DF}\times 0.9$ V_{IN}=1.0V V_{IN}=6.0V		 0.4 0.4	 1.0 1.0	 μA	 ②
Supply Current 2 (*2)	I_{SS2}	$V_{SEN}=V_{DF}\times 1.1$ V_{IN}=1.0V V_{IN}=6.0V		 0.8 0.9	 1.6 1.8	 μA	 ②
Output Current (*3)	I_{OUT1}	V_{SEN}=0V V_{DS}=0.5V(Nch) V_{IN}=1.0V V_{IN}=2.0V V_{IN}=3.0V V_{IN}=4.0V V_{IN}=5.0V V_{IN}=6.0V	 0.1 0.8 1.2 1.6 1.8 1.9	 0.7 1.6 2.0 2.3 2.4 2.5		mA	③
	I_{OUT2}	V_{SEN}=6.0V V_{DS}=0.5V(Pch) V_{IN}=1.0V V_{IN}=6.0V		 -0.30 -1.00	 -0.08 -0.70	mA	④
Leakage Current: CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{SEN}=0V, V_{OUT}=0V		-0.20		μA	③
Leakage Current: Nch Open Drain Output		V_{IN}=6.0V, V_{SEN}=6.0V, V_{OUT}=6.0V		0.20	0.40		
Temperature Characteristics	$\Delta V_{DF}/(\Delta T_{opr} \cdot V_{DF})$	-40℃≦T_{opr}≦85℃		±100		ppm/℃	①
Sense Resistance (*4)	R_{SEN}	V_{SEN}=5.0V V_{IN}=0V		E-4		MΩ	⑤
Undefined Operation (*5)	V_{UNS}	$V_{IN}=V_{SEN}$=0～1.0V		0.3	0.4	V	⑦
Detect Delay Time (*6)	t_{DF0}	V_{IN}=6.0V V_{SEN}=6.0→0V		30	230	μs	⑨
Release Delay Time (*7)	t_{DR0}	V_{IN}=6.0V V_{SEN}=0→6.0V		30	200	μs	⑨

NOTE:

*1: $V_{DF(T)}$: Nominal detect voltage

*2: Current to the sense resistor is not included.

*3: I_{OUT2} is applied only to the XC6118C series (CMOS output).

*4: It is calculated from the voltage value and the current value of the V_{SEN}.

*5: Maximum V_{OUT} voltage when V_{IN} is changed from 0V to 1.0V under connecting the V_{IN} pin to the V_{SEN} pin. This value is effective only to the XC6118C series (CMOS output).

*6: Delay time from the time of $V_{SEN}=V_{DF}$ to the time of V_{OUT}= 0.6V when the V_{SEN} falls.

*7: Delay time from the time of $V_{IN}= V_{DF} +V_{HYS}$ to the time of V_{OUT} = 5.4V when the V_{SEN} rises.

■VOLTAGE CHART

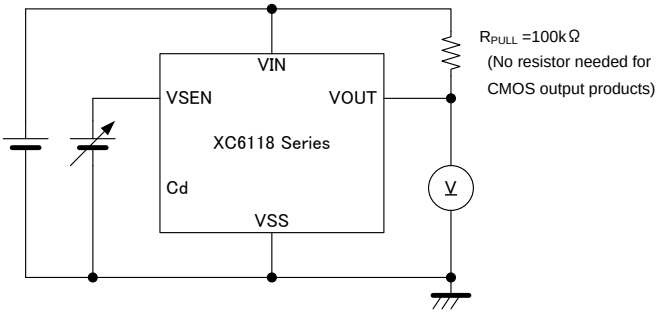
SYMBOL	E-1		E-2		E-3		E-4	
PARAMETER / NOMINAL VOLTAGE	DETECT VOLTAGE (*1) (V)		HYSTERESIS RANGE (V)		HYSTERESIS RANGE (V)		SENSE RESISTANCE (MΩ)	
$V_{DF(T)}$ (V)	V_{DF}		V_{HYS}		V_{HYS}		R_{SEN}	
	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	TYP.
0.8	0.770	0.830	0.015	0.066		0.008		
0.9	0.870	0.930	0.017	0.074		0.009		
1.0	0.970	1.030	0.019	0.082		0.010		
1.1	1.070	1.130	0.021	0.090		0.011		
1.2	1.170	1.230	0.023	0.098		0.012		
1.3	1.270	1.330	0.025	0.106		0.013	10	20
1.4	1.370	1.430	0.027	0.114		0.014		
1.5	1.470	1.530	0.029	0.122		0.015		
1.6	1.568	1.632	0.031	0.131		0.016		
1.7	1.666	1.734	0.033	0.085		0.017		
1.8	1.764	1.836	0.035	0.147		0.018		
1.9	1.862	1.938	0.037	0.155		0.019		
2.0	1.960	2.040	0.039	0.163		0.020		
2.1	2.058	2.142	0.041	0.171		0.021		
2.2	2.156	2.244	0.043	0.180		0.022		
2.3	2.254	2.346	0.045	0.188		0.023		
2.4	2.352	2.448	0.047	0.196		0.024		
2.5	2.450	2.550	0.049	0.204		0.026		
2.6	2.548	2.652	0.051	0.212		0.027		
2.7	2.646	2.754	0.053	0.220		0.028		
2.8	2.744	2.856	0.055	0.228		0.029		
2.9	2.842	2.958	0.057	0.237	0	0.030	13	24
3.0	2.940	3.060	0.059	0.245		0.031		
3.1	3.038	3.162	0.061	0.253		0.032		
3.2	3.136	3.264	0.063	0.261		0.033		
3.3	3.234	3.366	0.065	0.269		0.034		
3.4	3.332	3.468	0.067	0.277		0.035		
3.5	3.430	3.570	0.069	0.286		0.036		
3.6	3.528	3.672	0.071	0.294		0.037		
3.7	3.626	3.774	0.073	0.302		0.038		
3.8	3.724	3.876	0.074	0.310		0.039		
3.9	3.822	3.978	0.076	0.318		0.040		
4.0	3.920	4.080	0.078	0.326		0.041		
4.1	4.018	4.182	0.080	0.335		0.042		
4.2	4.116	4.284	0.082	0.343		0.043		
4.3	4.214	4.386	0.084	0.351		0.044		
4.4	4.312	4.488	0.086	0.359		0.045		
4.5	4.410	4.590	0.088	0.367		0.046	15	28
4.6	4.508	4.692	0.090	0.375		0.047		
4.7	4.606	4.794	0.092	0.384		0.048		
4.8	4.704	4.896	0.094	0.392		0.049		
4.9	4.802	4.998	0.096	0.400		0.050		
5.0	4.900	5.100	0.098	0.408		0.051		

NOTE:

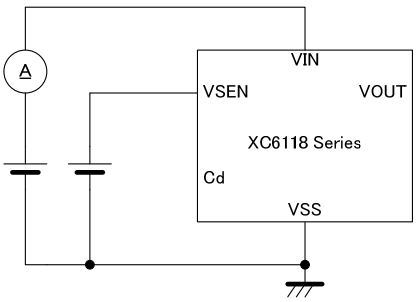
*1: When $V_{DF(T)} \leqq 1.4V$, the detection accuracy is ±30mV.
When $V_{DF(T)} \geqq 1.5V$, the detection accuracy is ±2%.

■TEST CIRCUITS

Circuit 1



Circuit 2



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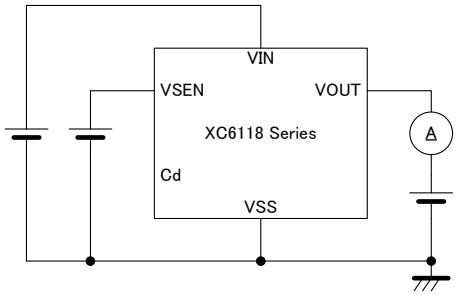
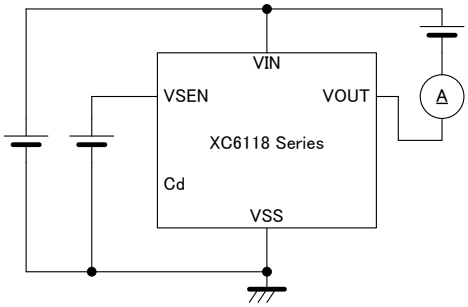
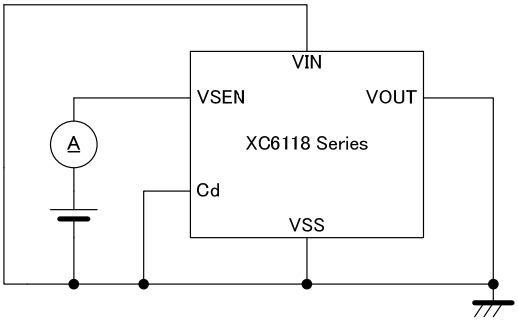


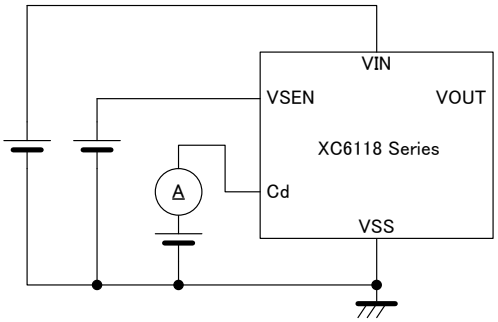
Circuit 4



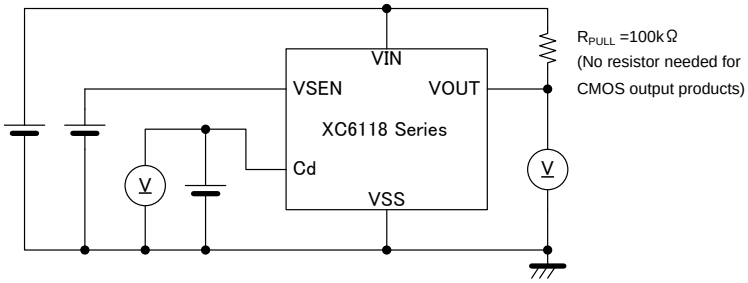
Circuit 5



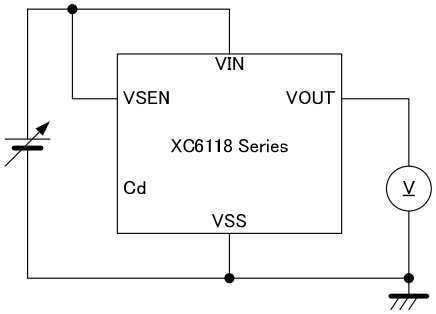
Circuit 6



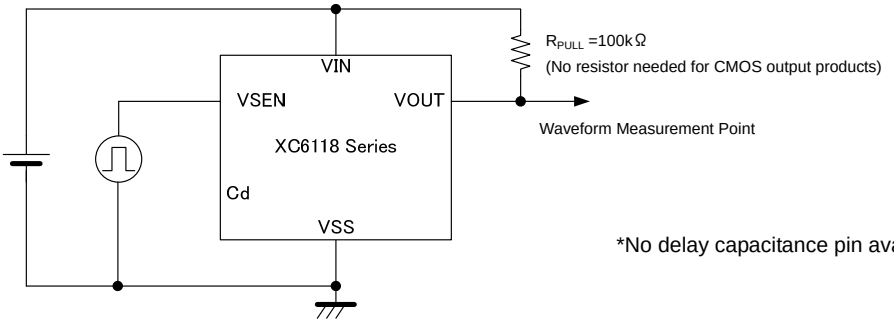
Circuit 7



Circuit 8



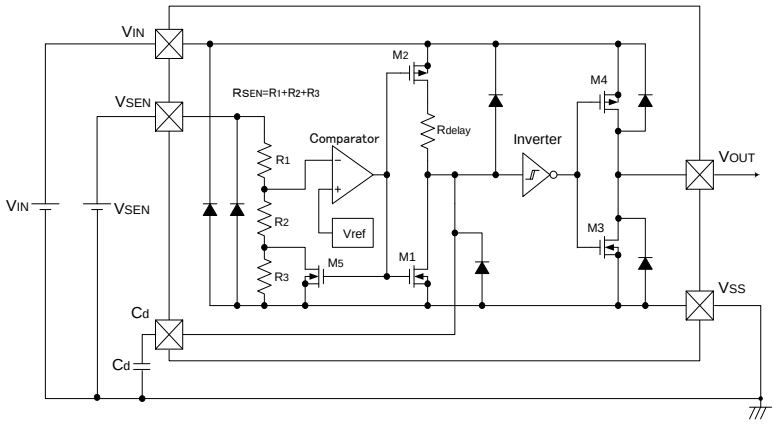
Circuit 9



*No delay capacitance pin available in the XC6118xxxC/D series.

■OPERATIONAL EXPLANATION

A typical circuit example is shown in Figure 1, and the timing chart of Figure 1 is shown in Figure 2.



*The XC6118N series (N-ch open drain output) requires a pull-up resistor for pulling up output.

Figure 1: Typical application circuit example

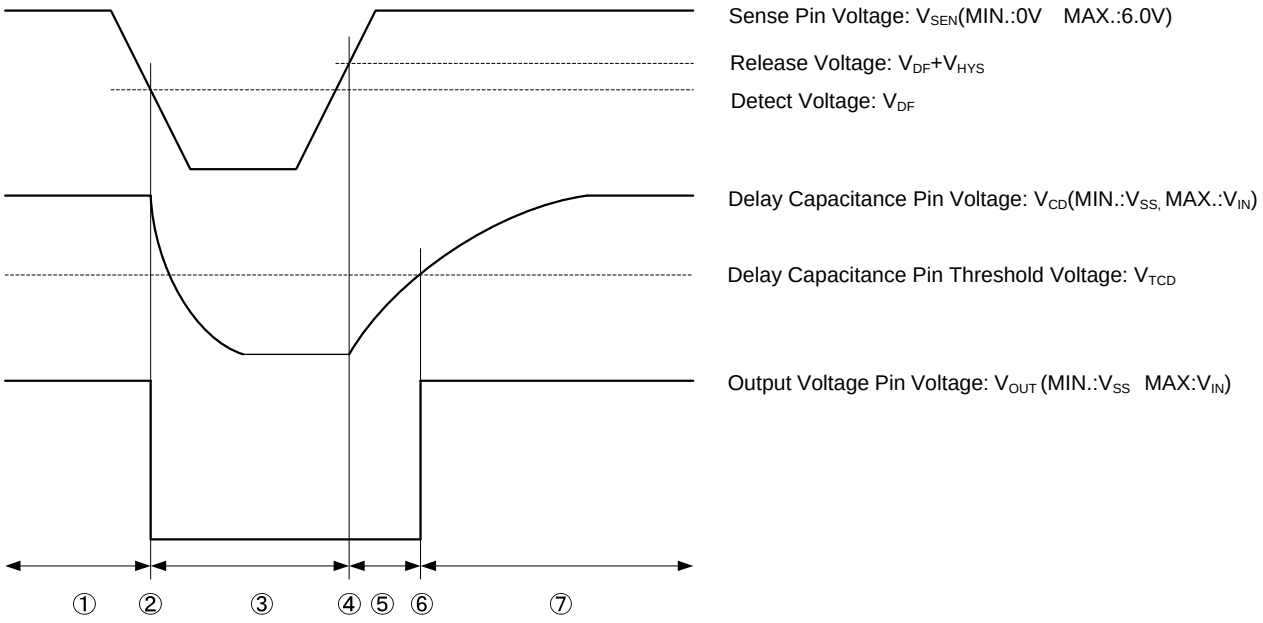


Figure 2: The timing chart of Figure 1

① As an early state, the sense pin is applied sufficiently high voltage (6.0V MAX.) and the delay capacitance (Cd) is charged to the power supply input voltage, (V_{IN}: 1.0V MIN., 6.0V MAX.). While the sense pin voltage (V_{SEN}) starts dropping to reach the detect voltage (V_{DF}) (V_{SEN}>V_{DF}), the output voltage (V_{OUT}) keeps the “High” level (=V_{IN}).
* If a pull-up resistor of the XC6118N series (N-ch open drain) is connected to added power supply different from the input voltage pin, the “High” level will be a voltage value where the pull-up resistor is connected.

② When the sense pin voltage keeps dropping and becomes equal to the detect voltage (V_{SEN} =V_{DF}), an N-ch transistor (M1) for the delay capacitance (Cd) discharge is turned ON, and starts to discharge the delay capacitance (Cd). An inverter (Inv.1) operates as a comparator of the reference voltage V_{IN}, and the output voltage changes into the “Low” level (=V_{SS}). The detect delay time [t_{DF}] is defined as time which ranges from V_{SEN}=V_{DF} to the V_{OUT} of “Low” level (especially, when the Cd pin is not connected: t_{DF0}).

③ While the sense pin voltage keeps below the detect voltage, the delay capacitance (Cd) is discharged to the ground voltage (=V_{SS}) level. Then, the output voltage maintains the “Low” level while the sense pin voltage increases again to reach the release voltage (V_{SEN}< V_{DF} +V_{HYS}).

■OPERATIONAL EXPLANATION (Continued)

④ When the sense pin voltage continues to increase up to the release voltage level ($V_{DF}+V_{HYS}$), the N-ch transistor (M1) for the delay capacitance (Cd) discharge will be turned OFF, and the delay capacitance (Cd) will start discharging via a delay resistor (R_{DELAY}). The inverter (Inv.1) will operate as a comparator (Rise Logic Threshold: $V_{TLH}=V_{TCD}$, Fall Logic Threshold: $V_{THL}=V_{SS}$) while the sense pin voltage keeps higher than the detect voltage ($V_{SEN} > V_{DF}$).

⑤ While the delay capacitance pin voltage (V_{CD}) rises to reach the delay capacitance pin threshold voltage (V_{TCD}) with the sense pin voltage equal to the release voltage or higher, the sense pin will be charged by the time constant of the RC series circuit. Assuming the time to the release delay time (t_{DR}), it can be given by the formula (1).

$$t_{DR}=-R_{DELAY} \times Cd \times ln(1-V_{TCD}/V_{IN}) \quad \cdots(1)$$

The release delay time can also be briefly calculated with the formula (2) because the delay resistance is 2.0MΩ (TYP.) and the delay capacitance pin threshold voltage is V_{IN} /2 (TYP.)

$$t_{DR}=R_{DELAY} \times Cd \times 0.69 \quad \cdots(2)$$

** : R_{DELAY} is 2.0MΩ (TYP.)*

As an example, presuming that the delay capacitance is 0.68μF, t_{DR} is :

$$2.0 \times 10^{6} \times 0.68 \times 10^{-6} \times 0.69=938(ms)$$

* Note that the release delay time may remarkably be short when the delay capacitance (Cd) is not discharged to the ground (=V_{SS}) level because time described in ③ is short.

⑥ When the delay capacitance pin voltage reaches to the delay capacitance pin threshold voltage ($V_{CD}=V_{TCD}$), the inverter (Inv.1) will be inverted. As a result, the output voltage changes into the "High" (=V_{IN}) level. t_{DR0} is defined as time which ranges from $V_{SEN}=V_{DF}+V_{HYS}$ to the V_{OUT} of "High" level without connecting to the Cd.

⑦ While the sense voltage is higher than the detect voltage ($V_{SEN} > V_{DF}$), the delay capacitance pin is charged until the delay capacitance pin voltage becomes the input voltage level. Therefore, the output voltage maintains the "High"(=V_{IN}) level.

●Function Chart

V_{SEN}	Cd	TRANSITION OF V_{OUT} CONDITION *1		
		①		②
L	L	L	⇒	L
	H			
	L	H		
	H			
H	L	L	⇒	L
	H		⇒	H
	L	H	⇒	
	H			

*1: V_{OUT} transits from condition ① to ② because of the combination of V_{SEN} and V_{CD},V_{IN}.
V_{IN} should be more than the lowest operation voltage.

●Example

ex. 1) V_{OUT} ranges from 'L' to 'H' in case of V_{SEN} = 'H' ($V_{DR} \geqq V_{SEN}$), Cd='H' ($V_{TCD} \geqq$ Cd) while V_{OUT} is 'L'.

ex. 2) V_{OUT} maintains 'H' when Cd ranges from 'H' to 'L', V_{SEN}='H' and Cd='L' when V_{OUT} becomes 'H' in ex.1.

●Release Delay Time Chart

DELAY CAPACITANCE [Cd] (μF)	RELEASE DELAY TIME [t_{DR}] (TYP.) (ms)	RELEASE DELAY TIME [t_{DR}] *2 (MIN. ~ MAX.) (ms)
0.010	13.8	11.0 ~ 16.6
0.022	30.4	24.3 ~ 36.4
0.047	64.9	51.9 ~ 77.8
0.100	138	110 ~ 166
0.220	304	243 ~ 364
0.470	649	519 ~ 778
1.000	1380	1100 ~ 1660

* The release delay time values above are calculated by using the formula (2).

*2: The release delay time (t_{DR}) is influenced by the delay capacitance Cd.

■NOTES ON USE

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. The power supply input pin voltage drops by the resistance between power supply and the V_{IN} pin, and by through current at operation of the IC. At this time, the operation may be wrong if the power supply input pin voltage falls below the minimum operating voltage range. In CMOS output, for output current, drops in the power supply input pin voltage similarly occur. Moreover, in CMOS output, when the V_{IN} pin and the sense pin are short-circuited and used, oscillation of the circuit may occur if the drops in voltage, which caused by through current at operation of the IC, exceed the hysteresis voltage. Note it especially when you use the IC with the V_{IN} pin connected to a resistor.
3. When the setting voltage is less than 1.0V, be sure to separate the V_{IN} pin and the sense pin, and to apply the voltage over 1.0V to the V_{IN} pin.
4. Note that a rapid and high fluctuation of the power supply input pin voltage may cause a wrong operation.
5. Power supply noise may cause operational function errors, Care must be taken to put the capacitor between V_{IN}-GND and test on the board carefully.
6. When there is a possibility of which the power supply input pin voltage falls rapidly (e.g.: 6.0V to 0V) at release operation with the delay capacitance pin (Cd) connected to a capacitor, use a Schottky barrier diode connected between the V_{IN} pin and the Cd pin as the Figure 3 shown below.
7. In N channel open drain output, V_{OUT} voltage at detect and release is determined by resistance of a pull up resistor connected at the V_{OUT} pin. Please choose proper resistance values with refer to Figure 4;

During detection: $V_{OUT} = V_{PULL} / (1+R_{PULL} / R_{ON})$
V_{PULL}: Pull up voltage
R_{ON}(※1)：On resistance of N channel driver M3 can be calculated as V_{DS} / I_{OUT1} from electrical characteristics,
For example, when (※2) $R_{ON} = 0.5 / 0.8 \times 10^{-3} = 625\Omega$ （MAX.）at V_{IN}=2.0V, V_{PULL} = 3.0V and V_{OUT} ≦0.1V at detect,
$R_{PULL} = (V_{PULL} / V_{OUT}-1) \times R_{ON} = (3 / 0.1-1) \times 625 \fallingdotseq 18 k\Omega$
In this case, R_{PULL} should be selected higher or equal to 18kΩ in order to keep the output voltage less than 0.1V during detection.
(※1) R_{ON} is bigger when V_{IN} is smaller, be noted.
(※2) For calculation, Minimum V_{IN} should be chosen among the input voltage range.

During releasing：$V_{OUT} = V_{PULL} / (1 + R_{PULL} / R_{OFF})$
V_{PULL}：Pull up voltage
R_{OFF}：On resistance of N channel driver M3 is 15MΩ（MIN.） when the driver is off (as to V_{OUT} / I_{LEAK})
For example：when V_{PULL} = 6.0V and V_{OUT} ≧ 5.99V,
$R_{PULL} = (V_{PULL} / V_{OUT}-1) \times R_{OFF} = (6/5.99-1) \times 15 \times 10^{6} \fallingdotseq 25 k\Omega$
In this case, R_{PULL} should be selected smaller or equal to 25 kΩ in order to obtain output voltage higher than 5.99V during releasing.

8. Torex places an importance on improving our products and their reliability.
We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

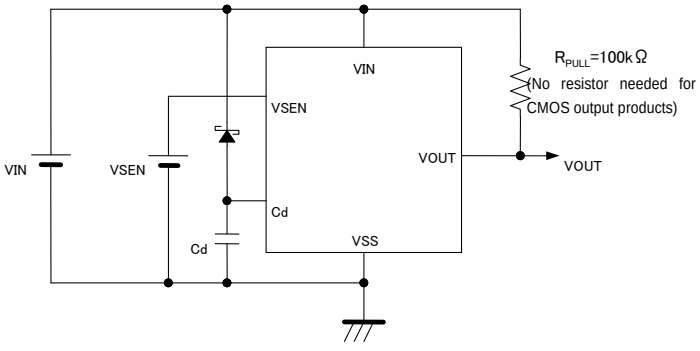
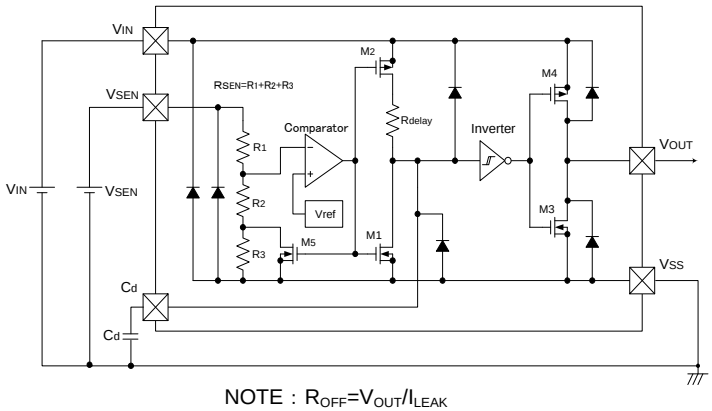


Figure 3: Circuit example with the delay capacitance pin (Cd) connected to a Schottky barrier diode



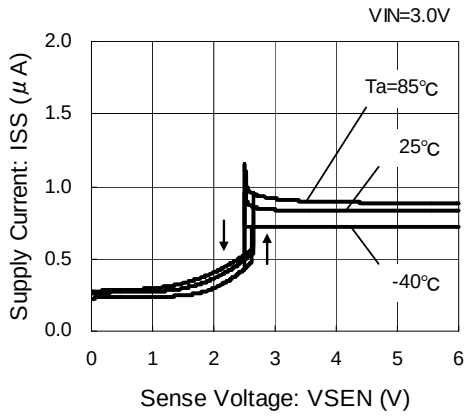
NOTE：$R_{OFF}=V_{OUT}/I_{LEAK}$

Figure 4: Circuit example of XC6118N Series

■TYPICAL PERFORMANCE CHARACTERISTICS

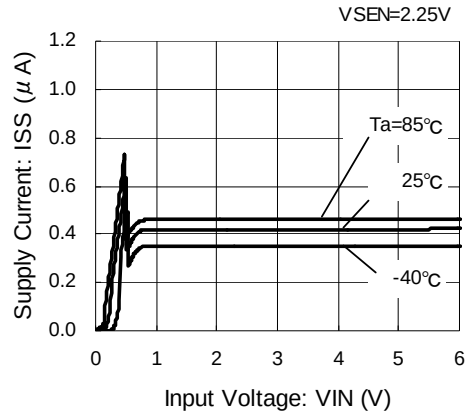
(1) Supply Current vs. Sense Voltage

XC6118C25Ax

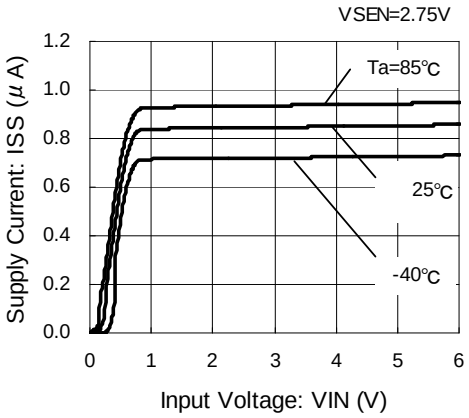


(2) Supply Current vs. Input Voltage

XC6118C25Ax

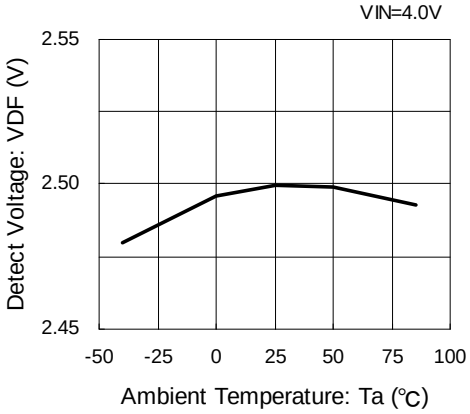


XC6118C25Ax



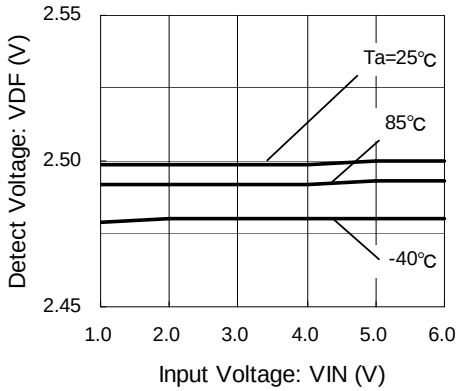
(3) Detect Voltage vs. Ambient Temperature

XC6118C25Ax



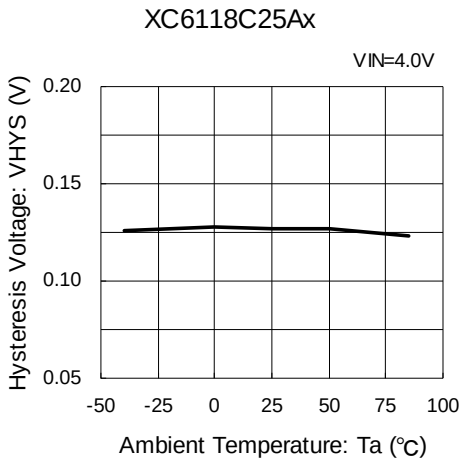
(4) Detect Voltage vs. Input Voltage

XC6118C25Ax

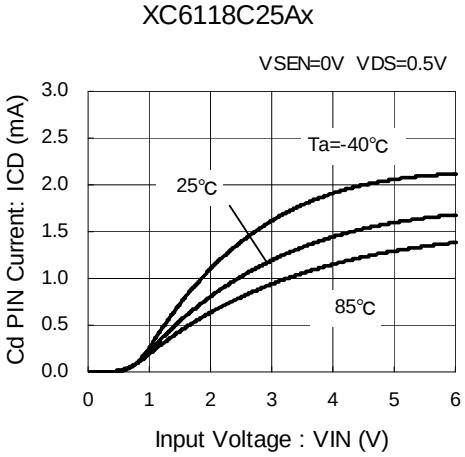


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

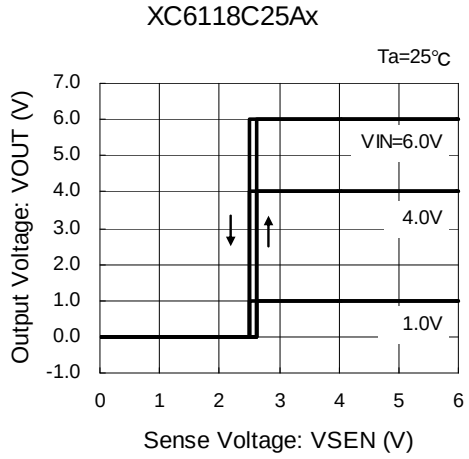
(5) Hysteresis Voltage vs. Ambient Temperature



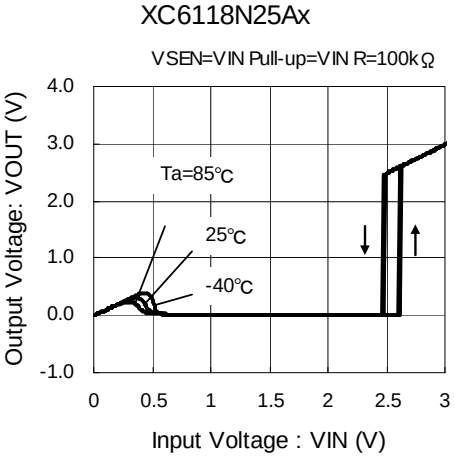
(6) CD Pin Sink Current vs. Input Voltage



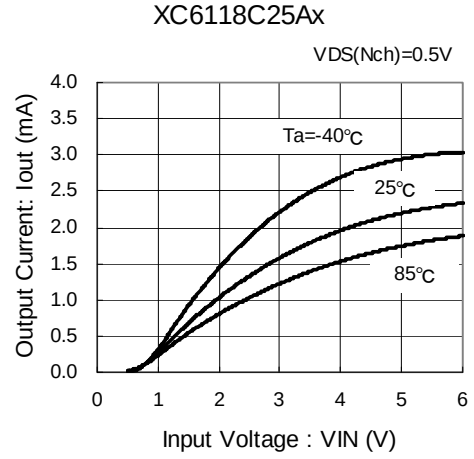
(7) Output Voltage vs. Sense Voltage

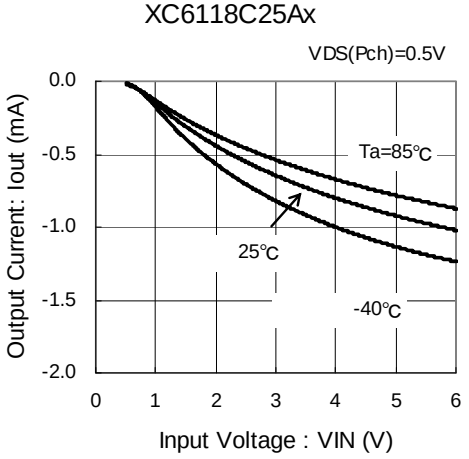


(8) Output Voltage vs. Input Voltage



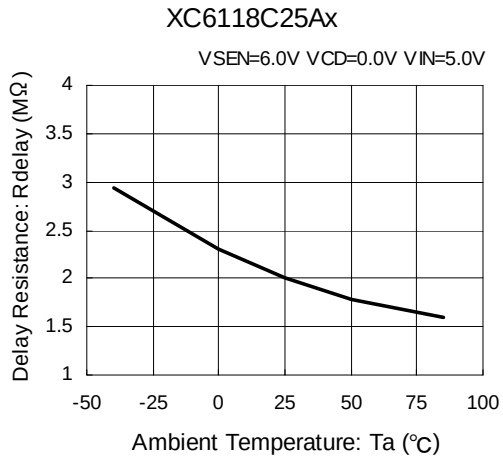
(9) Output Current vs. Input Voltage



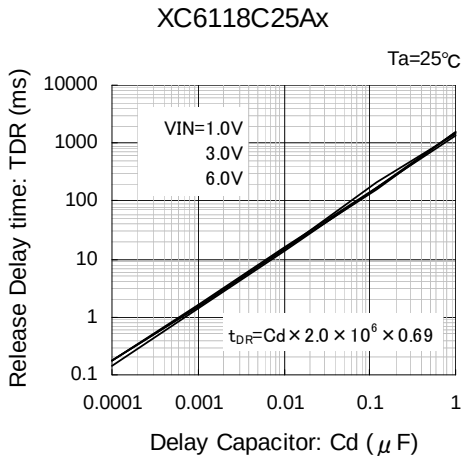


■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

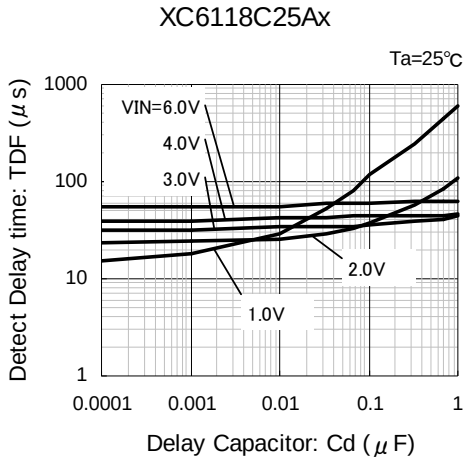
(10) Delay Resistance vs. Ambient Temperature



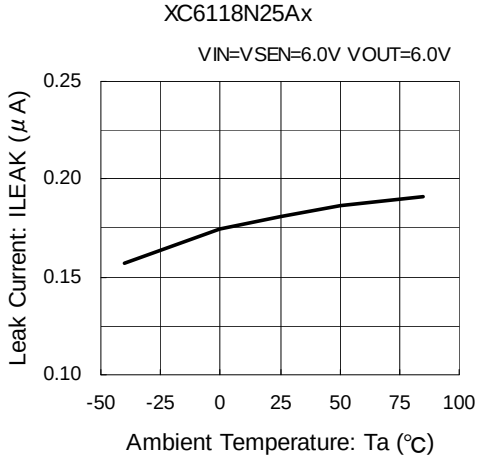
(11) Release Delay Time vs. Delay Capacitance



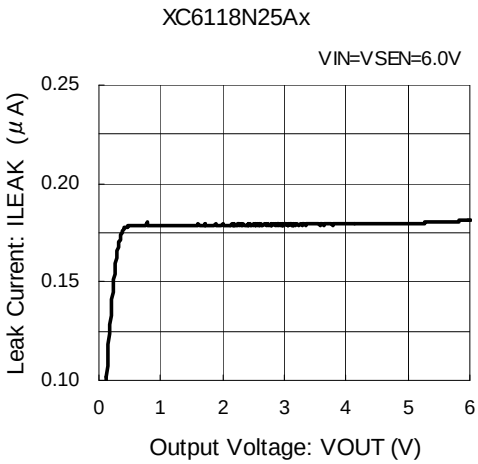
(12) Detect Delay Time vs. Delay Capacitance



(13) Leakage Current vs. Ambient Temperature

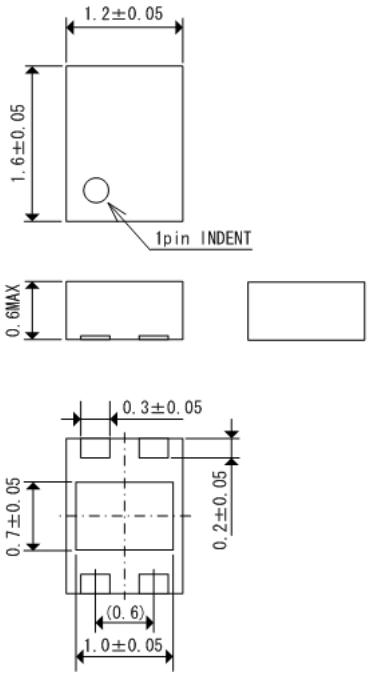


(14) Leakage Current vs. Supply Voltage



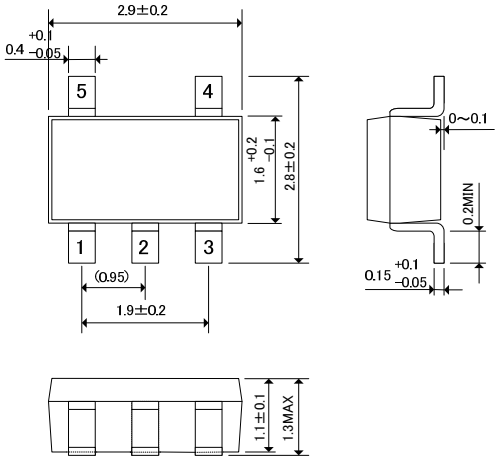
■PACKAGING INFORMATION

●USP-4

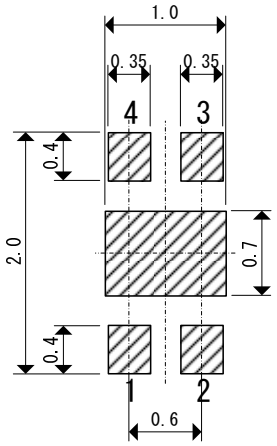


●SOT-25

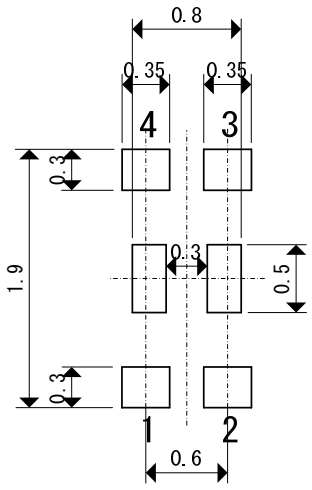
(unit : mm)



●USP-4 Reference Pattern Layout



●USP-4 Reference Metal Mask Design



■MARKING RULE

●SOT-25

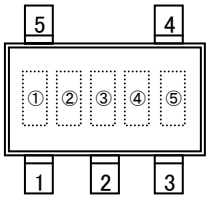
① represents output configuration and integer number of detect voltage

CMOS Output (XC6118C Series)

MARK	VOLTAGE (V)
L	0.X
M	1.X
N	2.X
P	3.X
R	4.X
S	5.X

N-ch Open Drain Output (XC6118N Series)

MARK	VOLTAGE (V)
T	0.X
U	1.X
V	2.X
X	3.X
Y	4.X
Z	5.X



SOT-25
(TOP VIEW)

② represents decimal number of detect voltage

(ex.)

MARK	VOLTAGE (V)	PRODUCT SERIES
3	X.3	XC6118**3***
0	X.0	XC6118**0***

③ represents options

MARK	OPTIONS	PRODUCT SERIES
A	Built-in delay capacitance pin with hysteresis 5% (TYP.) (Standard)	XC6118***A**
B	Built-in delay capacitance pin with hysteresis less than 1% (Standard)	XC6118***B**
C	No built-in delay capacitance pin with hysteresis 5% (TYP.) (Semi-custom)	XC6118***C**
D	No built-in delay capacitance pin with hysteresis less than 1% (Semi-custom)	XC6118***D**

④⑤ represents production lot number

0 to 9 A to Z, or inverted characters of 0 to 9, A to Z repeated.

(G, I, J, O, Q, and W excluded)

*No character inversion used.

■MARKING RULE (Continued)

●USP-4

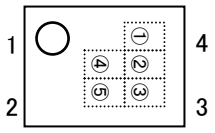
① represents output configuration and integer number of detect voltage

CMOS Output (XC6118C Series)

MARK	VOLTAGE (V)
L	0.X
M	1.X
N	2.X
P	3.X
R	4.X
S	5.X

N-ch Open Drain Output (XC6118N Series)

MARK	VOLTAGE (V)
T	0.X
U	1.X
V	2.X
X	3.X
Y	4.X
Z	5.X



USP-4
(TOP VIEW)

② represents decimal number of detect voltage

(ex.)

MARK	VOLTAGE (V)	PRODUCT SERIES
3	X.3	XC6118**3***
0	X.0	XC6118**0***

③ represents options

MARK	OPTIONS	PRODUCT SERIES
A	Built-in delay capacitance pin with hysteresis 5% (TYP.) (Standard)	XC6118***A**
B	Built-in delay capacitance pin with hysteresis less than 1% (Standard)	XC6118***B**
C	No built-in delay capacitance pin with hysteresis 5% (TYP.) (Semi-custom)	XC6118***C**
D	No built-in delay capacitance pin with hysteresis less than 1% (Semi-custom)	XC6118***D**

④⑤ represents production lot number

0 to 9, A to Z or inverted characters of 0 to 9, A to Z repeated.

(G, I, J, O, Q, and W excluded)

*No character inversion used.

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