

# High Performance Stepper Motor Drive Circuit

## FEATURES

- Full-Step, Half-Step and Micro-Step Capability.
- Bipolar Output Current up to 2A.
- Wide Range of Motor Supply Voltage: 10–50V
- Low Saturation Voltage
- Wide Range of Current Control: 5mA–2A.
- Current Levels Selected in Steps or Varied Continuously.
- Thermal Protection and Soft Intervention.

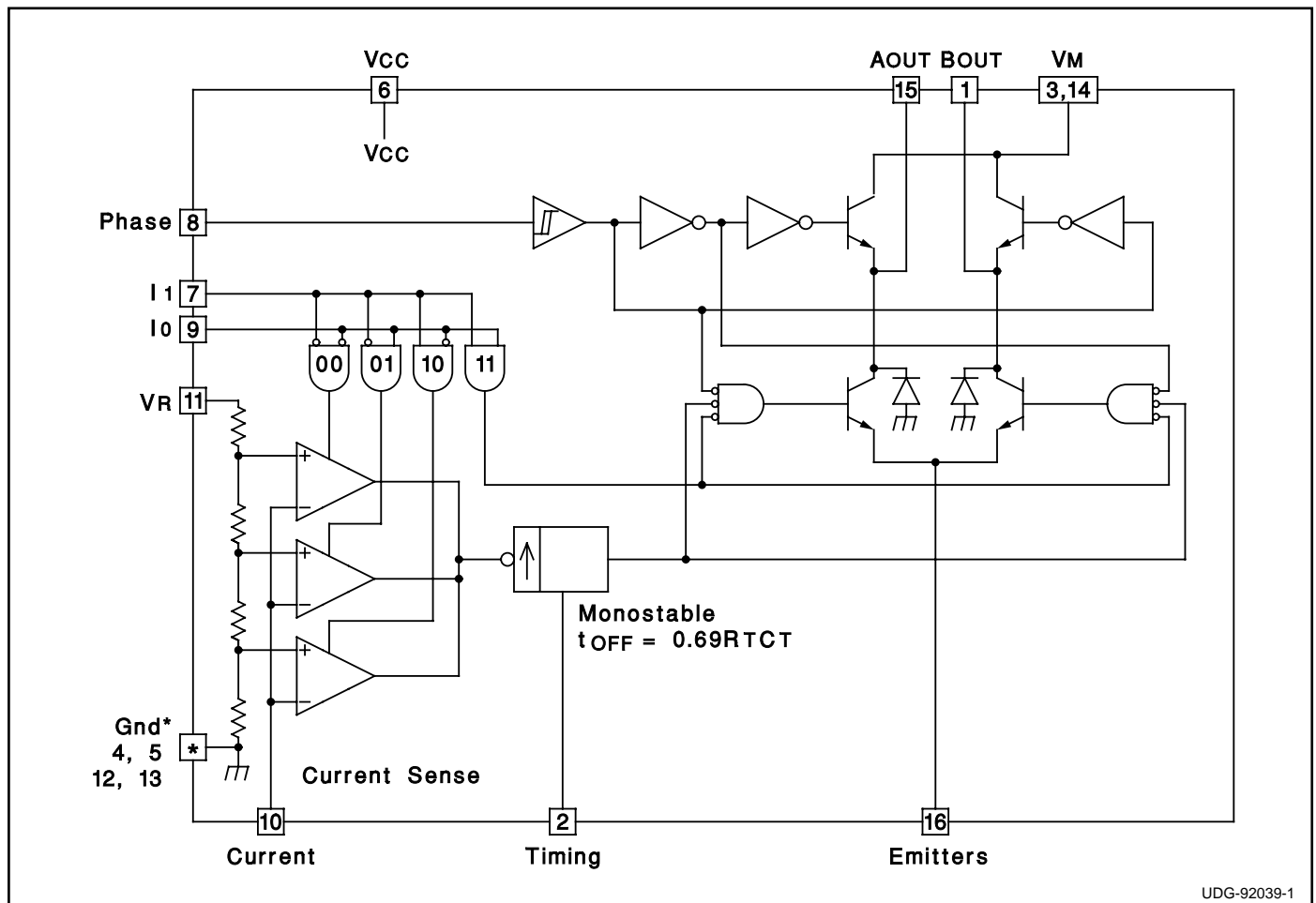
## DESCRIPTION

The UC3770A and UC3770B are high-performance full bridge drivers that offer higher current and lower saturation voltage than the UC3717 and the UC3770. Included in these devices are LS-TTL compatible logic inputs, current sense, monostable, thermal shut-down, and a power H-bridge output stage. Two UC3770As or UC3770Bs and a few external components form a complete micro-processor-controllable stepper motor power system.

Unlike the UC3717, the UC3770A and the UC3770B require external high-side clamp diodes. The UC3770A and UC3770B are identical in all regards except for the current sense thresholds. Thresholds for the UC3770A are identical to those of the older UC3717 permitting drop-in replacement in applications where high-side diodes are not required. Thresholds for the UC3770B are tailored for half stepping applications where 50%, 71%, and 100% current levels are desirable.

The UC3770A and UC3770B are specified for operation from 0°C to 70°C ambient.

## BLOCK DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Logic Supply Voltage, Vcc	7V
Output Supply Voltage, VMM	50V
Logic Input Voltage (Pins 7, 8, 9)	6V
Analog Input Voltage (Pin 10)	Vcc
Reference Input Voltage (Pin 11)	15V
Logic Input Current (Pins 7, 8, 9)	-10mA
Analog Input Current (Pins 10, 11)	-10mA
Output Current (Pins 1, 15)	±2A
Junction Temperature, Tj	+150°C

Note 1: All voltages are with respect to Gnd (DIL Pins 4, 5, 12, 13); all currents are positive into, negative out of the specified terminal.

Note 2: Consult Unitorde Integrated Circuits databook for thermal limitations and considerations of packages.

### CONNECTION DIAGRAMS

**DIL-16 (Top View)**  
J Or N Package

**PLCC-28 (Top View)**  
Q Package

PACKAGE PIN FUNCTION	
FUNCTION	PIN
Gnd	1-3
VM	4
N/C	5
AOUT	6
N/C	7
Emitters	8
Gnd	9
BOUT	10
Timing	11
VM	12
Gnd	13-17
Vcc	18
I1	19
Phase	20
Io	21
N/C	22
Current	23
VR	24
N/C	25-27
Gnd	28

**ELECTRICAL CHARACTERISTICS:** (All tests apply with VM = 36V, Vcc = 5V, VR = 5V, No Load, and 0°C < TA < 70°C, unless otherwise stated, TA = Tj.)

PARAMETER	TEST CONDITIONS	UC3770A			UC3770B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage VM (Pins 3, 14)		10		45	10		45	V
Logic Supply Voltage Vcc (Pin 6)		4.75	5	5.3	4.75	5	5.3	V
Logic Supply Current Icc (Pin 6)	Io = I1 = H, Im = 0		15	25		15	25	mA
	Io = I1 = L, Im = 0		18	28		18	28	mA
	Io = I1 = H, Im = 1.3A		33	40		33	40	mA
Thermal Shutdown Temperature			+170			+170		°C
Logic Threshold (Pins 7, 8, 9)		0.8		2.0	0.8		2.0	V
Input Current Low (Pin 8)	Vi = 0.4V			-100			-100	µA
Input Current Low (Pins 7, 9)	Vi = 0.4V			-400			-400	µA
Input Current High (Pins 7, 8, 9)	Vi = 2.4V			10			10	µA
Comparator Threshold (Pin 10)	VR = 5V, Io = L, I1 = L	400	415	430	400	415	430	mV
	VR = 5V, Io = H, I1 = L	240	255	265	290	300	315	mV
	VR = 5V, Io = L, I1 = H	70	80	90	195	210	225	mV
Comparator Input Current (Pin 10)				±20			±20	µA
Off Time	RT = 56k, CT = 820pF	25	30	35	25	30	35	ms

**ELECTRICAL CHARACTERISTICS (cont.):** (All tests apply with  $V_M = 36V$ ,  $V_{CC} = 5V$ ,  $V_R = 5V$ , No Load, and  $0^\circ C < T_A < 70^\circ C$ , unless otherwise stated,  $T_A = T_J$ .)

PARAMETER	TEST CONDITIONS	UC3770A			UC3770B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn Off Delay				2			2	ms
Sink Driver Saturation Voltage	$I_M = 1.0A$			0.8			0.8	V
	$I_M = 1.3A$			1.3			1.3	V
Source Driver Saturation Voltage	$I_M = 1.0A$			1.3			1.3	V
	$I_M = 1.3A$			1.6			1.6	V
Output Leakage Current	$V_M = 45V$			100			100	$\mu A$

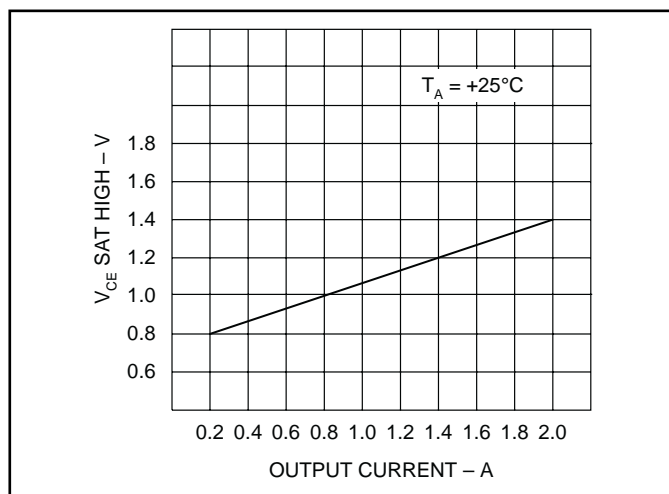


Figure 1. Typical source saturation voltages vs. load current

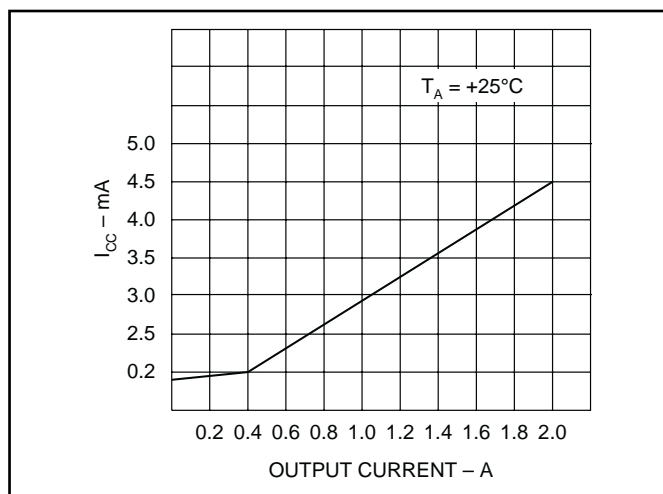


Figure 3. Typical supply current vs. load current.

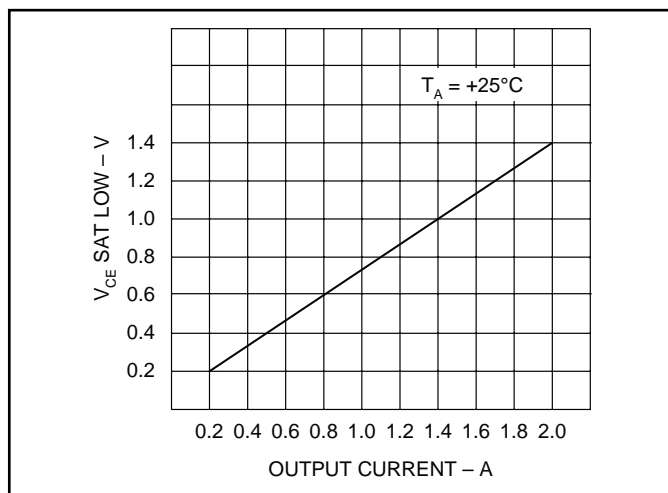


Figure 2. Typical sink saturation voltages vs. load current

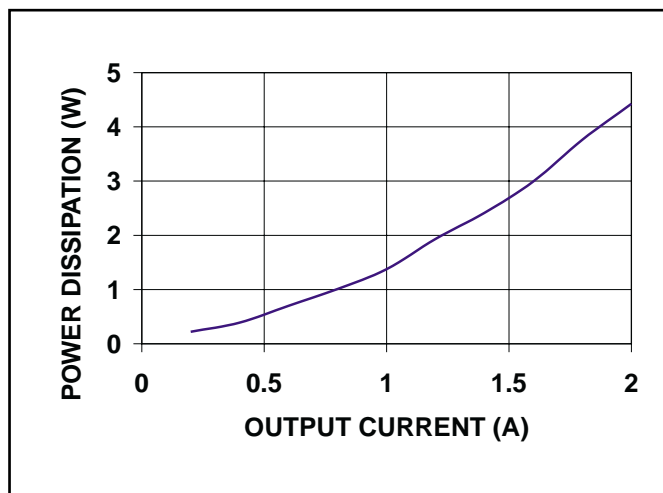


Figure 4. Typical power dissipation vs. output current.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC3770AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3770AN	<a href="#">Samples</a>
UC3770ANG4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3770AN	<a href="#">Samples</a>
UC3770BN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UC3770BN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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