TEXAS INSTRUMENTS

TPS65130, TPS65131

SLVS493D – MARCH 2004 – REVISED JANUARY 2016

TPS6513x Positive and Negative Output DC-DC Converter

1 Features

- 2.7-V to 5.5-V Input Voltage Range
- Dual Adjustable Output Voltages Up to 15 V and Down to –15 V
- 800-mA Typical Switch Current Limit at Boost and Inverter Main Switches at TPS65130
- 2-A Typical Switch Current Limit at Boost and Inverter Main Switches at TPS65131
- Up to 89% Efficiency at Positive Output Voltage Rail
- Up to 81% Efficiency at Negative Output Voltage Rail
- Power-Save Mode for High Efficiency at Low Load Currents
- Independent Enable Inputs for Power-Up and Power-Down Sequencing
- Control Output for External PFET to Support Completely Disconnecting the Battery
- Minimum 1.25-MHz Fixed Frequency PWM Operation
- Thermal Shutdown
- Overvoltage Protection on Both Outputs
- 1-µA Shutdown Current
- Small 4-mm x 4-mm VQFN-24 Package (RGE)

2 Applications

- LCD and OLED Displays
- Industrial Applications
- Data Acquisition
- Audio
- General-Purpose Split-Rail Supplies

3 Description

The TPS6513x is dual-output DC-DC converter generating a positive output voltage up to 15 V and a negative output voltage down to –15 V with output currents in a 200-mA range in typical applications, depending on input voltage to output voltage ratio. With a total efficiency up to 85%, the device is ideal for portable battery-powered equipment. The input voltage range of 2.7 V to 5.5 V allows the devices to be powered from batteries or from fixed 3.3-V or 5-V supplies. The TPS6513x comes in a small 4-mm × 4-mm VQFN-24 package. Together with a minimum switching frequency of 1.25 MHz, the device enables designing small power supply applications because it requires only a few small external components.

The converter operates with a fixed frequency PWM control topology and, if power-save mode is enabled, it uses a pulse-skipping mode at light-load currents. It operates with only 500-µA device quiescent current. Independent enable pins allow power-up and power-down sequencing for both outputs. The device has an internal current limit overvoltage protection and a thermal shutdown for highest reliability under fault conditions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65130	VQFN (24)	4.00 mm × 4.00 mm
TPS65131	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
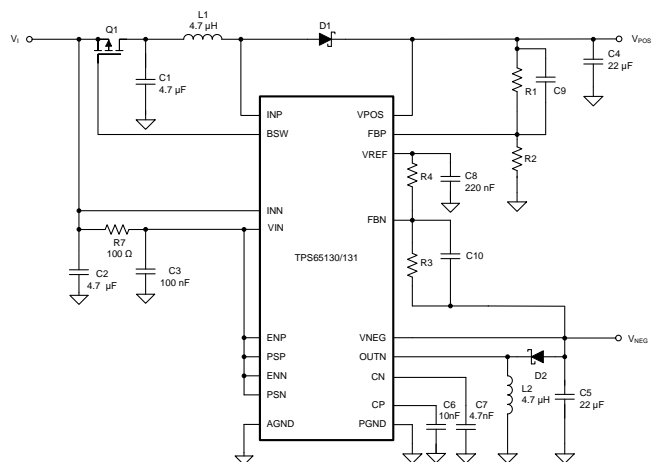
Typical Application Schematic

Table of Contents

4 Revision History

Changes from Revision C (June 2015) to Revision D   **Page**

Changes from Revision B (September 2004) to Revision C   **Page**

5 Pin Configuration and Functions

RGE Package
24-PIN VQFN With PowerPAD™
Top View

NC − No internal connection
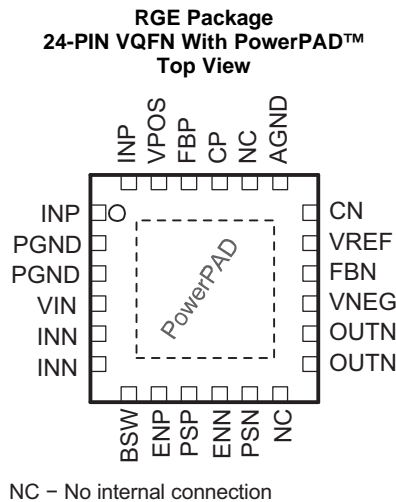
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	19	—	Analog ground pin
BSW	7	O	Gate control pin for external battery switch. This pin goes low when ENP is set high.
CN	18	—	Compensation pin for inverting converter control
CP	21	—	Compensation pin for boost converter control
ENN	10	I	Enable pin for the negative output voltage (0 V: disabled, VIN: enabled)
ENP	8	I	Enable pin for the positive output voltage (0 V: disabled, VIN: enabled)
FBN	16	I	Feedback pin for the negative output voltage divider
FBP	22	I	Feedback pin for the positive output voltage divider
INN	5, 6	I	Inverting converter switch input
INP	1, 24	I	Boost converter switch input.
NC	12, 20	—	Not connected
OUTN	13, 14	O	Inverting converter switch output.
PGND	2, 3	—	Power ground pin
PSN	11	I	Power-save mode enable for inverter stage (0 V: disabled, VIN: enabled)
PSP	9	I	Power-save mode enable for boost converter stage (0 V: disabled, VIN: enabled)
VIN	4	I	Control supply input
VNEG	15	I	Negative output voltage sense input
VPOS	23	I	Positive output voltage sense input
VREF	17	O	Reference output voltage. Bypass this pin with a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted [1]

		MIN	MAX	UNIT
VIN, INN	Input voltage at pins [2]	–0.3	6	V
VPOS	Maximum voltage at pin [2]	–0.3	17	V
VNEG	Minimum voltage at pin [2]	–17	V_{IN} + 0.3	V
	Voltage at pins ENN, ENP, FBP, FBN, CN, CP, PSP, PSN, BSW [2]	–0.3	V_{IN} + 0.3	V
INP	Input voltage at pin [2]	–0.3	17	V
	Differential voltage between pins OUTN to V_{INN} [2]	–0.3	24	V
T_J	Operating virtual junction temperature	–40	150	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature, unless otherwise noted

		MIN	MAX	UNIT
V_I , V_{IN}, V_{INN}	Application input voltage range, input voltage range at VIN and INN pins	2.7	5.5	V
V_{POS}	Adjustable output voltage range for the boost converter	V_I + 0.5	15	V
V_{NEG}	Adjustable output voltage range for the inverting converter	–15	–2	V
V_{ENN}, V_{ENP}	Enable signals voltage	0	5.5	V
V_{PSN}, V_{PSP}	Power-save mode enable signals voltage	0	5.5	V
T_A	Operating free-air temperature range	–40	85	°C
T_J	Operating junction temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS65130	TPS65131	UNIT
		RGE (VQFN)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	36.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.2	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.3	12.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and the *IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *TPS65130 TPS65131*

6.5 Electrical Characteristics

This specification applies over the full recommended input voltage range V_I = 2.7 V to 5.5 V and over the temperature range T_J = –40°C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE (V_{POS}, V_{NEG})						
V_{POS}	Adjustable output voltage range		V_{IN}+ 0.5 V		15	V
V_{NEG}	Adjustable output voltage range		–15		–2	V
V_{REF}	Reference voltage	I_{REF} = 10 μA	1.2	1.213	1.225	V
I_{FBP}	Positive feedback input bias current	$V_{FBP} = V_{REF}$		50		nA
I_{FBN}	Negative feedback input bias current	$V_{FBN} = 0.1\ V_{REF}$		50		nA
V_{FBP}	Positive feedback regulation voltage	V_{IN} = 2.7 V to 5.5 V	1.189	1.213	1.237	V
V_{FBN}	Negative feedback regulation voltage	V_{IN} = 2.7 V to 5.5 V	–0.024	0	0.024	V
	Total Output DC accuracy			3%		
$r_{DS(ON)(N)}$	Inverter switch ON-resistance	V_{IN} = 3.6 V		440	620	mΩ
		V_{IN} = 5 V		330	530	
I_{LIMN}	TPS65130 Inverter switch current limit	2.7 V < V_{IN} < 5.5 V	700	800	900	mA
I_{LIMN}	TPS65131 Inverter switch current limit	V_{IN} = 3.6 V	1800	1950	2200	mA
$r_{DS(ON)(P)}$	Boost switch ON-resistance	V_{POS} = 5 V		230	300	mΩ
		V_{POS} = 10 V		170	200	
I_{LIMP}	TPS65130 Boost switch current limit	2.7 V < V_{IN} < 5.5 V	700	800	900	mA
I_{LIMP}	TPS65131 Boost switch current limit	V_{IN} = 3.6 V, V_{POS} = 8 V	1800	1950	2200	mA
CONTROL STAGE						
V_{IH}	High level input voltage, ENP, ENN, PSP, PSN		1.4			V
V_{IL}	Low level input voltage, ENP, ENN, PSP, PSN				0.4	V
I_{IN}	Input current, ENP, ENN, PSP, PSN	ENP, ENN, PSP, PSN = GND or V_{IN}		0.01	0.1	μA
R_{BSW}	Output resistance			27		kΩ
V_{IN}	Input voltage range		2.7		5.5	V
I_Q	Quiescent current	VIN	V_{IN} = 3.6 V, $I_{POS} = I_{NEG}$ = 0, ENP = ENN = PSP = PSN = V_{IN}, V_{POS} = 8 V, V_{NEG} = –5 V		300	500	μA
		VPOS			100	120	μA
		VNEG			100	120	μA
I_{SD}	Shutdown supply current	ENN = ENP = GND		0.2	1.5	μA
V_{UVLO}	Undervoltage lockout threshold		2.1	2.35	2.7	V
	Thermal shutdown			150		°C
	Thermal shutdown hysteresis	Junction temperature decreasing		5		°C

6.6 Switching Characteristics

This specification applies over the full recommended input voltage range V_I = 2.7 V to 5.5 V and over the temperature range T_J = –40°C to 125°C unless otherwise noted. Typical values apply for V_I = 3.6 V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY						
f_S	Oscillator frequency		1250	1380	1500	kHz
DUTY CYCLE						
D_{MAXP}	Maximum duty cycle boost converter			87.5%		
D_{MAXN}	Maximum duty cycle inverting converter			87.5%		
D_{MINP}	Minimum duty cycle boost converter			12.5%		
D_{MINN}	Minimum duty cycle inverting converter			12.5%		

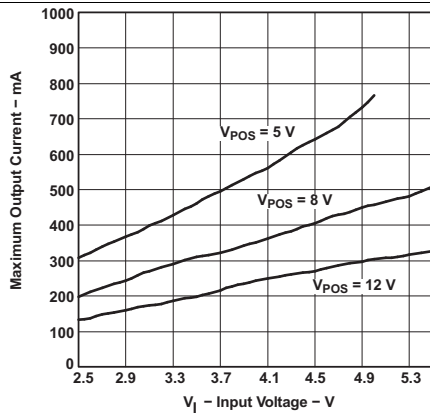## 6.7 Typical Characteristics

At 25°C, unless otherwise noted.

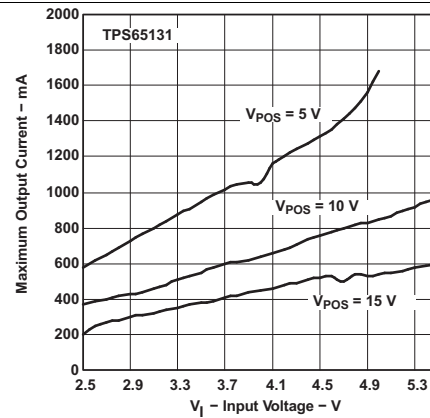**Figure 1. TPS65130 Maximum Output Current (V_{POS}) vs Input Voltage**

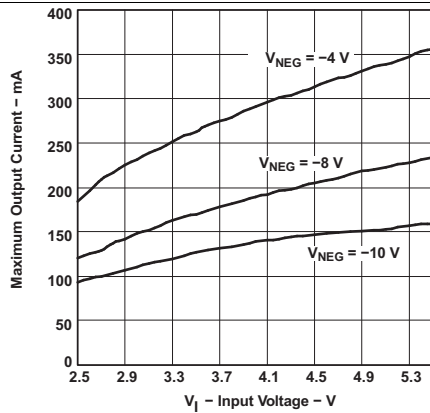**Figure 2. TPS65131 Maximum Output Current (V_{POS}) vs input Voltage**

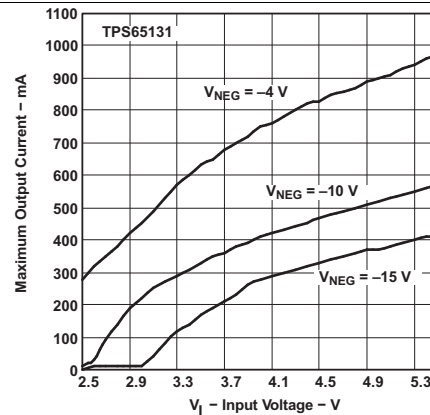**Figure 3. TPS65130 Maximum Output Current (V_{NEG}) vs Input Voltage**

Figure 4. TPS65131 Maximum Output Current (V_{NEG}) vs Input Voltage
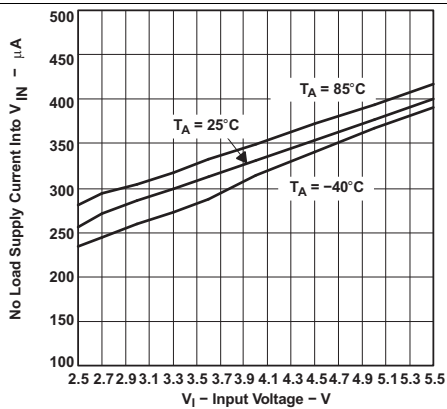

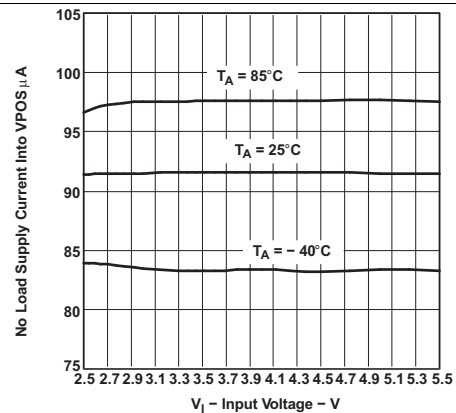**Figure 5. No Load Supply Current into V_{IN} vs Input Voltage**

Figure 6. No Load Supply Current into V_{POS} vs Input Voltage

Product Folder Links: *TPS65130 TPS65131*

Typical Characteristics (continued)

At 25°C, unless otherwise noted.
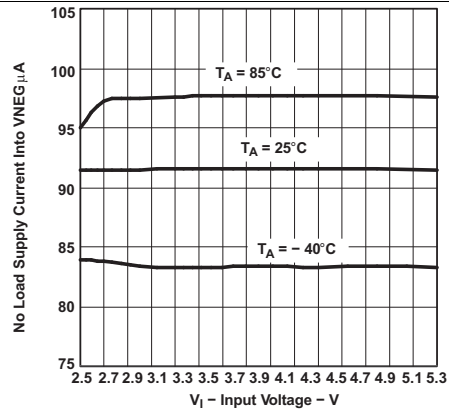
Figure 7. No Load Supply Current into V_{NEG} vs Input Voltage

Product Folder Links: *TPS65130 TPS65131*

7 Detailed Description

7.1 Overview

The TPS6513x operates with an input voltage range of 2.7 V to 5.5 V and can generate both a positive and negative output. Both converters work independently of each other. They only share a common clock and a common voltage reference. Both outputs are separately controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. In general, each converter operates at continuous conduction mode (CCM). At light loads, the negative converter can enter discontinuous conduction mode (DCM). As the load current decreases, the converters can enter a power-save mode if enabled. This works independently at both converters. Output voltages can go up to 15 V at the boost output and down to –15 V at the inverter output.

7.2 Functional Block Diagram
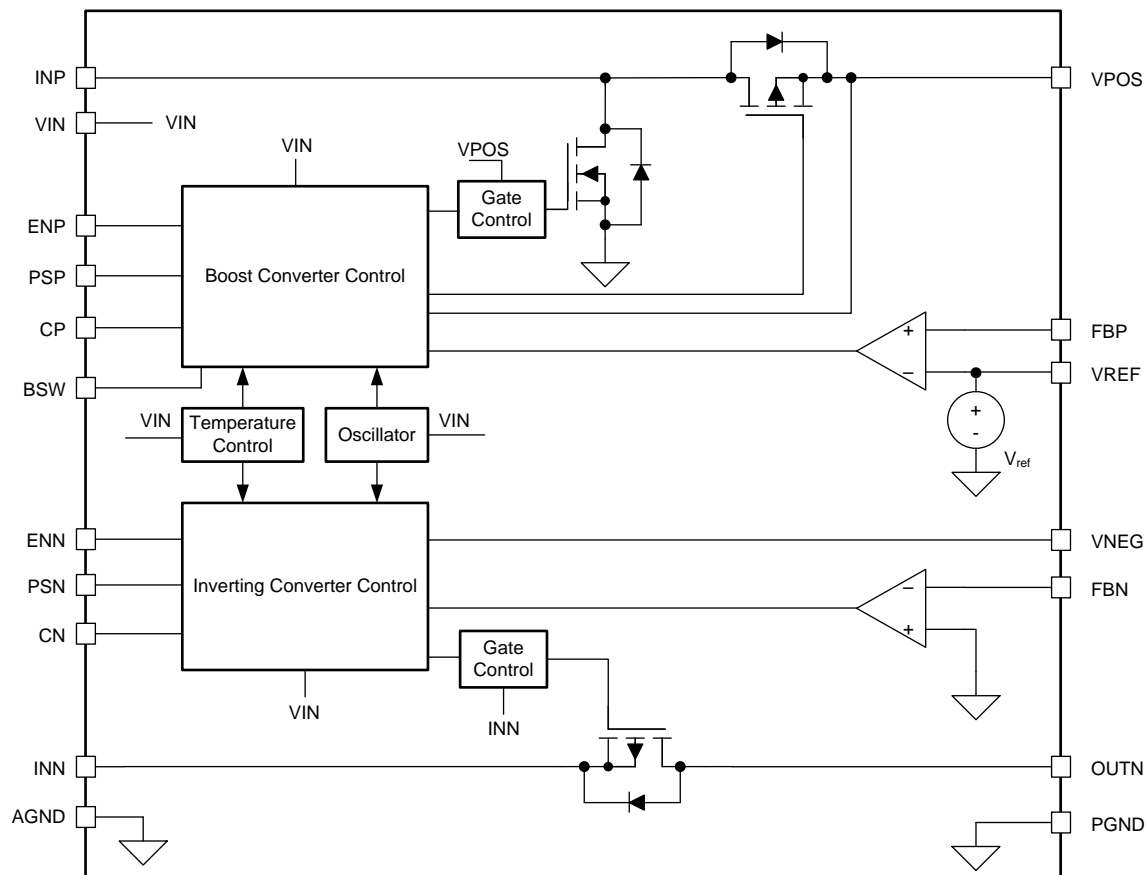
7.3 Feature Description

7.3.1 Power Conversion

Both converters operate in a fixed-frequency, PWM control scheme. So, the ON-time of the switches varies depending on input-to-output voltage ratio and the load. During this ON-time, the inductors connected to the converters charge with current. In the remaining time, the time period set by the fixed operating frequency, the inductors discharge into the output capacitors through the rectifier diodes. Usually at greater loads, the inductor currents are continuous. At lighter loads, the boost converter uses an additional internal switch to allow current flowing back to the input. This avoids inductor current becoming discontinuous in the boost converter. So, the boost converter is always controlled in a continuous current mode. At the inverting converter, during light loads, the inductor current can become discontinuous. In this case, the control circuit of the inverting controller output automatically takes care of these changing conditions to always operate with an optimum control setup.

Feature Description (continued)

7.3.2 Control

The controller circuits of both converters employ a fixed-frequency, multiple-feedforward controller topology. The circuits monitor input voltage, output voltage, and voltage drop across the switches. Changes in the operating conditions of the converters directly affect the duty cycle and must not take the indirect and slow way through the output voltage control loops. Measurement errors in this feedforward system are corrected by a self-learning control system. An external capacitor damps the output to avoid output-voltage steps due to output changes of this selflearning control system.

The voltage loops, determined by the error amplifiers, must only handle small signal errors. The error amplifiers feature internal compensation. Their inputs are the feedback voltages on the FBP and FBN pins. The device uses a comparison of these voltages with the internal reference voltage to generate an accurate and stable output voltage.

7.3.3 Enable

Both converters can be enabled or disabled individually. Applying a logic HIGH signal at the enable pins (ENP for the boost converter, ENN for the inverting converter) enables the corresponding output. After enabling, internal circuitry, necessary to operate the specific converter, then turns on, followed by the *Soft-Start*.

AApplying a low signal at the enable ENP or ENN pin shuts down the corresponding converter. When both enable pins are low, the device enters shutdown mode, where all internal circuitry turns off. The device now consumes shutdown current flowing into the VIN pin. The output loads of the converters can be disconnected from the input, see *Load Disconnect*.

7.3.4 Load Disconnect

The device supports completely disconnecting the load when the converters are disabled. For the inverting converter, the device turns off the internal PMOS switch. If the inverting converter is turned off, no DC current path remains which could discharge the battery or supply.

This is different for the boost converter. The external rectifying diode, together with the boost inductor, form a DC current path which could discharge the battery or supply if any load connects to the output. The device has no internal switch to prevent current from flowing. For this reason, the device offers a PMOS gate control output (BSW) to enable and disable a PMOS switch in this DC current path, ideally directly between the boost inductor and battery. To be able to fully disconnect the battery, the forward direction of the parasitic backgate diode of this switch must point to the battery or supply. The external PMOS switch, which connects to BSW, turns on when the boost converter is enabled and turns off when the boost converter is disabled.

7.3.5 Soft-Start

Both converters have implemented soft-start functions. When each converter is enabled, the implemented switch current limit ramps up slowly to its nominal programmed value in about 1 ms. Soft-start is implemented to limit the input current during start-up to avoid high peak currents at the battery which could interfere with other systems connected to the same battery. Without soft-start, the high input peak current could trigger the implemented switch current limit, which can lead to a significant voltage drops across the series resistance of the battery and its connections.

7.3.6 Overvoltage Protection

Both converters (boost and inverter) have implemented individual overvoltage protection. If the feedback voltage under normal operation exceeds the nominal value by typically 5%, the corresponding converter shuts down immediately to protect any connected circuitry from possible damage.

7.3.7 Undervoltage Lockout

An undervoltage lockout (UVLO) prevents the device from starting up and operating if the supply voltage at the VIN pin is lower than the undervoltage lockout threshold. For this case, the device automatically shuts down both converters when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown.

Submit Documentation Feedback   9

Product Folder Links: *TPS65130 TPS65131*

Feature Description (continued)

7.3.8 Overtemperature Shutdown

The device automatically shuts down both converters if the implemented internal temperature sensor detects a chip temperature above the thermal shutdown temperature. It automatically starts operating again when the chip temperature falls below this thermal shutdown temperature. The built-in hysteresis avoids undefined operation caused by ringing from shutdown and prevents operating at a temperature close to the overtemperature shutdown threshold.

7.4 Device Functional Modes

7.4.1 Power-Save Mode

The power-save mode can improve efficiency at light loads. In power-save mode, the converter only operates when the output voltage falls below an device internally set threshold voltage. The converter ramps up the output voltage with one or several operating pulses and goes again into power-save mode once the inductor current becomes discontinuous.

The PSN and PSP logic level selects between power-save mode and continuous-conduction mode. If the specific pins (PSP for the boost converter, PSN for the inverting converter) are HIGH, the power-save mode for the corresponding converter operates at light loads. Similarly, a LOW on the PSP pin or PSN pin disables the power-save mode for the corresponding converter.

7.4.2 Full Operation with $V_{IN} > 2.7$ V

The recommended minimum input supply voltage for the TPS6513x device is 2.7 V. Above this voltage, the device achieves the performance described in this data sheet.

7.4.3 Limited Operation with $V_{UVLO} < V_{IN} < 2.7$ V

With input supply voltages between V_{UVLO} and 2.7 V, the device continues to operate — no functions are disabled — but full performance is not ensure.

7.4.4 No Operation with $V_{IN} < V_{UVLO}$

The TPS6513x enters an undervoltage lockout condition when the input supply voltage is below the UVLO threshold. In this mode, all device functions are disabled, and the input supply current consumption is minimized. See also the *Undervoltage Lockout* section.

Product Folder Links: *TPS65130 TPS65131*

8 Applications and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS6513x boost converter output voltage, V_{POS}, and the inverting converter output voltage, V_{NEG}, require external components to set the required output voltages. The valid output voltage ranges are as shown in *Recommended Operating Conditions*. The following sections show a typical application example with different output voltage settings and guidance for external component choices.

8.2 Typical Application
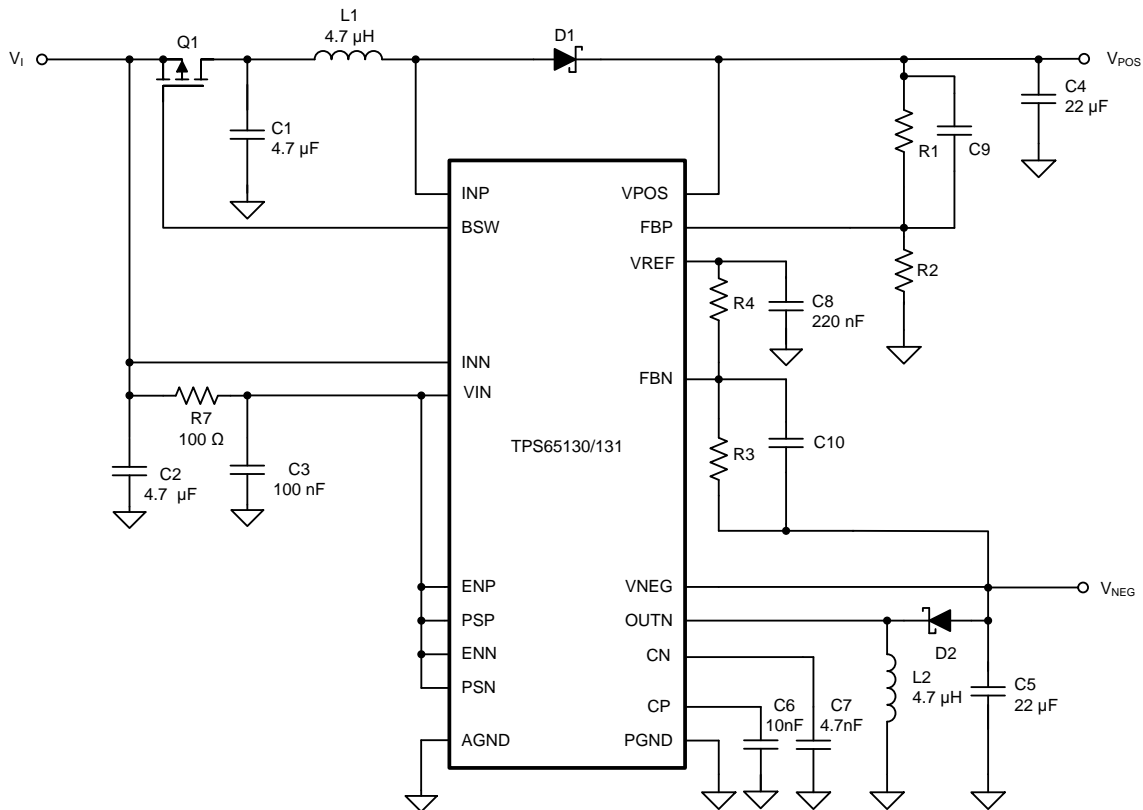
Figure 8. Typical Application Schematic With V_{POS} = 10.5 V, V_{NEG} = −10 V

Product Folder Links: *TPS65130 TPS65131*

Typical Application (continued)

8.2.1 Design Requirements

Figure 8 uses the following parameters:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE	
Input voltage range	2.7 V to 5.5 V	
Boost converter output voltage, V_{POS}	R1 = 1 MΩ R2 = 130kΩ C9 = 6.8 pF	10.5 V
Inverting converter output voltage, V_{NEG}	R3 = 1 MΩ R4 = 121.2 kΩ C10 = 7.5 pF	−10 V

Table 2. List of Components

REFERENCE	SETUP	VALUE, DESCRIPTION
C1, C2	—	4.7 µF, ceramic, 6.3 V, X5R
C3		0.1 µF, ceramic, 10 V, X5R
C4, C5		4 x 4.7 µF, ceramic, 25 V, X7R
C6		10 nF, ceramic, 16 V, X7R
C7		4.7 nF, 50 V, C0G
C8		220 nF, ceramic, 6.3 V, X5R
R1	V_{POS} = 10.5 V	1 MΩ
	V_{POS} = 15 V	975 kΩ
R2	V_{POS} = 10.5 V	130 kΩ
	V_{POS} = 15 V	85.8 kΩ
R3	V_{NEG} = −10 V	1 MΩ
	V_{NEG} = −15 V	1.3 MΩ
R4	V_{NEG} = −10 V	121.2 kΩ
	V_{NEG} = −15 V	104.8 kΩ
R7	—	100 Ω
D1, D2		Schottky, 1 A, 20 V, Onsemi MBRM120
L1, L2		Wurth Elektronik 7447789004 (TPS65130), EPCOS B82462-G4472 (TPS65131)
Q1		MOSFET, P-channel, 12 V, 4 A, Vishay Si2323DS

8.2.2 Detailed Design Procedure

The TPS6513x DC-DC converter is intended for systems typically powered by a single-cell Li-ion or Li-polymer battery with a terminal voltage from 2.7 V up to 4.2 V. Because the recommended input voltage goes up to 5.5 V, the device is also suitable for 3-cell alkaline, NiCd, or NiMH batteries, as well as any regulated supply voltages from 2.7 V to 5.5 V. It provides two independent output voltage rails which are programmed as follows.

8.2.2.1 *Programming the Output Voltage*

8.2.2.1.1 Boost Converter

The output voltage of the TPS6513x boost converter stage can be adjusted with an external resistor divider connected to the FBP pin. The typical value of the voltage at the FBP pin is the reference voltage, which is 1.213 V. The maximum recommended output voltage at the boost converter is 15 V. To achieve appropriate accuracy, the current through the feedback divider should be about 100 times greater than the current into the FBP pin. Typical current into the FBP pin is 0.05 µA, and the voltage across R2 is 1.213 V. Based on those values, the recommended value for R2 should be lower than 200 kΩ to set the divider current at 5 µA or greater.

Calculate the value of resistor R1, as a function of the needed output voltage (V_{POS}), with Equation 1:

$$R1 = R2 \times \left(\frac{V_{POS}}{V_{ref}} - 1 \right)$$

(1)

In this example, with R2 = 130 kΩ, choose R1 = 1 MΩ to set V_{POS} = 10.5 V.

8.2.2.1.2 Inverting Converter

The output voltage of the inverting converter stage can also be adjusted with an external resistor divider. It must be connected to the FBN pin. Unlike the feedback divider at the boost converter, the reference point of the feedback divider is not GND but V_{REF}. So the typical value of the voltage at the FBN pin is 0 V. The minimum recommended output voltage at the inverting converter is −15 V. Feedback divider current considerations are similar to the considerations at the boost converter. For the same reasons, the feedback divider current should be in the range of 5 µA or greater. The voltage across R4 is 1.213 V. Based on those values, the recommended value for R4 should be lower than 200 kΩ to set the divider current at the required value.

Calculate the value of resistor R3, as a function of the needed output voltage (V_{NEG}), with Equation 2:

$$R3 = -R4 \times \left(\frac{V_{NEG}}{V_{ref}} \right)$$

(2)

In this example, with R4 = 121.2 kΩ, choose R3 = 1 MΩ to set V_{NEG} = −10 V.

8.2.2.2 Inductor Selection

An inductive converter normally requires two main passive components for storing energy during the conversion. Therefore, each converter requires an inductor and a storage capacitor. In selecting the right inductor, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. To select the right inductor, TI recommends keeping the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the switch for the boost converter and for the inverting converters is nominally 800 mA for the TPS65130 device and 1950 mA for TPS65131 device. The highest peak current through the switches and the inductor depend on the output load, the input voltage (V_{IN}), and the output voltages (V_{POS}, V_{NEG}). Use Equation 3 to estimate the peak inductor current in the boost converter, I_{L_P}. Equation 4 shows the corresponding formula for the inverting converter, I_{L_N}.

$$I_{(L-P)} = \frac{V_{POS}}{V_I \times 0.64} \times I_{POS}$$

(3)

$$I_{(L-N)} = \frac{V_I - V_{NEG}}{V_I \times 0.64} \times I_{NEG}$$

(4)

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the losses in the inductor, as well as output voltage ripple and EMI. But in the same way, output voltage regulation gets slower, causing greater voltage changes at fast load changes. In addition, a larger inductor usually increases the total system cost. Keep those parameters in mind and calculate the possible inductor value with Equation 5 for the boost converter and Equation 6 for the inverting converter.

$$L1 = \frac{V_I \times (V_{POS} - V_I)}{\Delta I_{(L-P)} \times f \times V_{POS}}$$

(5)

$$L2 = \frac{V_I \times V_{NEG}}{\Delta I_{(L-N)} \times f \times (V_{NEG} - V_I)}$$

(6)

Parameter f is the switching frequency. For the boost converter, ΔI_{L-P} is the ripple current in the inductor, that is, 20% of I_{L-P}. Accordingly, for the inverting converter, ΔI_{L-N} is the ripple current in the inductor, that is, 20% of I_{L-N}. V_I is the input voltage, which is 3.3 V in this example. So, the calculated inductance value for the boost inductor is 5.1 µH and for the inverting converter inductor is 5.1 µH. With these calculated values and the calculated currents, it is possible to choose a suitable inductor.

In typical applications, the recommendation is to choose a 4.7-µH inductor. The device is optimized to work with inductance values from 3.3 µH to 6.8 µH. Nevertheless, operation with greater inductance values may be possible in some applications. Perform detailed stability analysis in this case. Be aware of the possibility that load transients and losses in the circuit can lead to higher currents than estimated in Equation 3 and Equation 4. Also, the losses caused by magnetic hysteresis and conductor resistance are a major parameter for total circuit efficiency.

Table 3 shows inductors from different suppliers used with the TPS6513x converter:

Table 3. List of Inductors

VENDOR	INDUCTOR SERIES
EPCOS	B8246284-G4
Wurth Elektronik	7447789XXX
	744031XXX
TDK	VLF3010
	VLF4012
Cooper Electronics Technologies	SD12

8.2.2.3 *Capacitor Selection*

8.2.2.3.1 Input Capacitor

As a recommendation, choose an input capacitors of at least 4.7 µF for the input of the boost converter (INP) and accordingly for the input of the inverting converter (INN). This improves transient behavior of the regulators and EMI behavior of the total power-supply circuit. Choose a ceramic capacitor or a tantalum capacitor. For the use of a tantalum capacitor, an additional, smaller ceramic capacitor (100 nF) in parallel is required. Place the input capacitor(s) close to the input pins..

8.2.2.3.2 Output Capacitors

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero. Use Equation 7 for the boost converter output capacitor (C4min) and Equation 8 for the inverting converter output capacitor (C5min).

$$C4\min = \frac{I_{POS} \times (V_{POS} - V_I)}{f \times \Delta V_{POS} \times V_{POS}}$$

(7)

$$C5\min = \frac{I_{NEG} \times V_{NEG}}{f \times \Delta V_{NEG} \times (V_{NEG} - V_I)}$$

(8)

The parameter f is the switching frequency. ΔV_{POS} and ΔV_{NEG} are the maximum allowed ripple voltages for each converter. Choosing a ripple voltage in the range of 10 mV requires a minimum capacitance of 12 µF. The total ripple is larger due to the ESR of the output capacitor. Use Equation 9 for he boost converter and Equation 10 for the inverting converter to calculate this additional ripple component.

$$\Delta V_{(ESR-P)} = I_{POS} \times R_{(ESR-C4)}$$

(9)

$$\Delta V_{(ESR-N)} = I_{NEG} \times R_{(ESR-C5)}$$

(10)

In this example, an additional ripple of 2 mV is the result of using a typical ceramic capacitor with an ESR in the 10-mΩ range. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 10 mV.

Load transients can create additional ripple. When the load current increases rapidly, the output capacitor must provide the additional current until the inductor current increases by the control loop which sets a higher ON-time (duty cycle) of the main switch. The higher duty cycle results in longer inductor charging periods. The inductance itself also limits the rate of increase of the inductor current. When the load current decreases rapidly, the output capacitor must store the excess energy (stored in the inductor) until the regulator has decreased the inductor current by reducing the duty cycle. TI recommends using greater capacitance values, as the foregoing calculations show.

8.2.2.4 Rectifier Diode Selection

Both converters (the boost and inverting converter) require rectifier diodes, D1 and D2. As a recommendation, to reduce losses, use Schottky diodes. The forward current rating needed is equal to the maximum output current. Consider that the maximum currents, I_{POS}max and I_{NEG}max, might differ for V_{POS} and V_{NEG} when choosing the diodes.

8.2.2.5 External PMOS Selection

During shutdown, when connected to a power supply, a path from the power supply to the positive output conducts through the inductor and an external diode. Optionally, to fully disconnect the positive output V_{POS} during shutdown, add an external PMOS (Q1). The BSW pin controls the gate of the PMOS. When choosing a proper PMOS, the V_{GS} and V_{GD} voltage ratings must cover the input voltage range, the drain current rating must not be lower than the maximum input current flowing into the application, and conditions of the PMOS operating area must fit.

If there is no intention to use an external PMOS, leave the BSW pin floating.

8.2.2.6 Stabilizing the Control Loop

8.2.2.6.1 Feedforward Capacitor

As a recommendation, to speed up the control loop, place feedforward capacitors in the feedback divider, parallel to R1 (boost converter) and R3 (inverting converter). Equation 11 shows how to calculate the appropriate value for the boost converter, and Equation 12 for the inverting converter.

$$C9 = \frac{6.8\ \mu s}{R1} \tag{11}$$

$$C10 = \frac{7.5\ \mu s}{R3} \tag{12}$$

To avoid coupling noise into the control loop from the feedforward capacitors, the feedforward effect can be bandwith-limited by adding a series resistor. Any value from 10 kΩ to 100 kΩ is suitable. The greater the resistance, the lower the noise coupled into the control loop system.

8.2.2.6.2 Compensation Capacitors

The device features completely internally compensated control loops for both converters. The internal feedforward system has built-in error correction which requires external capacitors. As a recommendation, use a 10-nF capacitor at the CP pin of the boost converter and a 4.7-nF capacitor at the CN pin of the inverting converter.

8.2.3 Application Curves

Figure 9. TPS65130 Efficiency vs Output Current

Figure 10. TPS65131 Efficiency vs Output Current

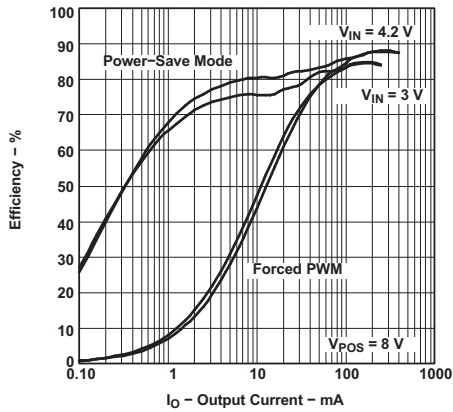Product Folder Links: *TPS65130 TPS65131*
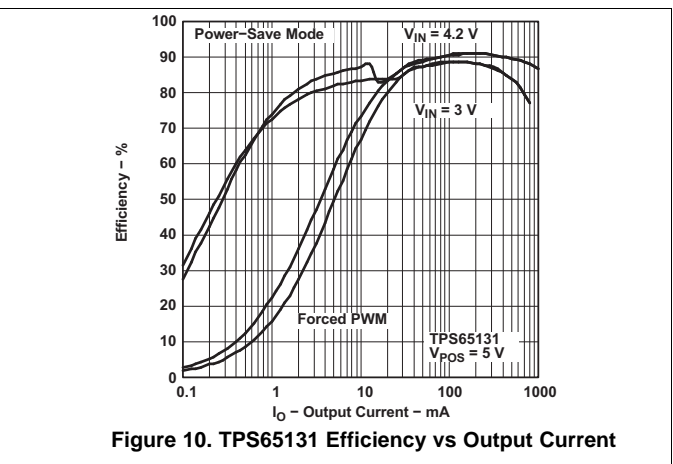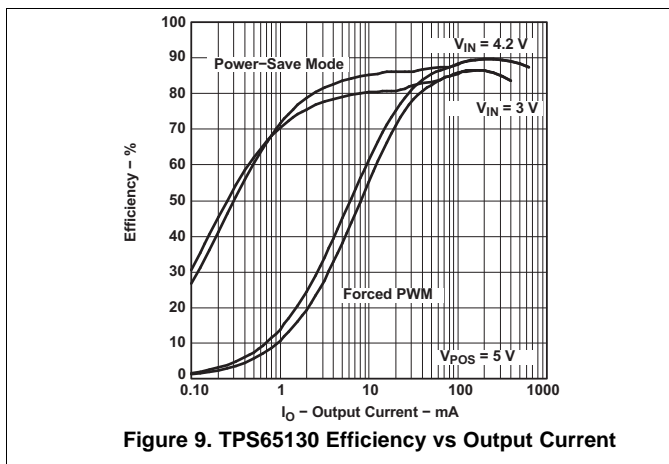
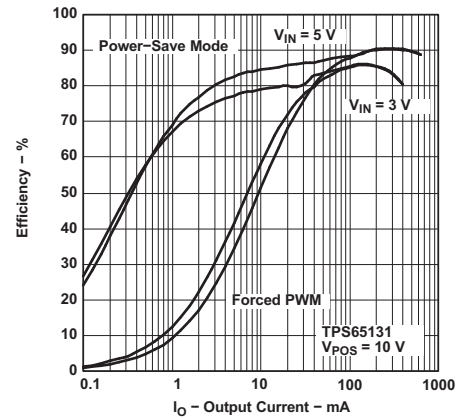Figure 11. TPS65130 Efficiency vs Output Current

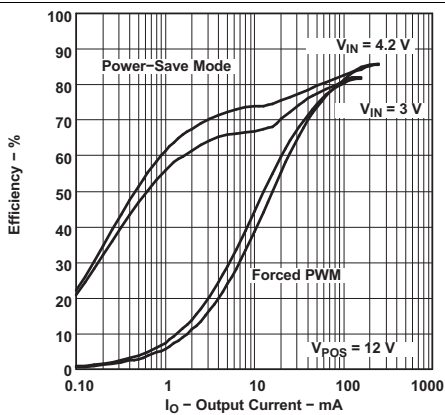Figure 12. TPS65131 Efficiency vs Output Current

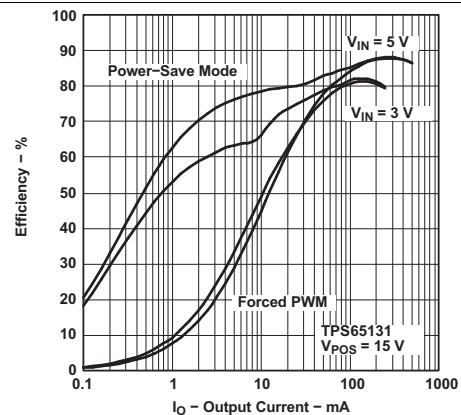Figure 13. TPS65130 Efficiency vs Output Current
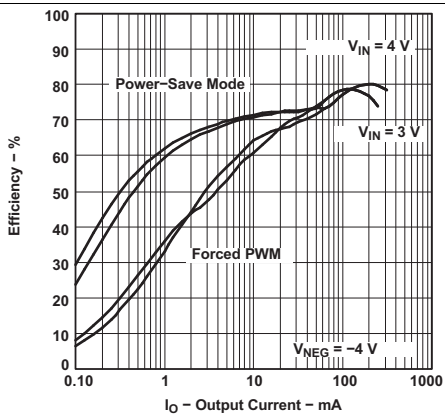

Figure 14. TPS65131 Efficiency vs Output Current
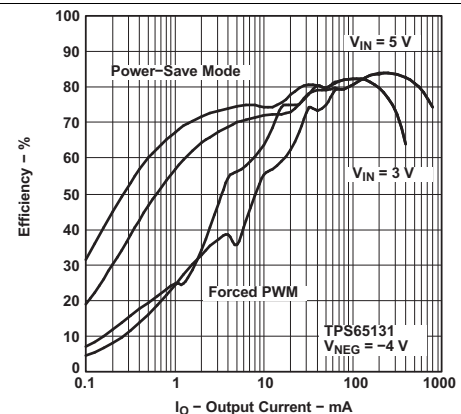

Figure 15. TPS65130 Efficiency vs Output Current
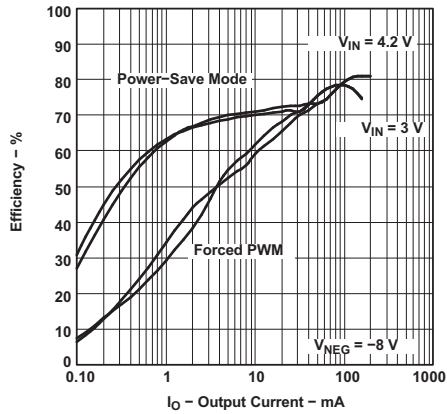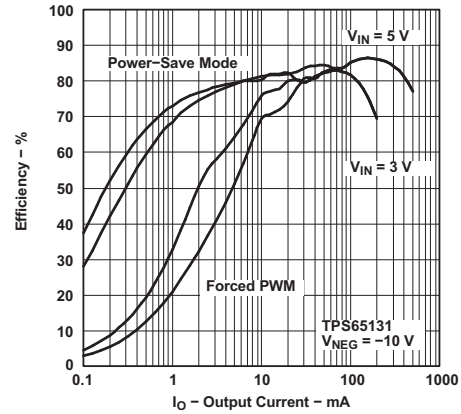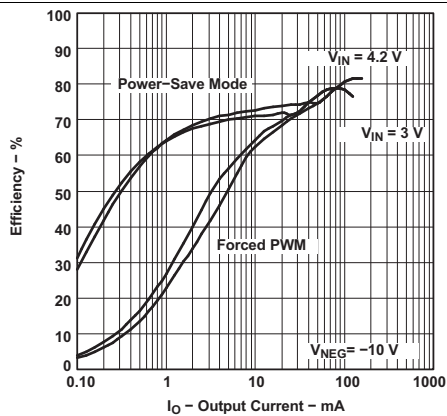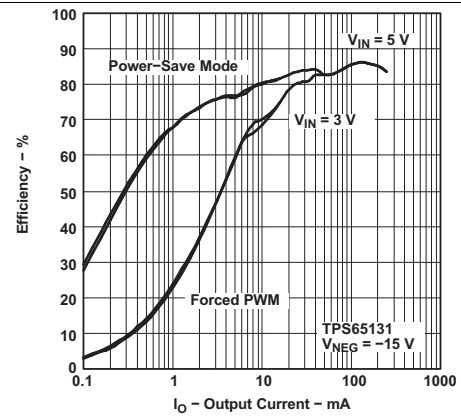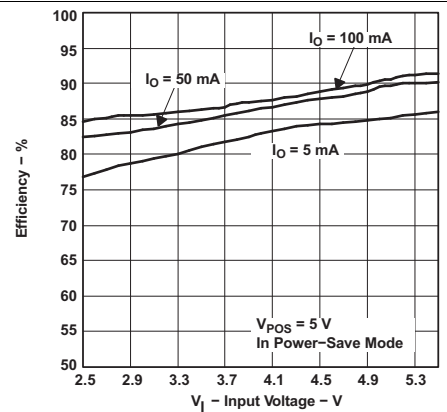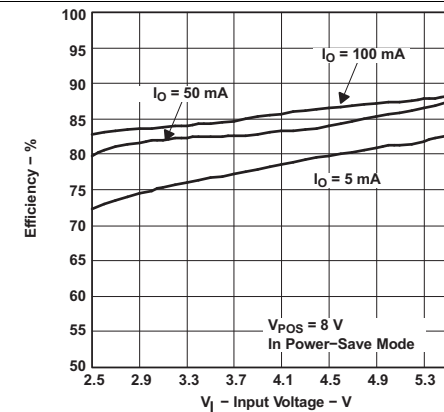

Figure 16. TPS65131 Efficiency vs Output Current

Product Folder Links: *TPS65130 TPS65131*

Figure 17. TPS65130 Efficiency vs Output Current

Figure 18. TPS65131 Efficiency vs Output Current

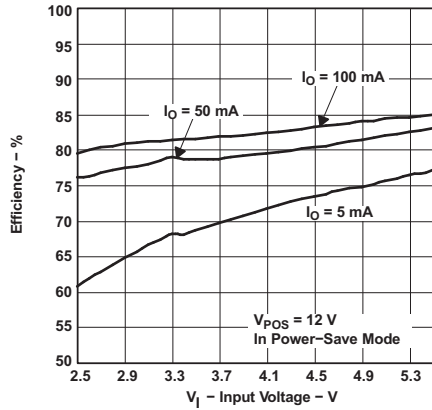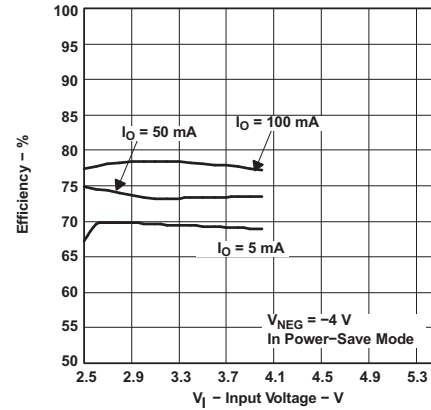Figure 19. TPS65130 Efficiency vs Output Current

Figure 20. TPS65131 Efficiency vs Output Current

Figure 21. TPS65130 Efficiency vs Input Voltage

Figure 22. TPS65130 Efficiency vs Input Voltage

Product Folder Links: *TPS65130 TPS65131*

Figure 23. TPS65130 Efficiency vs Input Voltage

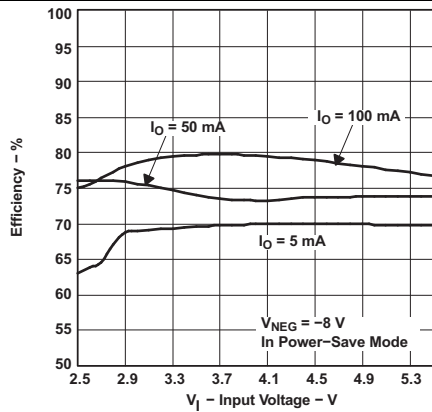Figure 24. TPS65130 Efficiency vs Input Voltage

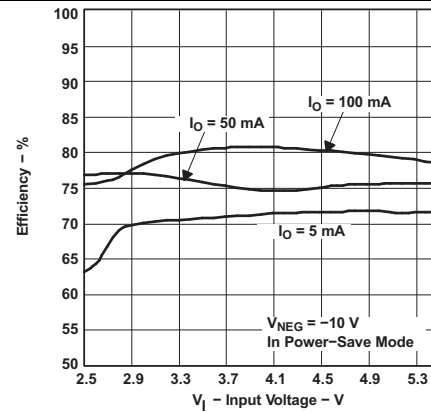Figure 25. TPS65130 Efficiency vs Input Voltage
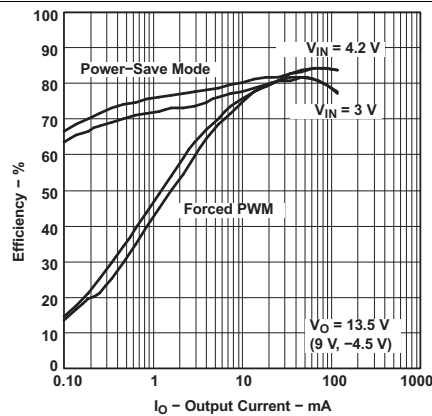

Figure 26. TPS65130 Efficiency vs Input Voltage

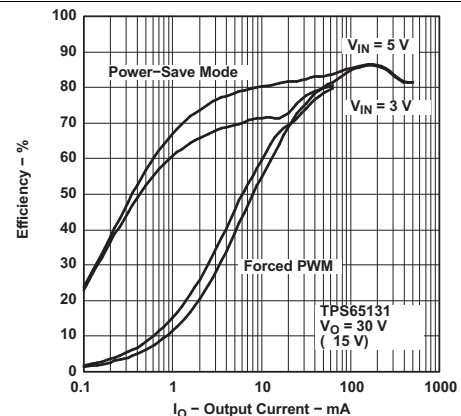Figure 27. TPS65130 Combined Efficiency vs Output Current

Figure 28. TPS65131 Combined Efficiency vs Output Current

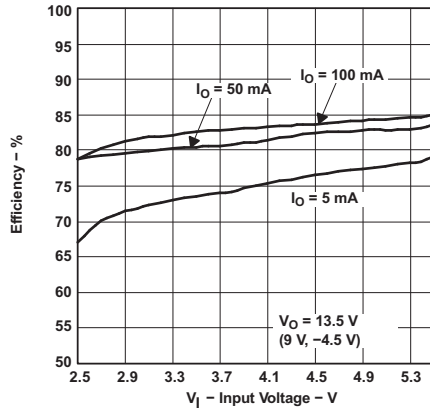Product Folder Links: *TPS65130 TPS65131*

Figure 29. TPS65130 Combined Efficiency vs Input Voltage
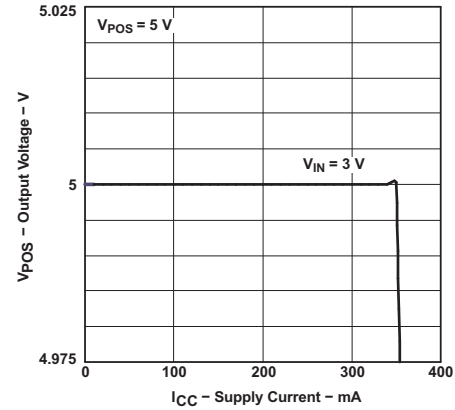

Figure 30. TPS65130 Output Voltage vs Output Current
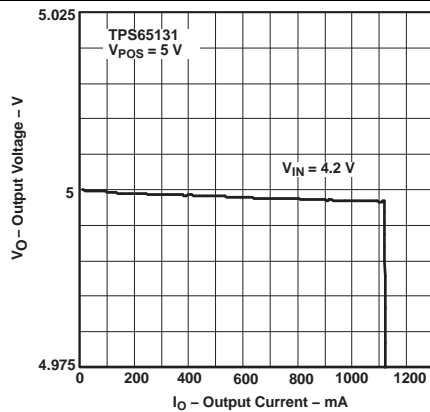

Figure 31. TPS65131 Output Voltage vs Output Current

Figure 32. TPS65130 Output Voltage vs Output Current

Figure 33. TPS65131 Output Voltage vs Output Current
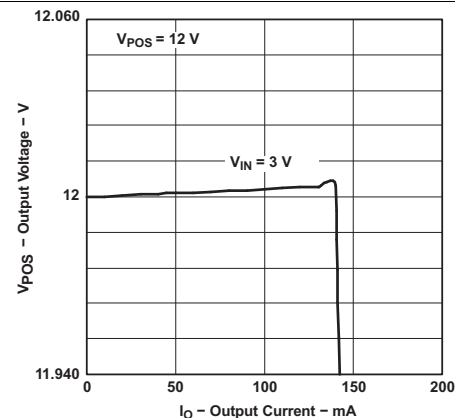
Figure 34. TPS65130 Output Voltage vs Output Current
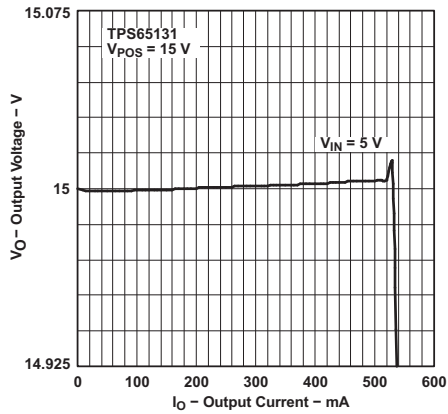
Figure 35. TPS65131 Output Voltage vs Output Current
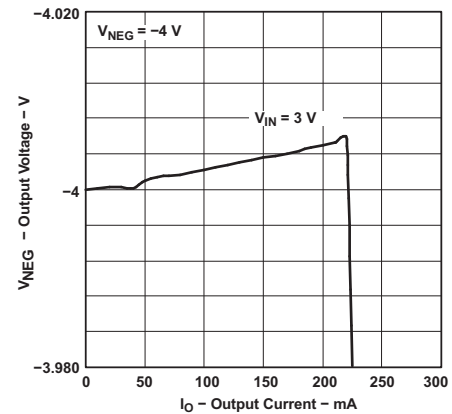
Figure 36. TPS65130 Output Voltage vs Output Current
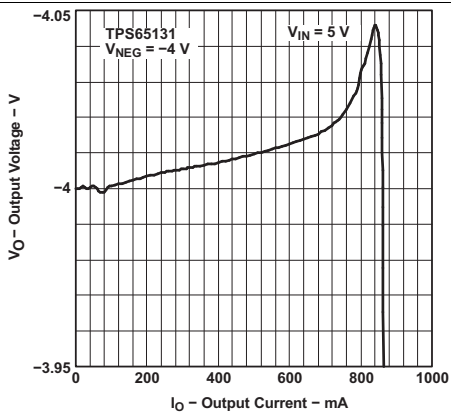
Figure 37. TPS65131 Output Voltage vs Output Current
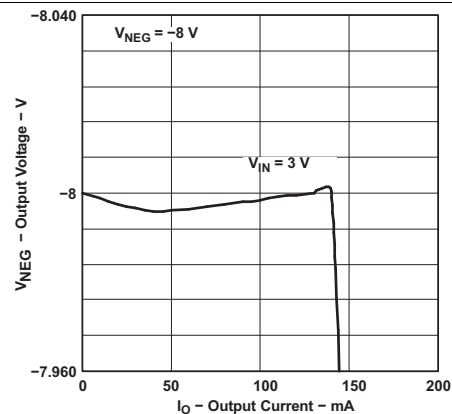
Figure 38. TPS65130 Output Voltage vs Output Current

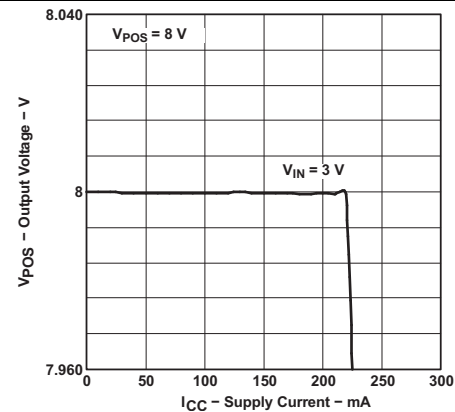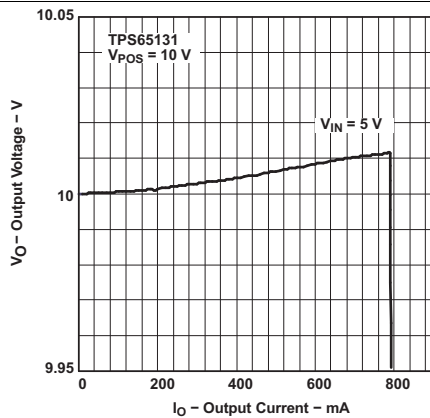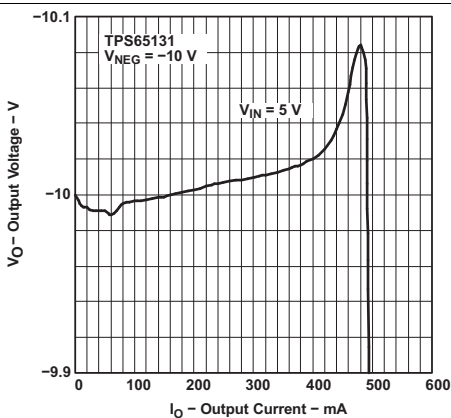**Figure 39. TPS65131 Output Voltage vs Output Current**
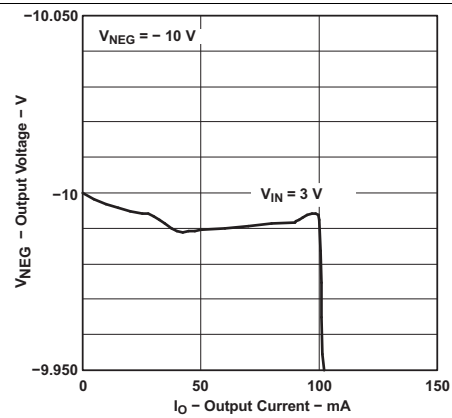
Figure 40. TPS65130 Output Voltage vs Output Current

Product Folder Links: *TPS65130 TPS65131*
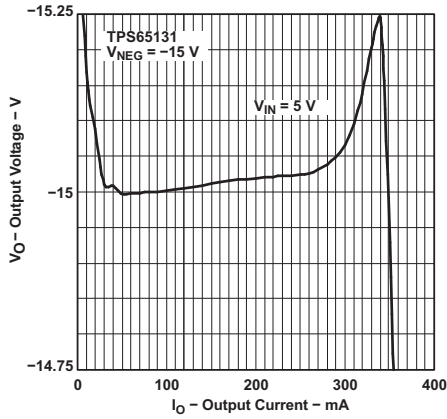
Figure 41. TPS65131 Output Voltage vs Output Current
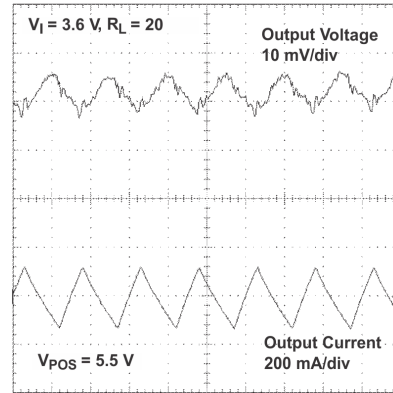
Figure 42. V_{POS} in Continuous Current Mode
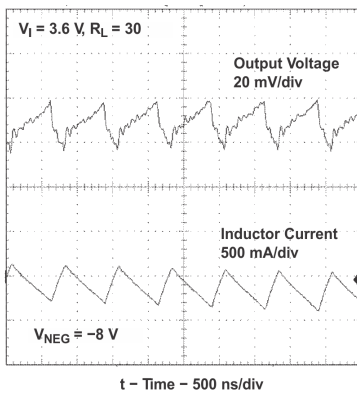
Figure 43. V_{NEG} in Continuous Current Mode
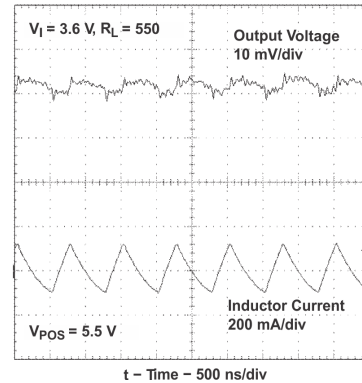
Figure 44. V_{POS} at Power-Save Mode Disabled
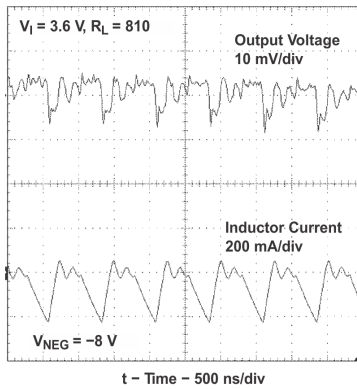
Figure 45. V_{NEG} at Power-Save Mode Disabled
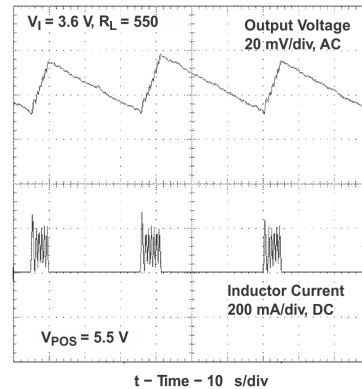
Figure 46. V_{POS} in Power-Save Mode
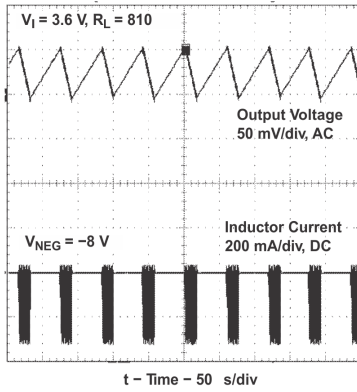
Figure 47. V_NEG in Power-Save Mode
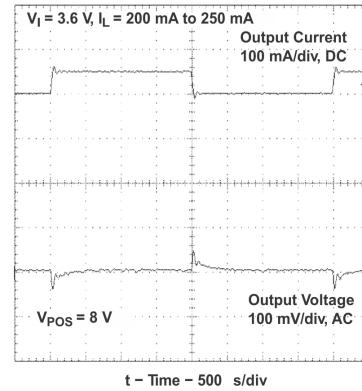
Figure 48. Load Transient Response
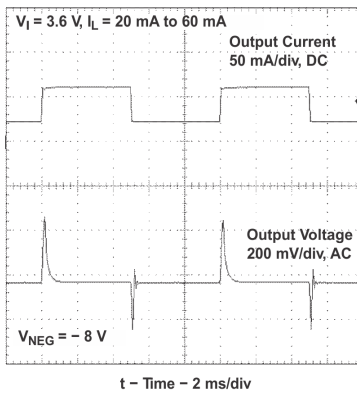
Figure 49. Load Transient Response
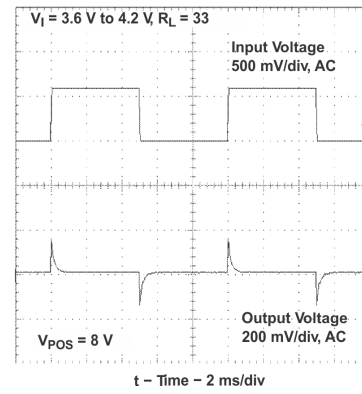
Figure 50. Line Transient Response
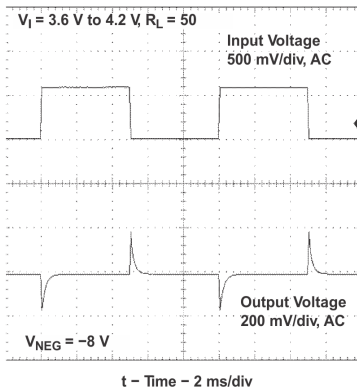
Figure 51. Line Transient Response
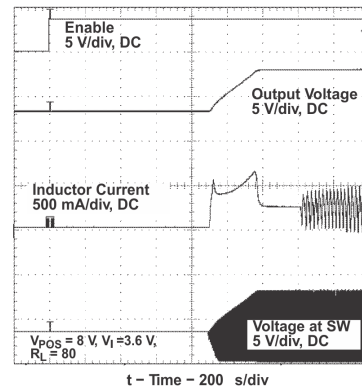
Figure 52. Start-up After Enable

Product Folder Links: *TPS65130 TPS65131*
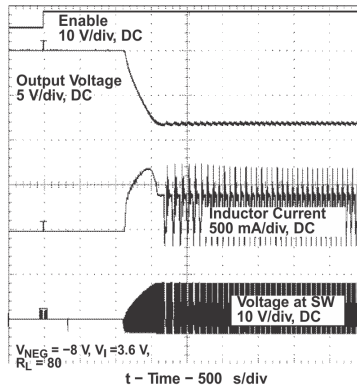
Figure 53. Start-up After Enable

9 Power Supply Recommendations

The TPS6513x input voltage ranges from 2.7 V to 5.5 V. Consequently, the supply can come, for example, from a 3.3-V or 5-V rail. If the device starts into load during the *Soft-Start* phase, the drawn input current can be higher than during post-start operation. Consider the application requirements when selecting the power supply. To avoid unintended toggling of the *Undervoltage Lockout*, connect the TPS6513x through a low-impedance path to the power supply.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. Therefore, use wide and short traces for the main current paths and for the power ground tracks. The input capacitors (C1, C2, C3), output capacitors (C4, C5), the inductors (L1, L2), and the rectifying diodes (D1, D2) should be placed as close as possible to the IC to keep parasitic inductances low. Use a wide power ground (PGND) plane. Connect the analog ground pin (AGND) to the PGND plane. Further, connect the PGND plane with the exposed thermal pad. Place the feedback dividers as close as possible to the control pin (boost converter) or the VREF pin (inverting converter) of the IC.

10.2 Layout Example
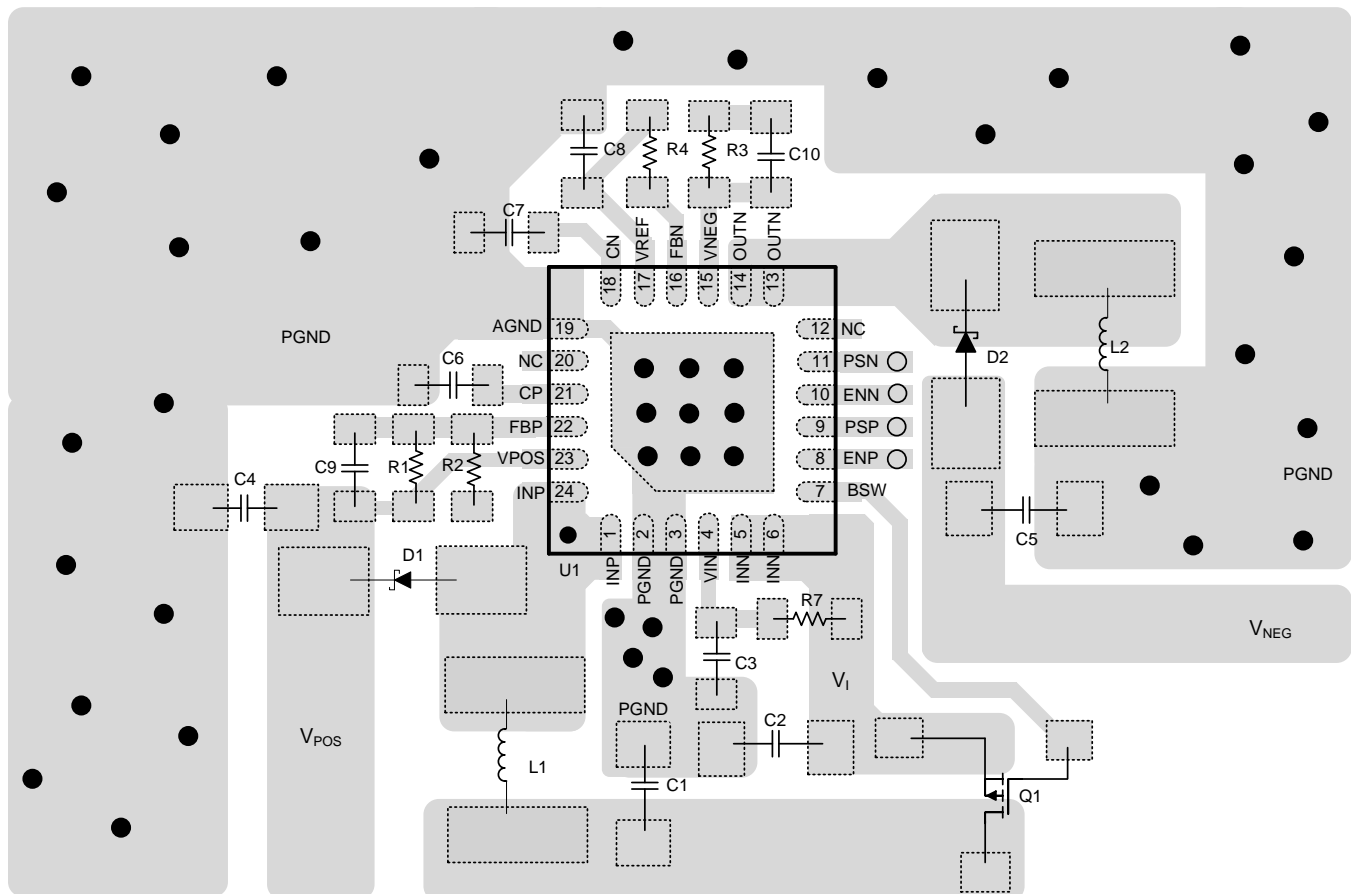
Figure 54. TPS6513x Layout Recommendation

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues, such as thermal coupling, airflow, added heatsinks and convection surfaces, and the presence of heat-generating components affect the power-dissipation limits of a given component.

The following are three basic approaches for enhancing thermal performance follow:
- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow to the system.

The recommended device junction temperature range, T_J, is –40°C to 125°C. The thermal resistance of the 24-pin QFN, 4–mm × 4–mm package (RGE) is $R_{\theta JA}$ = 34.1°C/W. The recommended operating ambient temperature range for the device is T_A = –40°C to 85°C. Use Equation 13 to calculate the maximum power dissipation, $P_D$max, as a function of T_A. In this equation, use T_J = 125°C to operate the device within the recommended temperature range, use T_J = T_{TS} to determine the absolute maximum threshold when the device might go into thermal shutdown. If the maximum ambient temperature of the application is lower, more heat dissipation is possible.

$$P_D\,max = \frac{T_J - T_A}{R_{\theta JA}}$$

(13)

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS65130	Click here	Click here	Click here	Click here	Click here
TPS65131	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TPS65130 TPS65131*

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65130RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS65130RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS65131RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS65131RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65130RGER	VQFN	RGE	24	3000	336.6	336.6	28.6
TPS65130RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS65131RGER	VQFN	RGE	24	3000	336.6	336.6	28.6
TPS65131RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{4,15}{3,85}$ Ⓐ

Ⓑ

$\frac{4,15}{3,85}$

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

Ⓒ

⌓ 0,08

$\frac{0,05}{0,00}$

0,50

24X $\frac{0,50}{0,30}$

1   6

24   7

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

19   12

18   13

24X $\frac{0,30}{0,18}$

⌖	0,10 Ⓜ	C	A	B
	0,05 Ⓜ	C		
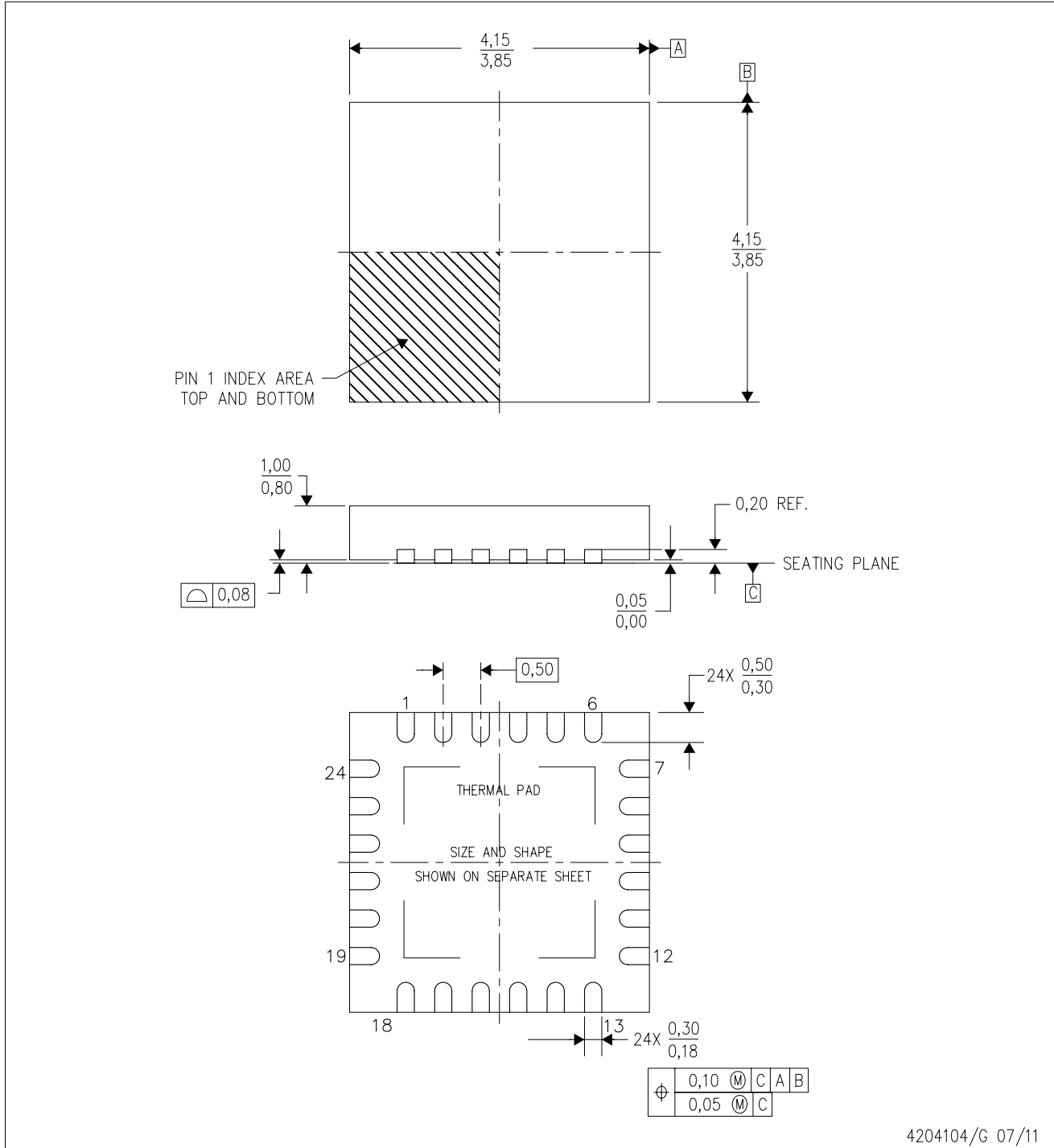
4204104/G 07/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Quad Flatpack, No−Leads (QFN) package configuration.
         D.   The package thermal pad must be soldered to the board for thermal and mechanical performance.
         E.   See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
         F.   Falls within JEDEC MO−220.

TEXAS
INSTRUMENTS
www.ti.com

RGE (S−PVQFN−N24)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
(OPTIONAL)

Exposed Thermal Pad

2,45±0,10

2,45±0,10

Bottom View

Exposed Thermal Pad Dimensions
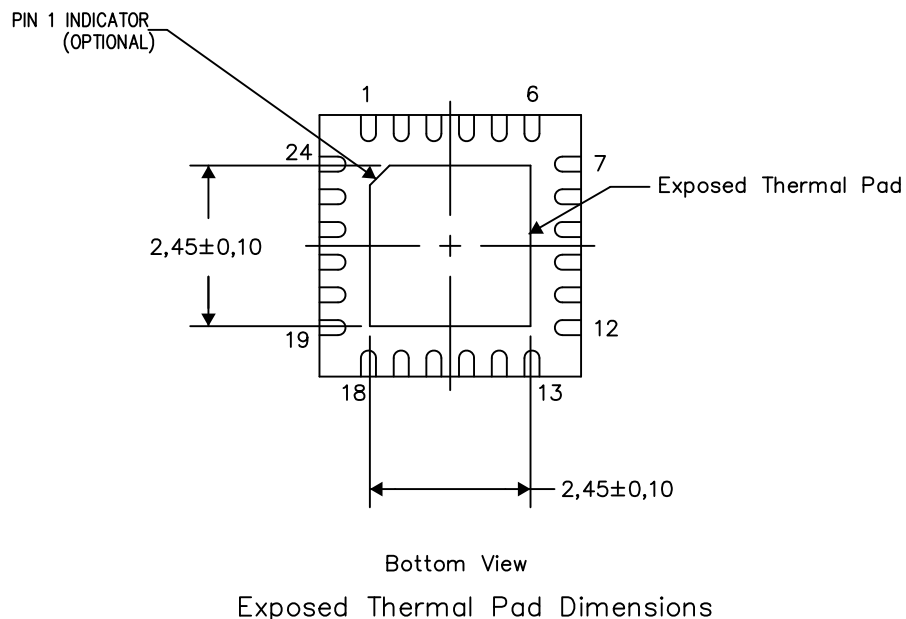
4206344−3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S—PVQFN—N24)   PLASTIC QUAD FLATPACK NO—LEAD

Example Board Layout

Pin 1 Via
Keep Out Area
0,72mm square

Note D

20x0,5

3,1   4,8

3,1

4,8

Example Stencil Design
0.125 Thick Stencil
(Note E)

20x0,5

24x0,8

0,3

24x0,23

0,3   4x1,0

R0,115   4x1,0

3,15   4,75

3,15

4,75
(66% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14   0,85

0,28

0,07   Pad Geometry
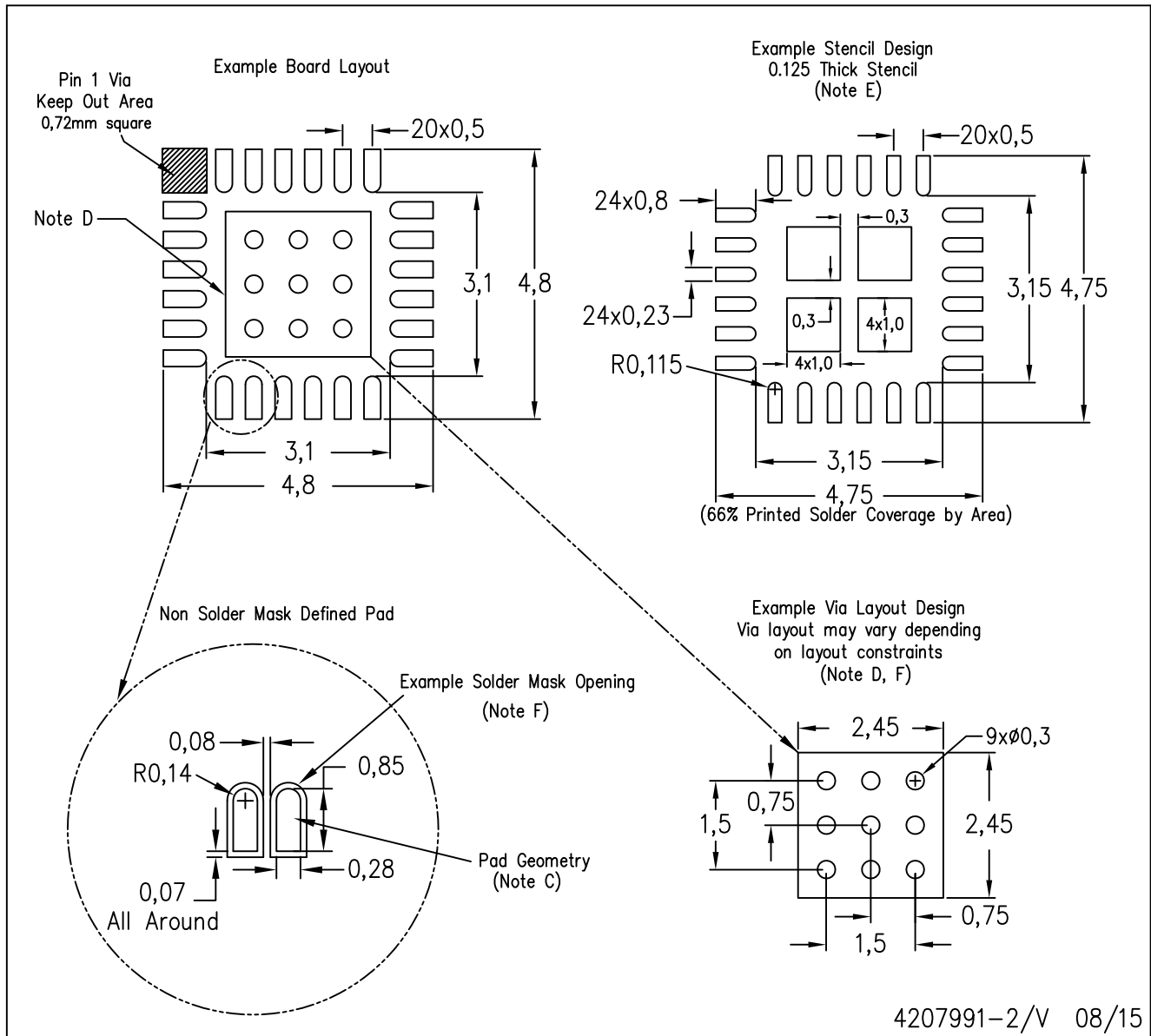(Note C)

All Around

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

2,45   9xØ0,3

0,75

1,5   2,45

0,75

1,5

4207991—2/V   08/15

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC—7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack
              Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design
              considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

Texas
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		