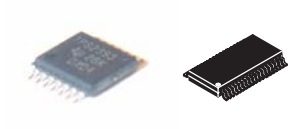


SLUS536C − AUGUST 2002 − REVISED AUGUST 2004

FULL-FEATURED −48-V HOT SWAP POWER MANAGER

FEATURES

- **Wide Input Supply Range: −20 V to −80 V**
- **Transient Rating to −100 V**
- **Programmable Current Limit**
- **Programmable Current Slew Rate**
- **Programmable UV/OV Thresholds/Hysteresis**
- **Debounced Insertion Detection Inputs**
- **Open-Drain Power Good ($\overline{PG}$) Output**
- **Fault Timer to Eliminate Nuisance Trips**
- **Open-Drain Fault Output ($\overline{FAULT}$)**
- **Enable Input (EN)**
- **14-Pin TSSOP package**
- **44-Pin TSSOP Package for Creapage/Clearance**

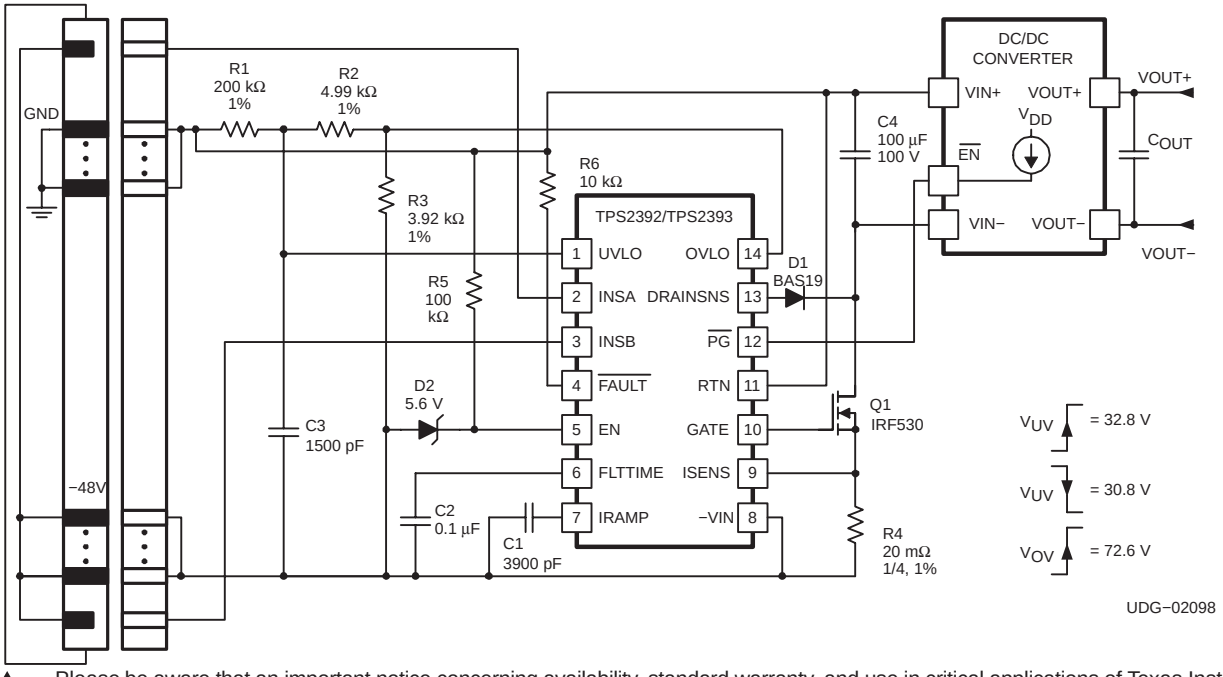
APPLICATIONS

- **−48-V Distributed Power Systems**
- **Central Office Switching**
- **Wireless Base Station**

DESCRIPTION

The TPS2392 and TPS2393 integrated circuits are hot swap power managers optimized for use in nominal −48-V systems. They operate with supply voltage ranges from −20-V to −80-V, and are rated to withstand spikes to −100 V. In conjunction with an external N-channel FET and sense resistor, they can be used to enable live insertion of plug-in cards and modules in powered systems. Each device provides load current slew rate control and peak magnitude limiting. Undervoltage and overvoltage shutdown thresholds are easily programmed via a three-resistor divider network. In addition, two active-low, debounced inputs provide plug-in insertion detection. A power good ($\overline{PG}$) output enables downstream converters. The TPS2392 and TPS2393 also provide the basic hot swap functions of electrical isolation of faulty cards, filtered protection against nuisance overcurrent trips, and single-line fault reporting. The 44-pin part supports designs where telecomm creepage and clearance requirements must be followed.

The TPS2392 latches off in response to current faults, while the TPS2393 periodically retries the load in the event of a fault.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	FAULT OPERATION	PACKAGE	PART NUMBER
−40°C to 85°C	LATCH OFF	TSSOP (PW)(1)	TPS2392PW
	PERIODIC RETRY	TSSOP (PW)(1)	TPS2393PW
	LATCH OFF	TSSOP (PW)(1)	TPS2392DBT
	PERIODIC RETRY	TSSOP (PW)(1)	TPS2393DBT

(1) The PW and DBT package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS2392PWR) for quantities of 2,500 per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		TPS2392 TPS2393	UNIT
Input voltage range, V_I	UVLO, INSA, INSB, FLTTIME, IRAMP, OVLO, DRAINSNS, GATE, ISENS(2)	−0.3 to 15	V
	RTN(2)	−0.3 to 100	
	EN(2)(3)		
Output voltage range, V_O	$\overline{\text{FAULT}}$(2)(4)		
	$\overline{\text{PG}}$(2)(4)		
Continuous output current	$\overline{\text{FAULT}}$	10	mA
	$\overline{\text{PG}}$		
Operating junction temperature range, T_J		−55 to 125	°C
Storage temperature, T_{stg}		−65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to −VIN (unless otherwise noted).
(3) With 100-kΩ minimum input series resistance.
(4) With 10-kΩ minimum series resistance.

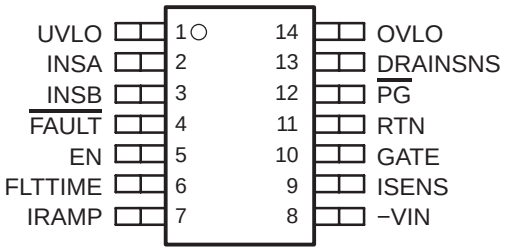
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input supply voltage, −VIN to RTN	−80		−20	V
Operating junction temperature, T_J	−40		85	°C

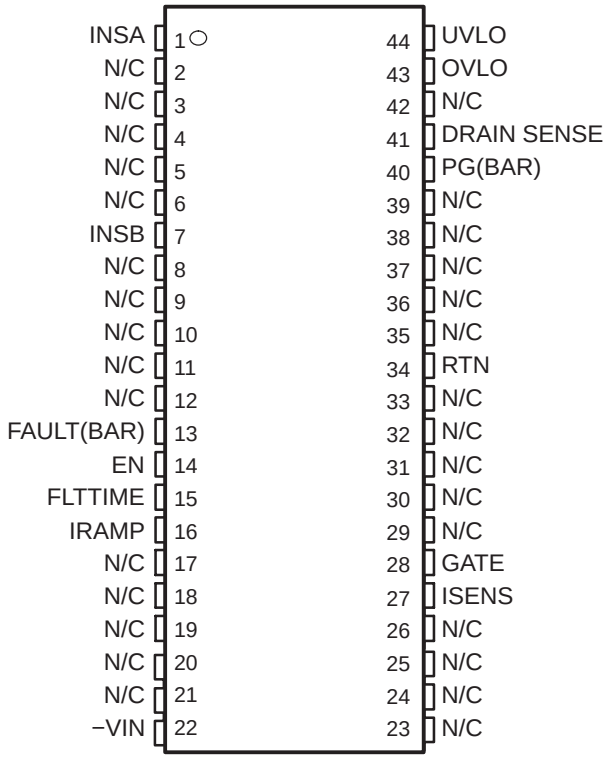
DISSIPATION RATINGS

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
TSSOP−14	750 mW	7.5 mW/°C	300 mW

PW PACKAGE
(TOP VIEW)



DBT PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

$V_{I(–VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(INSA)}$ = 0 V, $V_{I(INSB)}$ = 0 V, $V_{I(UVLO)}$ = 2.5 V, $V_{I(OVLO)}$ = 0 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, T_A = −40°C to 85°C (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
I_{CC1}	Supply current, RTN	$V_{I(RTN)}$ = 48 V		1050	1500	µA
I_{CC2}		$V_{I(RTN)}$ = 80 V		1350	1700	
V_{UVLO_L}	Internal UVLO threshold, V_{IN} rising	To GATE pull-up	−19	−16	−13	V
V_{HYS}	Internal UVLO hysteresis			200		mV
ENABLE INPUT (EN)						
V_{TH}	Threshold voltage, V_{IN} rising	To GATE pull-up	1.3	1.4	1.5	V
I_{SRC_EN}	EN pin switched pull-up current		−12	−10	−8	µA
UNDERVOLTAGE/OVERVOLTAGE COMPARATORS						
V_{TH_UV}	Threshold voltage, V_{IN} rising, UVLO	To GATE pull-up	1.36	1.40	1.44	V
I_{SRC_UV}	UVLO pin switched pull-up current	$V_{I(UVLO)}$ = 2.5 V	−11.7	−10.0	−8.3	µA
I_{IL}	UVLO low-level input current	$V_{I(UVLO)}$ = 1 V	−1		1	µA
V_{TH_OV}	Threshold voltage, V_{IN} rising, OVLO	To GATE pull-up	1.36	1.40	1.44	V
I_{SRC_OV}	OLVO pin switched pull-up current	$V_{I(OVLO)}$ = 2.5 V	−11.7	−10.0	−8.3	µA
I_{IL}	OVLO low-level input current	$V_{I(OVLO)}$ = 1 V	−1		1	µA
INSERTION DETECTION						
V_{TH}	Threshold voltage, V_{IN} rising, INSA, INSB	To GATE pull-down	1.0	1.4	1.8	V
I_{SRC_INSx}	INSA, INSB pin pull-up current	$V_{I(INSA)}$ = 0 V, $V_{I(INSB)}$ = 0 V	−14	−11	−8	µA
t_{D_INS}	Insertion delay time, V_{IN} falling, INSA, INSB	To GATE pull-up	1.5	2.5	4.1	ms
LINEAR CURRENT AMPLIFIER (LCA)						
V_{OH}	High-level output voltage, GATE	$V_{I(ISENS)}$ = 0 V, $I_{O(GATE)}$ = −10 µA	11	14	17	V
I_{SINK}	Output sink current, linear mode	$V_{I(ISENS)}$ = 80 mV, $V_{O(GATE)}$ = 5 V $V_{O(FLTTIME)}$ = 2 V		5	10	mA
I_{FAULT}	Output sink current, fault shutdown	$V_{I(ISENS)}$ = 80 mV, $V_{O(GATE)}$ = 5 V $V_{O(FLTTIME)}$ > 4 V	50	100		
I_I	Input current, ISENS	0 V < $V_{I(ISENS)}$ < 0.2 V	−1		1	µA
V_{REF_K}	Reference clamp voltage	$V_{O(IRAMP)}$ = OPEN	33	40	47	mV
V_{IO}	Input offset voltage	$V_{O(IRAMP)}$ = 2 V	−7		7	
RAMP GENERATOR						
I_{SRC1}	IRAMP source current, reduced rate turn-on	$V_{O(IRAMP)}$ = 0.25 V	−850	−600	−400	nA
I_{SRC2}	IRAMP source current, normal rate	$V_{O(IRAMP)}$ = 1 V	−11	−10	−9	µA
		$V_{O(IRAMP)}$ = 3 V	−11	−10	−9	
V_{OL}	Low-level output voltage, IRAMP	$V_{I(EN)}$ = 0 V			2	mV
A_V	Voltage gain, relative to ISENS		9.5	10.0	10.5	mV/V
OVERLOAD COMPARATOR						
V_{TH_OL}	Current overload threshold, ISENS		80	100	120	mV
t_{DLY}	Glitch filter delay time	$V_{I(ISENS)}$ = 200 mV	2	4	7	µs

(1) All voltages are with respect to the −VIN terminal, unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminals.

ELECTRICAL CHARACTERISTICS (continued)

$V_{I(-VIN)}$ = −48 V with respect to RTN, $V_{I(EN)}$ = 2.8 V, $V_{I(INSA)}$ = 0 V, $V_{I(INSB)}$ = 0 V, $V_{I(UVLO)}$ = 2.5 V, $V_{I(OVLO)}$ = 0 V, $V_{I(ISENS)}$ = 0 V, all outputs unloaded, T_A = −40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT TIMER							
V_{OL}	Low-level output voltage, FLTTIME		$V_{I(EN)}$ = 0 V			5	mV
I_{CHG}	Charging current, current limit mode		$V_{I(ISENS)}$ = 80 mV, $V_{O(FLTTIME)}$ = 2 V	−55	−50	−45	µA
V_{FLT}	Fault threshold voltage			3.75	4.00	4.25	V
I_{DSG}	Discharge current, retry mode	TPS2393	$V_{I(ISENS)}$ = 80 mV, $V_{O(FLTTIME)}$ = 2 V		0.38	0.61	µA
D	Output duty cycle	TPS2393	$V_{I(ISENS)}$ = 80 mV		1.0%	1.5%	
I_{RST}	Discharge current, timer reset mode		$V_{O(FLTTIME)}$ = 2 V, $V_{I(ISENS)}$ = 0 V		1		mA
POWERGOOD SENSING							
V_{TH}	DRAINSNS threshold voltage			1.20	1.35	1.50	V
I_{SRC}	DRAINSNS pull-up current		$V_{I(DRAINSNS)}$ = 0 V	−14	−11	−8	µA
I_{OH}	High-level output leakage current, $\overline{PG}$ output		$V_{I(EN)}$ = 0 V, $V_{O(\overline{PG})}$ = 65 V			10	
$R_{DS(on)}$	Driver on-resistance, $\overline{PG}$ output		$V_{I(ISENS)}$ = 0 V, $V_{I(DRAINSNS)}$ = 0 V $I_{O(PG)}$ = 1 mA		50	80	Ω
$\overline{FAULT}$ OUTPUT							
I_{OH}	High-level output leakage current, $\overline{FAULT}$		$V_{I(EN)}$ = 0 V, $V_{O(\overline{FAULT})}$ = 65 V			10	µA
$R_{DS(on)}$	Driver on-resistance, $\overline{FAULT}$		$V_{I(ISENS)}$ = 80 V, $V_{O(FLTTIME)}$ = 5 V $I_{O(\overline{FAULT})}$ = 1 mA		50	80	Ω

(1) All voltages are with respect to the −VIN terminal, unless otherwise stated.
(2) Currents are positive into and negative out of the specified terminals.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	PW	DBT		
DRAINSNS	13	41	I	Sense input for monitoring the load voltage status
EN	5	14	I	Enable input to turn on/off power to the load
$\overline{FAULT}$	4	13	O	Open-drain, active-low indication of a load fault condition
FLTTIME	6	15	I/O	Connection for user-programming of the fault timeout period
GATE	10	28	O	Gate drive for external N−channel FET
INSA	2	1	I	Insertion detection input pin A
INSB	3	7	I	Insertion detection input pin B
IRAMP	7	16	I/O	Programming input for setting the inrush current slew rate
ISENS	9	27	I	Current sense input
OVLO	14	43	I	Voltage sense input for supply overvoltage lockout (OVLO) protection
$\overline{PG}$	12	40	O	Open-drain, active-low indication of load power-good condition
RTN	11	34	I	Positive supply input
UVLO	1	44	I	Voltage sense input for supply undervoltage lockout (UVLO) protection
−VIN	8	22	I	Negative supply input and reference pin

PIN ASSIGNMENTS

DRAINSNS: Sense input for monitoring the load voltage status. The DRAINSNS pin determines the load status by sensing the voltage level on the external pass FET drain. DRAINSNS must be pulled low with repect to −VIN (less than 1.35 V typically) to declare a power good condition. This corresponds to a low V_{DS} across the FET, indicating that the load voltage has successfully ramped up to the DC input level. DRAINSNS must be connected to the FET drain through a small-signal blocking diode as shown in the typical application diagram. An internal pull-up maintains a high logic level at the pin until overridden by a fully-enhanced external FET.

EN: Enable input to turn on/off power to the load. The EN pin is referenced to the −VIN potential of the circuit. When this input is pulled high (above the nominal 1.4-V threshold), and all other input qualifications are met (supply above device undervoltage lockout (UVLO), UVLO pin high and OVLO pin low, INSx pins pulled low) the device enables the GATE output, and begins the ramp of current to the load. When this input is low, the linear current amplifier (LCA) is disabled, and a large pull-down device is applied to the FET gate, disabling power to the load.

$\overline{\text{FAULT}}$: Open-drain, active-low indication of a load fault condition. When the device EN is deasserted, or when enabled and the load current is less than the programmed limit, this output is high impedance. If the device remains in current regulation mode at the expiration of the fault timer, or if a fast-acting overload condition causes greater than 100-mV drop across the sense resistor, the fault is latched, the load is turned off, and the $\overline{\text{FAULT}}$ pin is pulled low (to −VIN). The TPS2392 remains latched off for a fault, and can be reset by cycling either the EN pin or power to the device. The TPS2393 retries the load at approximately a 1% duty cycle.

FLTTIME: Connection for user-programming of the fault timeout period. An external capacitor connected from FLTTIME to −VIN establishes the timeout period to declare a fault condtion. This timeout protects against indefinite current sourcing into a faulted load, and also provides a filter against nuisance trips from momentary current spikes or surges. The TPS2392 and TPS2393 define a fault condition as voltage at the ISENS pin at or greater than the 40-mV fault threshold. When a fault condition exists, the timer is active. The devices manage fault timing by charging the external capacitor to the 4-V fault threshold, then subsequently discharging it to reset the timer (TPS2392), or discharging it at approximately 1% the charge rate to establish the duty cycle for retrying the load (TPS2393). Whenever the internal fault latch is set (timer expired), the pass FET is rapidly turned off, and the $\overline{\text{FAULT}}$ output is asserted.

GATE: Gate drive for external N−channel FET. When enabled, and the input supply is above the UVLO threshold, the gate drive is enabled and the device begins charging an external capacitor connected to the IRAMP pin. This pin voltage is used to develop the reference voltage at the non-inverting input of the internal LCA. The inverting input is connected to the current sense node, ISENS. The LCA acts to slew the pass FET gate to force the ISENS voltage to track the reference. The reference is internally clamped at 40 mV, so the maximum current that can be sourced to the load is determined by the sense resistor value as $IMAX \leq 40\ mV/R_{SENSE}$. Once the load voltage has ramped up to the input dc potential, and current demand drops off, the LCA drives the GATE output to about 14 V to fully enhance the pass FET, completing the low-impedance supply return path for the load.

INSA: Insertion detection input pin A. The INSA and INSB inputs work together to provide an insertion detection function for TPS2392 and TPS2393 applications. In order to turn on the FET gate drive (the GATE output), both INSA and INSB must be pulled below the detection threshold, approximatey 1.4 V. Implementations using this feature provide a mechanism for pulling these pins directly to −VIN potential (device ground), eliminating any threshold ambiguity. An on-chip pull-up is provided at each INSx pin; no additional pull-up is needed to hold the pins high during the insertion process. The insertion inputs are debounced with a nominal 2.5-ms filter.

INSB: Insertion detection input pin B. See INSA description.

IRAMP: Programming input for setting the inrush current slew rate. An external capacitor connected between this pin and −VIN establishes the load current slew rate whenever power to the load is enabled. The device charges the external capacitor to establish the reference input to the LCA. The closed-loop control of the LCA and pass FET acts to maintain the current sense voltage at ISENS at the reference potential. Since the sense voltage is developed as the drop across a resistor, the load current slew rate is set by the voltage ramp rate at the IRAMP pin. When the output is disabled for any reason (e.g., EN deassertion, voltage or current fault, etc.), the capacitor is discharged and held low to initialize it for the next turn-on.

PIN ASSIGNMENTS

ISENS: Current sense input. An external low-value resistor connected between this pin and −VIN is used to feed back current magnitude information to the TPS2392 and TPS2393. There are two internal device thresholds associated with the voltage at the ISENS pin. During ramp-up of the load's input capacitance, or during other periods of excessive demand, the HSPM acts to limit this voltage to 40 mV. Whenever the LCA is in current regulation mode, the capacitor at FLTTIME is charged to activate the timer. If, when the LCA is driving to its supply rail, a fast-acting fault such as a short-circuit, causes the ISENS voltage to exceed 100 mV (the overload threshold), the GATE pin is pulled low rapidly, bypassing the fault timer.

OVLO: Voltage sense input for supply overvoltage lockout (OVLO) protection. Overvoltage protection can be achieved by applying a divided down sample of the input supply voltage to this pin. In order to turn on gate drive to the external FET, the OVLO pin must be below the 1.4-V typical threshold, while all other input qualifications are met. If the OVLO pin is raised above this threshold, as with increasing supply voltage, the GATE output is pulled low, interrupting the supply to the load. An internal 10-µA pull-up is switched to this pin when the threshold is exceeded, providing a mechanism for setting the amount of OVLO hysteresis along with the trip threshold.

$\overline{\text{PG}}$: Open-drain, active-low indication of load power good condition. The TPS2392 and TPS2393 devices define power good as the voltage at the DRAINSNS pin below the power good threshold, and the voltage at the IRAMP pin being above 5 V. This assures that full programmed sourcing current is available to the load prior to declaring power good, even with very slow current ramp rates. The additional protection prevents potential discharging of the module bulk capacitance during load turn-on.

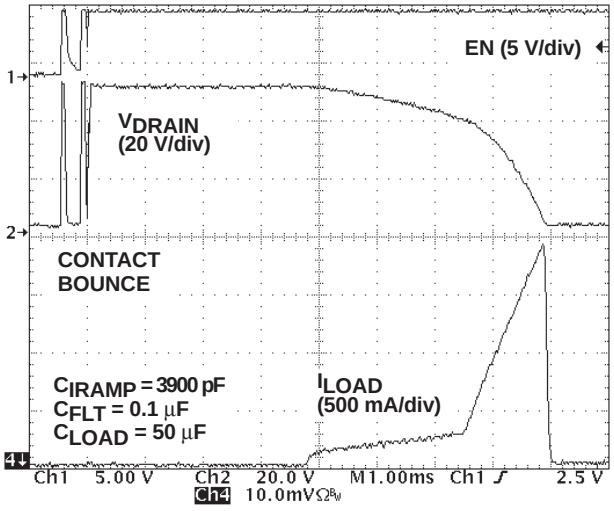
RTN: Positive supply input for the TPS2392 and TPS2393. For negative voltage systems, the supply pin connects directly to the return node of the input power bus. Internal regulators step down the input voltage to generate the various supply levels used by the TPS2392 and TPS2393.

UVLO: Voltage sense input for supply uvervoltage lockout (UVLO) protection. Undervoltage protection can be achieved by applying a divided down sample of the input supply voltage to this pin. In order to turn on the gate drive to the external FET, the UVLO pin must be above the 1.4-V typical threshold, while all other input qualifications are met. If the UVLO pin drops below this threshold, as with decreasing supply voltage, the GATE output is pulled low, interrupting the supply to the load. An internal 10-µA pull−up is switched to this pin when the threshold is exceeded, providing a mechanism for setting the amount of UVLO hysteresis along with the trip threshold.

For proper operation, a minimum 1500-pF capacitor, connected between the UVLO and −VIN pins, is required.

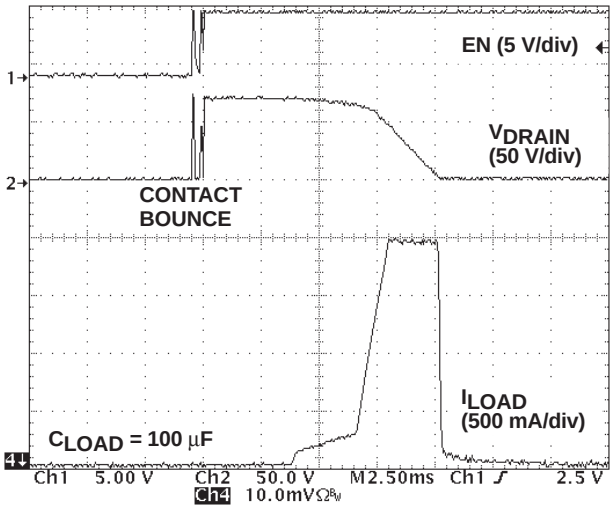
−**VIN**: Negative supply input and reference pin for the TPS2392 and TPS2393. This pin connects directly to the input supply negative rail. The input and output pins and all internal circuitry are referenced to this pin, so it is essentially the GND or VSS pin of the device.

TYPICAL CHARACTERISTICS



t − Time − 1 ms / div

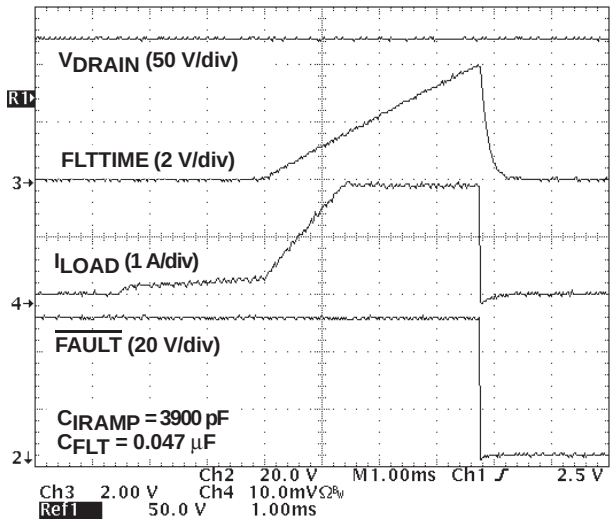
Figure 1. Live Insertion Event − V_{IN} = −48 V



t − Time − 2.5 ms / div

Figure 2. Live Insertion Event − V_{IN} = −70 V

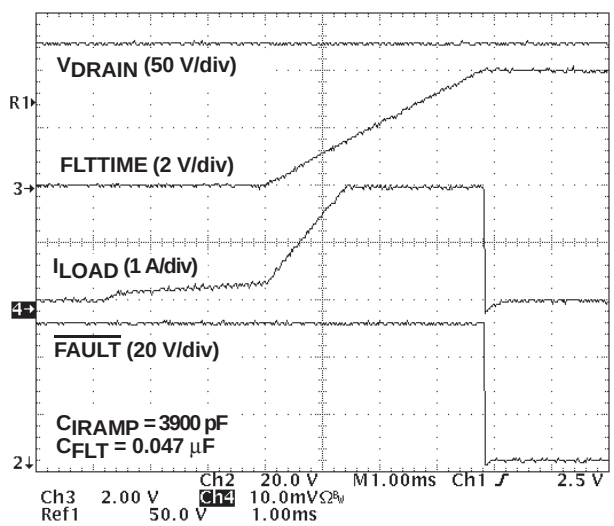
TPS2392 ONLY



t − Time − 1 ms / div

Figure 3. Turn−On Into Shorted Load

TPS2393 ONLY



t − Time − 1 ms / div

Figure 4. Turn−On Into Shorted Load (TPS2393)

TYPICAL CHARACTERISTICS

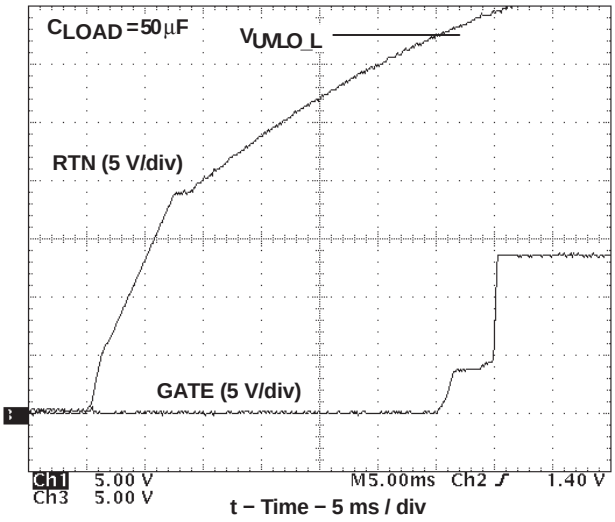


Figure 5. UVLO Protection, Supply Rising

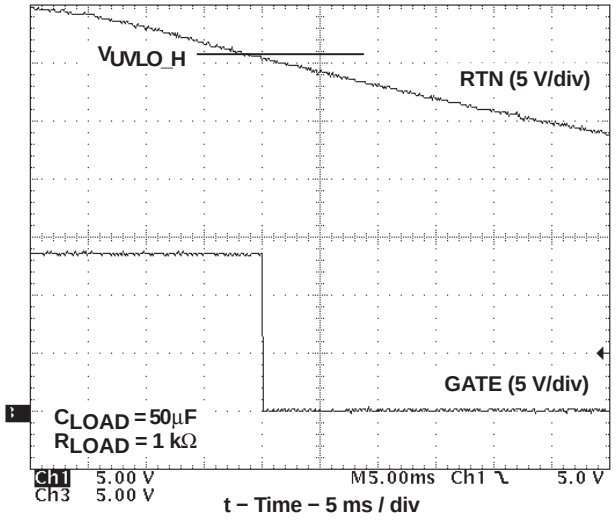


Figure 6. UVLO Protection Supply Falling

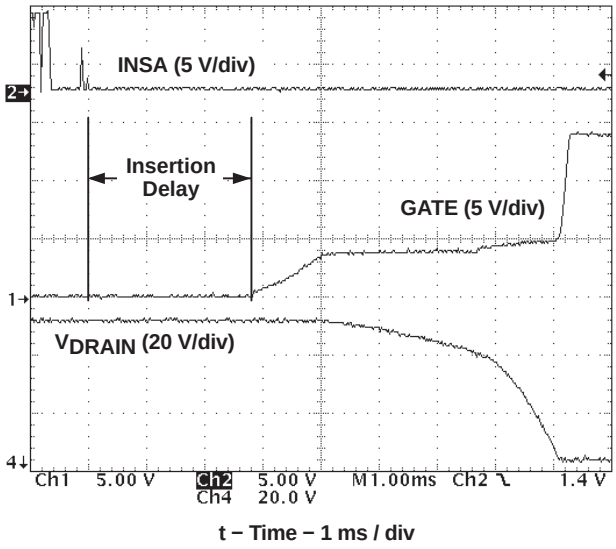


Figure 7. Inertion Detection Function

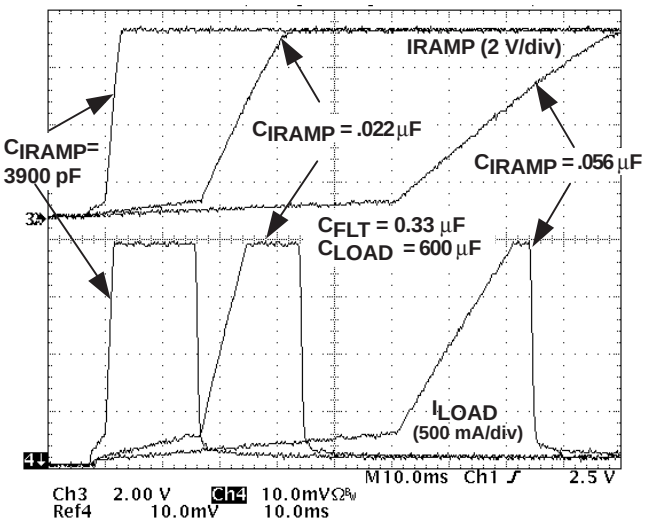


Figure 8. Load Current Ramp Profiles

TYPICAL CHARACTERISTICS

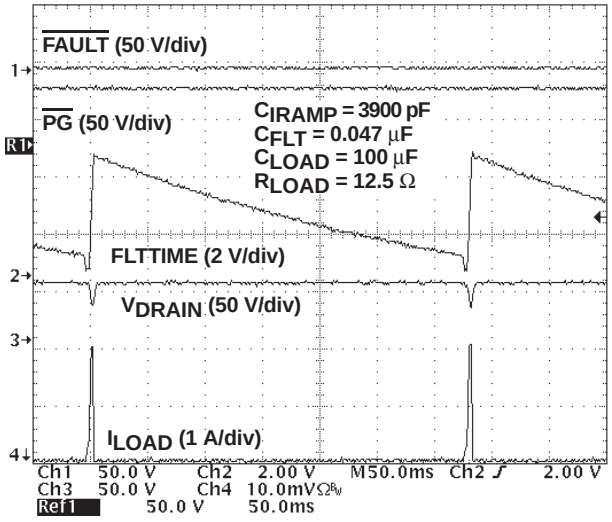


Figure 9. Fault Retry Operation (TPS2393)

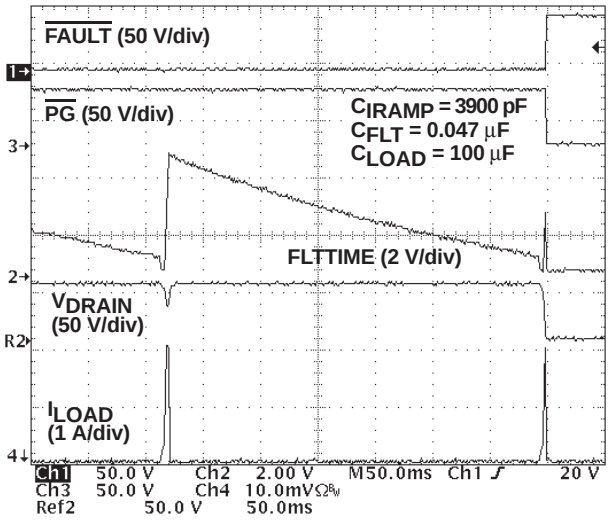


Figure 10. Fault Recovery (Large Scale View)

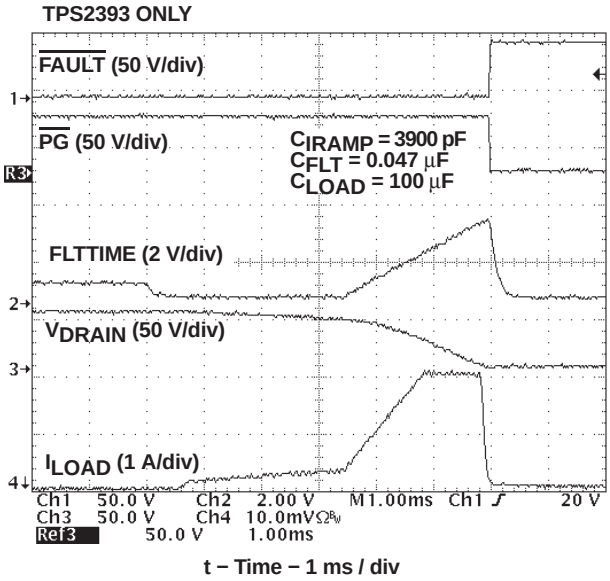


Figure 11. Fault Recovery − Expanded View

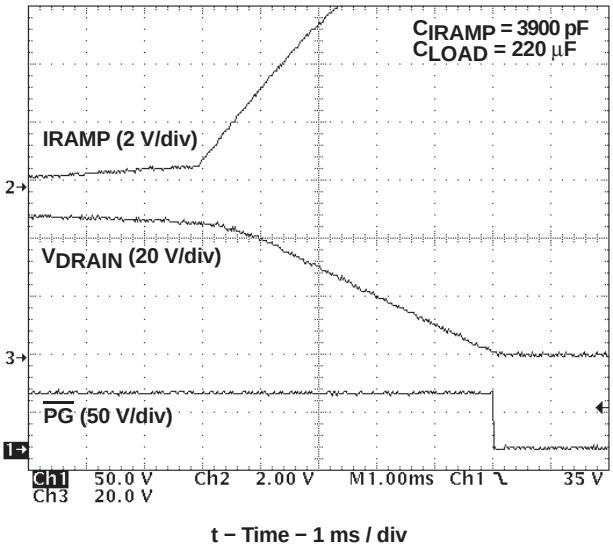


Figure 12. $\overline{PG}$ Output Timing, Voltage Qualified

TYPICAL CHARACTERISTICS

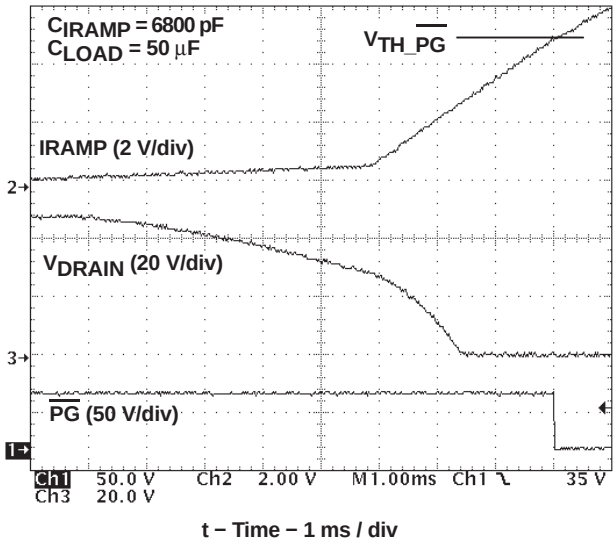


Figure 13. $\overline{PG}$ Output Timing, Current Qualified

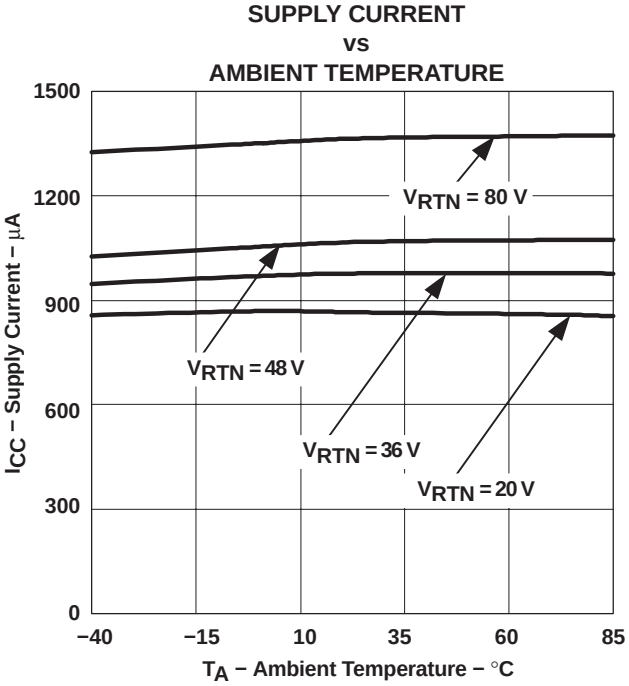


Figure 14.

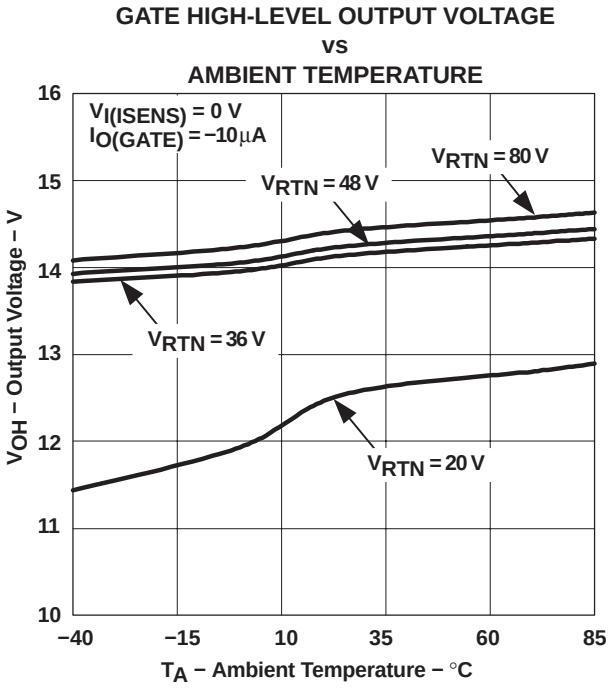


Figure 15.

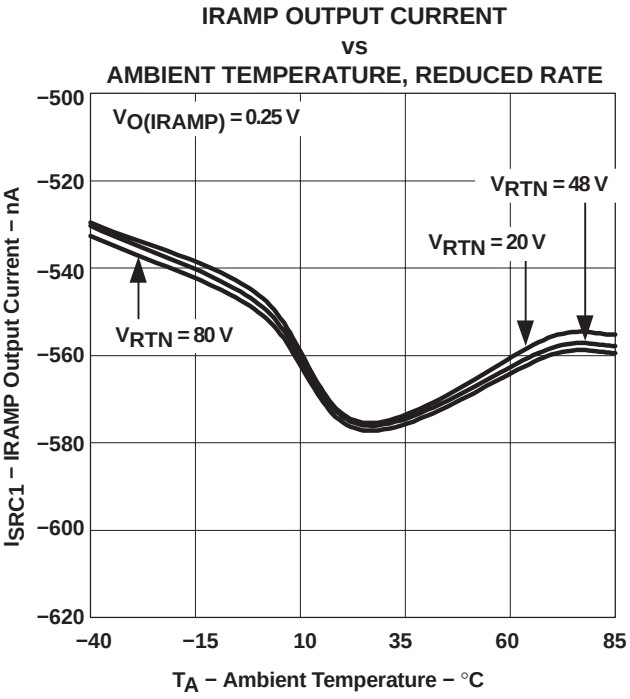


Figure 16.

TYPICAL CHARACTERISTICS

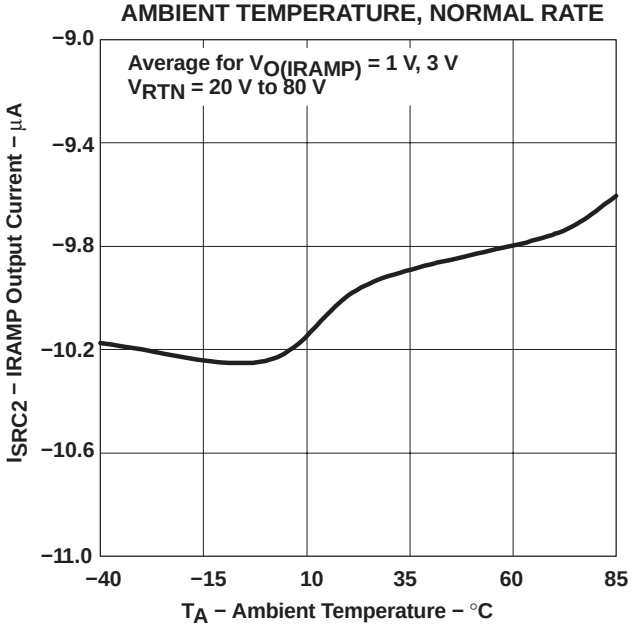


Figure 17.

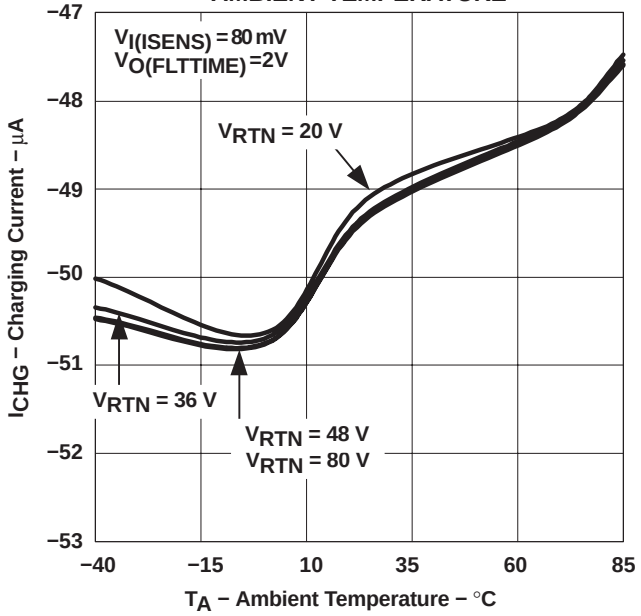


Figure 18.

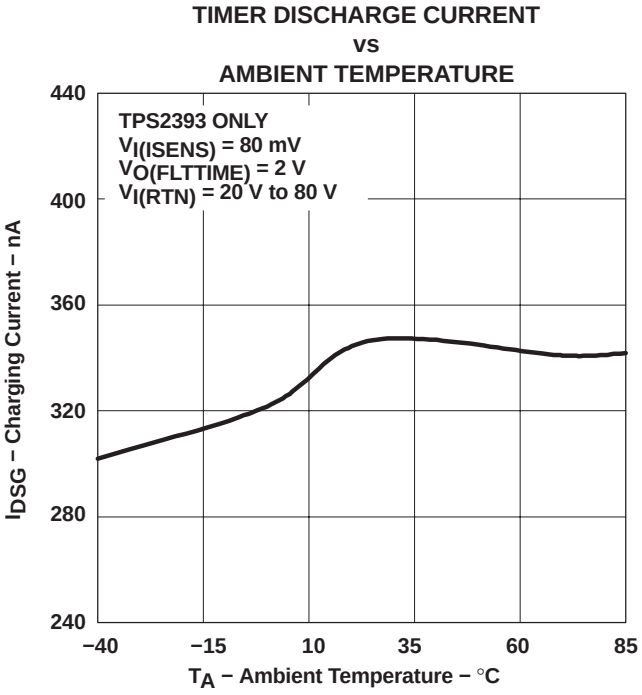


Figure 19.

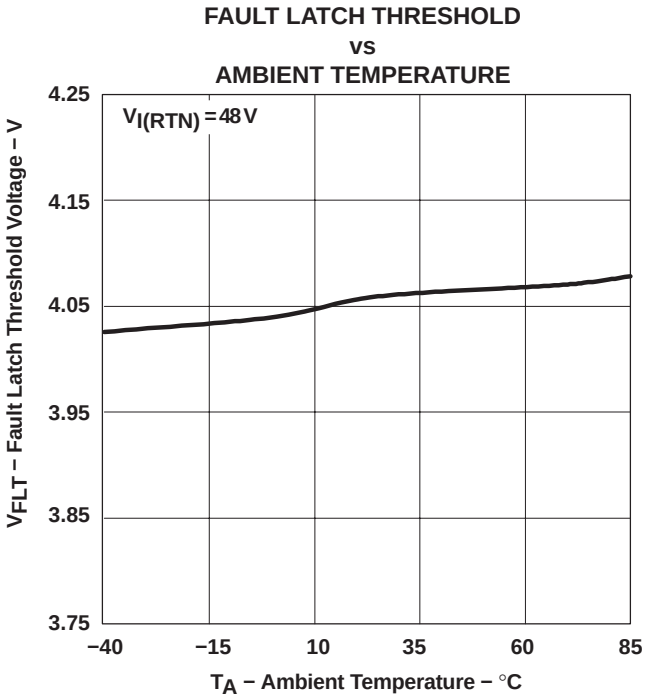


Figure 20.

TYPICAL CHARACTERISTICS

VOLTAGE COMPARATOR THRESHOLD vs AMBIENT TEMPERATURE

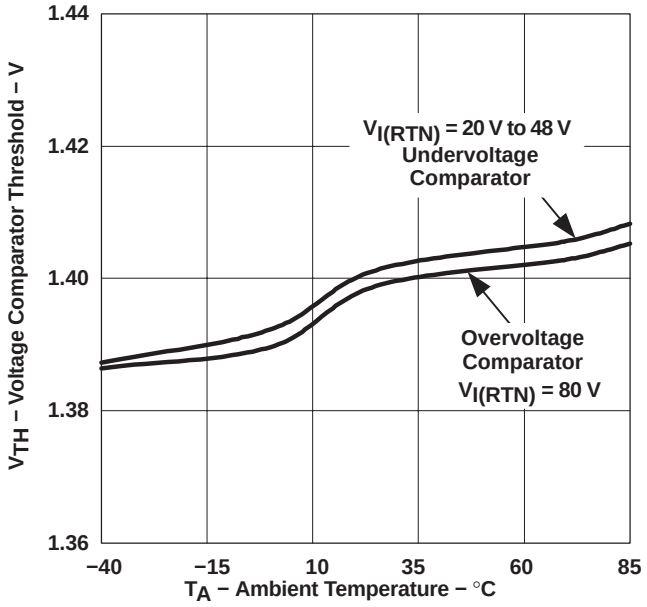


Figure 21.

UVLO PIN PULL-UP CURRENT vs AMBIENT TEMPERATURE

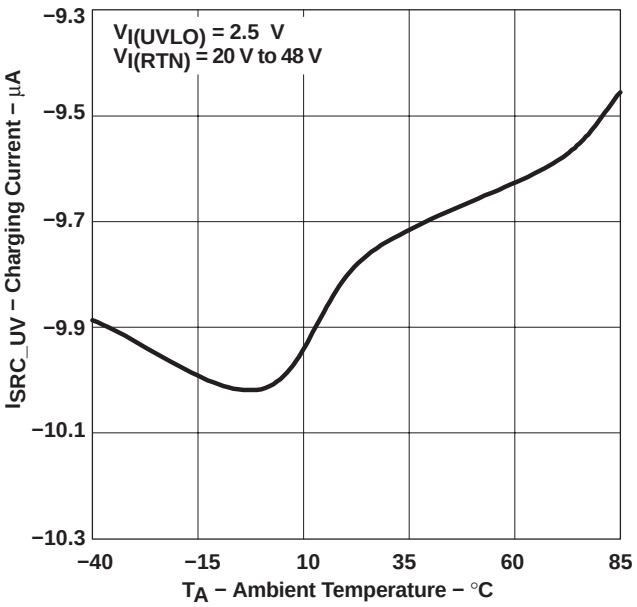


Figure 22.

INSA PIN INSERTION DELAY TIME vs AMBIENT TEMPERATURE

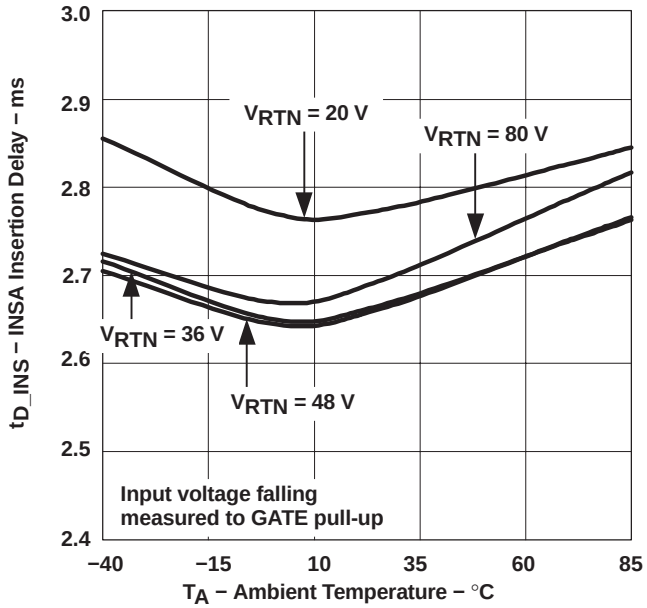


Figure 23.

DETAILED DESCRIPTION

When a plug-in module or printed circuit card is inserted into a live chassis slot, discharged supply bulk capacitance on the board can draw huge transient currents from the system supplies. Without some form of inrush limiting, these currents can reach peak magnitudes ranging over 100 A, particularly in high-voltage systems. Such large transients can damage connector pins, PCB etch, and plug-in and supply components. In addition, current spikes can cause voltage droops on the power distribution bus, causing other boards in the system to reset.

The TPS2392 and TPS2393 are hot swap power managers that limit current peaks to preset levels, as well as control the slew rate (di/dt) at which charging current ramps to the programmed limit. These devices use an external N-channel pass FET and sense element to provide closed-loop control of current sourced to the load. Input undervoltage lockout (UVLO) and overvoltage lockout (OVLO) functions control automatic turn-on when the input supply voltage is within the specified operational window, otherwise inhibiting card operation by turning off the pass FET. In addition, load power can be controlled with a system logic command via the EN input, allowing electrical isolation of faulty cards from the power bus. Two active-low inputs can be connected to provide card insertion detection. An internal overload comparator provides circuit breaker protection against short-circuits occurring during steady-state (post-turn-on) operation of the card. Load power status is continuously monitored and reported via the $\overline{PG}$ (powergood) and $\overline{FAULT}$ outputs.

The TPS2392 and TPS2393 operate directly from the input supply (nominal −48 Vdc rail). The −VIN pin connects to the negative voltage rail, and the RTN pin connects to the supply return. Internal regulators convert input power to the supply levels required by the device circuitry. An input UVLO circuit holds the GATE output low until the supply voltage reaches a nominal 16-V level, regardless of the status of all other control inputs. A block of comparators monitors input supply voltage and other output enable conditions. As shown in Figure 24, the status of these five comparators is AND'd together in order to enable turning on power to the load. Two precision comparators monitor the voltage levels at the UVLO and OVLO pins. Typically, these pins are driven with a divided-down sample of the supply voltage to establish the UVLO and OVLO trip thresholds for the circuit. The UVLO input must be above the internal 1.4-V reference, and the OVLO pin must remain below the reference voltage to enable the load. Both of these inputs are provided with a small, 10-µA pull-up source, which is switched to the input pin whenever the associated comparator is tripped. These current sources provide a mechanism for user-programming of the amount of hysteresis for the UVLO and OVLO thresholds.

The same comparator circuit is also available at the EN pin, providing a third precision input. A switched pull-up is also available at this pin for hysteresis programming. Alternatively, this input can be used as a logic enable command, with a nominal 1.4-V logic threshold.

The INSA and INSB pins provide an optional insertion detection function to the hot swap circuit. Both these pins must be pulled low, below 1.0 -V minimum, to enable a load start-up. Internal pull-ups at these inputs maintain a HI logic level (about 6.5 V) at the device pins when floating. This eliminates the need for additional external components to maintain the HI logic level during insertion and extraction events. An external mechanism for pulling these inputs low completes the qualification for turning on power to the load.

Once the device is enabled (internal EN_A signal asserted), the GATE output pull-down is turned off, and the linear control amplifier (LCA) is enabled. A current source in the ramp generator block begins charging an external capacitor connected between the IRAMP and −VIN pins. The resultant voltage ramp at the IRAMP pin is scaled by a factor of 1/100, and applied to the non-inverting input of the LCA (the VLIM signal). Load current magnitude information at the ISENS pin is applied to the inverting input. This sense voltage is developed by connecting the current sense resistor between ISENS and −VIN. As the external FET begins to conduct, the LCA slews its gate to force the ISENS voltage to track the internal reference (VLIM). Consequently, the load current slew rate tracks the linear voltage ramp at the IRAMP pin, producing a linear di/dt of current to the load.

DETAILED DESCRIPTION

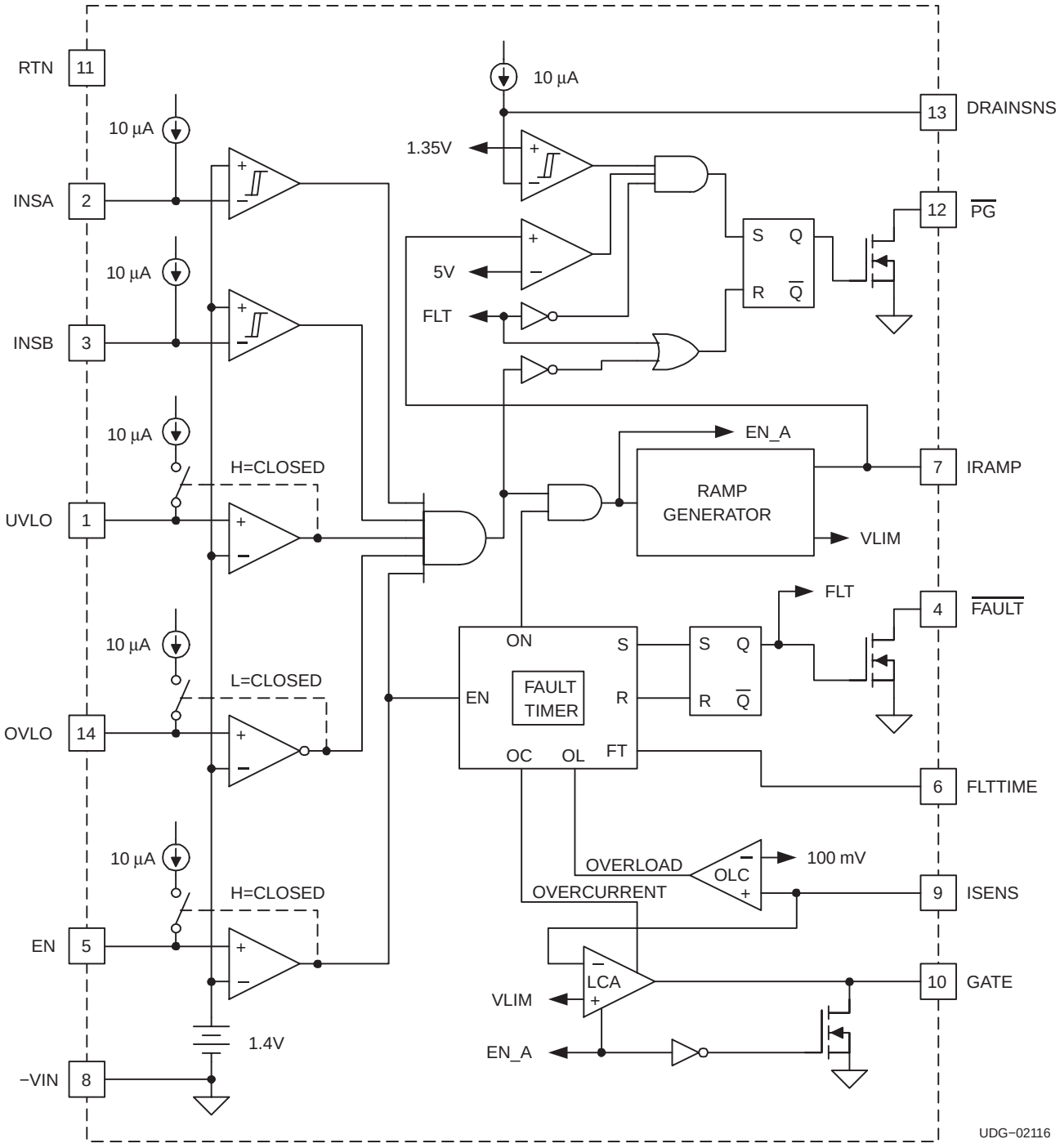


Figure 24. Block Diagram of PW Package

Under normal load and input supply conditions, this controlled current charges the module's input bulk capacitance up to the input dc voltage level. At this point, the load demand drops off, and the voltage at ISENS decreases. The LCA now drives the GATE output to its supply rail. The 14-V typical output level ensures sufficient overdrive to fully enhance the external FET, while not exceeding the typical 20-V V_{GS} rating of common N-channel power MOSFETs.

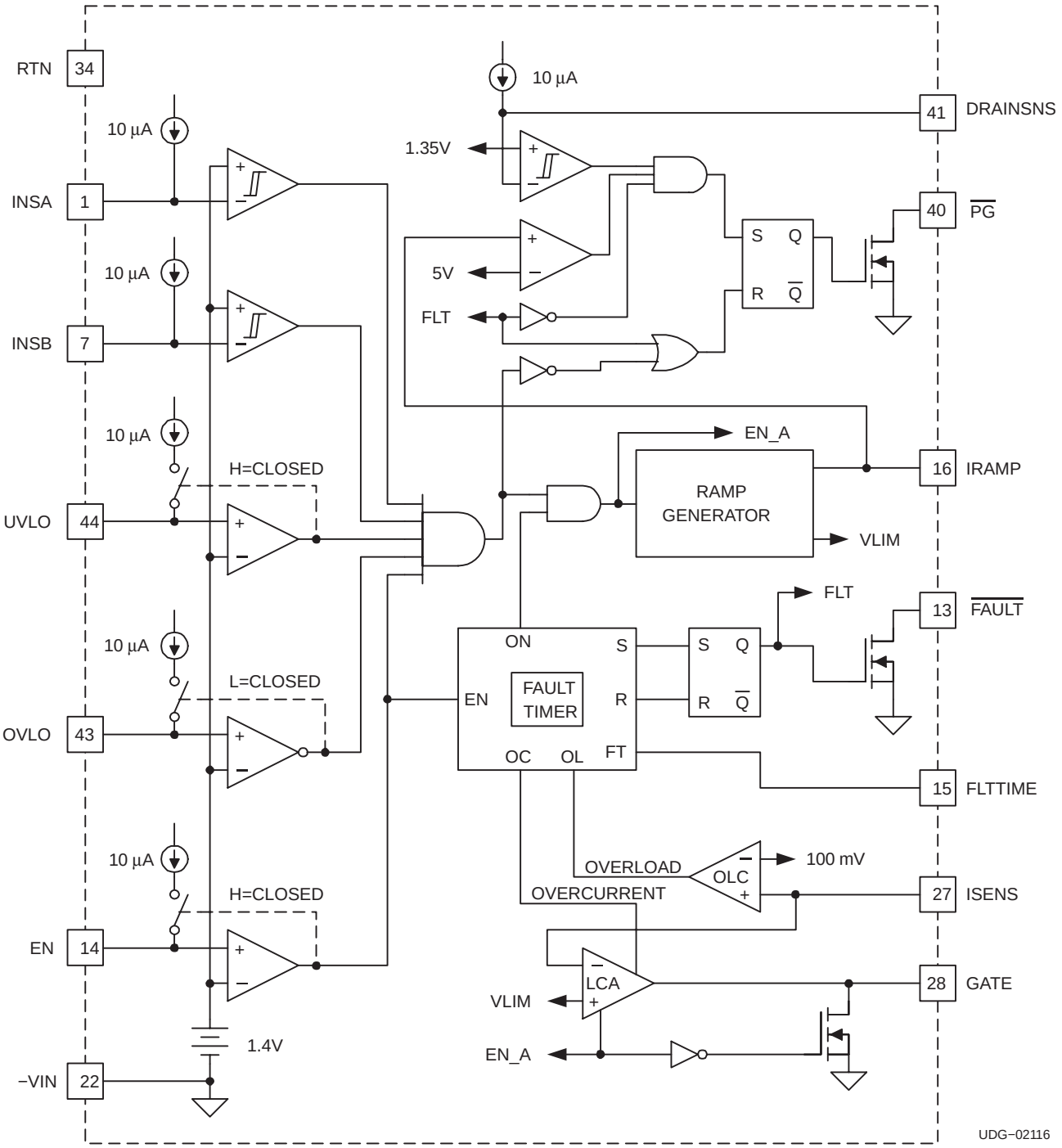


Figure 25. Block Diagram of DBT Package

DETAILED DESCRIPTION

Current fault response timing and retry duty cycle are accomplished by the fault timer block in conjunction with an external capacitor connected between the FLTTIME and −VIN pins. Whenever the hot swap controller is in current control mode, such as during inrush limiting at insertion, or in response to excessive demand during operation of the plug-in, the LCA asserts the OVERCURRENT signal shown in Figure 24. This signal starts the charging of the FLTTIME capacitor. If this capacitor charges to the pin's 4-V trip threshold, the fault is latched. A latched fault disables the LCA drive, and turns on a large pull-down device at the GATE output to rapidly turn off the external FET. The fault condition is indicated by turning on the open-drain $\overline{\text{FAULT}}$ output driver. A latched fault also causes discharge of the external capacitors at the IRAMP and FLTTIME pins, in order to reset the hot swap circuit for the next output enable event, if and when conditions permit.

An internal overload comparator (OLC in Figure 24) also monitors the ISENS voltage against a nominal 100-mV threshold. This comparator provides circuit breaker protection against sudden current fault conditions, such as a load short-circuit. The OVERLOAD output of this comparator also drives the fault timer. The timer circuit applies a 4-µs deglitch filter to help reduce nuisance trips. However, if the overload condition exceeds the filter length, the fault is latched, the LCA disabled, and the FET gate rapidly pulled down, bypassing the programmed timeout period.

The $\overline{\text{PG}}$ pin is an open-drain, active-low indication of a load power good status. Load voltage sensing is provided at the DRAINSNS pin. To assert $\overline{\text{PG}}$, the device must not be in latched current fault status, the DRAINSNS pin must be pulled below the 1.35-V nominal threshold, and the voltage at the IRAMP pin must be greater than approximately 5 V. This last criteria ensures that maximum allowed sourcing current is available to the load before declaring power good. Once all the conditions are met, the $\overline{\text{PG}}$ status is latched on-chip. This prevents instances of momentary current-limit operation (e.g., due to load surges or voltage spikes on the input supply) from propagating through to the $\overline{\text{PG}}$ output. However, if input conditions are not met, or if a persistent load fault does result in fault timeout, the $\overline{\text{PG}}$ latch will be cleared.

Additional details of the ramp generator operation are shown in Figure 25. To enable the generator, the large NMOS device shown in this circuit is turned off. This allows a small current source to charge the external capacitor connected at the IRAMP pin. The voltage ramp on the capacitor actually has two discrete, linear slopes. As shown in Figure 25, current is supplied from either of two sources. An internal comparator monitors the IRAMP voltage level, and selects the appropriate charging rate. Initially at turn-on, when the pin voltage is 0 V, the 600-nA source is selected, to provide a slow turn-on (or reduced-rate) sourcing period. This slow turn-on ensures that the LCA is pulled out of saturation, and is slewing to the voltage at its non-inverting input before normal rate load charging is allowed. This scheme helps reduce or eliminate current steps at the external FET on-threshold. Once the voltage at the IRAMP pin reaches approximately 0.5 V, the SLOW signal is deasserted, and the 10-µA source is selected for the remainder of the ramp period.

The IRAMP pin voltage is divided down by a factor of 100, and applied to the non-inverting input of the LCA (see Figure 24). Although the IRAMP capacitor is charged to about 6.5 V, the VLIM reference is clamped at 40 mV. Therefore, current sourced to the load during turn-on is limited to a value given by $IMAX \leq 40\ mV/R_{SENSE}$, where R_{SENSE} is the value of the external sense resistor. Therefore, both load current maximum slew rate and peak magnitude are easily set with just two external components.

DETAILED DESCRIPTION

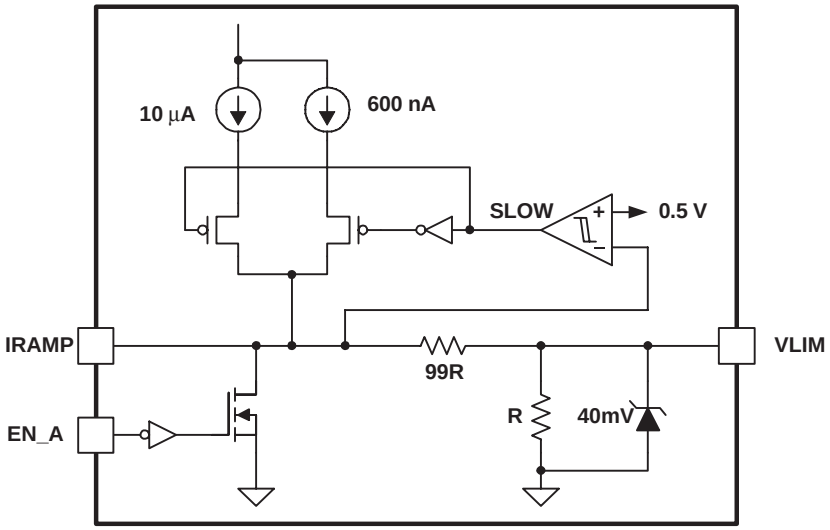


Figure 26. Ramp Generator Block Details

Note that any condition which causes turn-off of the external FET (EN_A signal goes low) also causes a rapid discharge of the IRAMP capacitor. In this manner, the soft-start function is automatically reset by the TPS2392 and TPS2393, and ready for the next load enable event.

Fault timer operation is further detailed in Figure 26. As described earlier, the LCA OVERCURRENT output drives the OC input signal shown in Figure 26. Overcurrent fault timing is actually inhibited during the reduced rate (slow turn-on) portion of the IRAMP voltage waveform. However, once the device transitions to the normal rate current ramp ($V_{O(IRAMP)} \geq 0.5$ V), the FLTTIME capacitor is charge by the 50-μA current source, generating a second voltage ramp at the FLTTIME pin. This voltage is monitored by the two comparators shown in the fault timer block. If this voltage reaches the nominal 4-V comparator threshold, the fault is latched, the GATE pin pulled low rapidly, and the $\overline{\text{FAULT}}$ output asserted. The filtered overload signal (OL) can also set the fault latch. Once a fault is latched, capacitor charging ceases (ON signal deasserted) and the timing capacitor is discharged.

The TPS2392 latches off in response to faults. Once a fault timeout occurs, the RESET signal turns on a large NMOS device to rapidly discharge the external capacitor, resetting the timer for any subsequent device reset. The TPS2392 can be reset only by cycling power to the device, or by cycling the EN input.

In response to a latched fault condition, the TPS2393 enters a fault retry mode, wherein it periodically retries the load to test for continued existence of the fault. In this mode, the FLTTIME capacitor is discharged slowly by a about a 0.4-μA constant-current sink. When the voltage at the FLTTIME pin decays below 0.5 V, the ON signal once again enables the LCA and ramp generator circuits, and a normal turn-on current ramp ensues. Again, during the load charging, the OC signal causes charging of the FLTTIME capacitor until the next delay period elapses. The sequential charging and discharging of the FLTTIME capacitor results in a typical 1% retry duty cycle. If the current-limit fault subsides (GATE pin drives to high-level output), the timing cap is rapidly discharged, duty-cycle operation stops, and the fault latch is reset. For an initial latched fault that was due to an overload condition (i.e., overload comparator response), the latching action causes charging of the timer capacitor, with GATE output already off, to initiate fault retry timing.

DETAILED DESCRIPTION

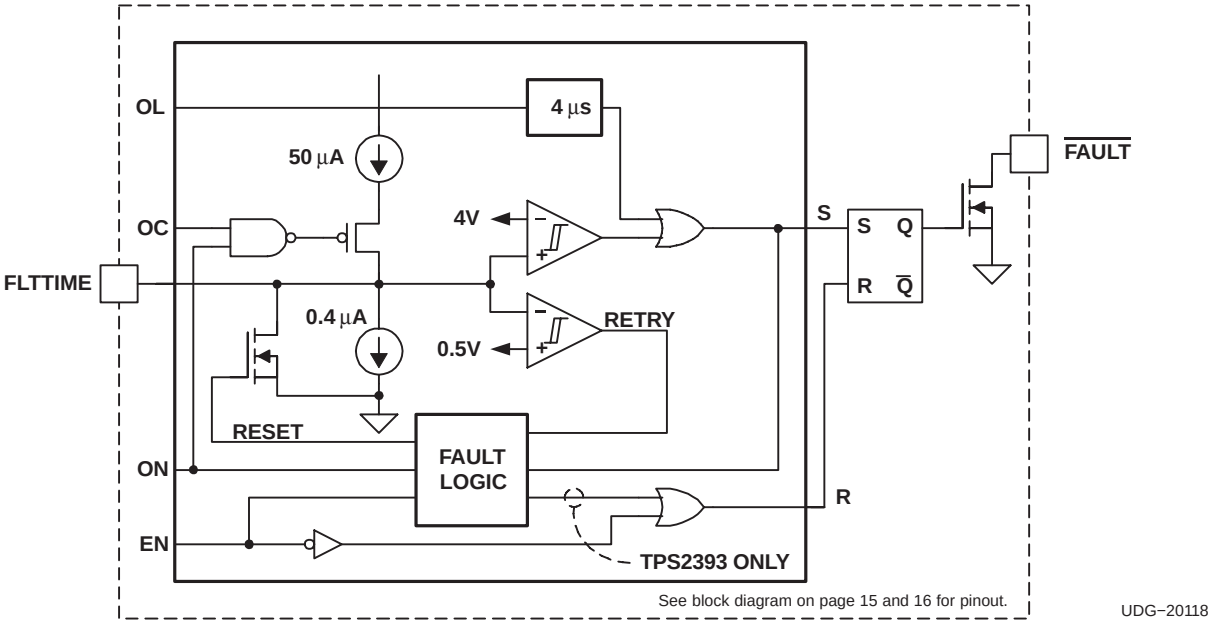


Figure 27. Fault Timer Block Operation

Note that because of the timing inhibit during the initial slow ramp period, the duty cycle in practice is slightly greater than the nominal 1% value. However, sourced current during this period peaks at only about one-eighth the maximum limit. The duty cycle of the normal ramp and constant-current periods will be about 1%.

The fault logic within the timer block automatically manages capacitor charge and discharge rates (RESET signal), and the operational status of other device-internal circuits (ON signal). For the TPS2393, the FAULT output remains asserted continuously during retry mode; it is only released if the fault condition clears.

APPLICATION INFORMATION

setting the sense resistor value

Due to the current−limiting action of the internal LCA, the maximum allowable load current for an implementation is easily programmed by selecting the appropriate sense resistor value. The LCA acts to limit the sense voltage $V_{I(ISENS)}$ to its internal reference. Once the voltage at the IRAMP pin exceeds approximately 4 V, this limit is the clamp voltage, V_{REF_K}. Therefore, a maximum sense resistor value can be determined from equation (1).

$$R_{SENSE} \leq \frac{33\ mV}{IMAX} \quad (1)$$

where:

- R_{SENSE} is the resistor value
- IMAX is the desired current limit

When setting the sense resistor value, it is important to consider two factors, the minimum current that may be imposed by the TPS2392 or TPS2393, and the maximum load under normal operation of the module. For the first factor, the specification minimum clamp value is used, as seen in equation (1). This method accounts for the tolerance in the sourced current limit below the typical level expected (40 mV/R_{SENSE}). (The clamp measurement includes LCA input offset voltage; therefore, this offset does not have to be factored into the current limit again.) Second, if the load current varies over a range of values under normal operating conditions, then the maximum load level must be allowed for by the value of R_{SENSE}. One example of this is when the load is a switching converter, or brick, which draws higher input current, for a given power output, when the distribution bus is at the low end of its operating range, with decreasing draw at higher supply voltages. To avoid current-limit operation under normal loading, some margin should be designed in between this maximum anticipated load and the minimum current limit level, or IMAX > $I_{LOAD(max)}$, for equation (1).

For example, using a 20-mΩ sense resistor for a nominal 1-A load application provides a minimum of 650 mA of overhead for load variance/margin. Typical bulk capacitor charging current during turn-on ia 2 A (40 mV/20 mΩ).

setting the inrush slew rate

The TPS2392/93 devices enable user-programming of the maximum current slew rate during load start-up events. A capacitor tied to the IRAMP pin (C1 in the typical application diagram) controls the di/dt rate. Once the sense resistor value has been established, a value for ramp capacitor C_{IRAMP}, in microfarads, can be determined from equation (2).

$$C_{IRAMP} = \frac{11}{100 \times R_{SENSE} \times \left(\frac{di}{dt}\right)_{MAX}} \quad (2)$$

where:

- R_{SENSE} is the sense resistor value in Ω
- $(di/dt)_{MAX}$ is the desired maximum slew rate in A/s

For example, if the desired slew rate for the typical application shown is 1500 mA/mS, the calculated value for C_{IRAMP} is about 3700 pF. Selecting the next larger standard value of 3900 pF (as shown in the diagram) provides some margin for capacitor and sense resistor tolerances.

As described in the Detailed Description section of this datasheet, the TPS2392 and TPS2393 initiate ramp capacitor charging, and consequently, load current di/dt at a reduced rate. This reduced rate applies until the voltage on the IRAMP pin is about 0.5 V. The maximum di/dt rate, as set by equation (2), is effective once the device has switched to the 10-µA charging source.

APPLICATION INFORMATION

setting the fault timing capacitor

The fault timeout period is established by the value of the capacitor connected to the FLTTIME pin, C_{FLT}. The timeout period permits riding out spurious current glitches and surges that may occur during operation of the system, and prevents indefinite sourcing into faulted loads swapped into a live system. However, to ensure smooth voltage ramping under all conditions of load capacitance and input supply potential, the minimum timeout should be set to accommodate these system variables. To do this, a rough estimate of the maximum voltage ramp time for a completely discharged plug-in card provides a good basis for setting the minimum timer delay.

Due to the three-phase nature of the load current at turn-on, the load voltage ramp has potentially three distinct phases and is seen by comparing Figure 1 and Figure 2. This profile depends on the relative values of load capacitance, input dc potential, maximum current limit and other factors. The first two phases are characterized by the two different slopes of the current ramp; the third phase, if required to complete load charging, is the constant-current charging at IMAX. Considering the two current ramp phases to be one period at an average di/dt simplifies calculation of the required timing capacitor.

For the TPS2392 and TPS2393, the typical duration of the soft-start ramp period, t_{SS}, is given by equation (3).

$$t_{SS} = 1183 \times C_{IRAMP} \tag{3}$$

where:

- t_{SS} is the soft-start period in milliseconds, and
- C_{IRAMP} is given in µF

During this current ramp period, the load voltage magnitude which is attained is estimated by equation (4).

$$V_{LSS} = \frac{i_{AVG}}{2 \times C_L \times C_{IRAMP} \times 100 \times R_{SENSE}} \times \left(t_{SS}\right)^2 \tag{4}$$

where:

- V_{LSS} is the load voltage reached during soft-start
- i_{AVG} is 3.38 µA for the TPS2392 and TPS2393
- C_L is the amount of the load capacitance
- t_{SS} is the soft−start period, in seconds

The quantity i_{AVG} in equation (4) is a weighted average of the two charge currents applied to C_{IRAMP} during turn-on, considering the typical output values.

If the result of equation (4) is larger than the maximum input supply value, then the load can be expected to charge completely during the inrush slewing portion of the insertion event. However, if this voltage is less than the maximum supply input, $V_{IN(max)}$, the HSPM transitions to the constant-current charging of the load. The remaining amount of time required at IMAX is determined from equation (5).

$$t_{CC} = \frac{C_L \times \left(V_{IN(max)} - V_{LSS}\right)}{\left(\frac{V_{REF\_K(min)}}{R_{SENSE}}\right)} \tag{5}$$

where:

- t_{CC} is the constant-current voltage ramp time, in seconds
- $V_{REF\_K(min)}$ is the minimum clamp voltage, 33 mV.

APPLICATION INFORMATION

With this information, the minimum recommended value timing capacitor C_{FLT} can be determined. The delay time needed will be either t_{SS} or the sum of t_{SS} and t_{CC}, according to the estimated time to charge the load. Since fault timing is generated by the constant-current charging of C_{FLT}, the capacitor value is determined by equation (6) or (7).

$$C_{FLT(min)} = \frac{55 \times t_{SS}}{3.75} \quad (6)$$

$$C_{FLT(min)} = \frac{55 \times \left(t_{SS} + t_{CC}\right)}{3.75} \quad (7)$$

where:

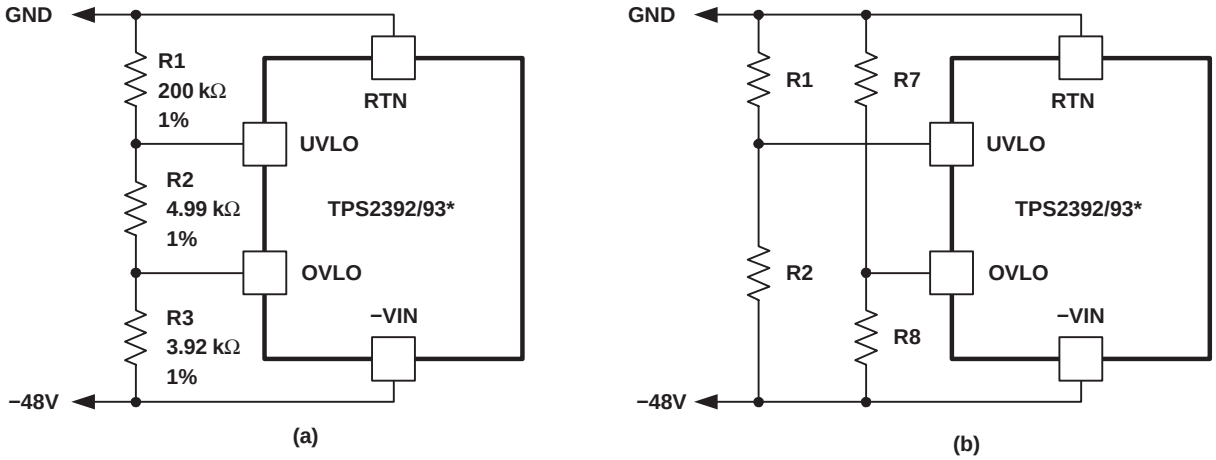
- $C_{FLT(min)}$ is the recommended capacitor value, in microfarads
- t_{SS} is the result of equation (3), in seconds
- t_{CC} is the result of equation (5), in seconds

For the typical application example, with the 100-µF filter capacitor in front of the dc-to-dc converter, equations (3) and (4) estimate the load voltage ramping to −46 V during the soft-start period. If the module should operate down to −72-V input supply, approximately another 1.58 ms of constant-current charging may be required. Therefore, equation (7) is used to determine $C_{FLT(min)}$, and the result is approximately 0.1 µF.

setting the undervoltage and overvoltage thresholds

The UVLO and OVLO pins can be used to set the undervoltage (V_{UV}) and overvoltage (V_{OV}) thresholds of the hot swap circuit. When the input supply is below V_{UV} or above V_{OV}, the GATE pin is held low, disconnecting power from the load, and deasserting the $\overline{PG}$ output. When input voltage is within the UV/OV window, the GATE drive is enabled, assuming all other input conditions are valid for turn-on.

Threshold hysteresis is provided via two internal sources which are switched to either pin whenever the corresponding input level exceeds the internal 1.4-V reference. The additional bias shifts the pin voltage in proportion to the external resistance connected to it. This small voltage shift at the device pin is gained up by the external divider to input supply levels.



$$V_{UV\_L} = \frac{R1 + R2 + R3}{R2 + R3} \times V_{REF}$$

$$V_{OV\_L} = \frac{R1 + R2 + R3}{R3} \times V_{REF} - I_{SRC\_UV} \times R1$$

$$V_{UV\_L} = \frac{R1 + R2}{R2} \times V_{TH\_UV}$$

$$V_{OV\_L} = \frac{R7 + R8}{R8} \times V_{TH\_OV}$$

*Additional details omitted for clarity. See block diagram on page 15 and 16 for pinout.

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Figure 28. Programming the Undervoltage and Overvoltage Thresholds

APPLICATION INFORMATION

The UV and OV thresholds can be individually programmed with a three-resistor divider connected to it as shown in the typical application diagram, and again in Figure 27a. When the desired trip voltages and undervoltage hysteresis have been established for the protected board, the resistor values needed can be determined from the following equations. Generally, the process is simplest by first selecting the top leg of the divider (R1 in the diagram) needed to obtain the threshold hysteresis. This value is calculated from equation (8).

$$R1 = \frac{V_{HYS\_UV}}{10\ \mu A} \tag{8}$$

where:

- V_{HYS_UV} is the undervoltage hysteresis value

For example, assume the typical application design targets have been set to undervoltage turn-on at 33 V (input supply rising), turn-off at 31 V (input voltage falling), and overvoltage shutdown at 72 V. Then equation (8) yields R1 = 200 kΩ for the 2-V hysteresis. Once the value of R1 is selected, it is used to calculate resistors R2 and R3.

$$R2 = \frac{1.4 \times R1}{\left(V_{UV\_L} - 1.4\right)} \times \left[1 - \frac{V_{UV\_L}}{\left(V_{OV\_L} + 10^{-5} \times R1\right)}\right] \tag{9}$$

$$R3 = \frac{1.4 \times R1 \times V_{UV\_L}}{\left(V_{UV\_L} - 1.4\right) \times \left(V_{OV\_L} + 10^{-5} \times R1\right)} \tag{10}$$

where:

- V_{UV_L} is the UVLO threshold when the input supply is low; i.e., less than V_{UV}
- V_{OV_L} is the OVLO threshold when the input supply is low; .i.e., less than V_{OV}

Again referring to the example schematic, equations (9) and (10) produce R2 = 4.909 kΩ (4.99 kΩ selected) and R3 = 3.951 kΩ (3.92 kΩ selected), as shown. For the selected resistor values, the expected nominal supply thresholds are as shown on the typical application diagram. The hysteresis on the overvoltage threshold, as seen at the supply inputs, is given by the quantity (10 μA) * (R1 + R2). For the majority of applications, this value will be very nearly the same as the UV hysteresis, since typically R1 >> R2.

If more independent control is needed for the OVLO hysteresis, there are several options. One option is to use separate dividers for both the UVLO and OVLO pins, as shown in Figure 27b. In this case, once R1 and R7 have been selected for the required hysteresis per equation (8), the bottom resistors in the dividers (R2 and R8 in Figure 27b) can be found from equation (11).

$$R_{XVLO} = \frac{V_{REF}}{\left(V_{XV\_L} - V_{REF}\right)} \times R_{TOP} \tag{11}$$

where:

- R_{XVLO} is R2 or R8
- R_{TOP} is R1 or R7 as appropriate for the threshold being set
- V_{XV_L} is the under (V_{UV_L}) or overvoltage (V_{OV_L}) threshold at the supply input
- V_{REF} is either V_{TH_UV} or V_{TH_OV} from the specification table, as required for the resistor being calculated

capacitor on UVLO pin

As shown in the typical application diagram, a minimum 1500 pF capacitor is required on the UVLO pin of the TPS2392 or TPS2393. For some systems, it may be desirable to slow down the response of the controller to undervoltage conditions. For example, if frequent voltage dips are anticipated due to other power events in the system, it may be beneficial to delay somewhat the response of the detection circuit. For these situations, the size of the capacitor can be increased accordingly, over the value shown.

APPLICATION INFORMATION

using the $\overline{PG}$ output

The $\overline{PG}$ output is an indication of the load power status. $\overline{PG}$ is asserted after a load turn-on, once the load voltage has ramped up to the input dc level, as indicated by a small VDS drop across the pass FET. The load voltage is sensed by the DRAINSNS pin, which is connected to the pass FET drain through a small-signal blocking diode. Also, the TPS2392 and TPS2393 first confirm that the full programmed sourcing current (typically 40 mV/R_{SENSE}) is available to the load electronics prior to declaring power good. The $\overline{PG}$ status is latched once the power conditions are met, so that momentary current limiting operation due to input supply transients is not reflected in this output status. This pin can be used to enable downstream converters, provide a visual indication of load power good, or be level-translated or optocoupled to provide status reporting back to the host controller.

When using $\overline{PG}$ to drive the enable input of a converter, care should be taken not to exceed the manufacturer's maximum voltage ratings for the pin. When asserted, the output driver pulls the $\overline{PG}$ pin to the −VIN pin potential. Because this status in latched, subsequent current limit operation of the circuit could result in pulling the enable input below the brick's VIN− potential during the fault timeout period. If the brick does not provide an internal clamp on this pin, a diode can be connected as shown in Figure 28 to externally limit the swing below VIN−. In either case, a resistor (R7 in Figure 28) should be used to limit the current pulled from this pin, protecting both the converter and the $\overline{PG}$ output. R7 should be large enough to limit the $\overline{PG}$ input current to less than 10 mA, while still allowing the brick enable to be pulled below its maximum V_{IL} threshold.

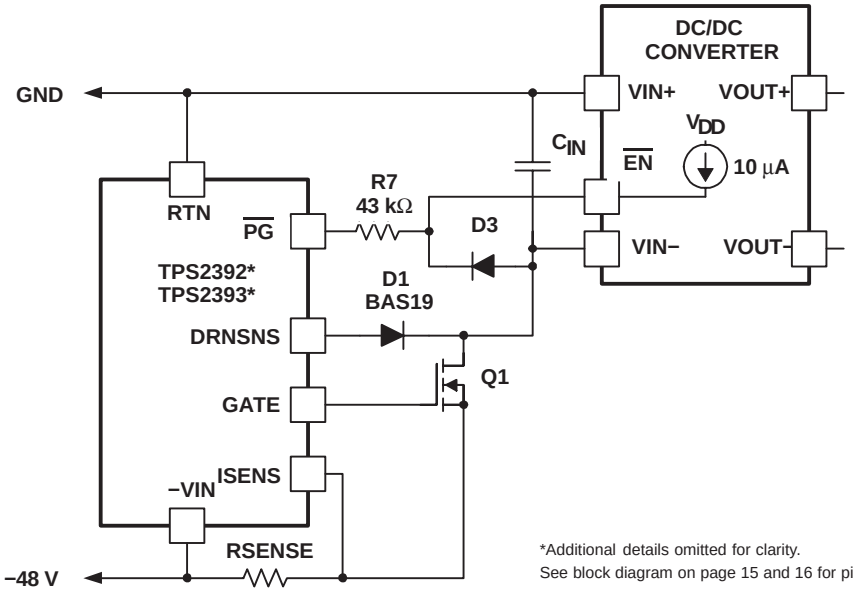


Figure 29. TPS2392/TPS2393 Active-Low Converter Enable

APPLICATION INFORMATION

If the selected converter cannot tolerate any voltage excursions below VIN− potential, an alternative is to drive the enable through an optocoupler. An implementation is shown in Figure 29.

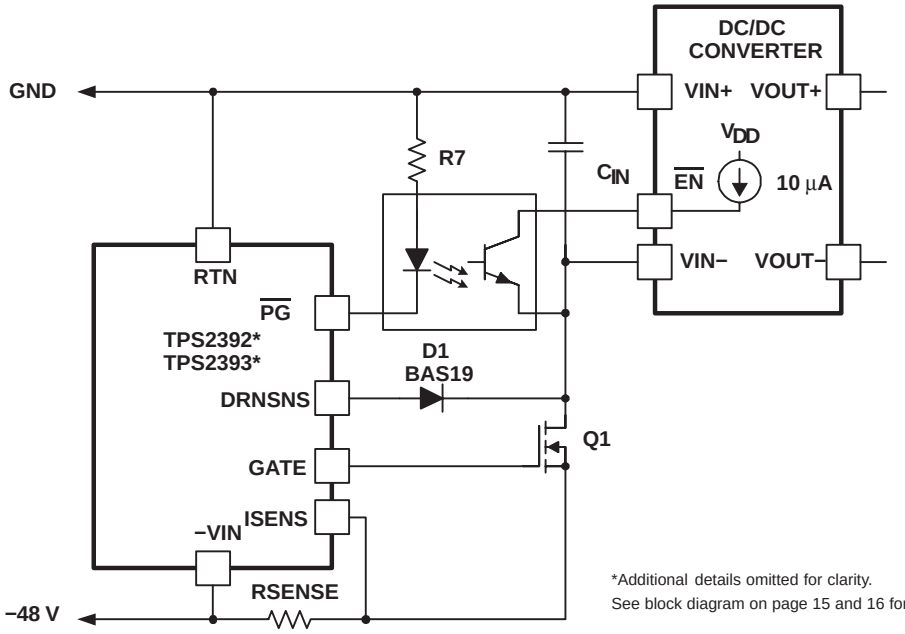


Figure 30. $\overline{PG}$ Driving An Optocoupler

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2393DBT	LIFEBUY	TSSOP	DBT	44	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS2393	
TPS2393PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2393	Samples
TPS2393PWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2393	Samples
TPS2393PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPS2393	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

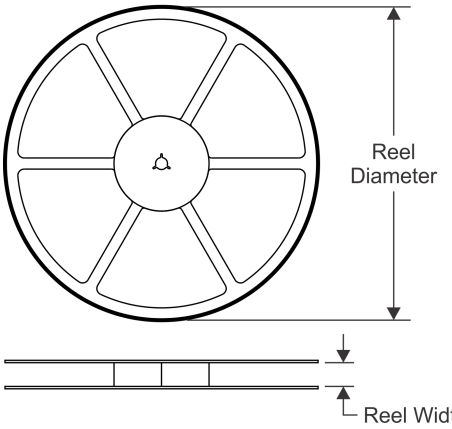
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

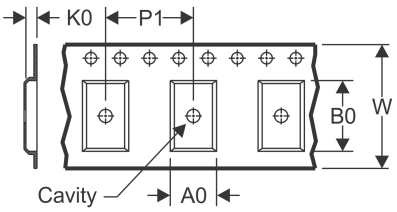
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

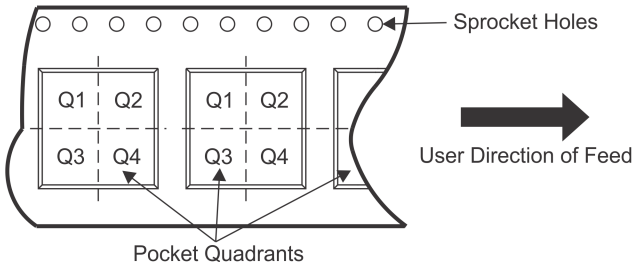


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

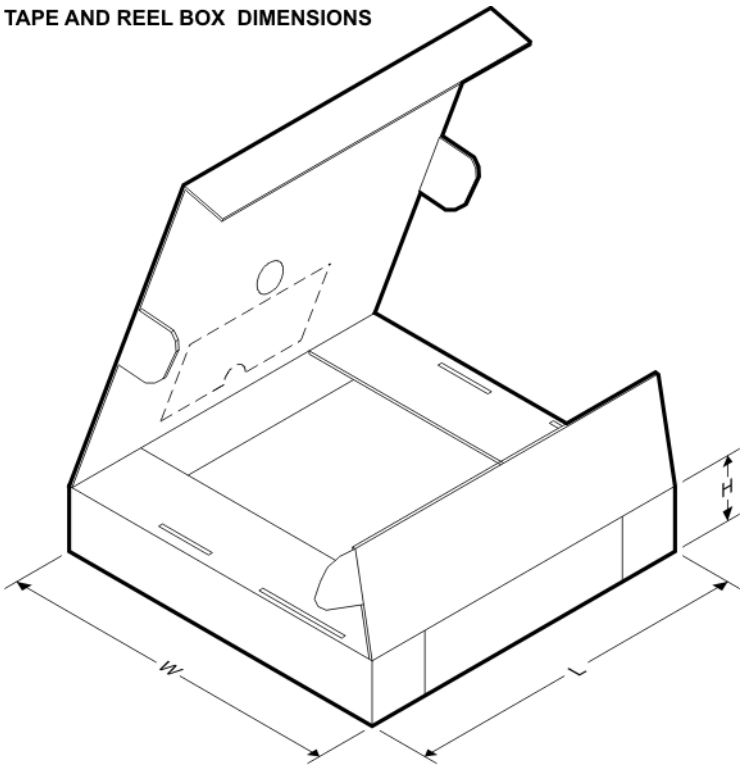
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2393PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

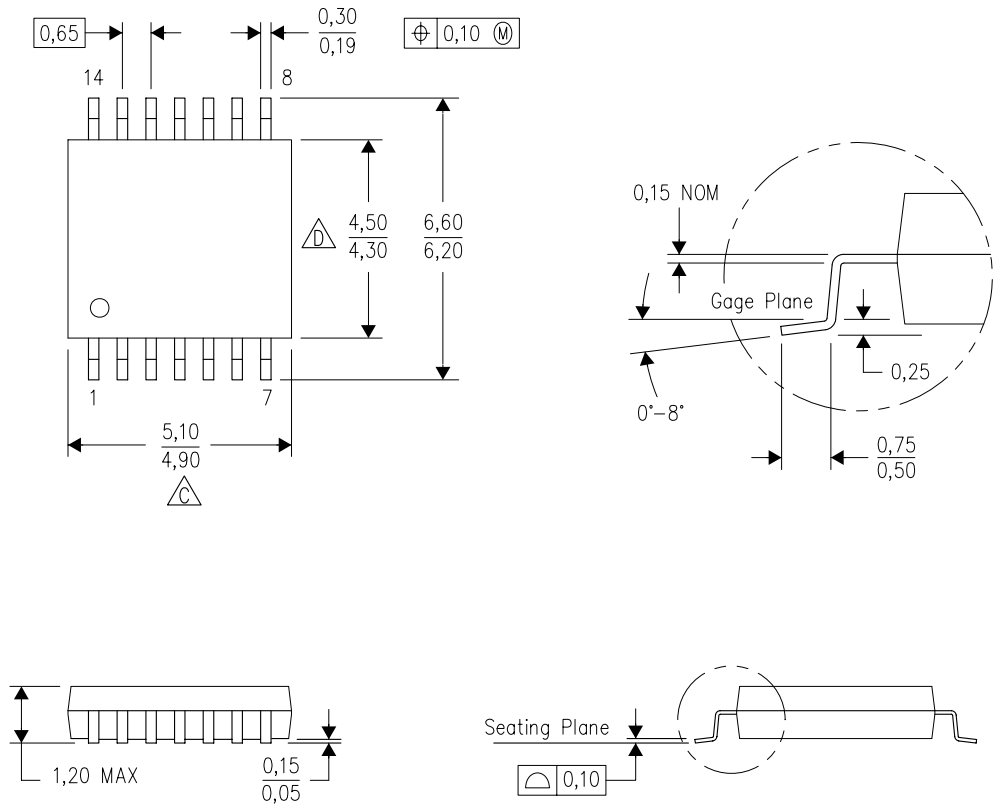
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2393PWR	TSSOP	PW	14	2000	853.0	449.0	35.0

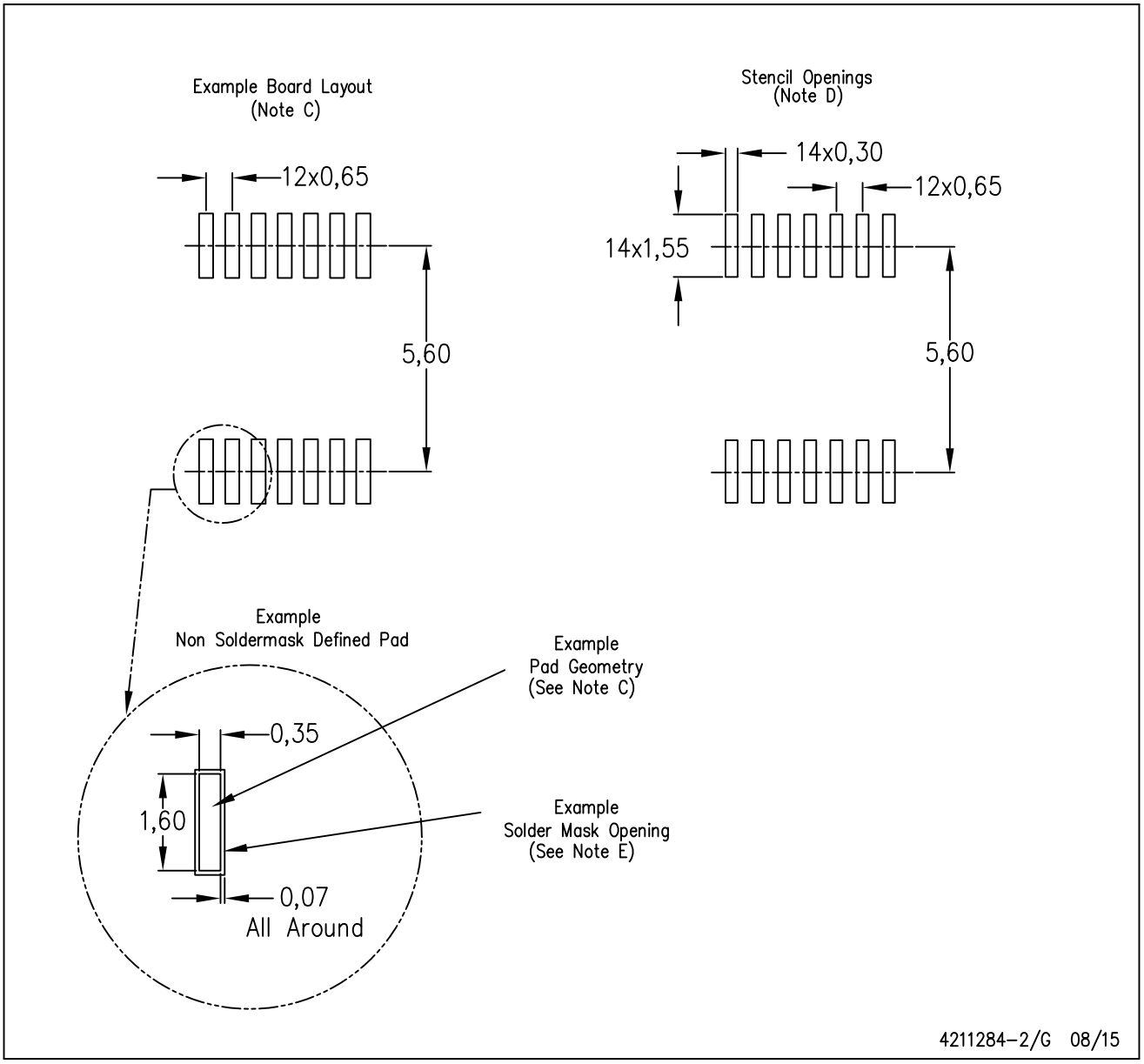
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



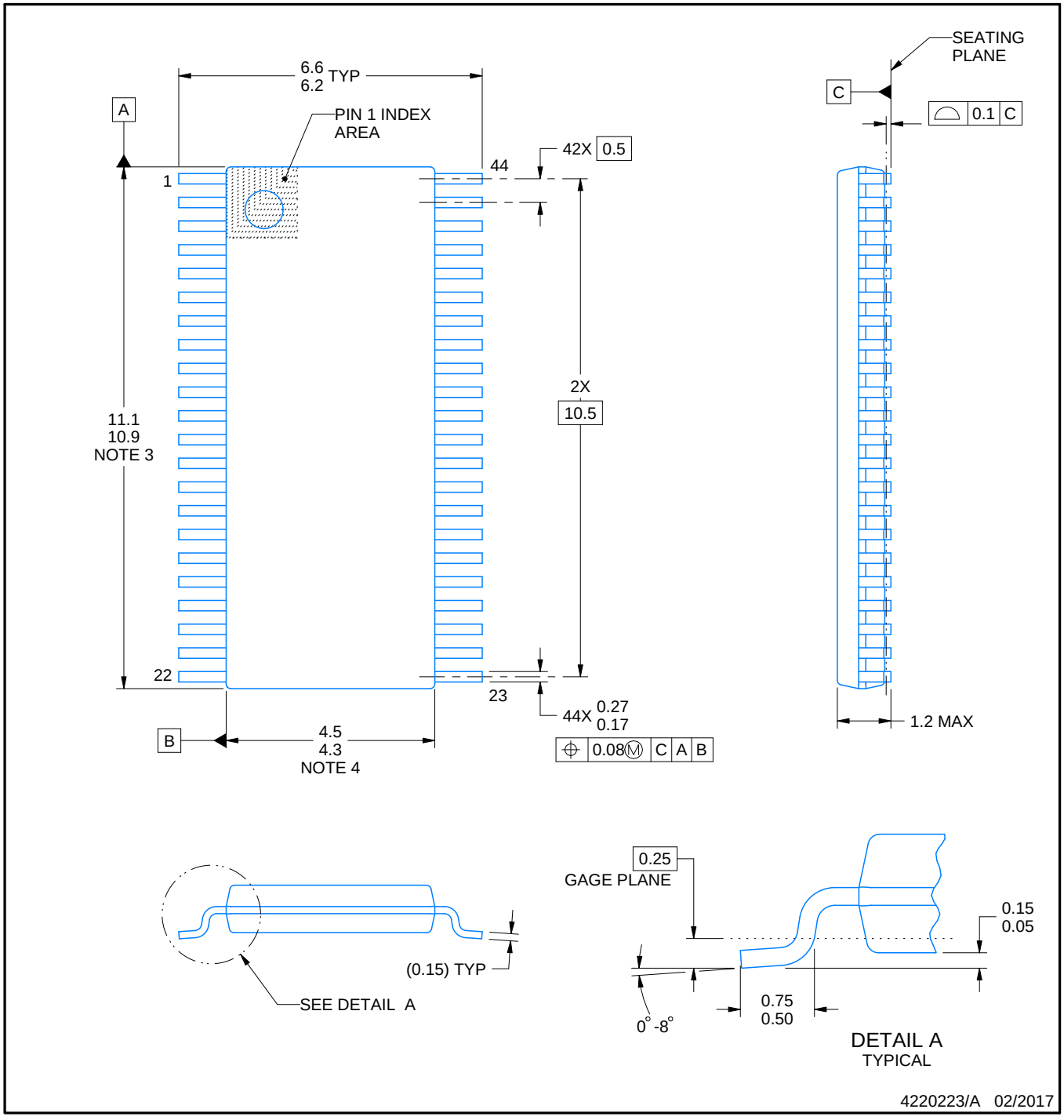
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DBT0044A

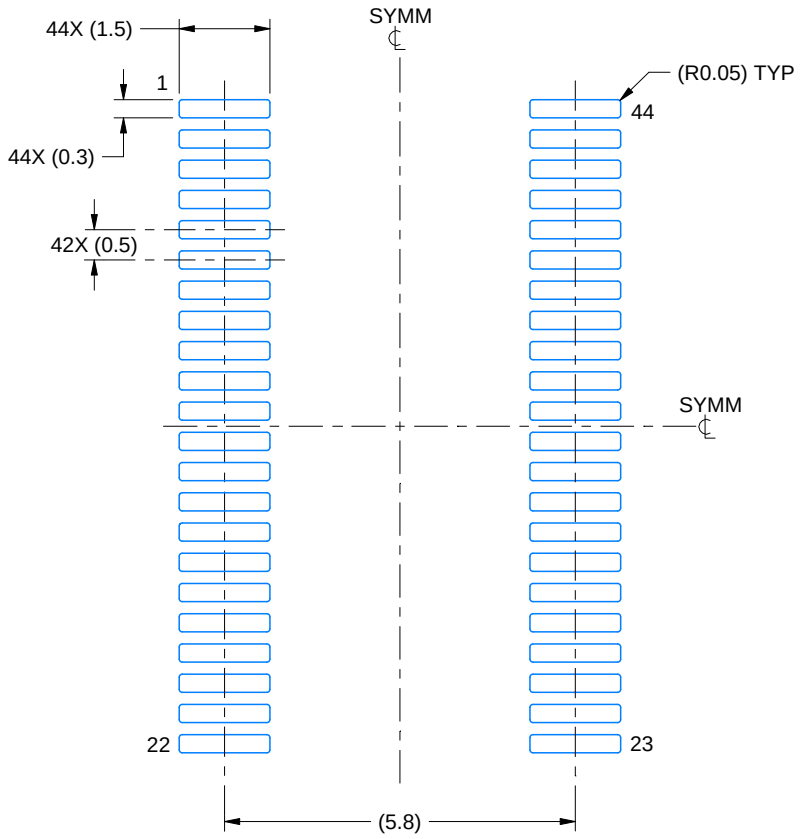
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

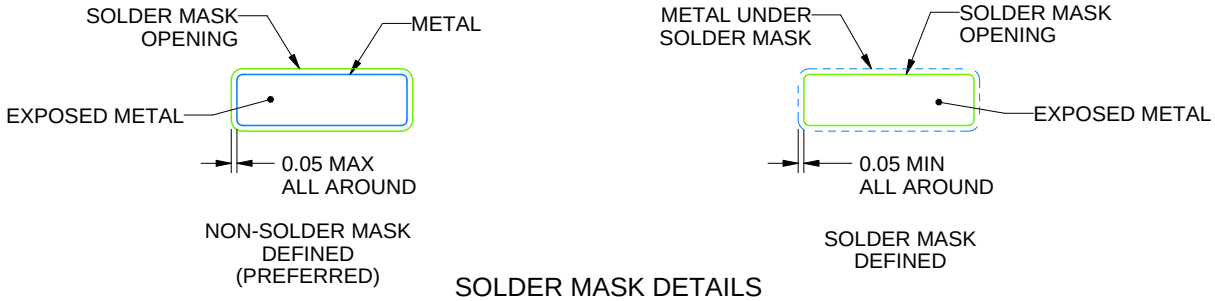


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

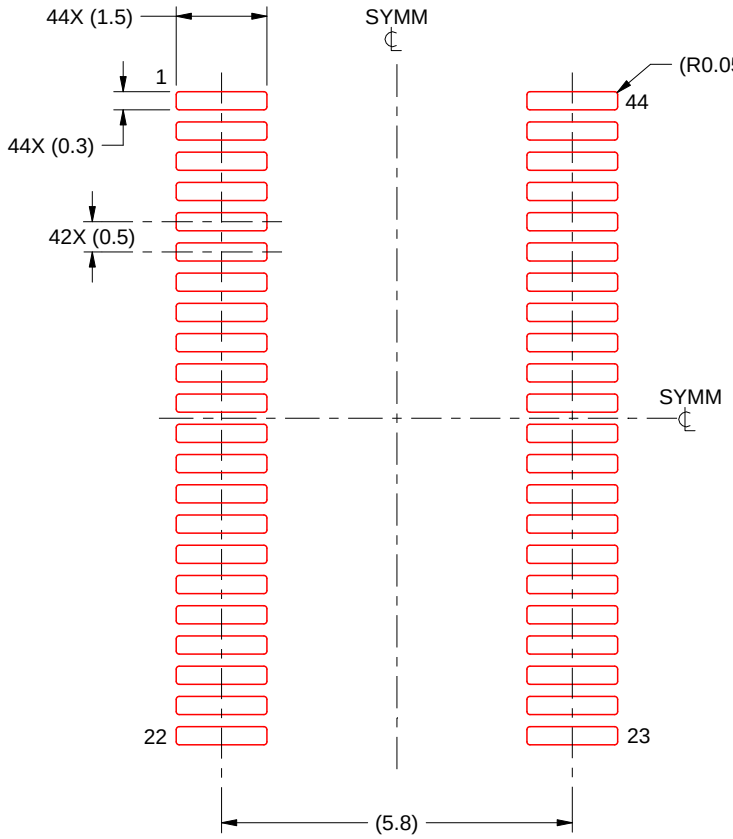


SOLDER MASK DETAILS

4220223/A 02/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4220223/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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