采用微封装的 TMP302-Q1 汽车级、简单易用型、低功耗温度开关

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C6
- 低功耗：15µA（最大值）
- SOT563 封装：1.6mm × 1.6mm × 0.6mm
- 跳闸点精度：在 40°C 至 125°C 温度范围内为 ± 0.2°C（典型值）
- 引脚可选跳变点
- 开漏输出，低电平有效
- 可选滞后：5°C 或 10°C
- 低电源电压范围: 1.4V 至 3.6V

2 应用

- 信息娱乐
- 汽车空调
- 引擎控制单元
- 汽车黑匣子
- 车身控制模块
- 安全气囊控制单元
- 过热监控
- 电子保护系统

3 说明

TMP302-Q1 系列器件是一款采用微封装 (SOT563) 的温度开关。TMP302-Q1 系列器件可通过引脚来选择跳闸点和迟滞，因而具有低功耗（最大 15µA）且简单易用的特点。

这些器件运行时无需额外组件；其功能不受微处理器或微控制器的影响。

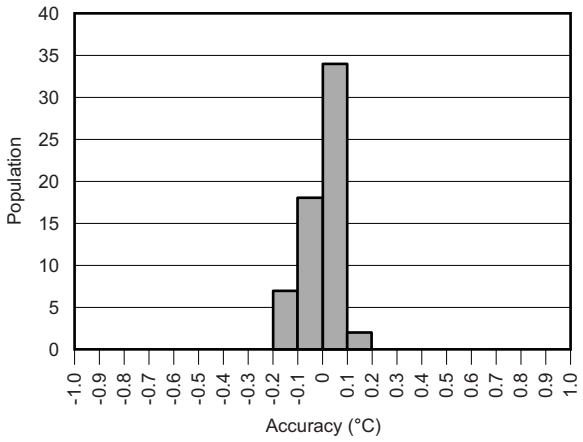
TMP302-Q1 系列器件具有多种不同的版本，跳闸点为 50ºC 至 125ºC（以 5ºC 为递增单位）（参阅*器件比较表*）。

器件信息

器件型号	封装	
TMP302-Q1	SOT563 (6)	1.60mm x 1.20mm

1. 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

跳变阈值精度



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4 修订历史记录

Changes from Revision B (July 2015) to Revision C — **Page**

- Changed the supply voltage maximum value from: 3.6 V to: 4 V ... 4
- Changed the input pin supply voltage maximum value from: V_S + 0.5 V to: V_S + 0.3 and ≤ 4 V ... 4
- Changed the output pin voltage maximum value from: 3.6 V to: 4 V ... 4
- Added the specified temperature to the *Recommended Operating Conditions* table ... 4
- Updated junction-to-ambient thermal resistance from 200 to 210.3 ... 4
- Updated junction-to-case (top) thermal resistance from 73.7 to 105.0 ... 4
- Updated junction-to-board thermal resistance from 34.4 to 87.5 ... 4
- Updated junction-to-top characterization parameter from 3.1 to 6.1 ... 4
- Updated junction-to-board characterization parameter from 34.2 to 87.0 ... 4
- Changed the *Design Requirements* section ... 10
- 添加了*接收文档更新通知* 部分 ... 12

Changes from Revision A (November 2014) to Revision B — **Page**

- Changed the *Handling Ratings* table to E*SD Ratings* and moved storage temperature to the *Absolute Maximum Ratings* table ... 4

Changes from Original (October 2014) to Revision A — **Page**

- 将器件状态从“产品预览”更改为“生产” ... 1

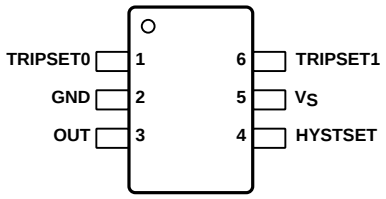
5 器件比较表

器件	可选跳闸点 (°C)(1)
TMP302A-Q1	50、55、60、65
TMP302B-Q1	70、75、80、85
TMP302C-Q1	90、95、100、105
TMP302D-Q1	110、115、120、125

(1) 如需了解其他可用跳闸点，请联系 TI 代表。

6 Pin Configuration and Functions

DRL Package
6-Pin SOT563
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	TRIPSET0	Digital Input	Used in combination with TRIPSET1 to select the temperature at which the device trips
2	GND	Ground	Ground
3	$\overline{OUT}$	Digital Output	Open drain, active-low output
4	HYSTSET	Digital Input	Used to set amount of thermal hysteresis
5	V_S	Power Supply	Power supply
6	TRIPSET1	Digital Input	Used in combination with TRIPSET0 to select the temperature at which the device trips

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply		4	V
	Input pin (TRIPSET0, TRIPSET1, HYSTSET)	–0.5	V_S + 0.3 and ≤ 4	
	Output pin ($\overline{OUT}$)	–0.5	4	
Current	Output pin ($\overline{OUT}$)		10	mA
Temperature	Operating	–55	130	°C
	Junction		150	
	Storage	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Power supply voltage	1.4	3.3	3.6	V
R_{pullup}	Pullup resistor connected from $\overline{OUT}$ to V_S	10		100	kΩ
T_A	Specified temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TMP302-Q1 DRL (SOT563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	210.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	105.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	87.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

At T_A = –40°C to +125°C, and V_S = 1.4 to 3.6 V (unless otherwise noted). 100% of all units are production tested at T_A = 25°C; overtemperature specifications are specified by design.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT						
	Trip point accuracy			±0.2	±2	°C
	Trip point accuracy versus supply			±0.2	±0.5	°C/V
	Trip point hysteresis	HYSTSET = GND		5		°C
		HYSTSET = V_S		10		°C
TEMPERATURE TRIP POINT SET						
	Temperature trip point set	TRIPSET1 = GND, TRIPSET0 = GND		Default		°C
		TRIPSET1 = GND, TRIPSET0 = V_S		Default + 5		°C
		TRIPSET1 = V_S, TRIPSET0 = GND		Default + 10		°C
		TRIPSET1 = V_S, TRIPSET0 = V_S		Default + 15		°C
HYSTERESIS SET INPUT						
V_{IH}	Input logic level high		0.7 × V_S		V_S	V
V_{IL}	Input logic level low		–0.5		0.3 × V_S	V
I_I	Input current	0 < V_I < 3.6 V			1	µA
DIGITAL OUTPUT						
V_{OL}	Output logic level low	V_S > 2 V, I_{OL} = 3 mA	0		0.4	V
		V_S < 2 V, I_{OL} = 3 mA	0		0.2 × V_S	V
POWER SUPPLY						
	Operating Supply Range		1.4		3.6	V
I_Q	Quiescent Current	T_A = –40°C to +125°C		8	15	µA
		V_S = 3.3 V, T_A = 50°C		7		µA

7.6 Typical Characteristics

At T_A = 25°C and V_S = 3.3 V, unless otherwise noted.

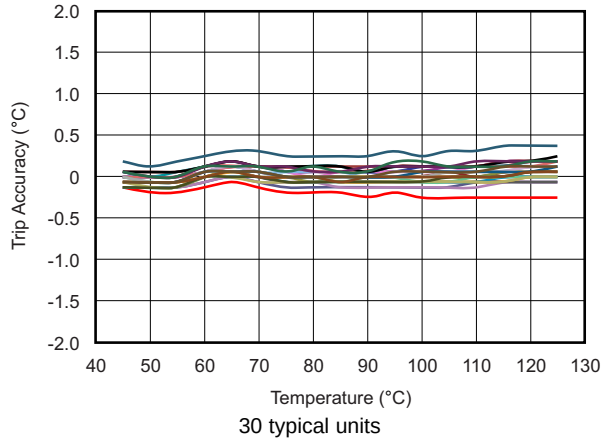


Figure 1. Trip Accuracy Error vs Temperature

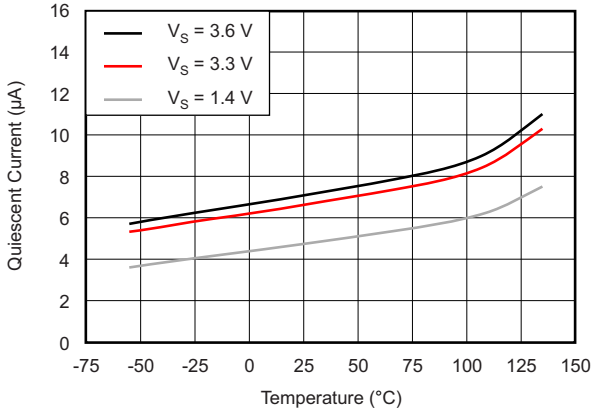


Figure 2. Quiescent Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C and V_S = 3.3 V, unless otherwise noted.

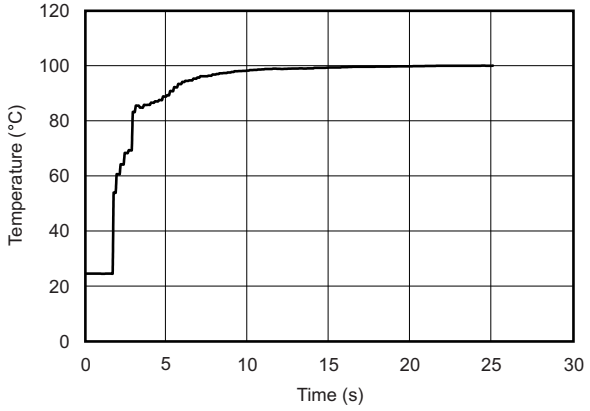


Figure 3. Temperature Step Response in Perfluorinated Fluid at 100°C vs Time

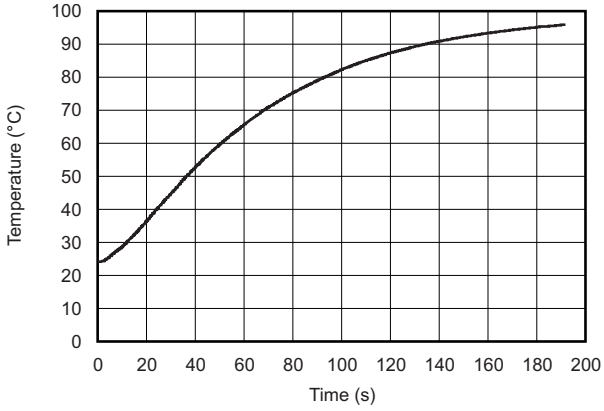


Figure 4. Thermal Step Response in Air at 100°C vs Time

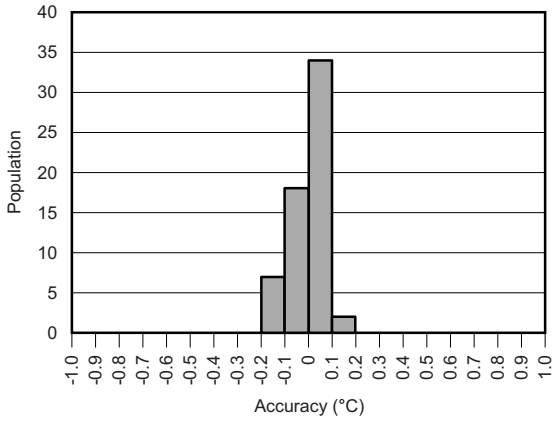


Figure 5. Trip Threshold Accuracy

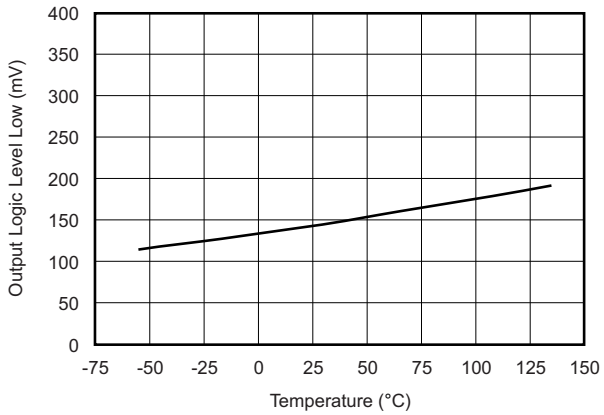


Figure 6. Output Logic-Level Low V_{OL} vs Temperature

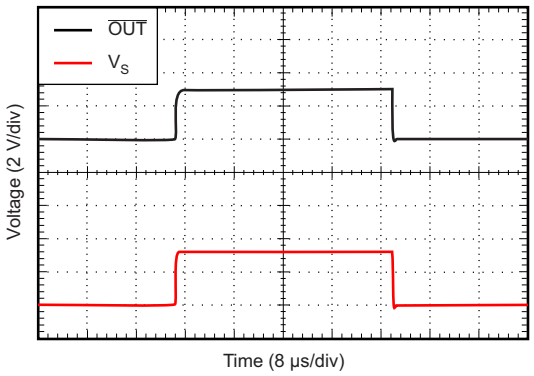


Figure 7. Power-Up and Power-Down Response

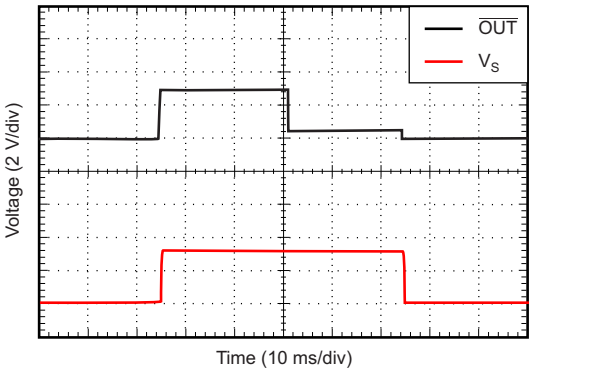


Figure 8. Power-Up, Trip, and Power-Down Response

8 Detailed Description

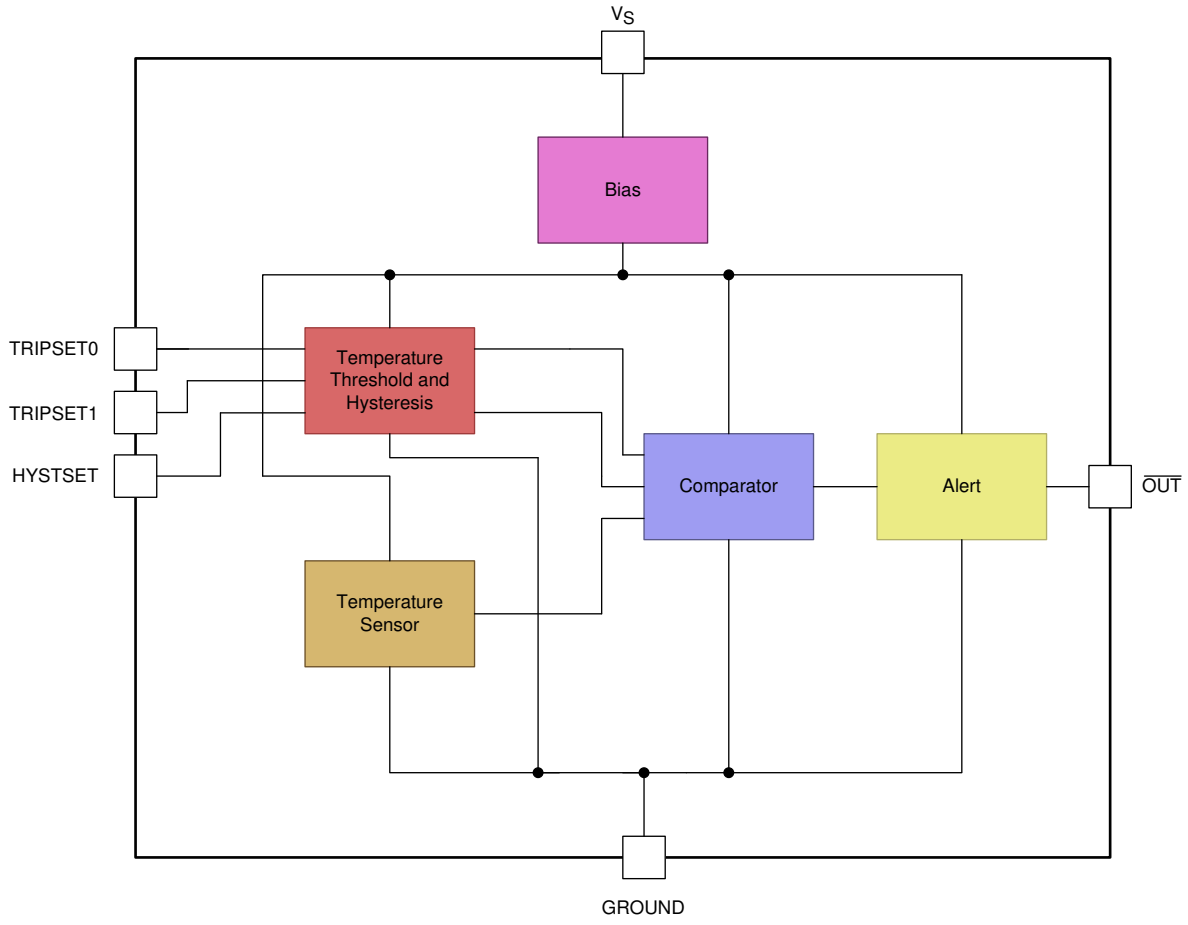
8.1 Overview

The TMP302-Q1 temperature switch is optimal for ultra low-power applications that require accurate trip thresholds. A temperature switch is a device that issues an alert response when a temperature threshold is reached or exceeded. The trip thresholds are programmable to four different settings using the TRIPSET1 and TRIPSET0 pins. Table 1 lists the pin settings versus trip points.

Table 1. Trip Point versus TRIPSET1 and TRIPSET0

TRIPSET1	TRIPSET0	TMP302A-Q1	TMP302B-Q1	TMP302C-Q1	TMP302D-Q1
GND	GND	50°C	70°C	90°C	110°C
GND	V_S	55°C	75°C	95°C	115°C
V_S	GND	60°C	80°C	100°C	120°C
V_S	V_S	65°C	85°C	105°C	125°C

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 HYSTSET

If the temperature trip threshold is crossed, the open-drain, active low output ($\overline{OUT}$) goes low and does not return to the original high state (that is, V_S) until the temperature returns to a value within a hysteresis window set by the HYSTSET pin. The HYSTSET pin allows the user to choose between a 5°C and a 10°C hysteresis window. Table 2 lists the hysteresis window that corresponds to the HYSTSET setting.

Table 2. HYSTSET Window

HYSTSET	THRESHOLD HYSTERESIS
GND	5°C
V_S	10°C

For the specific case of the device, if the HYSTSET pin is set to 10°C (that is, connected to V_S) and the device is configured with a 60°C trip point (TRIPSET1 = V_S, TRIPSET0 = GND), when this threshold is exceeded the output does not return to the original high state until it reaches 50°C. This case is more clearly shown in Figure 9.

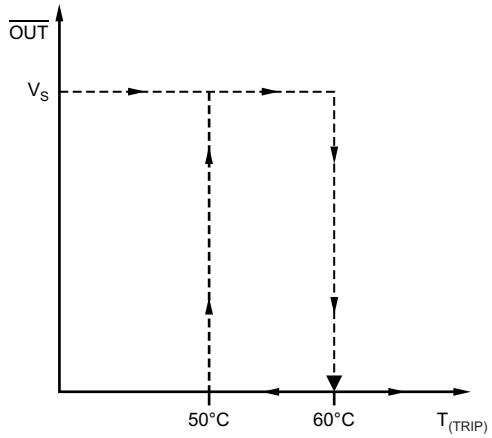


Figure 9. TMP302A-Q1: HYSTSET = V_S, TRIPSET1 = V_S, TRIPSET0 = GND

8.4 Device Functional Modes

The TMP302-Q1 family of devices has a single functional mode. Normal operation for the TMP302-Q1 family of devices occurs when the power-supply voltage applied between the V_S pin and GND is within the specified operating range of 1.4 to 3.6 V. The temperature threshold is selected by connecting the TRIPSET0 and TRIPSET1 pins to either the GND or V_S pins (see Table 1). Hysteresis is selected by connecting the HYSTSET pin to either the GND or V_S pins (see Table 2). The output pin, $\overline{OUT}$, remains high when the temperature is below the selected temperature threshold. The $\overline{OUT}$ pin remains low when the temperature is at or above the selected temperature threshold. The $\overline{OUT}$ pin returns from a low state back to the high state based upon the amount of selected hysteresis (see the *HYSTSET* section).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Configuring the TMP302-Q1

The TMP302-Q1 family of devices is simple to configure. The only external components that the device requires are a bypass capacitor and pullup resistor. Power-supply bypassing is strongly recommended. Use a 0.1-µF capacitor placed as close as possible to the supply pin. To minimize the internal power dissipation of the TMP302-Q1 family of devices, use a pullup resistor value greater than 10 kΩ from the $\overline{OUT}$ pin to the V_S pin. Refer to Table 1 for trip-point temperature configuration. The TRIPSET pins can be toggled dynamically; however, the voltage of these pins must not exceed V_S. To ensure a proper logic high, the voltage must not drop below 0.7 V × V_S.

9.2 Typical Application

Figure 10 shows the typical circuit configuration for the TMP302-Q1 family of devices. The TMP302-Q1 family of devices is configured for the default temperature threshold by connecting the TRIPSET0 and TRIPSET1 pins directly to ground. Connecting the $\overline{HYST}$SET pin to ground configures the device for 5°C of hysteresis. Place a 10-kΩ pullup resistor between the $\overline{OUT}$ and V_S pins. Place a 0.1-µF bypass capacitor between the V_S pin and ground, close to the TMP302-Q1 device.

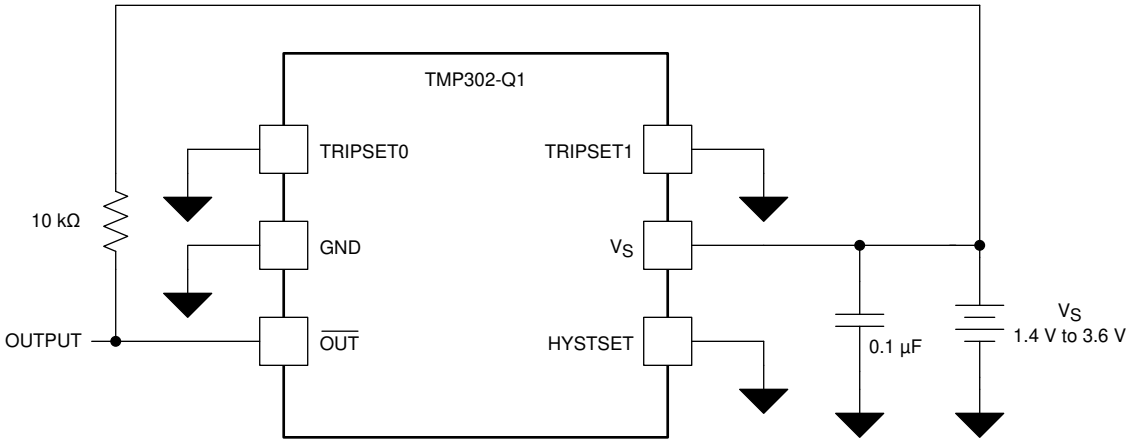


Figure 10. TMP302-Q1 Typical Application Schematic

Figure 11 shows the most generic implementation of the TMP302-Q1 family of devices. Switches are shown connecting the TMPSET0, TMPSET1 and HYSTSET pins to either V_S or ground. The use of switches is not strictly required; the switches are shown only to illustrate the various pin connection combinations. In practice, connecting the TMPSET0, TMPSET1 and HYSTSET pins to ground or directly to the V_S pin is sufficient and minimizes space and cost. If additional flexibility is desired, connections from the TMPSET0, TMPSET1 and HYSTSET pins can be made through 0-Ω resistors which can be either populated or not populated depending upon the desired connection.

Typical Application (continued)

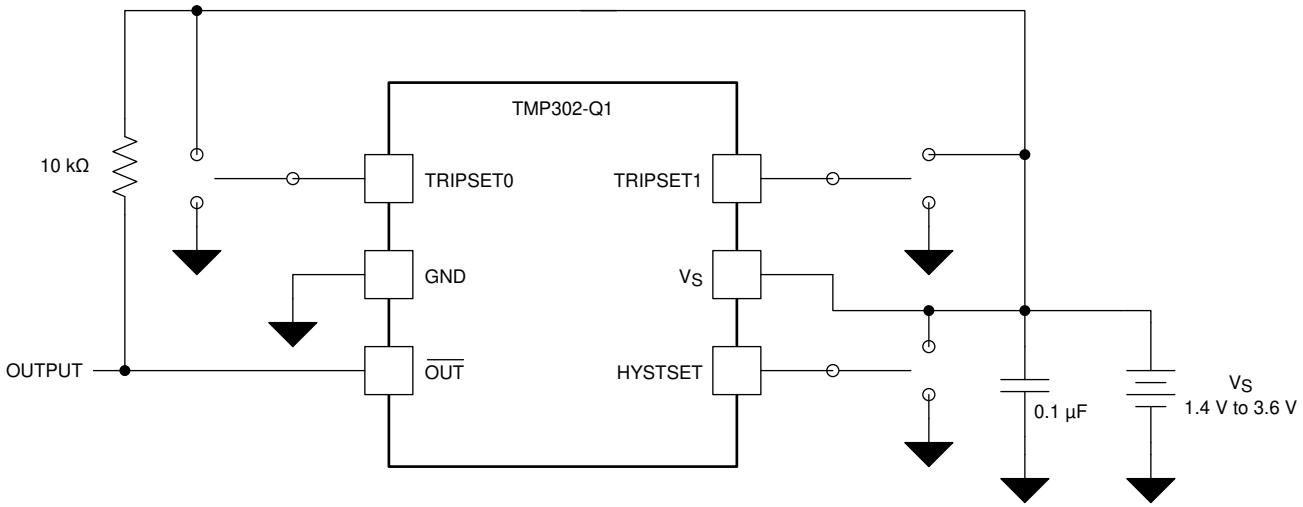


Figure 11. TMP302-Q1 Generic Application Schematic

9.2.1 Design Requirements

Designing with the TMP302-Q1 family of devices is simple. The TMP302-Q1 family of devices is a temperature switch commonly used to signal a microprocessor in the event of an over temperature condition. The temperature at which the TMP302-Q1 family of devices issues an active low alert is determined by the configuration of the TRIPSET0 and TRIPSET1 pins. These two pins are digital inputs and must be tied either high or low, according to Table 1. The TMP302-Q1 family of devices issues an active low alert when the temperature threshold is exceeded. The device has built-in hysteresis to avoid the device from signaling the microprocessor as soon as the temperature drops below the temperature threshold. The amount of hysteresis is determined by the HYSTSET pin. This pin is a digital input and must be tied either high or low, according to Table 2.

See Figure 10 and Figure 11 for typical circuit configurations.

9.2.2 Detailed Design Procedure

Determine the threshold temperature and hysteresis required for the application. Connect the TMPSET0, TMPSET1, and HYSTSET pins according to the design requirements. Refer to Table 1 and Table 2. Use a 10-kΩ pullup resistor from the $\overline{OUT}$ pin to the V_S pin. To minimize power, a larger-value pullup resistor can be used but must not exceed 100 kΩ. Place a 0.1-µF bypass capacitor close to the TMP302-Q1 device to reduce noise coupled from the power supply.

9.2.3 Application Curves

Figure 12 and Figure 13 show the TMP302A-Q1 power-on response with the ambient temperature less than 50°C and greater than 50°C respectively. The TMP302A-Q1 was configured with trip point set to 50°C. The TMP302B-Q1, TMP302C-Q1, and TMP302D-Q1 devices behave similarly with regards to power on response with T_A below or above the trip point. Note that the $\overline{OUT}$ signal typically requires 35 ms following power on to become valid.

Typical Application (continued)

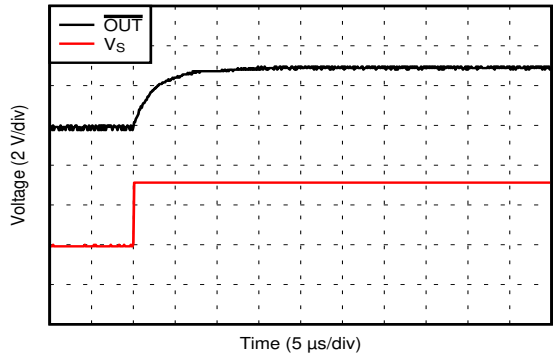


Figure 12. TMP302A-Q1 Power-On Response, T_A Less than 50°C

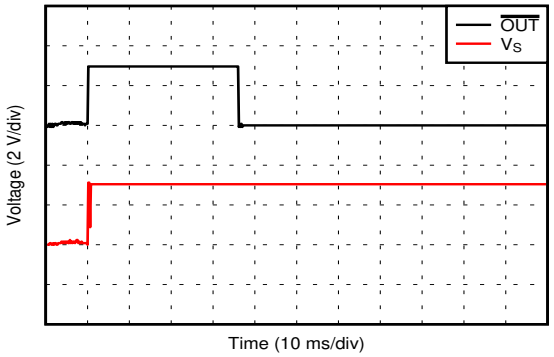


Figure 13. TMP302A-Q1 Power-On Response, T_A Greater than 50°C

10 Power Supply Recommendations

The TMP302-Q1 family of devices is designed to operate from a single power supply within the range 1.4 V and 3.6 V. No specific power supply sequencing with respect to any of the input or output pins is required. The TMP302-Q1 family of devices is fully functional within 35 ms of the voltage at the V_S pin reaching or exceeding 1.4 V.

11 Layout

11.1 Layout Guidelines

Place the power supply bypass capacitor as close as possible to the V_S and GND pins. The recommended value for this bypass capacitor is 0.1-µF. Additional bypass capacitance can be added to compensate for noisy or high-impedance power supplies. Place a 10-kΩ pullup resistor from the open drain $\overline{OUT}$ pin to the power supply pin V_S.

11.2 Layout Example

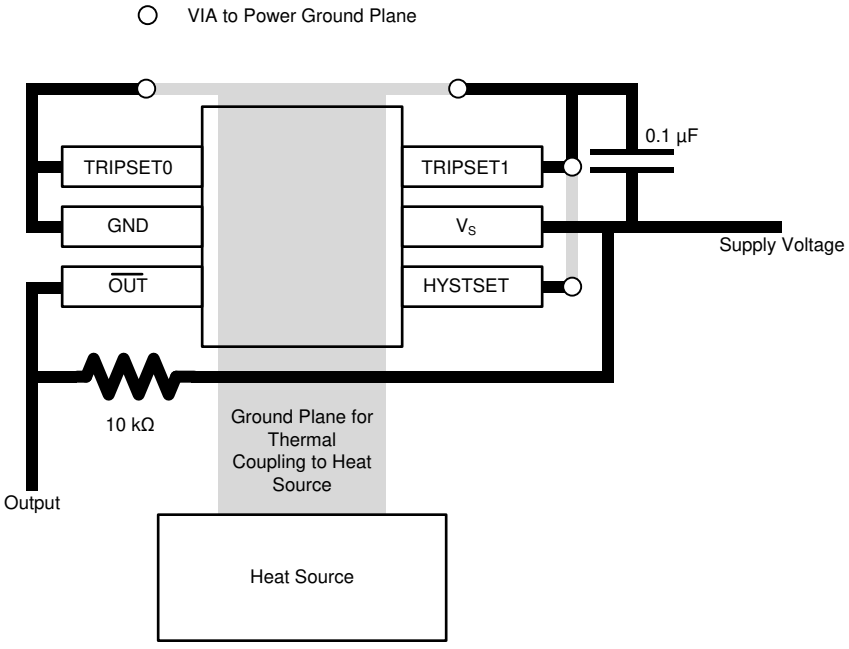


Figure 14. Layout Example

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP302AQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHQ	Samples
TMP302BQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHR	Samples
TMP302CQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHS	Samples
TMP302DQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SHT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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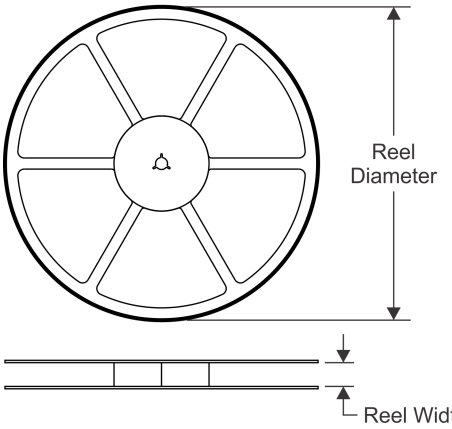
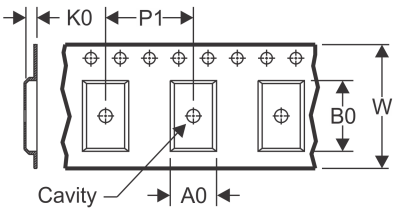
TAPE AND REEL INFORMATION

REEL DIMENSIONS

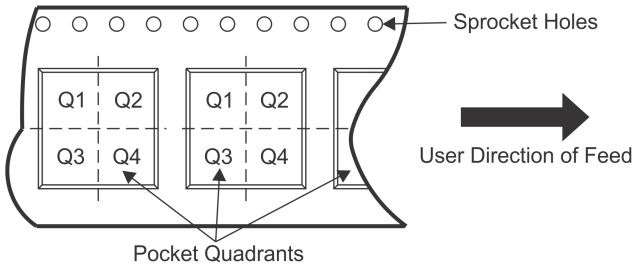


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

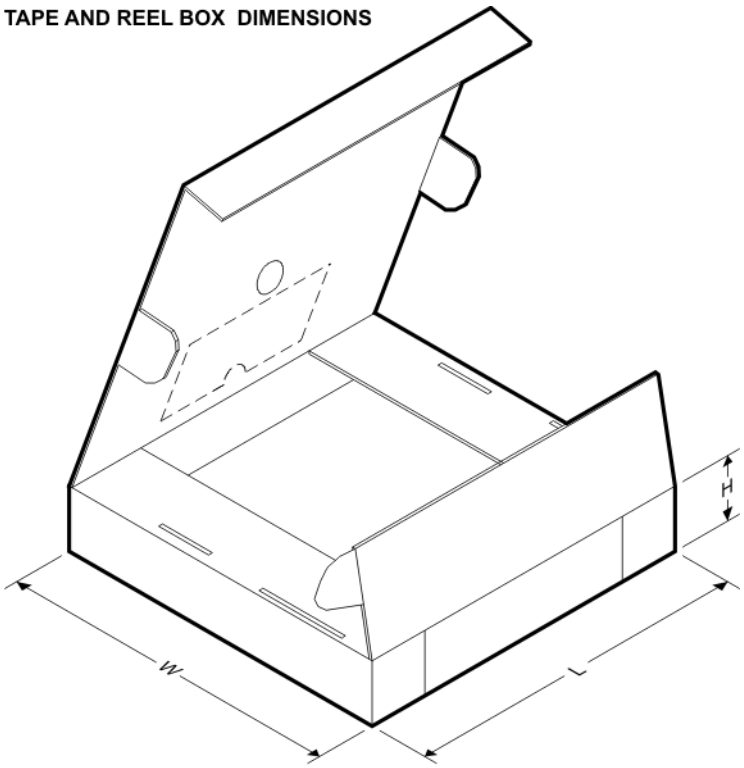
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

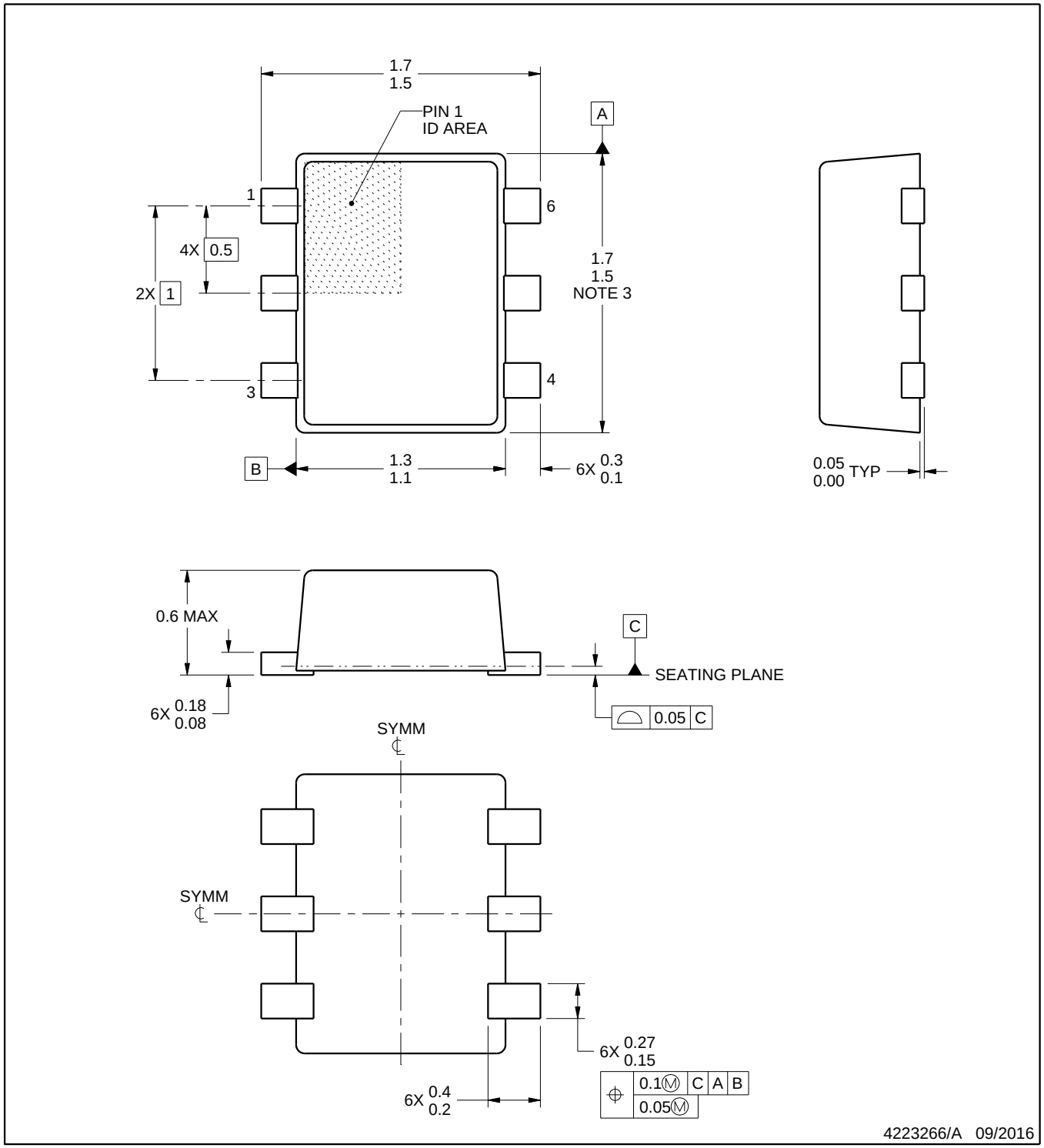
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP302AQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302CQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302DQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP302AQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0
TMP302BQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0
TMP302CQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0
TMP302DQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0



NOTES:

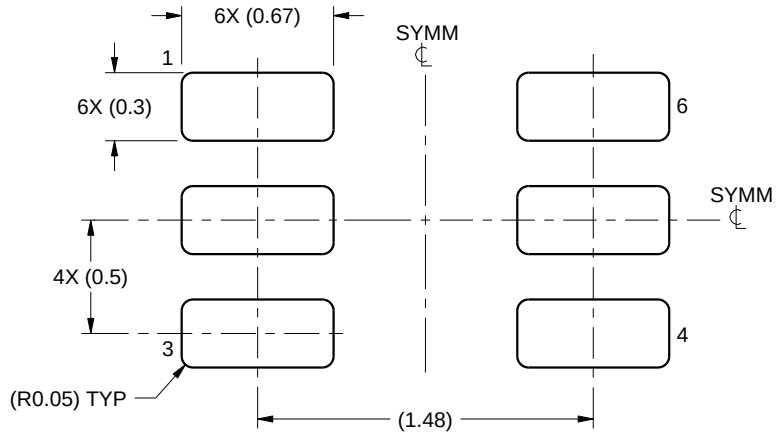
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

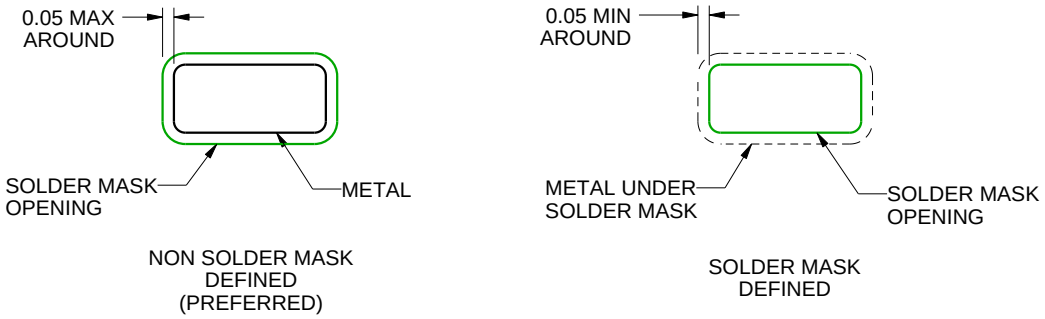
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

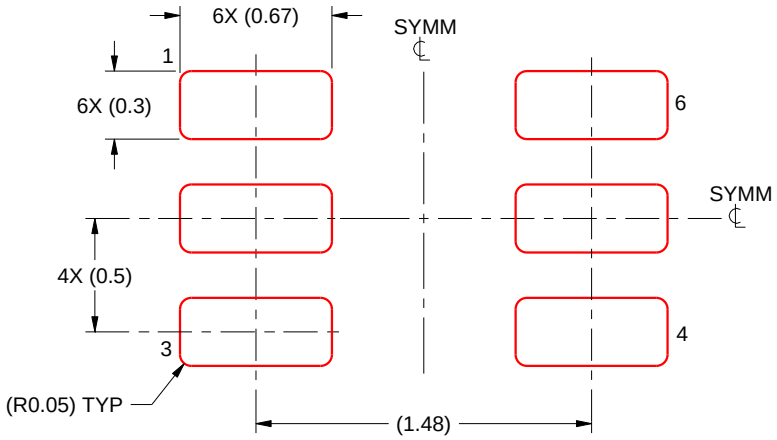
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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