# SN74LVC1GU04 Single Inverter Gate

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V $V_{CC}$ Operation
- Inputs Accept Voltages to 5.5 V
- Unbuffered Output
- Maximum $t_{pd}$ of 3.7 ns at 3.3 V
- Low Power Consumption, 10-μA Maximum $I_{CC}$
- ±24-mA Output Drive at 3.3 V
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid-State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable
- DLP Front Projection Systems
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Cameras

## 3 Description

This single inverter gate is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The SN74LVC1GU04 device contains one inverter with an unbuffered output and performs the Boolean function $Y = \overline{A}$.

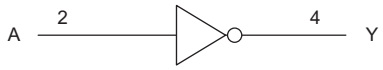
NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC1GU04DBV | SOT-23 (5) | 2.90 mm × 1.60 mm |
| SN74LVC1GU04DCK | SC70 (5) | 2.00 mm × 1.25 mm |
| SN74LVC1GU04DRL | SOT (5) | 1.60 mm × 1.20 mm |
| SN74LVC1GU04DRY | SON (6) | 1.45 mm × 1.00 mm |
| SN74LVC1GU04DSF | SON (6) | 1.00 mm × 1.00 mm |
| SN74LVC1GU04YZP | DSBGA (5) | 1.44 mm × 0.94 mm |
| SN74LVC1GU04YZV | DSBGA (4) | 0.91 mm × 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Logic Diagram (Positive Logic)**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision V (November 2013) to Revision W** — **Page**

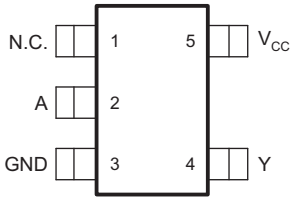
- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

**Changes from Revision U (June 2011) to Revision V** — **Page**

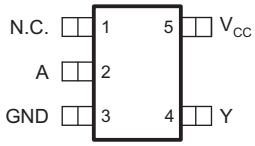
- Updated document to new TI data sheet format. ... 1
- Updated operating temperature range. ... 5

# 5 Pin Configuration and Functions

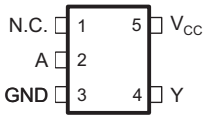
**DBV Package**
**5-Pin SOT-23**
**Top View**



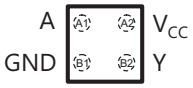

**DCK Package**
**5-Pin SC70**
**Top View**




**DRL Package**
**5-Pin SOT**
**Top View**




**YZV Package**
**4-Pin DSBGA**
**Top View**

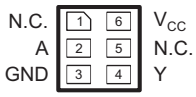



**Pin Functions – 4 and 5 Pins (1)(2)**

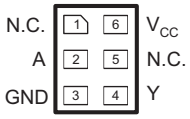
| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SOT-23, SOT, SC70 | DSBGA | | |
| A | 2 | A1 | I | Input |
| GND | 3 | B1 | — | Ground |
| NC | 1 | – | — | Not connected |
| $V_{CC}$ | 5 | A2 | — | Power pin |
| Y | 4 | B2 | O | Output |

(1) N.C. – No internal connection
(2) See *Mechanical, Packaging, and Orderable Information* for dimensions

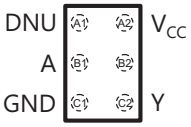
**DSF Package**
**6-Pin SON**
**Top View**




**DRY Package**
**6-Pin SON**
**Top View**




**YZP Package**
**6-Pin DSBGA**
**Top View**




DNU – Do not use

**Pin Functions – 6 Pins** (1) (2)

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | SON | DSBGA | | |
| A | 2 | B1 | I | Input |
| GND | 3 | C1 | — | Ground |
| NC | 1, 5 | A1, B2 | — | Not connected |
| $V_{CC}$ | 6 | A2 | — | Power pin |
| Y | 4 | C2 | O | Output |

(1) N.C. – No internal connection
(2) See *Mechanical, Packaging, and Orderable Information* for dimensions

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage(2) | | 0.5 | 6.5 | V |
| $V_O$ | Voltage applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_J$ | Maximum junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in *Recommended Operating Conditions* .

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 | ±1000 | |

## 6.3 Recommended Operating Conditions

See (1).

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $I_O$ = –100 µA | 0.75 × $V_{CC}$ | | V |
| $V_{IL}$ | Low-level input voltage | $I_O$ = 100 µA | | 0.25 × $V_{CC}$ | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | |
| | | $V_{CC}$ = 3 V | | –16 | |
| | | | | –24 | |
| | | $V_{CC}$ = 4.5 V | | –32 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC1GU04 | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRL (SOT) | DRY (SON) | YZP (DSBGA) | DSF (SON) | YZV (DSBGA) | |
| | | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 6 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 206 | 252 | 142 | 234 | 132 | 300 | 116 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | $T_A$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{IL}$ = 0 V | $I_{OH}$ = –100 µA | 1.65 V to 5.5 V | | $V_{CC}$ – 0.1 | | | V |
| | | | $I_{OH}$ = –4 mA | 1.65 V | | 1.2 | | | |
| | | | $I_{OH}$ = –8 mA | 2.3 V | | 1.9 | | | |
| | | | $I_{OH}$ = –16 mA | 3 V | | 2.4 | | | |
| | | | $I_{OH}$ = –24 mA | | | 2.3 | | | |
| | | | $I_{OH}$ = –32 mA | 4.5 V | | 3.8 | | | |
| $V_{OL}$ | | $V_{IH}$ = $V_{CC}$ | $I_{OL}$ = 100 µA | 1.65 V to 5.5 V | | | | 0.1 | V |
| | | | $I_{OL}$ = 4 mA | 1.65 V | | | | 0.45 | |
| | | | $I_{OL}$ = 8 mA | 2.3 V | | | | 0.3 | |
| | | | $I_{OL}$ = 16 mA | 3 V | | | | 0.4 | |
| | | | $I_{OL}$ = 24 mA | | | | | 0.55 | |
| | | | $I_{OL}$ = 32 mA | 4.5 V | | | | 0.55 | |
| $I_I$ | A input | $V_I$ = 5.5 V or GND | | 0 V to 5.5 V | | | | ±5 | µA |
| $I_{CC}$ | | $V_I$ = 5.5 V or GND, | $I_O$ = 0 | 1.65 V to 5.5 V | | | | 10 | µA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | 3.3 V | $T_A$ = –40°C to 85°C | | 7 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

## 6.6 Switching Characteristics, $T_A$ = –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 2)

| PARAMETER | FROM (INPUT) | TO (INPUT) | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | $V_{CC}$ = 1.8 V ± 0.15 V | 1.3 | 5 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 4 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.1 | 3.7 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3 | |

## 6.7 Switching Characteristics, $T_A$ = –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 2)

| PARAMETER | FROM (INPUT) | TO (INPUT) | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$ | A | Y | $V_{CC}$ = 1.8 V ± 0.15 V | 1.3 | 5.5 | ns |
| | | | $V_{CC}$ = 2.5 V ± 0.2 V | 1 | 4.5 | |
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | 1.1 | 4.2 | |
| | | | $V_{CC}$ = 5 V ± 0.5 V | 1 | 3.5 | |

## 6.8 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | $V_{CC}$ = 1.8 V | 9 | pF |
| | | | $V_{CC}$ = 2.5 V | 11 | |
| | | | $V_{CC}$ = 3.3 V | 13 | |
| | | | $V_{CC}$ = 5 V | 27 | |

## 6.9 Typical Characteristic

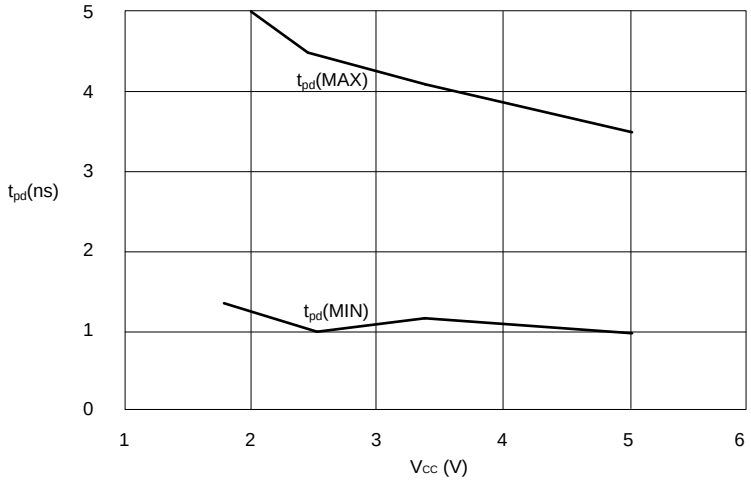
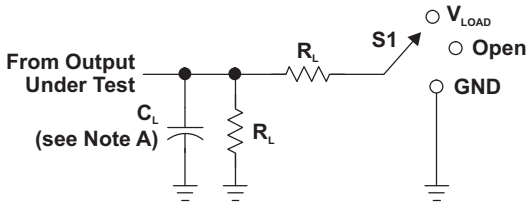



**Figure 1. $t_{pd}$ vs $V_{CC}$**

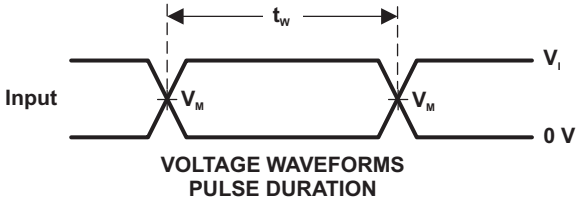
# 7 Parameter Measurement Information



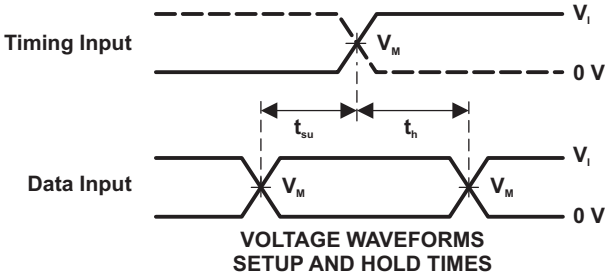

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

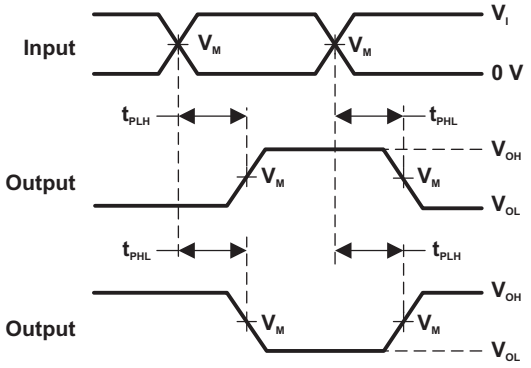
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤2.5 ns | $V_{CC}/2$ | 2 × $V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



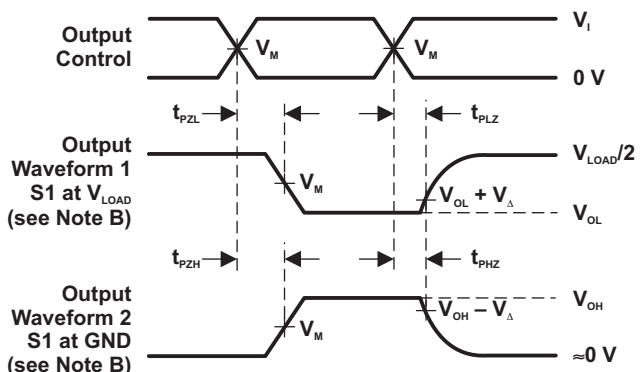

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SN74LVC1GU04 device contains one inverter with an unbuffered output with a maximum sink current of 32 mA.

## 8.2 Functional Block Diagram

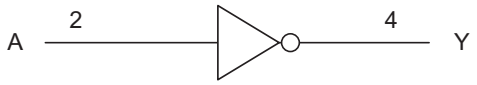



**Figure 3. Logic Diagram (Positive Logic)**

## 8.3 Feature Description

The wide operating voltage range of 1.65 V to 5.5 V allows the SN74LVC1GU04 to be used in systems with many different voltage rails. In addition, the voltage tolerance on the output allows the device to be used for inverting up-translation or down-translation.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1GU04.

**Table 1. Function Table**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The SN74LVC1GU04 is a high-drive CMOS device that can be used to implement a high-output drive buffer, such as an LED application. It can sink 32 mA of current at 4.5 V, making it ideal for high-drive applications. It is good for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant, allowing it to translate up or down to $V_{CC}$. Figure 4 shows a simple LED driver application for a single channel of the device.

## 9.2 Typical Application

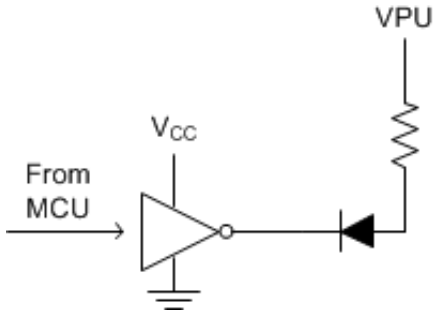



**Figure 4. Typical Application Diagram**

### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specifications. See (Δt/ΔV) in *Recommended Operating Conditions*.
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as ($V_I$ max) in *Recommended Operating Conditions* at any valid $V_{CC}$.
2. Absolute Maximum Output Conditions
   - Load currents must not exceed ($I_O$ max) per output and must not exceed (Continuous current through $V_{CC}$ or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
   - Outputs must not be pulled above 5.5 V.

## Typical Application (continued)

### 9.2.3 Application Curve

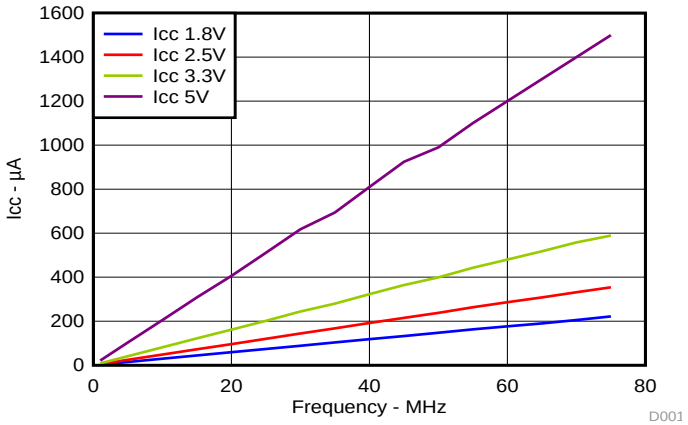



**Figure 5. $I_{CC}$ vs Frequency**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended, and if there are multiple $V_{CC}$ pins, then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Observe the following rules under all circumstances:

1. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
2. The logic level that should be applied to any particular unused input depends on the function of the device.
3. Generally they will be tied to GND or $V_{CC}$ whichever make more sense or is more convenient.

### 11.2 Layout Example

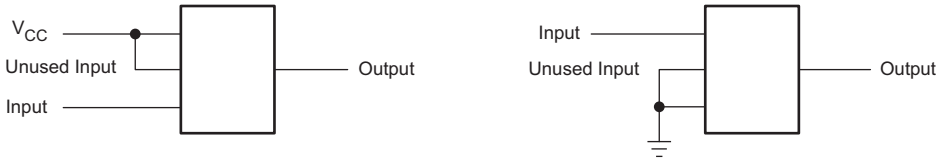



**Figure 6. Layout Diagram**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, SCBA004

## 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74LVC1GU04DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CU4F | Samples |
| 74LVC1GU04DBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CU4F | Samples |
| 74LVC1GU04DBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CU4F | Samples |
| 74LVC1GU04DCKRE4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CD5 ~ CDF ~ CDK ~ CDR ~ CDT) (CDH ~ CDP ~ CDS) | Samples |
| 74LVC1GU04DCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CD5 ~ CDF ~ CDK ~ CDR ~ CDT) (CDH ~ CDP ~ CDS) | Samples |
| 74LVC1GU04DCKTE4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CD5 ~ CDF ~ CDK ~ CDR ~ CDT) (CDH ~ CDP ~ CDS) | Samples |
| 74LVC1GU04DCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CD5 ~ CDF ~ CDK ~ CDR ~ CDT) (CDH ~ CDP ~ CDS) | Samples |
| 74LVC1GU04DRLRG4 | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CDR | Samples |
| SN74LVC1GU04DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (CU45 ~ CU4F ~ CU4R ~ CU4T) (CU4H ~ CU4P ~ CU4S) | Samples |
| SN74LVC1GU04DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | (CU45 ~ CU4F ~ CU4R) (CU4H ~ CU4P ~ CU4S) | Samples |
| SN74LVC1GU04DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CD5 ~ CDF ~ CDK ~ CDR ~ CDT) (CDH ~ CDP ~ CDS) | Samples |
| SN74LVC1GU04DCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (CD5 ~ CDF ~ CDK ~ CDR ~ CDT) (CDH ~ CDP ~ CDS) | Samples |
| SN74LVC1GU04DRLR | ACTIVE | SOT-5X3 | DRL | 5 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CDR | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1GU04DRY2 | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD | Samples |
| SN74LVC1GU04DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CD | Samples |
| SN74LVC1GU04DSFR | ACTIVE | SON | DSF | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CD | Samples |
| SN74LVC1GU04YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CDN | Samples |
| SN74LVC1GU04YZVR | ACTIVE | DSBGA | YZV | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | CD (7 ~ N) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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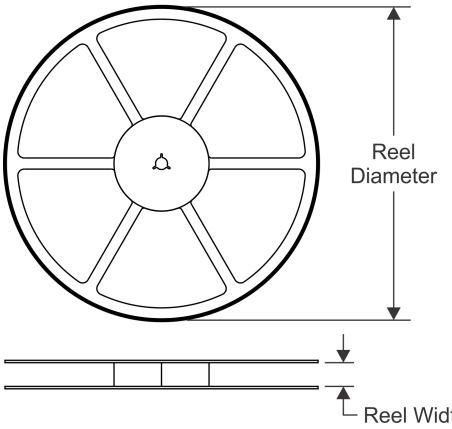
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

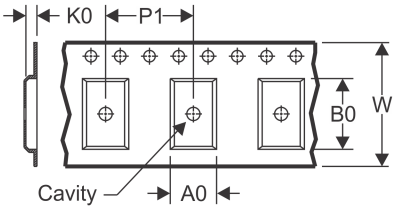
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

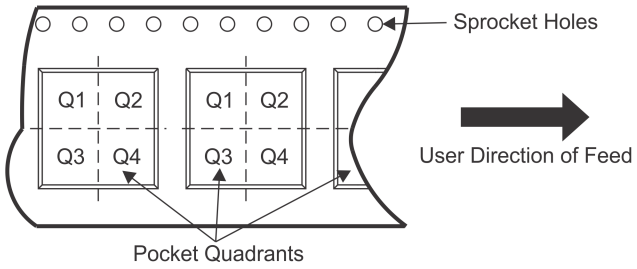



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

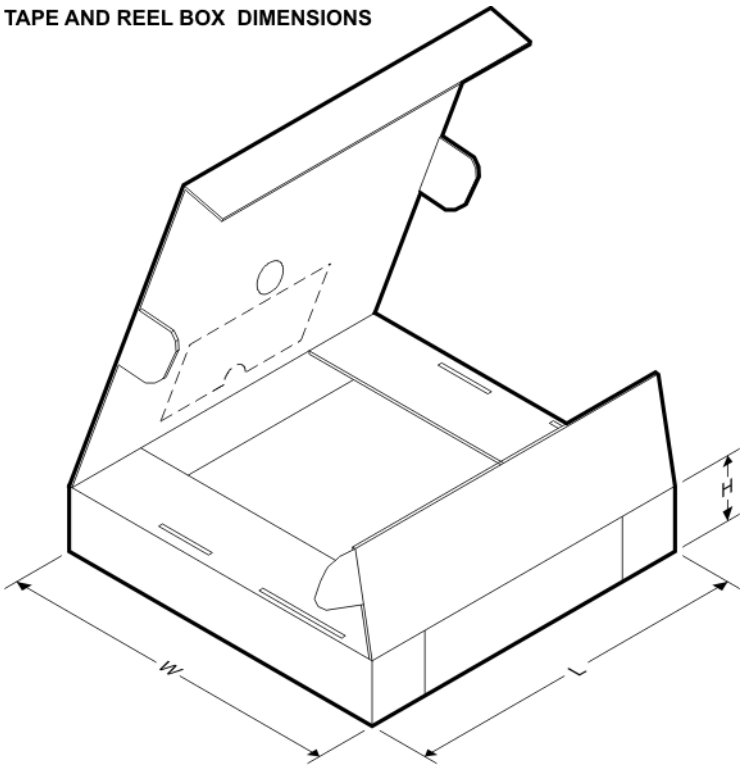



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74LVC1GU04DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| 74LVC1GU04DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 180.0 | 8.4 | 1.65 | 1.2 | 0.7 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.6 | 1.15 | 0.75 | 4.0 | 8.0 | Q3 |
| SN74LVC1GU04DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC1GU04DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1GU04YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |
| SN74LVC1GU04YZVR | DSBGA | YZV | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.63 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

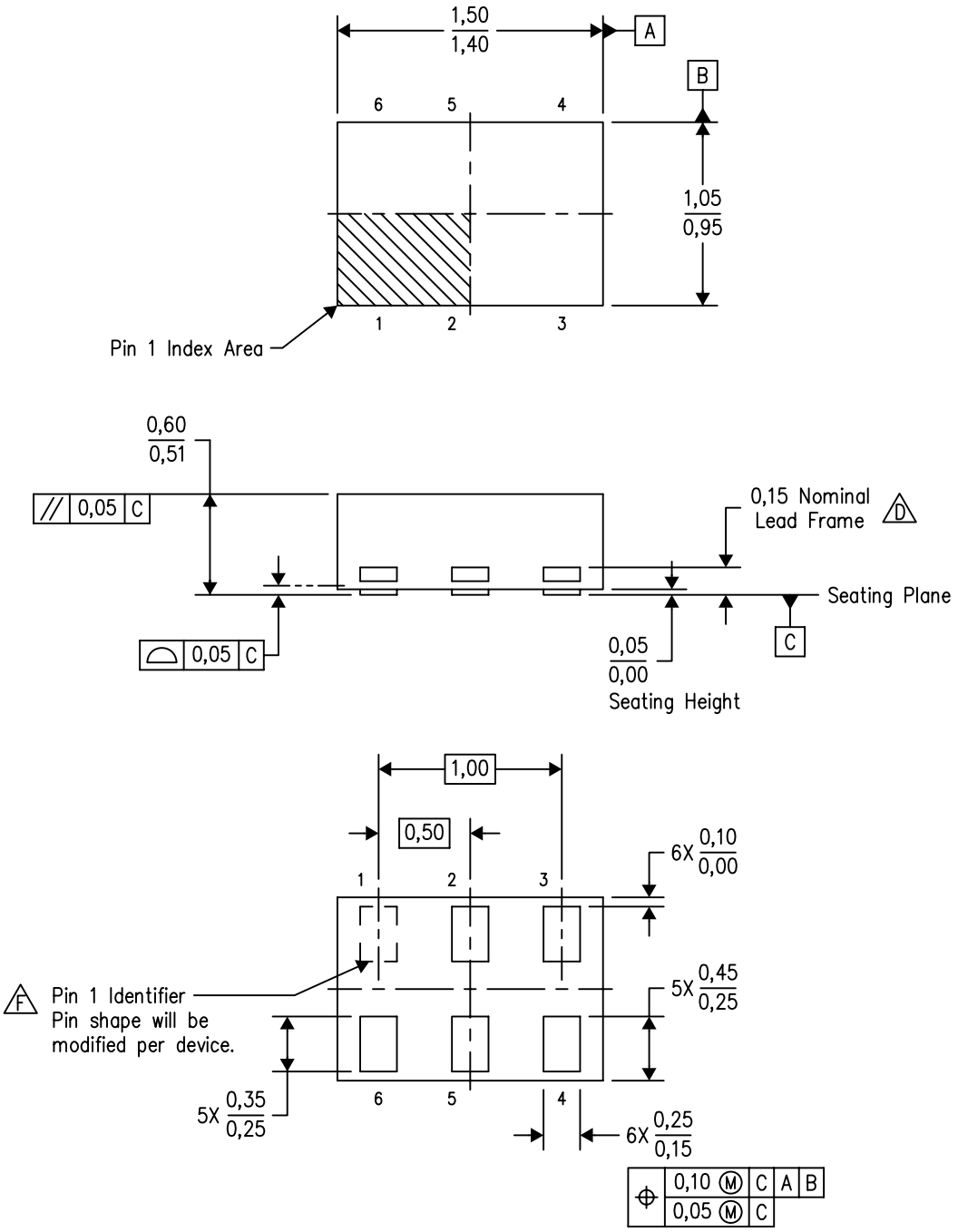



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74LVC1GU04DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| 74LVC1GU04DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DBVT | SOT-23 | DBV | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 205.0 | 200.0 | 33.0 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1GU04DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC1GU04DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1GU04DRY2 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1GU04DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1GU04DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1GU04YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74LVC1GU04YZVR | DSBGA | YZV | 4 | 3000 | 220.0 | 220.0 | 35.0 |

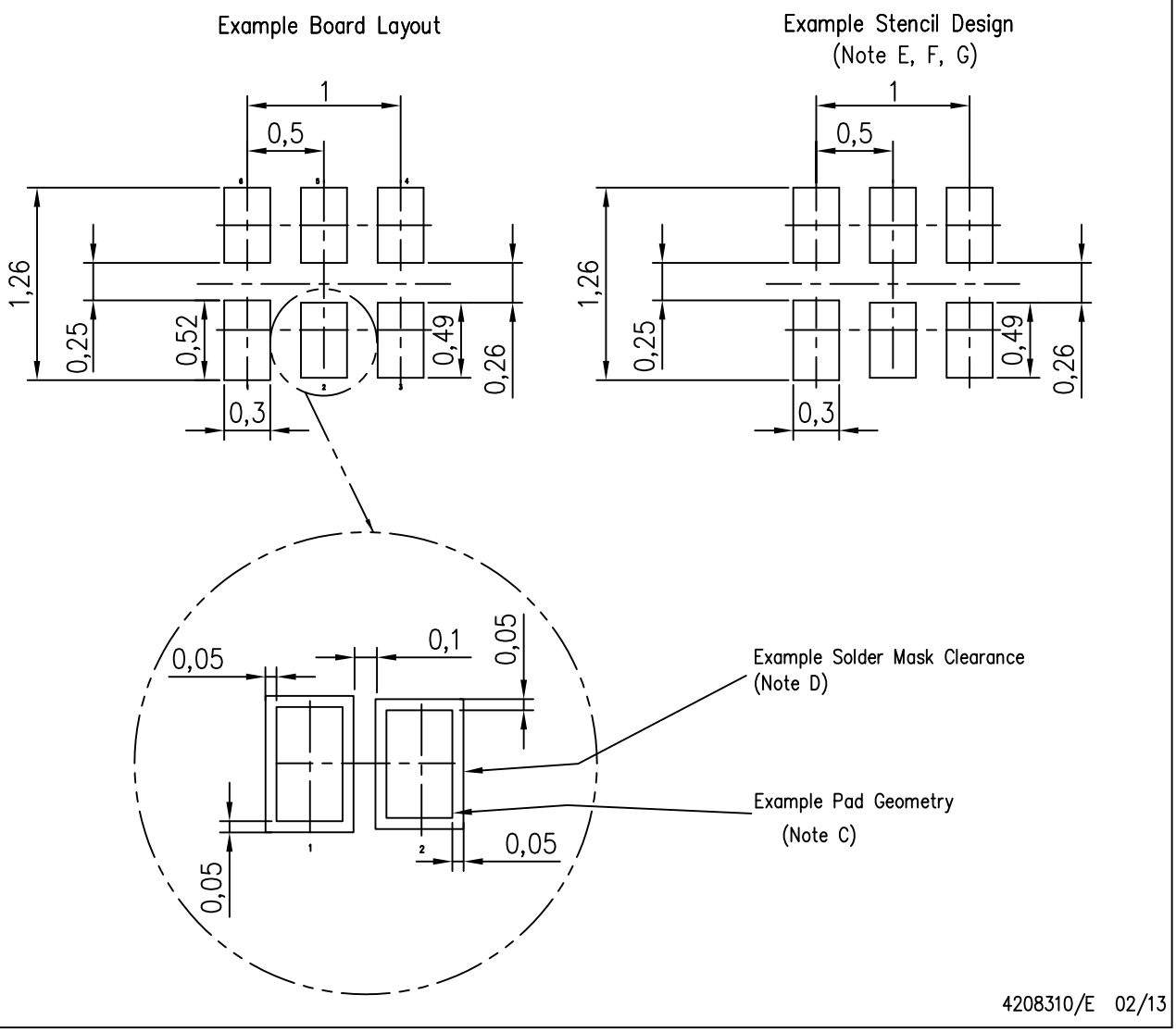
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



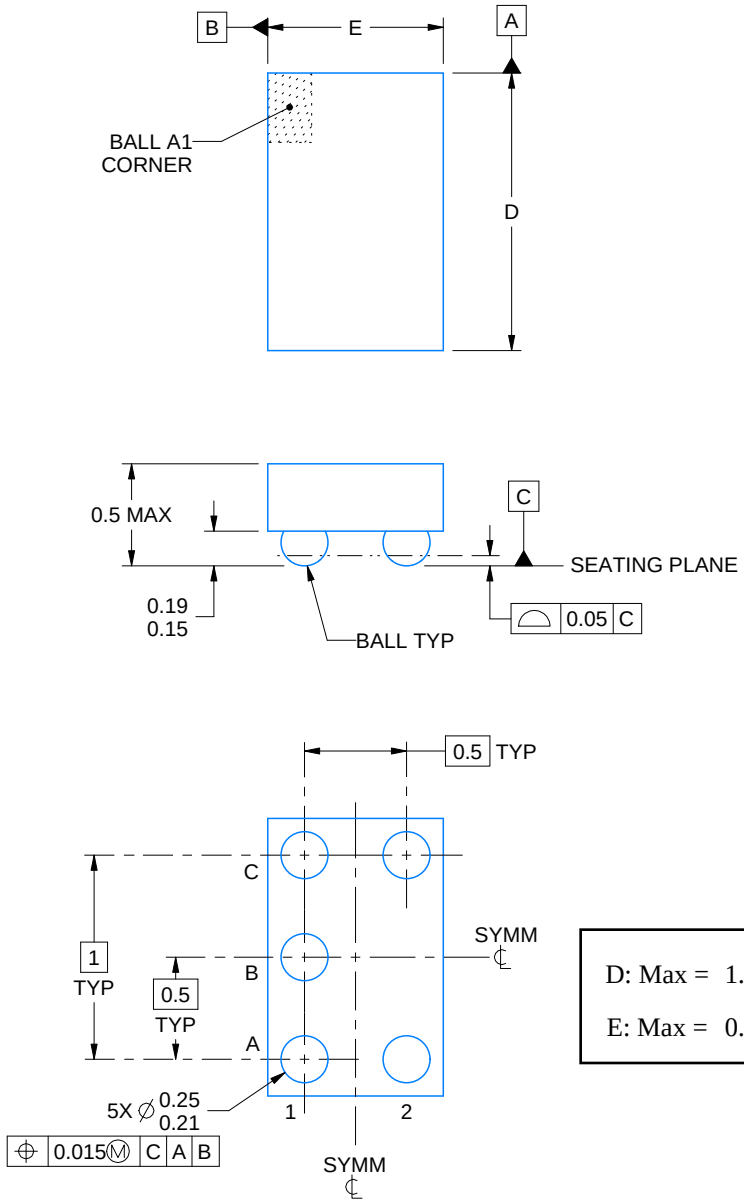

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

# PACKAGE OUTLINE

## YZP0005

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



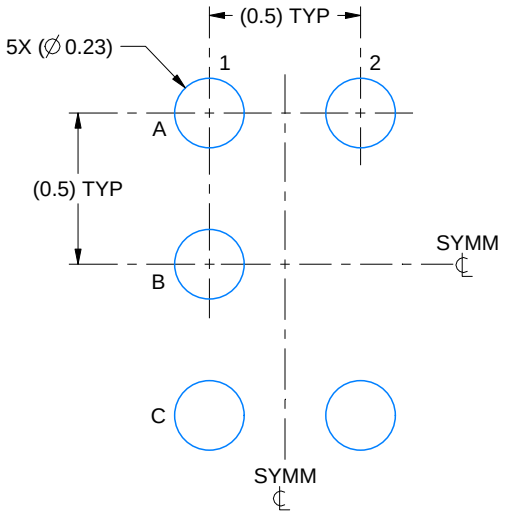

D: Max = 1.44 mm, Min = 1.38 mm

E: Max = 0.94 mm, Min = 0.88 mm

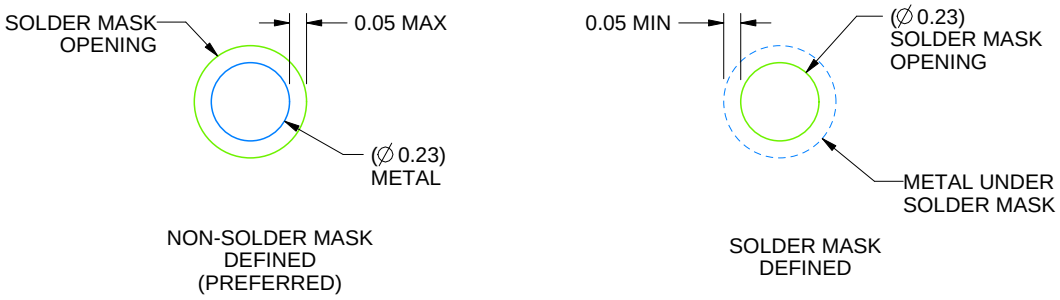
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:40X

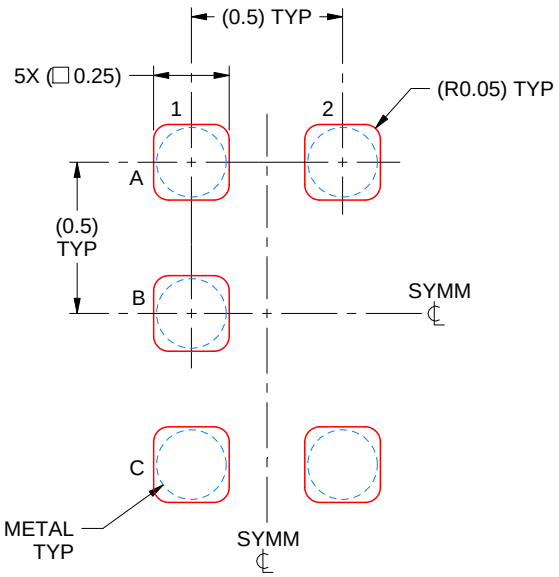



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



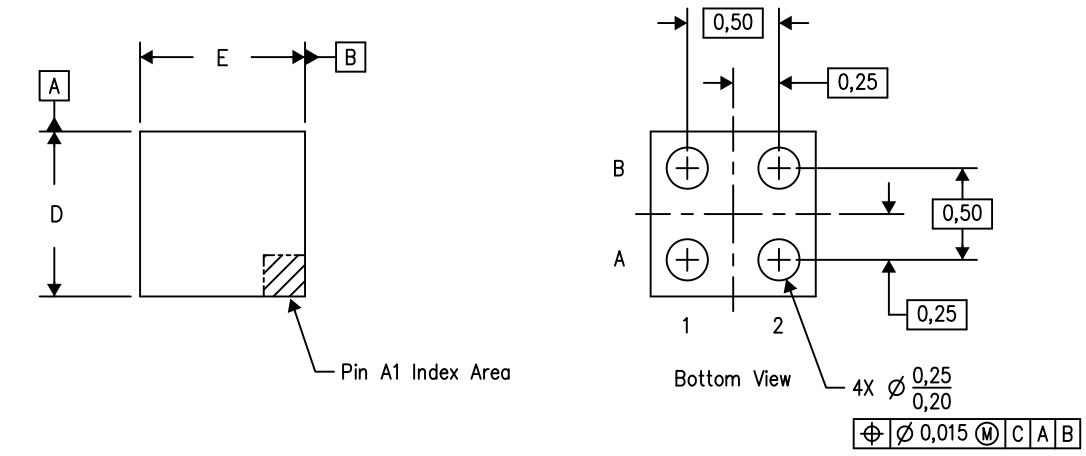

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

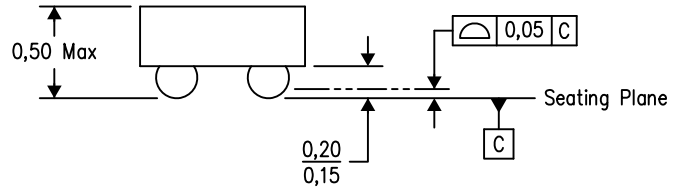
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



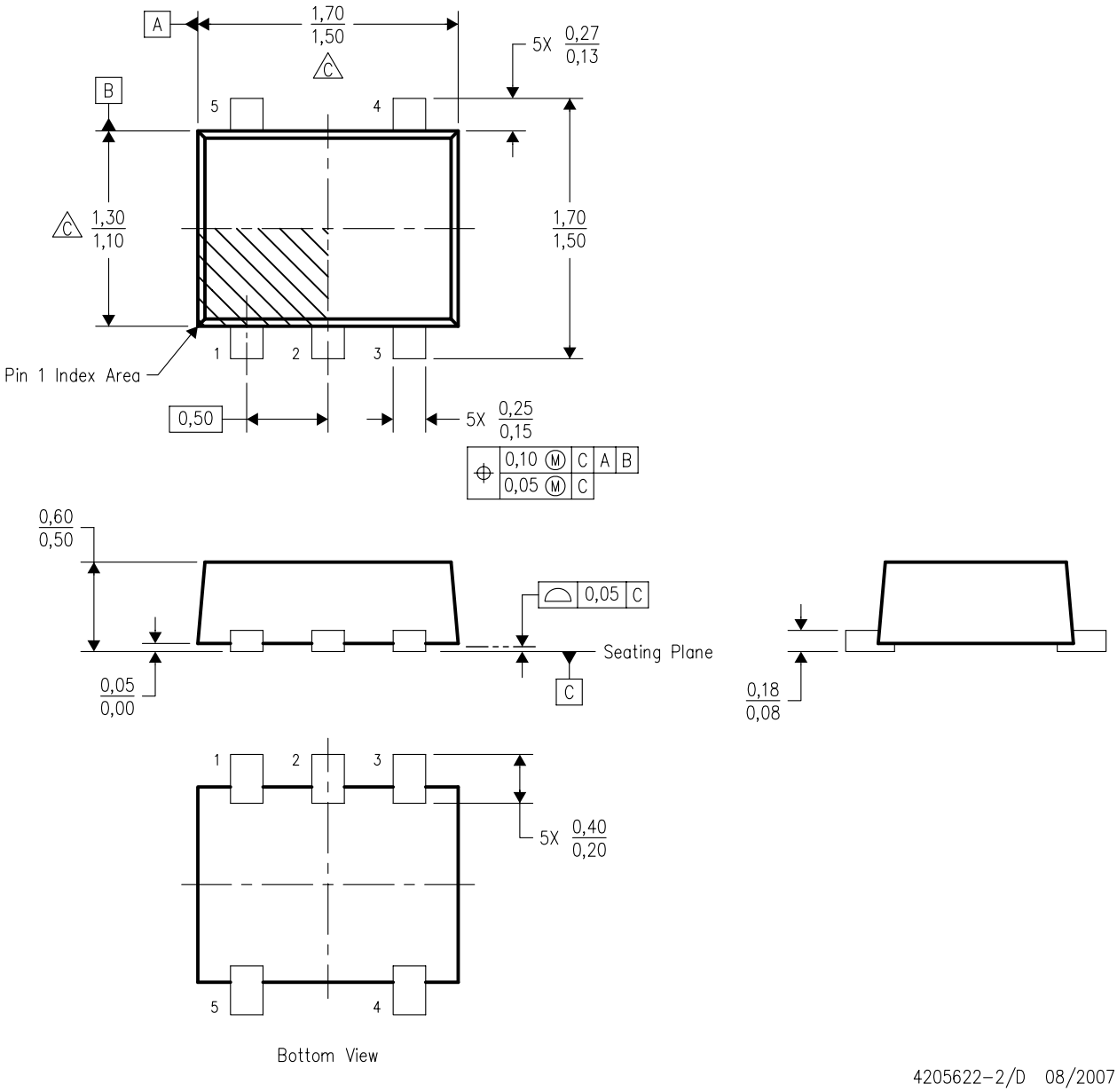

D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

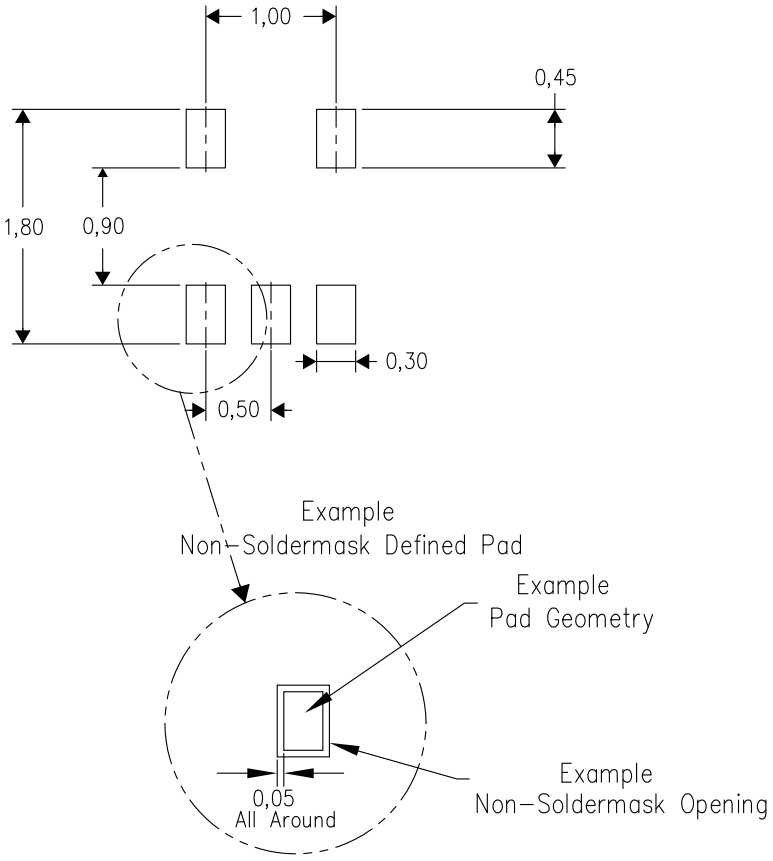
NanoFree is a trademark of Texas Instruments.



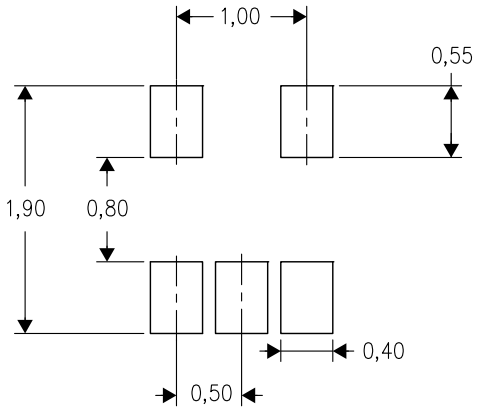

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



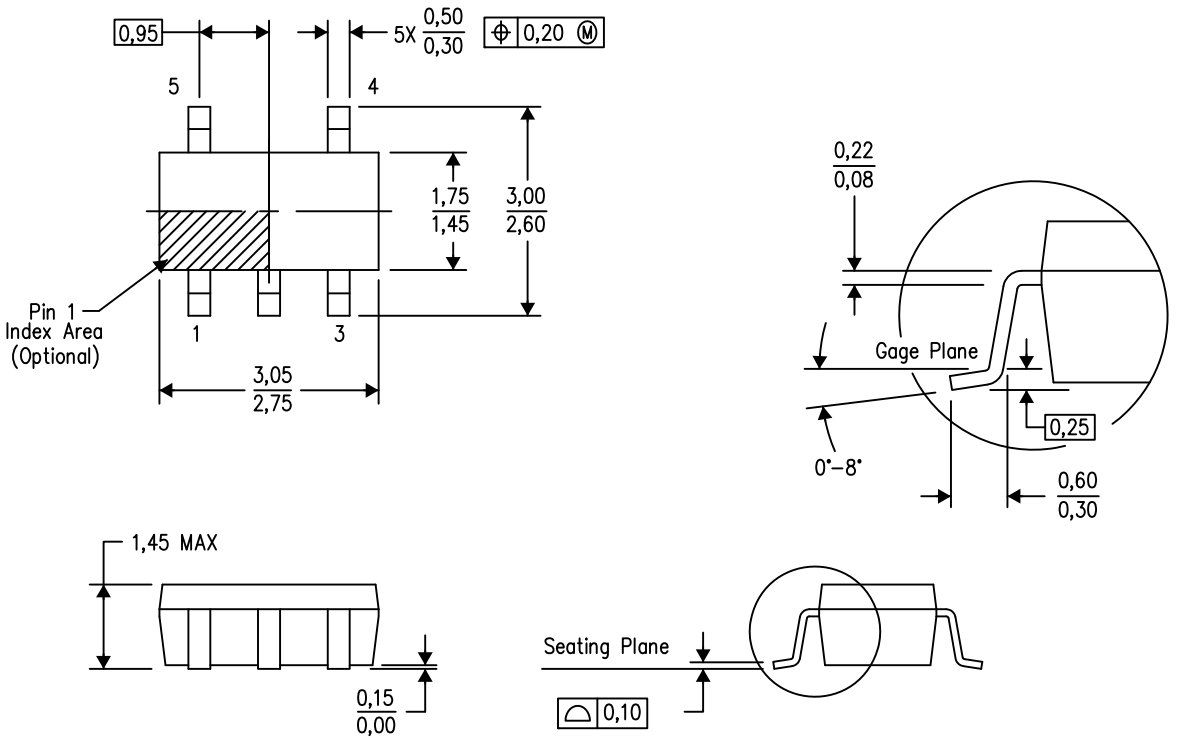

Example Stencil Design
(Note E)




4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

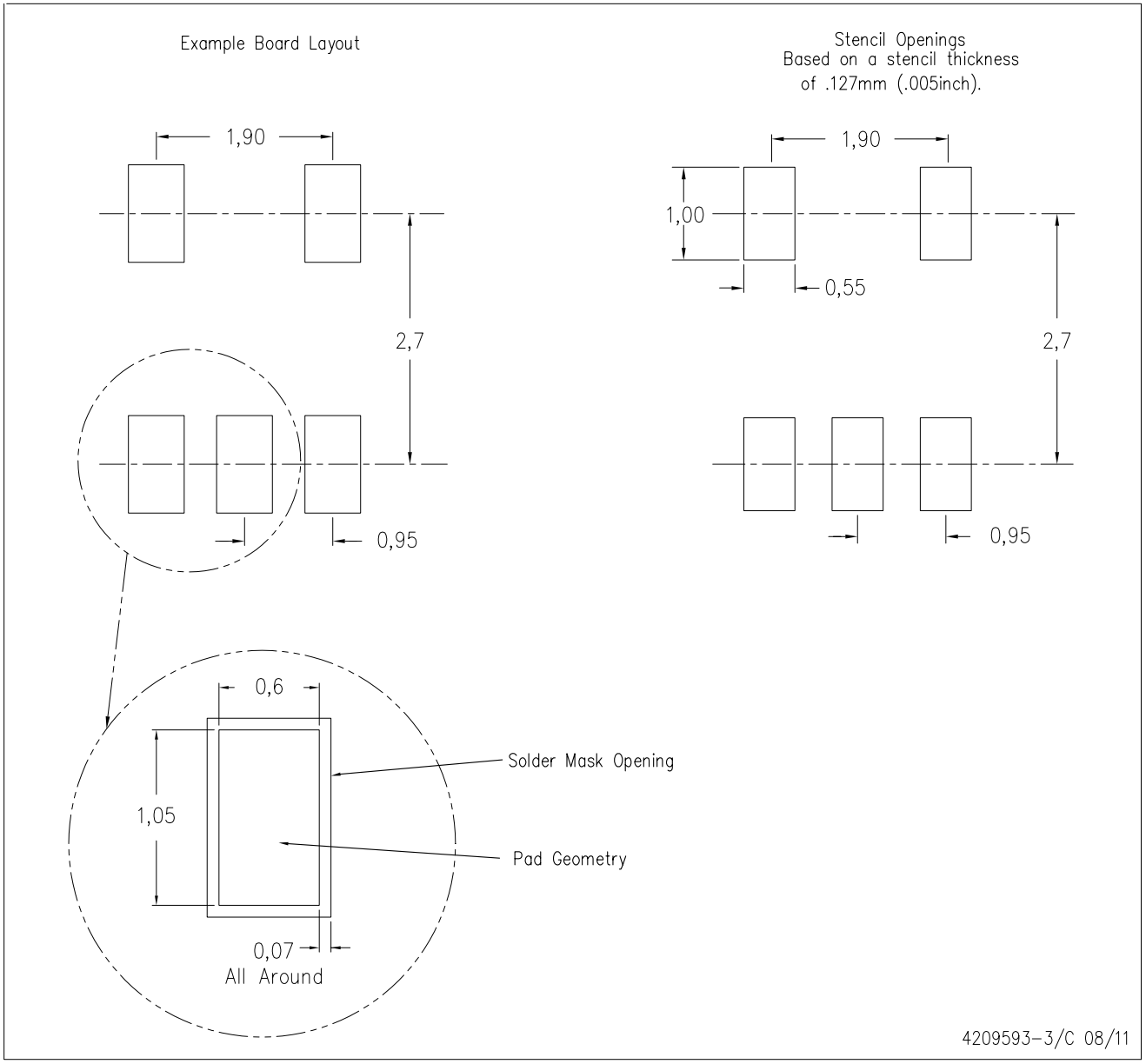
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/N 12/14

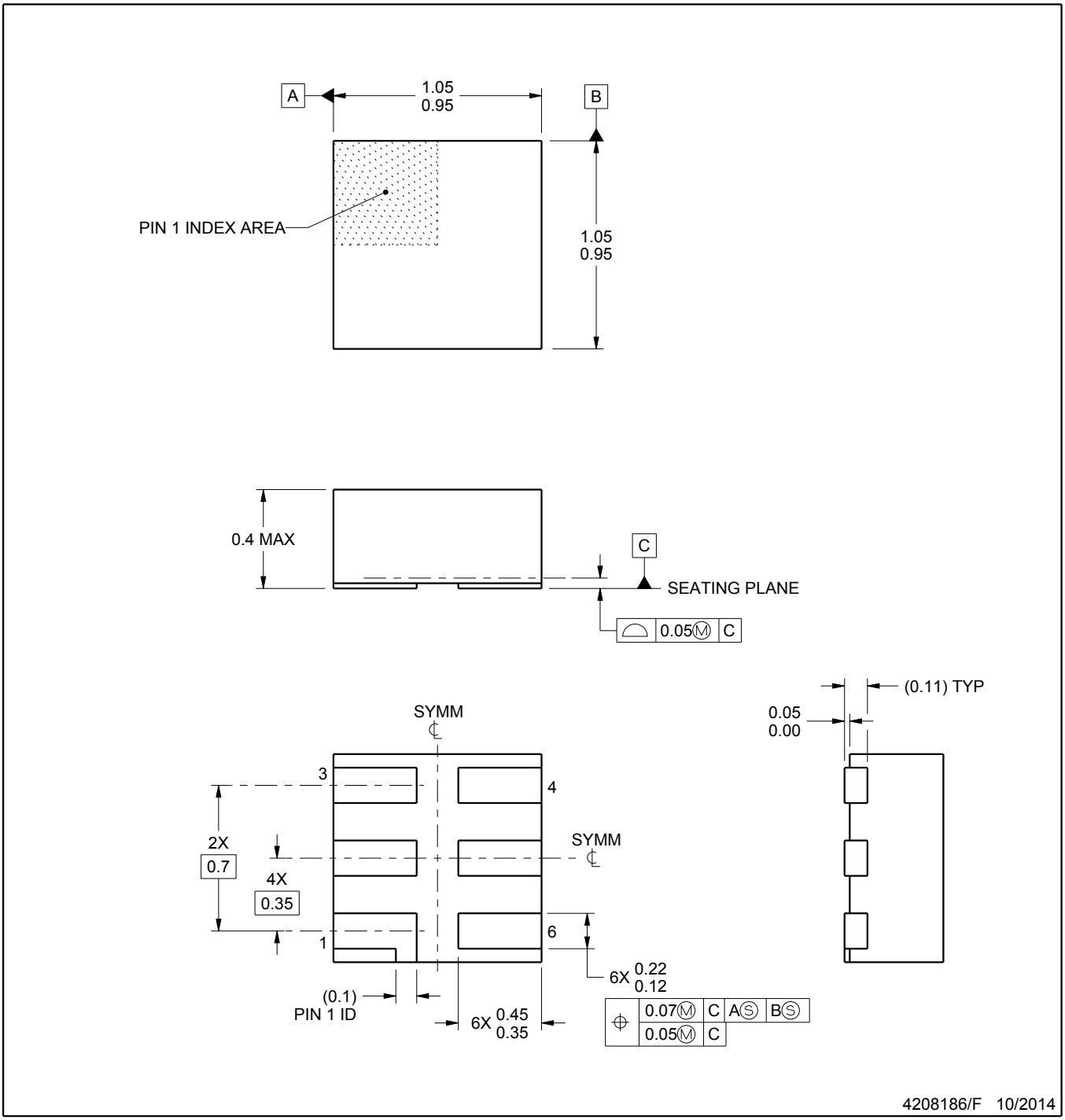
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

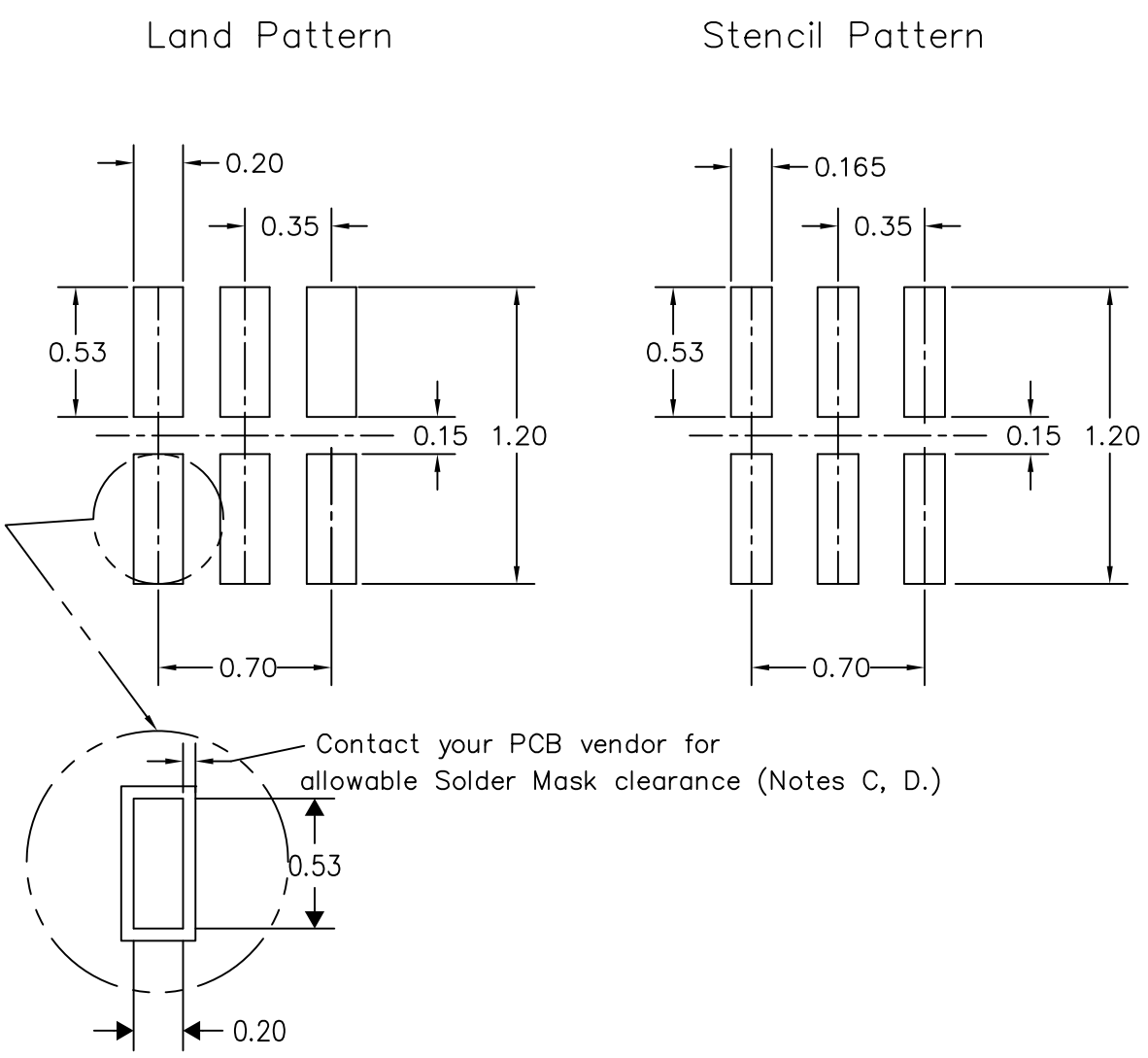
DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

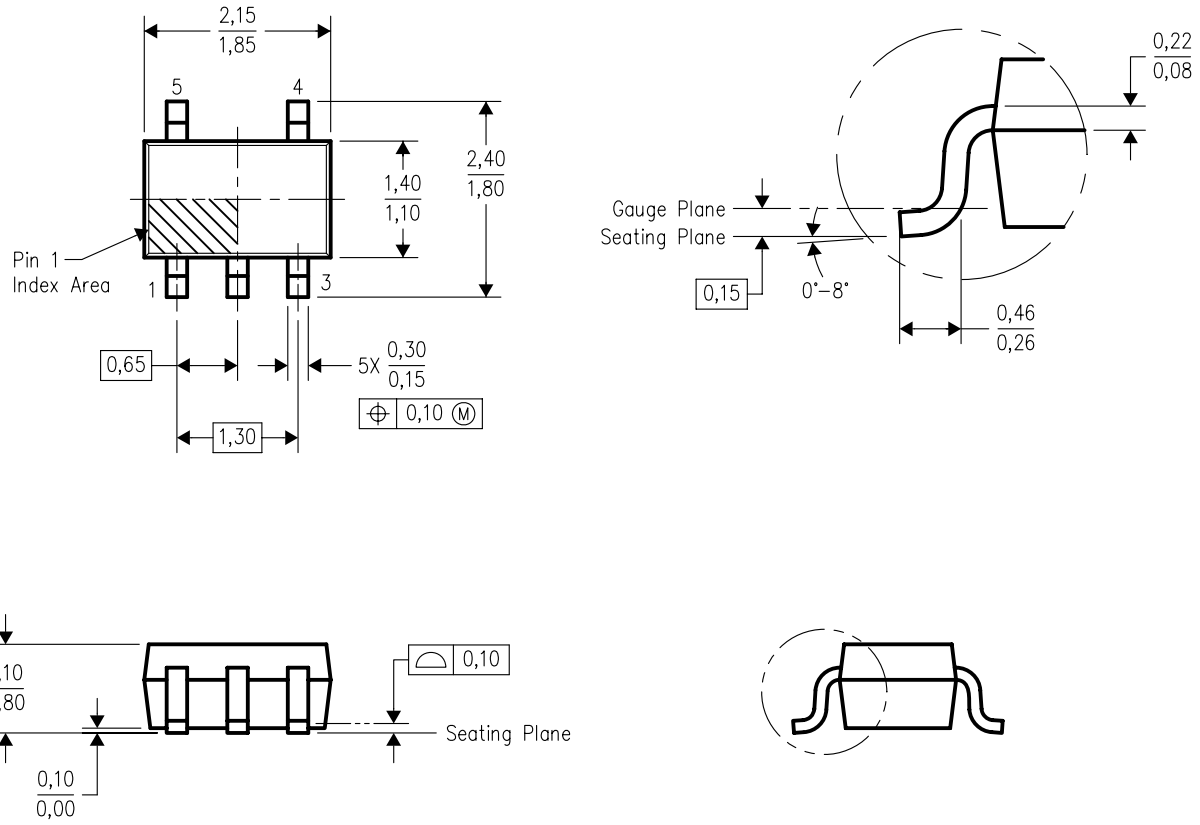
DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4210277/D 05/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
H. Component placement force should be minimized to prevent excessive paste block deformation.

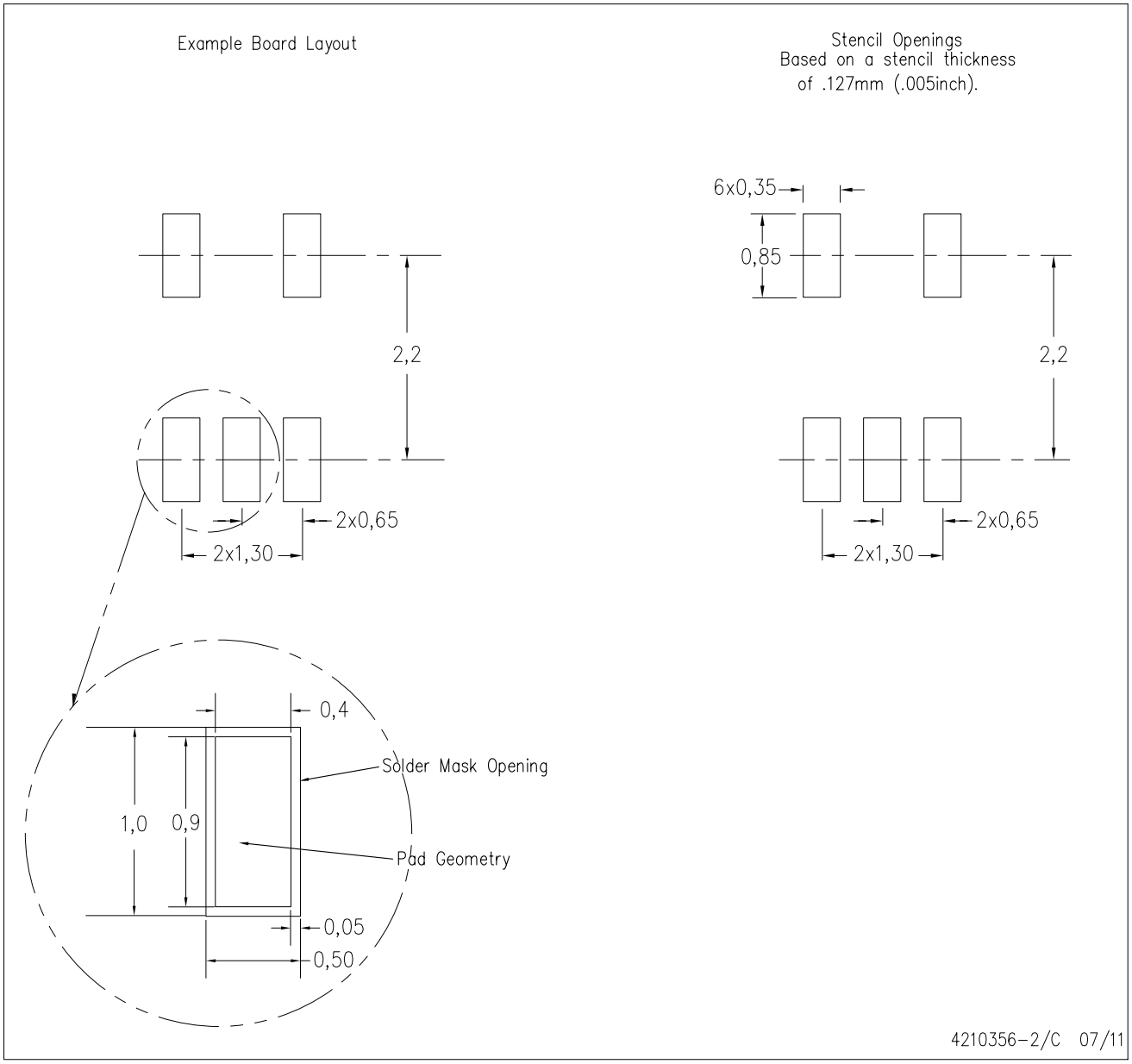
## DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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