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4 Revision History

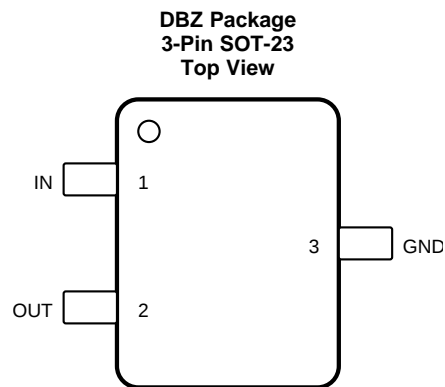
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2017	*	Initial release

5 Device Comparison Table

PRODUCT	VOLTAGE (V)
REF3112-Q1	1.25
REF3120-Q1	2.048
REF3125-Q1	2.5
REF3130-Q1	3
REF3133-Q1	3.3
REF3140-Q1	4.096

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input supply voltage
2	OUT	O	Reference output voltage
3	GND	—	Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V+ to V–		7	V
Output short circuit	Continuous		
Operating temperature	–55	135	°C
Junction temperature		150	°C
Storage temperature, T _{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
			V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input voltage	V _{REF} + 0.05 ⁽¹⁾	5.5	V
I _{LOAD}	Load current		25	mA
T _A	Operating temperature	–40	125	°C

(1) Minimum supply voltage for the REF3112-Q1 is 1.8 V.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF31xx-Q1	UNIT
		DBZ (SOT-23)	
		3 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	292.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	124.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	89	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	11.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	87.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

at T_A = 25°C, I_{LOAD} = 0 mA, and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF3312-Q1 ⁽¹⁾ — 1.25 V						
V _{OUT}	Output voltage		1.2475	1.25	1.2525	V
	Initial accuracy		–0.2%		0.2%	
Output voltage noise		f = 0.1 Hz to 10 Hz		17		μV _{PP}
		f = 10 Hz to 10 kHz		24		μV _{RMS}

(1) Minimum supply voltage for the REF3112 is 1.8 V.

Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $I_{\text{LOAD}} = 0 \text{ mA}$, and $V_{\text{IN}} = 5 \text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF3120-Q1 — 2.048 V						
V_{OUT}	Output voltage		2.0439	2.048	2.0521	V
	Initial accuracy		-0.2%		0.2%	
Output voltage noise		f = 0.1 Hz to 10 Hz		27		μV_{PP}
		f = 10 Hz to 10 kHz		39		μV_{RMS}
REF3125-Q1 — 2.5 V						
V_{OUT}	Output voltage		2.495	2.5	2.505	V
	Initial accuracy		-0.2%		0.2%	
Output voltage noise		f = 0.1 Hz to 10 Hz		33		μV_{PP}
		f = 10 Hz to 10 kHz		48		μV_{RMS}
REF3130-Q1 — 3 V						
V_{OUT}	Output voltage		2.994	3	3.006	V
	Initial accuracy		-0.2%		0.2%	
Output voltage noise		f = 0.1 Hz to 10 Hz		39		μV_{PP}
		f = 10 Hz to 10 kHz		57		μV_{RMS}
REF3133-Q1 — 3.3 V						
V_{OUT}	Output voltage		3.2934	3.3	3.3066	V
	Initial accuracy		-0.2%		0.2%	
Output voltage noise		f = 0.1 Hz to 10 Hz		43		μV_{PP}
		f = 10 Hz to 10 kHz		63		μV_{RMS}
REF3140-Q1 — 4.096 V						
V_{OUT}	Output voltage		4.0878	4.096	4.1042	V
	Initial accuracy		-0.2%		0.2%	
Output voltage noise		f = 0.1 Hz to 10 Hz		53		μV_{PP}
		f = 10 Hz to 10 kHz		78		μV_{RMS}
REF31xx-Q1 (REF3112-Q1, REF3120-Q1, REF3125-Q1, REF3130-Q1, REF3133-Q1, REF3140-Q1)						
dV_{OUT}/dT	Output voltage temperature drift ⁽²⁾	$T_A = 0^\circ\text{C}$ to 70°C .		5	15	ppm/ $^\circ\text{C}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.		10	20	
Long-term stability		0 to 1000 hours		70		ppm
Line regulation		$V_{\text{REF}} + 0.05^{(1)} \leq V_{\text{IN}} \leq 5.5 \text{ V}$		20	65	ppm/V
$dV_{\text{OUT}}/dI_{\text{LOAD}}$	Load regulation ⁽³⁾	Sourcing	0 mA < $I_{\text{LOAD}} < 10 \text{ mA}$, $V_{\text{IN}} = V_{\text{REF}} + 250 \text{ mV}^{(1)}$		10	30
		Sinking	$-10 \text{ mA} < I_{\text{LOAD}} < 0 \text{ mA}$, $V_{\text{IN}} = V_{\text{REF}} + 100 \text{ mV}^{(1)}$		20	50
dT	Thermal hysteresis ⁽⁴⁾	First Cycle		100		ppm
		Additional Cycles		25		
$V_{\text{IN}} - V_{\text{OUT}}$	Dropout voltage ⁽¹⁾	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.		5	50	mV
I_{LOAD}	Output current		-10		10	mA
I_{SC}	Short-circuit current	Sourcing		50		mA
		Sinking		40		
Turnon settling time		To 0.1% at $V_{\text{IN}} = +5 \text{ V}$ with $C_L = 0 \mu\text{F}$		400		μs
POWER SUPPLY						
V_S	Voltage	$I_{\text{LOAD}} = 0$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.	$V_{\text{REF}} + 0.05^{(1)}$		5.5	V
I_Q	Quiescent current	$I_{\text{LOAD}} = 0$, $T_A = 25^\circ\text{C}$			100	115
		$I_{\text{LOAD}} = 0$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			115	135

(2) Box Method used to determine temperature drift.

(3) Typical value of load regulation reflects measurements using force and sense contacts; see [Load Regulation](#).

(4) Thermal hysteresis is explained in more detail in [Application and Implementation](#) of this data sheet.

7.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{-V}$ power supply, and REF3125-Q1 is used for typical characteristic measurements, unless otherwise noted.

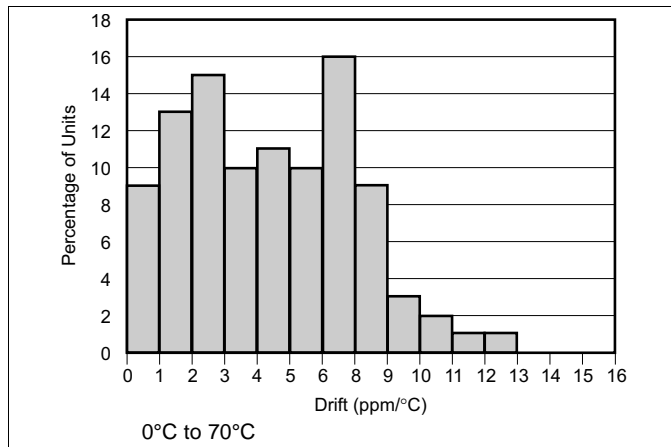


Figure 1. Temperature Drift

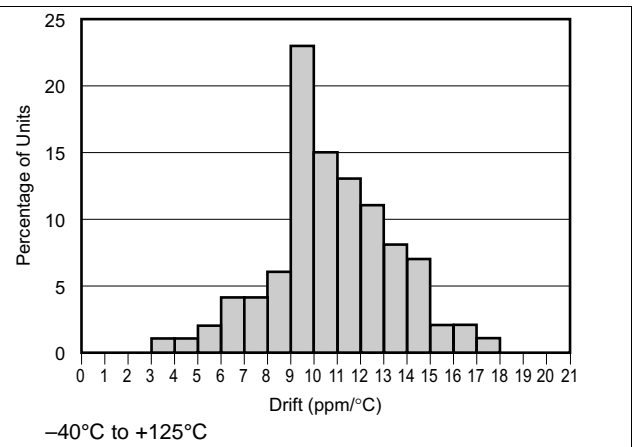


Figure 2. Temperature Drift

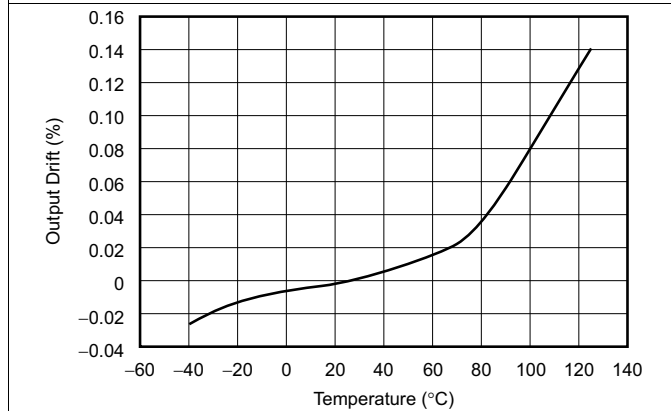


Figure 3. Output Voltage vs Temperature

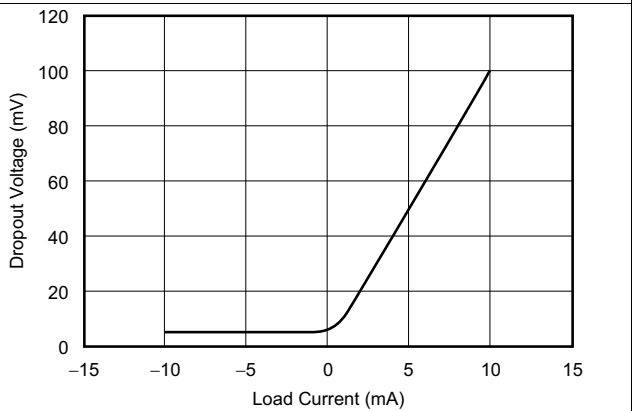


Figure 4. Dropout Voltage vs Load Current

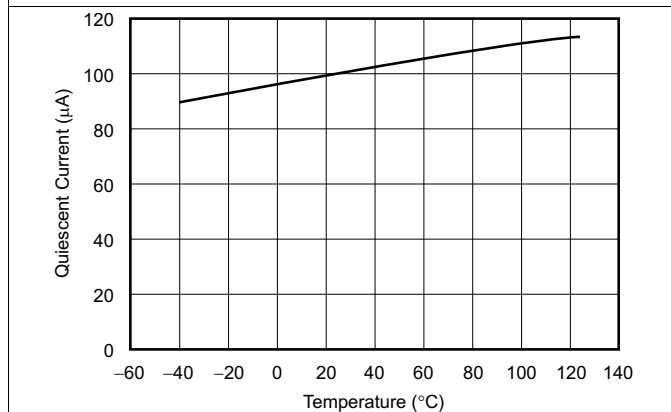


Figure 5. Quiescent Current vs Temperature

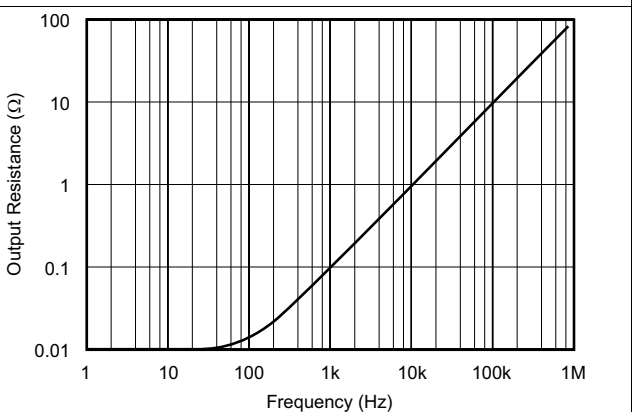


Figure 6. Output Impedance vs Frequency

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{-V}$ power supply, and REF3125-Q1 is used for typical characteristic measurements, unless otherwise noted.

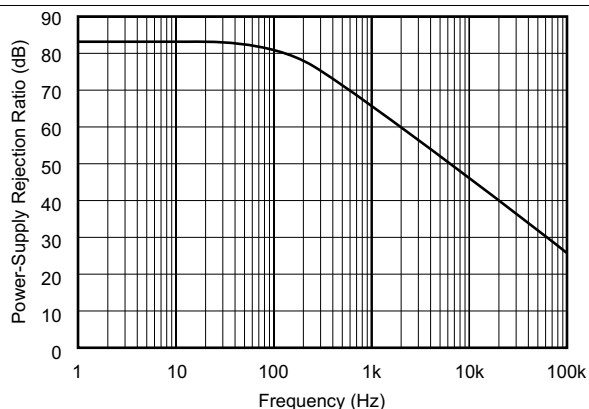


Figure 7. PSRR vs Frequency

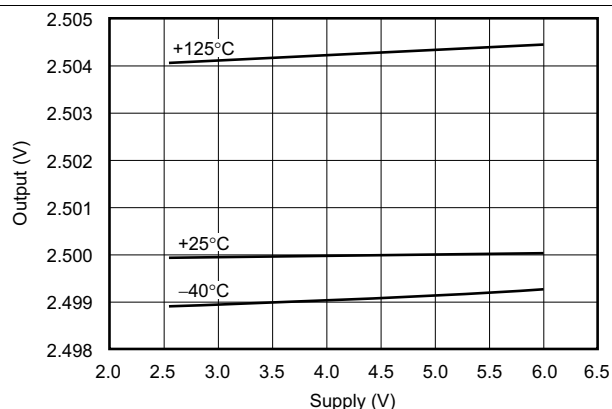


Figure 8. Output vs Supply

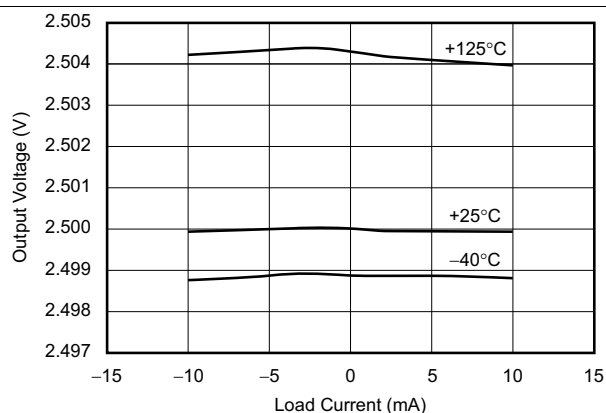


Figure 9. Output Voltage vs Load Current

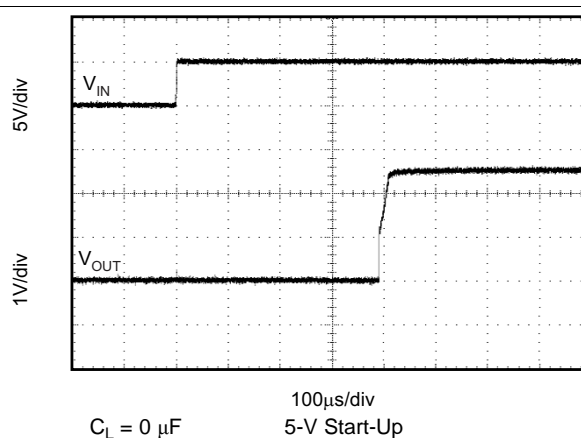


Figure 10. Step Response

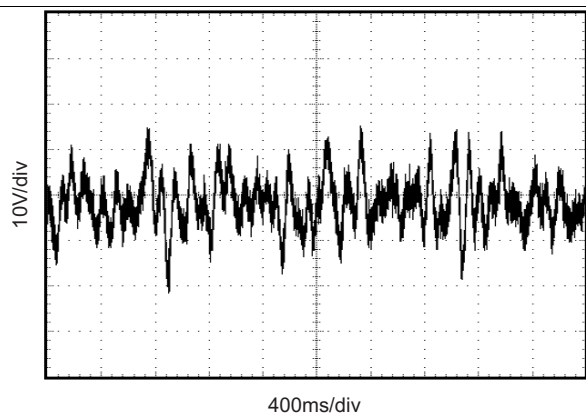


Figure 11. 0.1-Hz to 10-Hz Noise

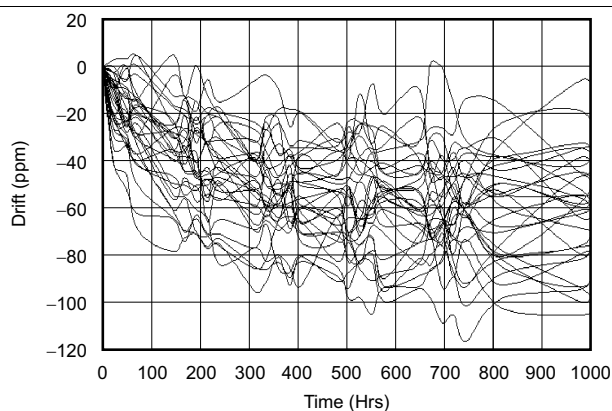


Figure 12. REF3112 Long-Term Stability

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{-V}$ power supply, and REF3125-Q1 is used for typical characteristic measurements, unless otherwise noted.

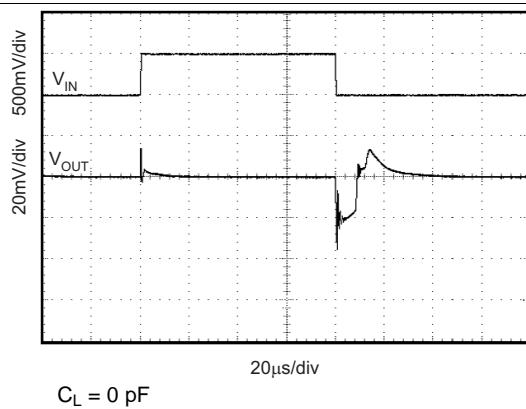


Figure 13. Line Transient

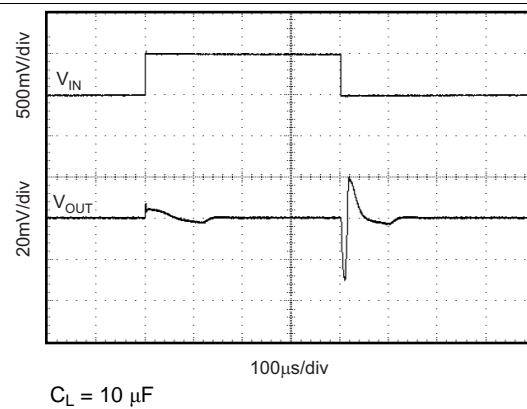


Figure 14. Line Transient

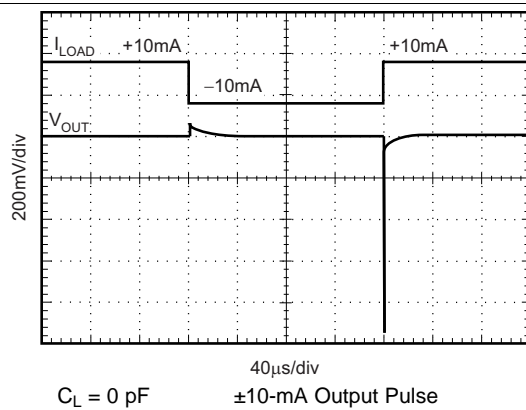


Figure 15. Load Transient

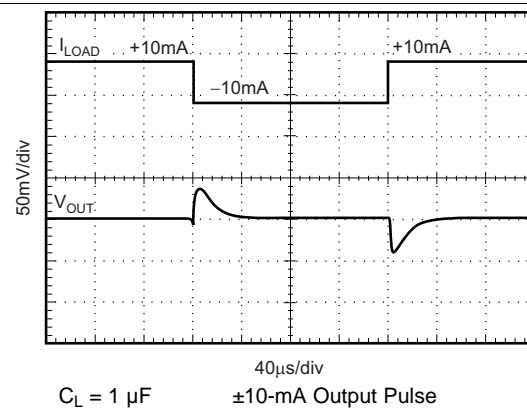


Figure 16. Load Transient

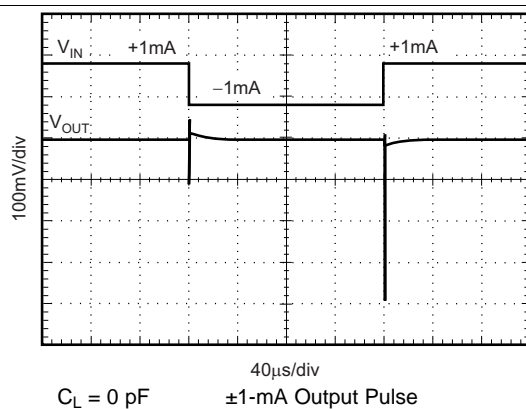


Figure 17. Load Transient

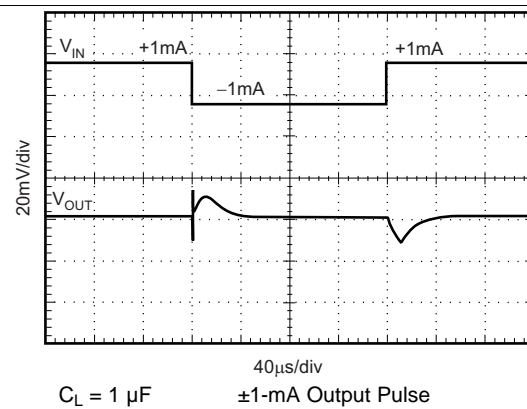


Figure 18. Load Transient

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{-V}$ power supply, and REF3125-Q1 is used for typical characteristic measurements, unless otherwise noted.

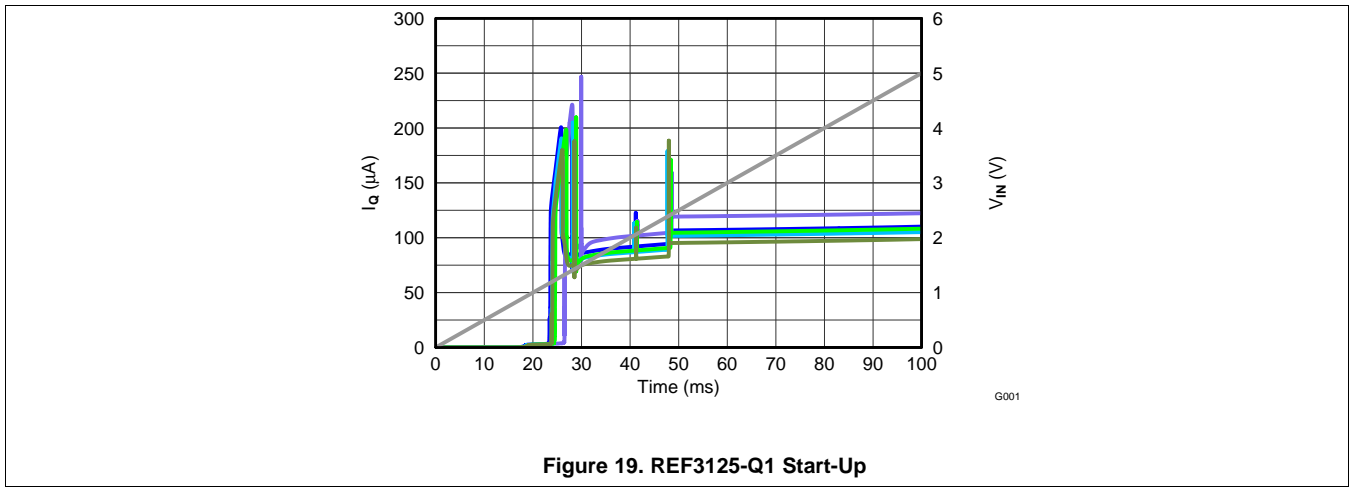


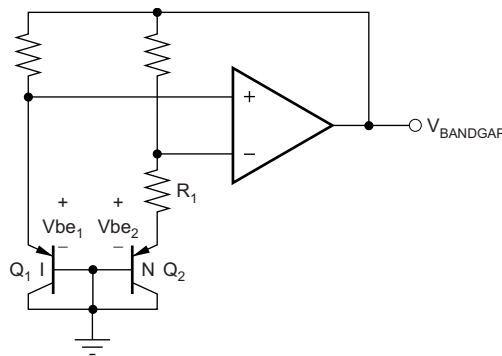
Figure 19. REF3125-Q1 Start-Up

8 Detailed Description

8.1 Overview

The REF31xx-Q1 is a family of series, CMOS, precision bandgap voltage references. The basic bandgap topology is shown in [Functional Block Diagram](#). Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2 . The difference of the two base-emitter voltages, $V_{be_1} - V_{be_2}$, has a positive temperature coefficient and is forced across resistor R_1 . This voltage is gained up and added to the base-emitter voltage of Q_2 , which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The curvature of the bandgap voltage, as shown in [Figure 3](#), is due to the slightly nonlinear temperature coefficient of the base-emitter voltage of Q_2 .

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Supply Voltage

The REF31xx-Q1 family of references features an extremely low dropout voltage. With the exception of the REF3112, which has a minimum supply requirement of 1.8 V, these references can be operated with a supply of only 5 mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load is shown in [Typical Characteristics](#).

The REF31xx-Q1 features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 100 μA , and the maximum quiescent current over temperature is just 135 μA . The quiescent current typically changes less than 2 μA over the entire supply range, as shown in [Figure 20](#).

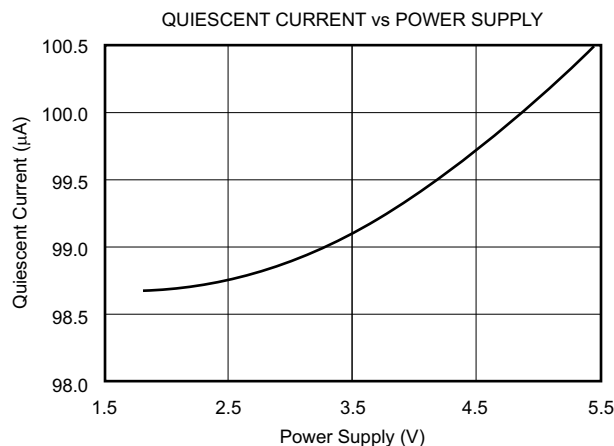


Figure 20. Supply Current vs Supply Voltage

Feature Description (continued)

Supply voltages below the specified levels can cause the REF31xx-Q1 to momentarily draw currents greater than the typical quiescent current. This can be prevented by using a power supply with a fast rising edge and low output impedance.

8.3.2 Thermal Hysteresis

Thermal hysteresis for the REF31xx-Q1 is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. It can be expressed as:

$$V_{\text{HYST}} = \left(\frac{\text{abs}|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \times 10^6 \text{ (ppm)}$$

Where:

V_{HYST} = Thermal hysteresis.

V_{PRE} = Output voltage measured at 25°C pretemperature cycling.

V_{POST} = Output voltage measured after the device has been cycled through the specified temperature range of –40°C to +125°C and returned to 25°C. (1)

8.3.3 Temperature Drift

The REF31xx-Q1 is designed to exhibit minimal drift error, defined as the change in output voltage over varying temperature. The drift is calculated using the *box* method, which is described in [Equation 2](#):

$$\text{Drift} = \left(\frac{V_{\text{OUTMAX}} - V_{\text{OUTMIN}}}{V_{\text{OUT}} \times \text{Temperature Range}} \right) \times 10^6 \text{ (ppm)} \quad (2)$$

The REF31xx-Q1 features a typical drift coefficient of 5 ppm from 0°C to 70°C, the primary temperature range for many applications. For the industrial temperature range of –40°C to +125°C, the REF31xx-Q1 family drift increases to a typical value of 10 ppm.

8.3.4 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in [Figure 21](#). The noise voltage of the REF31xx-Q1 increases with output voltage and operating temperature. Additional filtering may be used to improve output noise levels, although take care to ensure the output impedance does not degrade the AC performance.

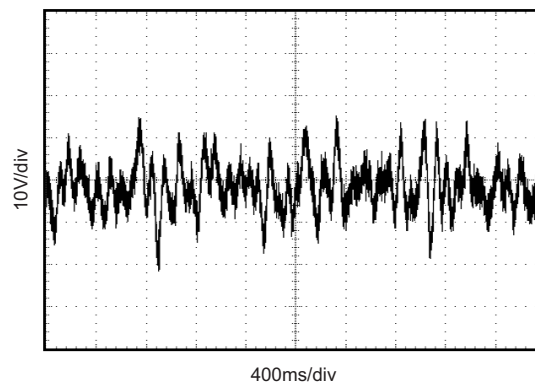


Figure 21. 0.1-Hz to 10-Hz Noise

Feature Description (continued)

8.3.5 Long-Term Stability

Long-term stability refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses, as is shown by the long-term stability curves. The typical drift value for the REF31xx-Q1 is 70 ppm from 0 to 1000 hours. This parameter is characterized by measuring 30 units at regular intervals for a period of 1000 hours.

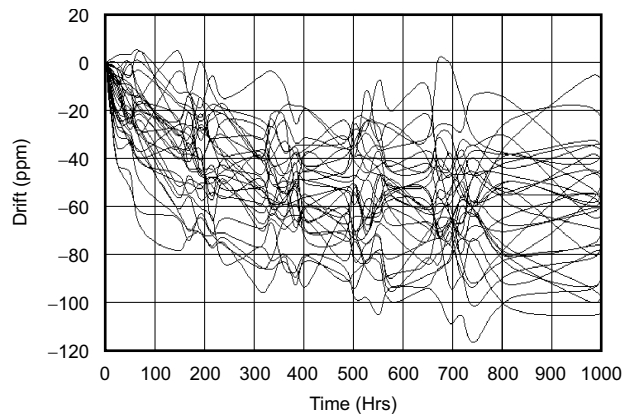
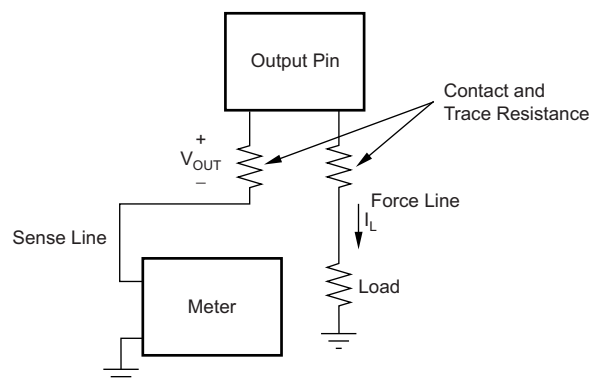


Figure 22. REF3112 Long-Term Stability

8.3.6 Load Regulation

Load regulation is defined as the change in output voltage due to changes in load current. The load regulation of the REF31xx-Q1 is measured using force and sense contacts as pictured in Figure 23. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the REF31xx-Q1. For applications requiring improved load regulation, force and sense lines must be used.



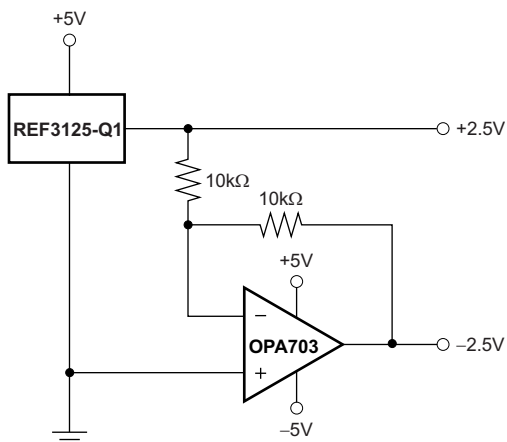
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Figure 23. Accurate Load Regulation of REF31xx-Q1

8.4 Device Functional Modes

8.4.1 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF31xx-Q1 and OPA703 can be used to provide a dual-supply reference from a $\pm 5\text{-V}$ supply. Figure 24 shows the REF3125-Q1 used to provide a $\pm 2.5\text{-V}$ supply reference voltage. The low drift performance of the REF31xx-Q1 complements the low offset voltage and low drift of the OPA703 to provide an accurate solution for split-supply applications.

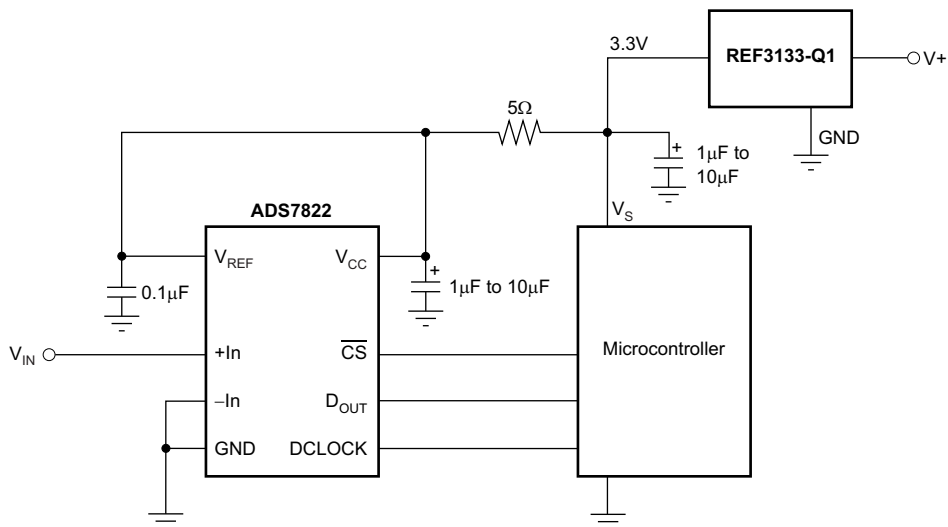


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Figure 24. REF3125-Q1 Combined With OPA703 to Create Positive and Negative Reference Voltages

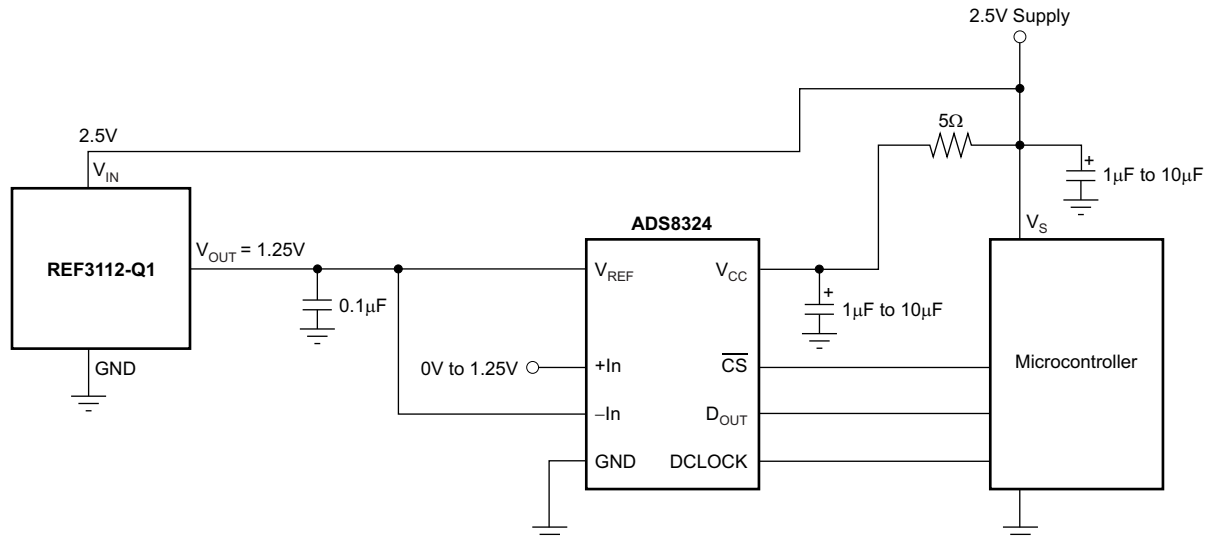
8.4.2 Data Acquisition

Data acquisition systems often require stable voltage references to maintain accuracy. The REF31xx-Q1 family features stability and a wide range of voltages suitable for most microcontrollers and data converters. Figure 25, Figure 26, and Figure 27 show basic data acquisition systems.



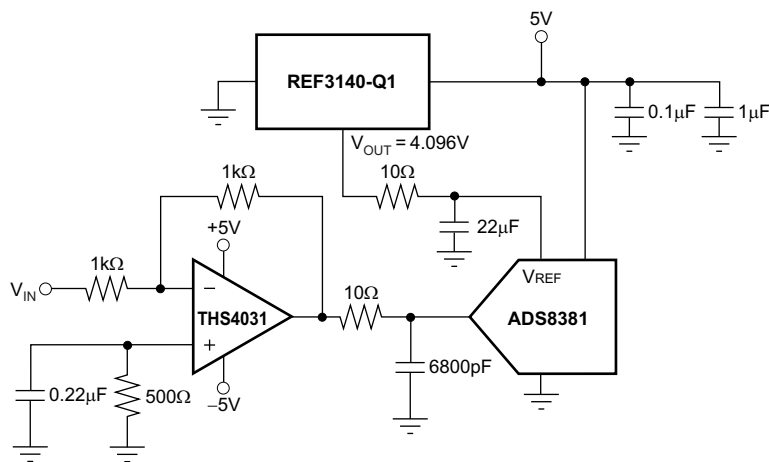
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Figure 25. Basic Data Acquisition System 1



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Figure 26. Basic Data Acquisition System 2



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Figure 27. REF3140-Q1 Provides an Accurate Reference for Driving the ADS8381

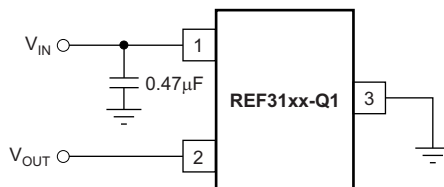
9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The REF31xx-Q1 does not require a load capacitor and is stable with any capacitive load. Figure 28 shows typical connections required for operation of the REF31xx-Q1. TI recommends a supply bypass capacitor of 0.47 μ F.

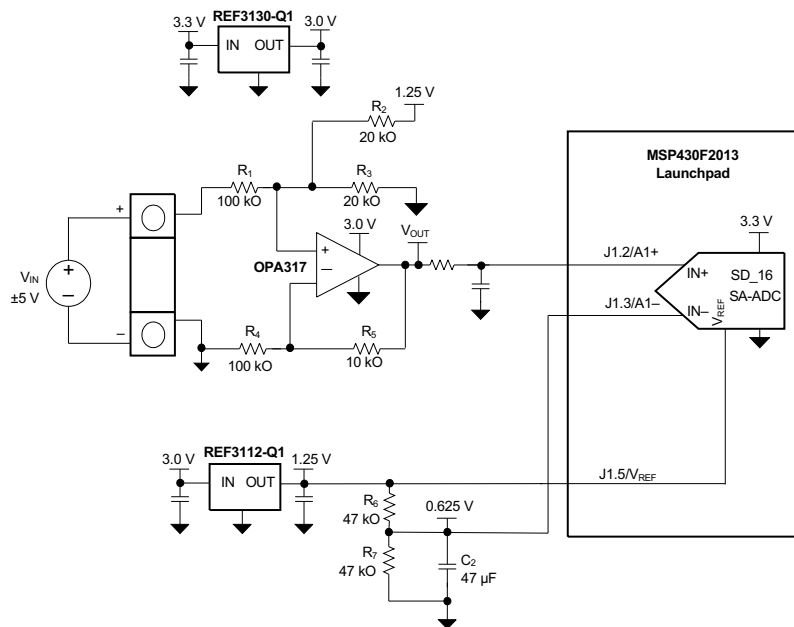


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Figure 28. Typical Connections for Operating REF31xx-Q1

9.2 Typical Application

Figure 29 shows a low-power reference and conditioning circuit. This circuit attenuates and level-shifts a bipolar input voltage within the proper input range of a single-supply, low-power, 16-bit $\Delta\Sigma$ ADC, such as the one inside the MSP430™ or other similar single-supply ADCs. Precision reference circuits are used to level-shift the input signal, provide the ADC reference voltage, and to create a well-regulated supply voltage for the low-power analog circuitry. A low-power, zero-drift, op-amp circuit is used to attenuate and level-shift the input signal.



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Figure 29. Low-Power Reference and Bipolar Voltage Conditioning Circuit for Low-Power ADCs

Typical Application (continued)

9.2.1 Design Requirements

For typical REF31xx-Q1 applications, use these parameters:

- Supply voltage: 3.3 V
- Maximum input voltage: ± 6 V
- Specified input voltage: ± 5 V
- ADC reference voltage: 1.25 V

The goal for this design is to accurately condition a ± 5 -V bipolar input voltage into a voltage suitable for conversion by a low-voltage ADC with a 1.25-V reference voltage, V_{REF} , and an input voltage range of $V_{REF} / 2$. The circuit must function with reduced performance over a wider input range of at least ± 6 V to protect from overvoltage conditions.

9.2.2 Detailed Design Procedure

Figure 29 depicts a simplified schematic for this design showing the MSP430 ADC inputs and full input conditioning circuitry. The ADC is configured for a bipolar measurement where final conversion result is the differential voltage between the voltage at the positive and negative ADC inputs. The bipolar, GND-referenced input signal must be level-shifted and attenuated by the operational amplifier so that the output is biased to $V_{REF}/2$ and has a differential voltage that is within the $\pm V_{REF}/2$ input range of the ADC.

9.2.3 Application Curves

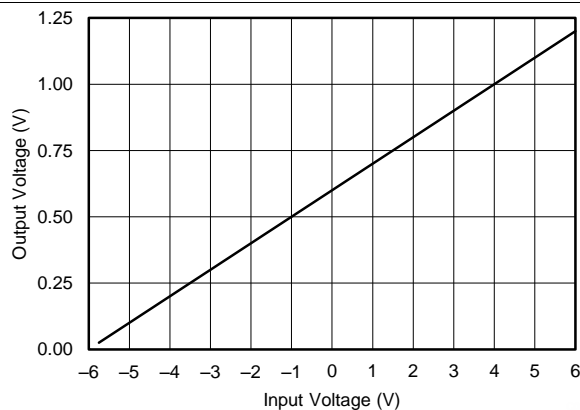


Figure 30. OPA317 Output Voltage vs Input Voltage

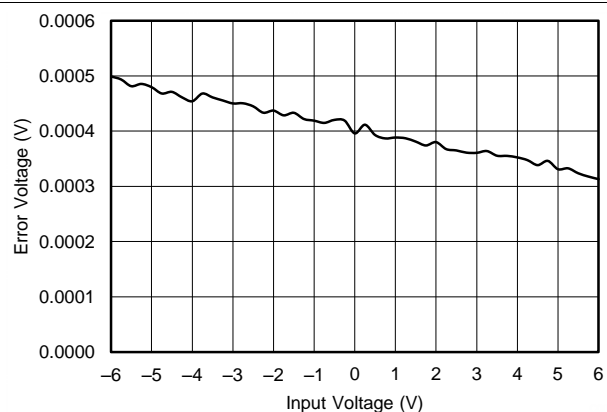


Figure 31. OPA317 Output Voltage Error vs Input Voltage

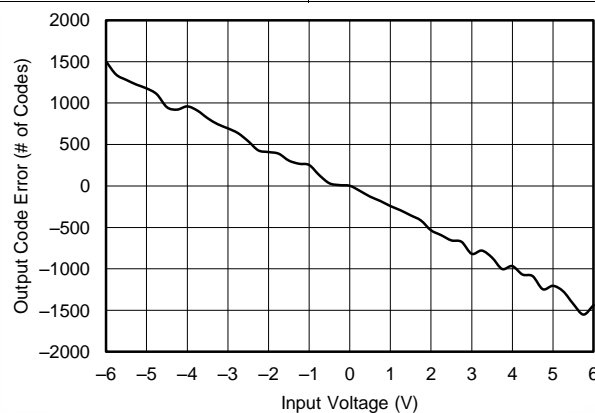


Figure 32. Output Code Error vs Input Voltage

10 Power Supply Recommendations

The REF31xx-Q1 family of references features an extremely low dropout voltage. With the exception of the REF3112, which has a minimum supply requirement of 1.8 V, these references can be operated with a supply of only 5 mV above the output voltage in an unloaded condition. For loaded conditions see [Figure 4](#). TI recommends a supply bypass capacitor greater than 0.47 μ F.

11 Layout

11.1 Layout Guidelines

[Figure 33](#) shows an example of a printed-circuit board (PCB) layout using the REF31xx-Q1. Some key considerations are:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors at V_{IN} of the REF31xx-Q1.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane to help distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close as possible to the device. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

11.2 Layout Example

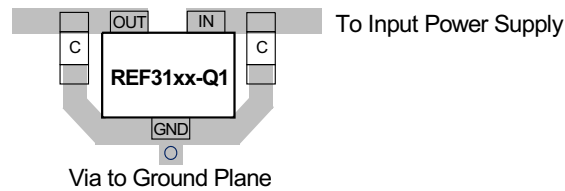


Figure 33. Layout Example

12 Device and Documentation Support

12.1 Device Support

For device support, see the following:

[Voltage References Forum](#)

12.2 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
REF3112-Q1	Click here	Click here	Click here	Click here	Click here
REF3120-Q1	Click here	Click here	Click here	Click here	Click here
REF3125-Q1	Click here	Click here	Click here	Click here	Click here
REF3130-Q1	Click here	Click here	Click here	Click here	Click here
REF3133-Q1	Click here	Click here	Click here	Click here	Click here
REF3140-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates — go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button to register and receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

MSP430, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF3112AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(31AQ ~ R31A)	Samples
REF3120AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	31BQ	Samples
REF3125AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	31CQ	Samples
REF3130AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	31EQ	Samples
REF3133AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(31FQ ~ R31A)	Samples
REF3140AQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	31DQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF3112AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
REF3120AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
REF3125AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
REF3130AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
REF3133AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
REF3140AQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF3112AQDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
REF3120AQDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
REF3125AQDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
REF3130AQDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
REF3133AQDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
REF3140AQDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

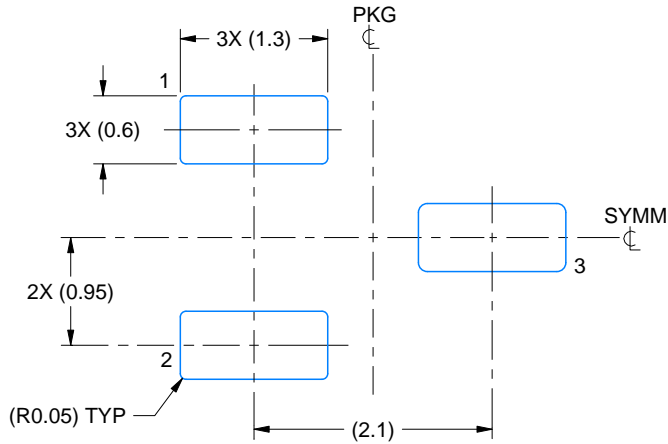
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

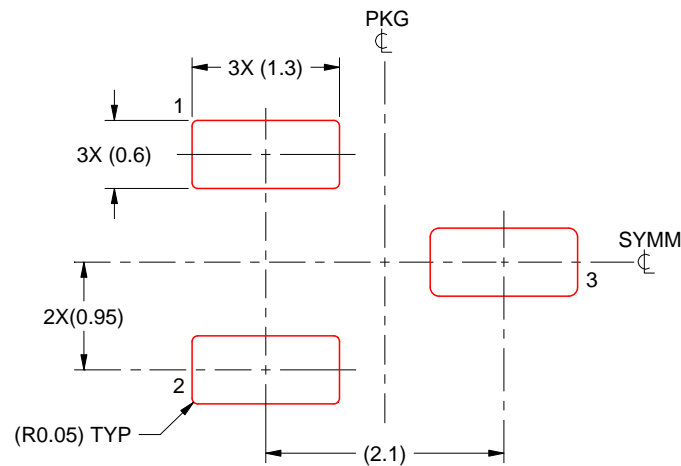
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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