





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage:	-0.5V to 3.6V
Input Voltage (all inputs)	-0.3V to $V_{CC}+0.3V$
Output Current	28 mA
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Package Thermal Resistance	
$\theta_{JA}$ 8-pin SOIC	+160°C/W
$\theta_{JA}$ 16-pin WQFN	+78.9°C/W
$\theta_{JC}$ 8-pin SOIC	+105°C/W
$\theta_{JC}$ 16-pin WQFN	+42.7°C/W
ESD Rating (HBM)	5kV
ESD Rating (MM)	250V

- (1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be ensured. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of [Electrical Characteristics](#) specifies acceptable device operating conditions.

### Recommended Operating Conditions

Supply Voltage ( $V_{CC} - V_{EE}$ ):	3.3V $\pm 5\%$
Operating Free Air Temperature ( $T_A$ )	
LMH0002MA	0°C to +70°C
LMH0002TMA and LMH0002SQ	-40°C to +85°C

## DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)(2)</sup>.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
$V_{CMIN}$	Input Common Mode Voltage		SDI, $\overline{SDI}$	$1.6 + V_{SDI}/2$		$V_{CC} - V_{SDI}/2$	V
$V_{SDI}$	Input Voltage Swing	Differential		100		2000	mV <sub>P-P</sub>
$V_{CMOUT}$	Output Common Mode Voltage		SDO, $\overline{SDO}$		$V_{CC} - V_{SDO}$		V
$V_{SDO}$	Output Voltage Swing	Single-ended, 75Ω load, $R_{REF} = 750\Omega$ 1%		750	800	850	mV <sub>P-P</sub>
		Single-ended, 75Ω load, $R_{REF} = 590\Omega$ 1%		900	1000	1100	mV <sub>P-P</sub>
	SD/ $\overline{HD}$ Input Voltage	Min for SD	SD/ $\overline{HD}$	2.4			V
		Max for HD				0.8	V
	SD/ $\overline{HD}$ Input Current			3.7			μA
$I_{CC}$	Supply Current	SD/ $\overline{HD} = 0$ <sup>(3)</sup>			45	49	mA
		SD/ $\overline{HD} = 1$ <sup>(3)</sup>			38	43	mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to  $V_{EE} = 0$  Volts.

(2) Typical values are stated for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .

(3) Maximum  $I_{CC}$  is measured at  $V_{CC} = +3.465V$  and  $T_A = +70^\circ C$ .

## AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified<sup>(1)</sup>.

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
$DR_{SDI}$	Input Data Rate	<sup>(2)</sup>	SDI, $\overline{SDI}$			1485	Mbps
$t_{jit}$	Additive Jitter	1.485 Gbps	SDO, $\overline{SDO}$		26		pS <sub>P-P</sub>
		270 Mbps			18		pS <sub>P-P</sub>
$t_r, t_f$	Output Rise Time, Fall Time	SD/ $\overline{HD} = 0$ , 20% – 80%, <sup>(3)</sup>			120	220	ps
		SD/ $\overline{HD} = 1$ , 20% – 80%		400	560	800	ps
	Mismatch in Rise/Fall Time	<sup>(2)</sup>				30	ps
	Duty Cycle Distortion	SD/ $\overline{HD} = 0$ , <sup>(2)</sup>				30	ps
		SD/ $\overline{HD} = 1$ , <sup>(2)</sup>				100	ps
$t_{OS}$	Output Overshoot	<sup>(2)</sup>				8	%
$RL_{SDO}$	Output Return Loss	<sup>(4)</sup>		15	20		dB

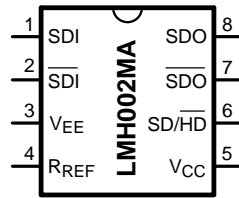
(1) Typical values are stated for  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$ .

(2) Specification is ensured by characterization.

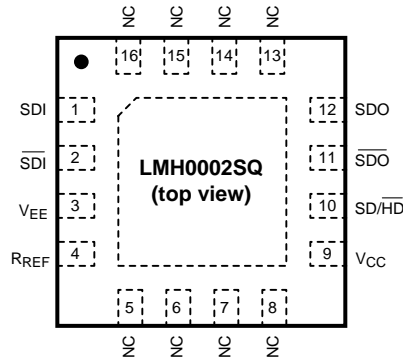
(3) Specification is ensured by characterization and verified by test.

(4) Output return loss is dependent on board design. The LMH0002 meets this specification on the SD002 evaluation board from 5MHz to 1.5GHz.

**CONNECTION DIAGRAM**



**Figure 1. 8-Pin SOIC  
See D Package**



**Figure 2. 16-Pin WQFN  
See RUM0016A Package**

**Table 1. PIN DESCRIPTIONS**

SOIC Pin #	WQFN Pin #	Name	Description
1	1	SDI	Serial data true input.
2	2	$\overline{\text{SDI}}$	Serial data complement input.
3	3	$V_{EE}$	Negative power supply (ground).
4	4	$R_{REF}$	Output driver level control. Connect a resistor to $V_{CC}$ to set output voltage swing.
5	9	$V_{CC}$	Positive power supply (+3.3V).
6	10	$\text{SD}/\overline{\text{HD}}$	Output slew rate control. Output rise/fall time complies with SMPTE 292M when low and SMPTE 259M when high.
7	11	$\overline{\text{SDO}}$	Serial data complement output.
8	12	SDO	Serial data true output.
—	5, 6, 7, 8, 13, 14, 15, 16	NC	No connect.
—	DAP	$V_{EE}$	Connect exposed DAP to negative power supply (ground).

## APPLICATION INFORMATION

### Device Operation

#### INPUT INTERFACING

The LMH0002 accepts either differential or single-ended input. The inputs are self-biased, allowing for simple AC or DC coupling. DC-coupled inputs must be kept within the specified common-mode range. SDI and  $\overline{\text{SDI}}$  are self-biased at approximately 2.1V with  $V_{CC} = 3.3\text{V}$ . Figure 3 shows the differential input stage for SDI and  $\overline{\text{SDI}}$ .

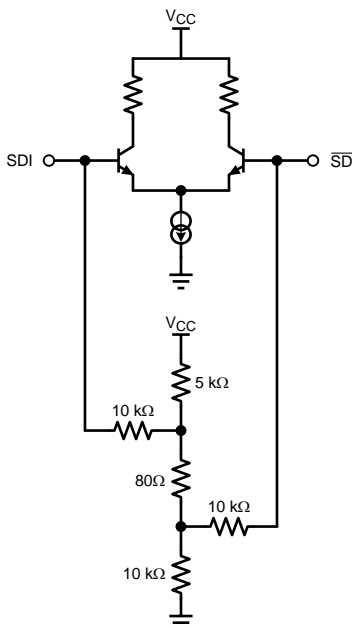


Figure 3. Differential Input Stage for SDI and  $\overline{\text{SDI}}$ .

#### OUTPUT INTERFACING

The LMH0002 uses current mode outputs. Single-ended output levels are 800 mV<sub>P-P</sub> into 75Ω AC-coupled coaxial cable (with  $R_{REF} = 750\Omega$ ). Output level is controlled by the value of the  $R_{REF}$  resistor connected between the  $R_{REF}$  pin and  $V_{CC}$ .

The  $R_{REF}$  resistor should be placed as close as possible to the  $R_{REF}$  pin. In addition, the copper in the plane layers below the  $R_{REF}$  network should be removed to minimize parasitic capacitance.

#### OUTPUT SLEW RATE CONTROL

The LMH0002 output rise and fall times are selectable for either SMPTE 259M or SMPTE 292M compliance via the SD/HD pin. For slower rise and fall times, or SMPTE 259M compliance, SD/HD is set high. For faster rise and fall times, or SMPTE 292M compliance, SD/HD is set low.

#### REPLACING THE GENNUM GS1528, GS1528A, and GS1578A

The LMH0002MA is form-fit-function compatible with the Gennum GS1528 and GS1528A. The LMH0002SQ is form-fit-function compatible with the Gennum GS1578A.

## REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">5</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0002MA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L002	<a href="#">Samples</a>
LMH0002MAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L002	<a href="#">Samples</a>
LMH0002SQ/NOPB	ACTIVE	WQFN	RUM	16	1000	RoHS & Green	SN	Level-1-260C-UNLIM		L002	<a href="#">Samples</a>
LMH0002SQE/NOPB	ACTIVE	WQFN	RUM	16	250	RoHS & Green	SN	Level-1-260C-UNLIM		L002	<a href="#">Samples</a>
LMH0002TMA/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L002T	<a href="#">Samples</a>
LMH0002TMAX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L002T	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0002MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH0002SQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0002SQE/NOPB	WQFN	RUM	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0002TMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0002MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH0002SQ/NOPB	WQFN	RUM	16	1000	210.0	185.0	35.0
LMH0002SQE/NOPB	WQFN	RUM	16	250	210.0	185.0	35.0
LMH0002TMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0





D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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