SiT9367

220 MHz to 725 MHz Ultra-low Jitter Differential Oscillator

Description

The SiT9367 is a 220.000001 MHz to 725 MHz differential MEMS XO engineered for low-jitter applications. Utilizing SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technology, the SiT9367 delivers exceptional dynamic performance by providing resistance to airflow, thermal gradients, shock and vibration. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT9367 can be factory programmed for any combination of frequency, stability, voltage, and output signaling. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

The wide frequency range and programmability makes this device ideal for telecom, networking, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to Manufacturing Notes for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Any frequency between 220.000001 MHz and 725 MHz, accurate to 6 decimal places.
  For HCSL output signaling, maximum frequency is 500 MHz. Contact SiTime for higher frequency options.
  (For additional frequencies, refer to SiT9366 and SiT9365 datasheets)
- LVPECL, Low-swing LVPECL, LVDS and HCSL output signaling
- 0.1ps RMS phase jitter (random) for Ethernet applications
- Frequency stability as low ±10 ppm
- Wide temperature range from -40°C to 105°C
  Contact SiTime for higher temperature range options
- Industry-standard packages: 3.2 x 2.5 mm^2, 7.0 x 5.0 mm^2 and 5.0 x 3.2 mm^2 package

Applications

- 100 Gbps Ethernet, SONET, SATA, SAS, Fibre Channel
- Telecom, networking, instrumentation, storage, servers

Block Diagram

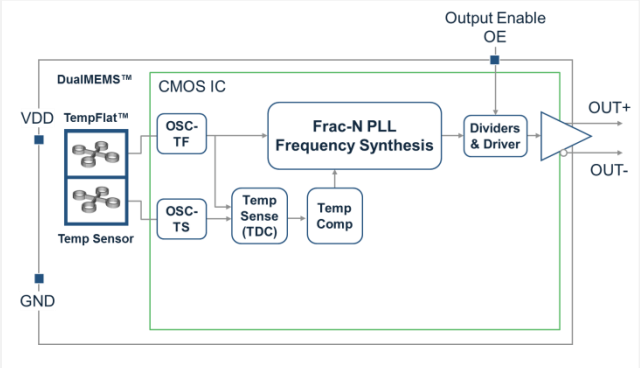


Figure 1. SiT9367 Block Diagram

Package Pinout

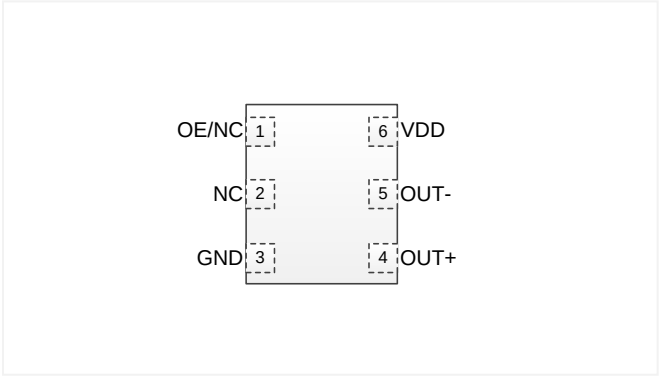
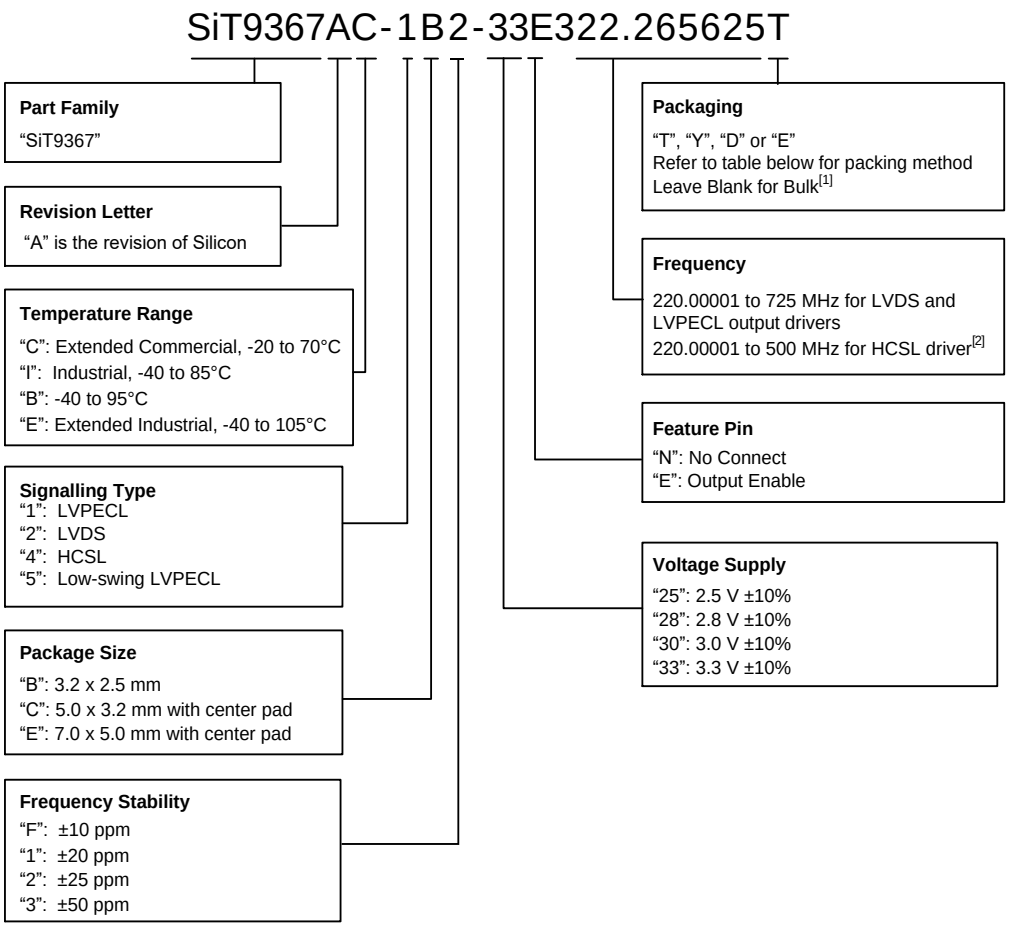


Figure 2. Pin Assignments (Top view)
(Refer to Table 6 for Pin Descriptions)

Ordering Information



Notes:
1. Bulk is available for sampling only.
2. Contact SiTime for higher frequency HCSL options.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
5.0 x 3.2			T	Y		
3.2 x 2.5	D	E			—	—

TABLE OF CONTENTS

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C at nominal supply voltage.

Table 2. Electrical Characteristics – Common to LVPECL, Low-swing LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	220.000001	–	725	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_1y	-0.7	±0.4	+0.7	ppm	At 85°C
5 Year Aging	F_5y	-1.1	±0.7	+1.1	ppm	At 85°C
10 Year Aging	F_10y	-1.3	±0.8	+1.3	ppm	At 85°C
20 Year Aging	F_20y	-1.5	±1.0	+1.5	ppm	At 85°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
		-40	–	+95	°C	
		-40	–	+105	°C	Extended Industrial
Supply Voltage						
Supply Voltage	Vdd	2.97	3.30	3.63	V	
		2.70	3.00	3.30	V	
		2.52	2.80	3.08	V	
		2.25	2.50	2.75	V	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 1, OE logic high or logic low
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Startup Time	T_start	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	3.8	µs	f = 322.265625 MHz. Measured from the time OE pin reaches rated VIH and VIL to the time clock pins reach 90% of swing and high-Z. See Figure 8 and Figure 9

Table 3. Electrical Characteristics – LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	94	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	63	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	33	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics for LVPECL						
Output High Voltage	VOH	Vdd-1.15	–	Vdd-0.7	V	See Figure 4
Output Low Voltage	VOL	Vdd-2.0	–	Vdd-1.5	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	225	330	ps	20% to 80%, see Figure 5
Output Characteristics for Low-swing LVPECL						
Output High Voltage	VOH	Vdd-1.2	–	Vdd-0.75	V	See Figure 4
Output Low Voltage	VOL	Vdd-1.8	–	Vdd-1.25	V	See Figure 4
Output Differential Voltage Swing	V_Swing	0.4	1	1.2	V	Output frequency 1 to 220 MHz, See Figure 5
		0.4	1	1.6	V	Output frequency greater than 220 MHz, See Figure 5
Rise/Fall Time	Tr, Tf	–	225	320	ps	20% to 80%. See Figure 5
Jitter – 7.0 x 5.0 mm Package						
RMS Period Jitter[3]	T_jitt	–	1.0	1.6	Ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.220	0.270	Ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC.
		–	0.220	0.300	Ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -40 to 95ºC and -40 to 105ºC
		–	0.1	–	Ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all Vdd levels
Jitter – 5.0 x 3.2 and 3.2 x 2.5 mm Packages						
RMS Period Jitter[3]	T_jitt	–	1.0	1.6	Ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.225	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC.
		–	0.225	0.315	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -40 to 95ºC and -40 to 105ºC
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all Vdd levels

Notes:
3. Measured according to JESD65B

Table 4. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	85	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	63	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	300	–	450	mV	See Figure 6
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 6
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 6
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 6
Rise/Fall Time	Tr, Tf	–	370	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 3
Jitter – 7.0 x 5.0 mm Package						
RMS Period Jitter[4]	T_jitt	–	0.92	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40-85ºC.
		–	0.215	0.280	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges are -40 to 95ºC and -40 to 105ºC.
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz. Includes spurs for all Vdd levels.
Jitter – 5.0 x 3.2 and 3.2 x 2.5 mm Packages						
RMS Period Jitter[4]	T_jitt	–	0.92	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.235	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40-85ºC.
		–	0.235	0.310	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges are -40 to 95ºC and -40 to 105ºC.
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz. Includes spurs for all Vdd levels.

Notes:
4. Measured according to JESD65B

Table 5. Electrical Characteristics – HCSL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	97	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	63	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	µA	OE = Low
Maximum Output Current	I_driver	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 4
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1.2	1.4	1.9	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	360	505	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
Jitter – 7.0 x 5.0 mm Package						
RMS Period Jitter[5]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.215	0.265	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC
		–	0.215	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature range ranges -40 to 95ºC and -40 to 105ºC
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all Vdd levels
Jitter – 5.0 x 3.2 and 3.2 x 2.5 mm Packages						
RMS Period Jitter[5]	T_jitt	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, Vdd = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.235	0.282	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -20 to 70ºC and -40 to 85ºC
		–	0.235	0.305	ps	f = 322.265625 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdd levels, includes spurs. Temperature ranges -40 to 95ºC and -40 to 105ºC
		–	0.1	–	ps	f = 322.265625 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs for all Vdd levels.

Note:
5. Measured according to JESD65B

Table 6. Pin Description

Pin	Map	Functionality	
1	OE/NC	Output Enable (OE)	H[6]: specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions.
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[7]

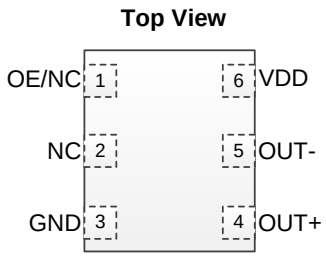


Figure 3. Pin Assignments

Notes:
6. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
7. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.

Table 7. Absolute Maximum Ratings

Caution: Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	ºC
Maximum Junction Temperature		130	ºC
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	ºC

Table 8. Thermal Considerations[8]

Package	θ_{JA}, 4 Layer Board (°C/W)	θ_{JC}, Bottom (°C/W)
3225, 6-pin	80	30
5032, 6-pin	53	20
7050, 6-pin	52	19

Notes:

8. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 9. Maximum Operating Junction Temperature[9]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C
95°C	120°C
105°C	130°C

Notes:

9. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 10. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Waveform Diagrams

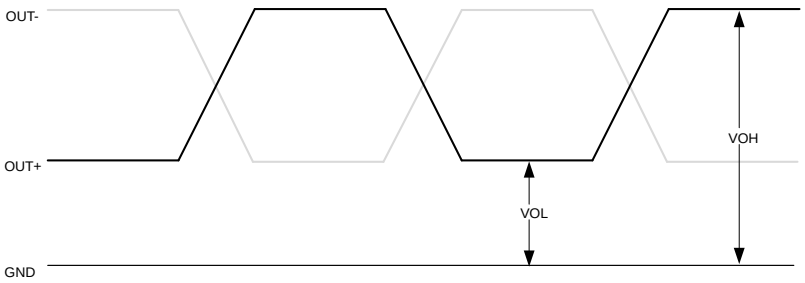


Figure 4. LVPECL, Low-swing LVPECL, and HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

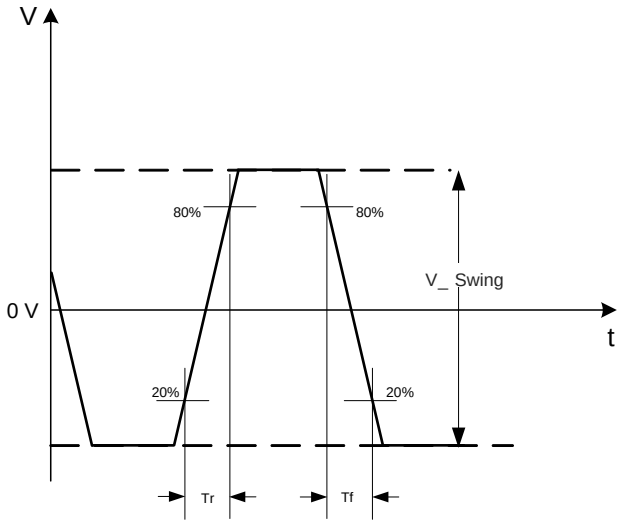


Figure 5. LVPECL, Low-swing LVPECL, and HCSL Voltage Levels Across Differential Pair (i.e. OUT+ minus OUT-)

Waveform Diagrams (continued)

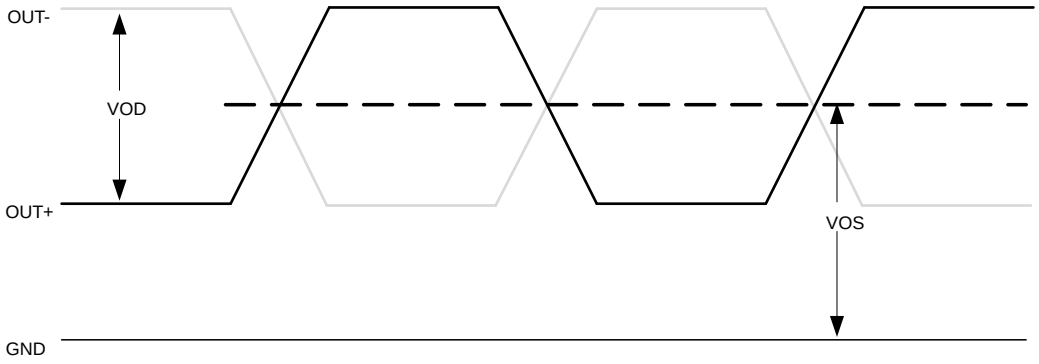


Figure 6. LVDS Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

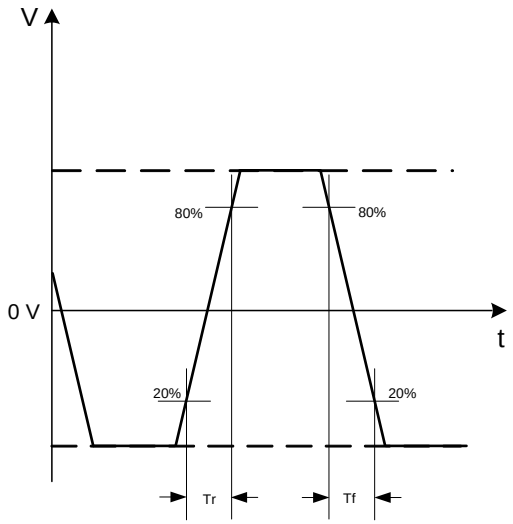


Figure 7. LVDS Differential Waveform (i.e. OUT+ minus OUT-)

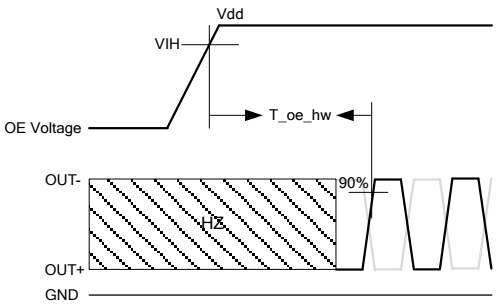


Figure 8. Hardware OE Enable Timing

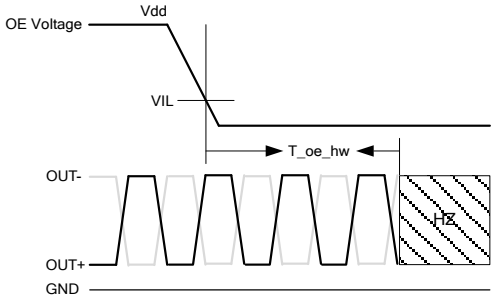


Figure 9. Hardware OE Disable Timing

Termination Diagrams

LVPECL and Low-swing LVPECL

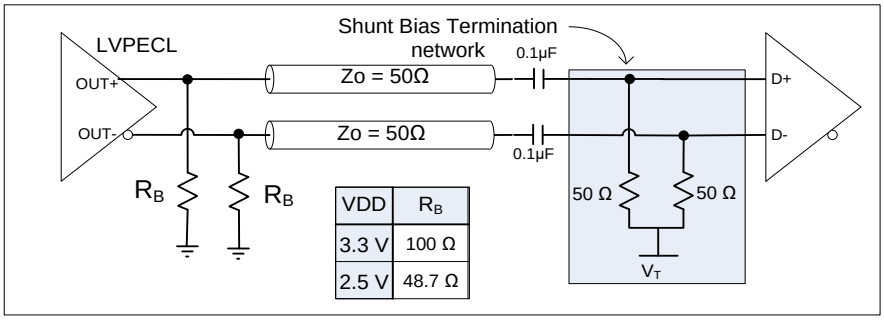


Figure 10. LVPECL and Low-swing LVPECL with AC-coupled Termination

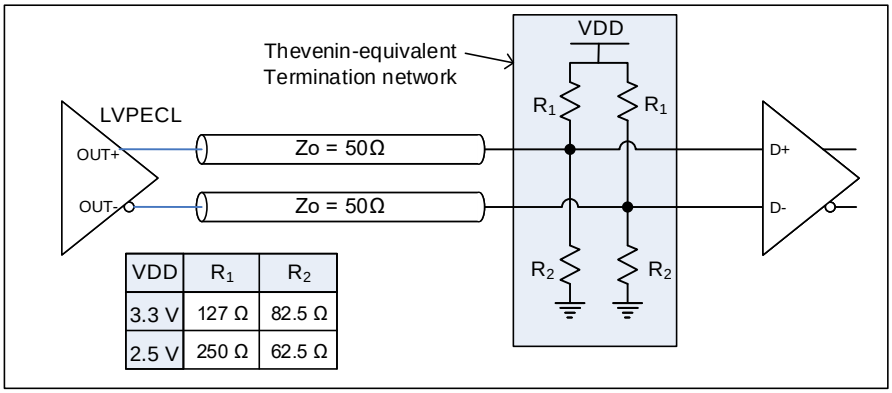


Figure 11. LVPECL and Low-swing LVPECL DC-coupled Load Termination with Thevenin Equivalent Network

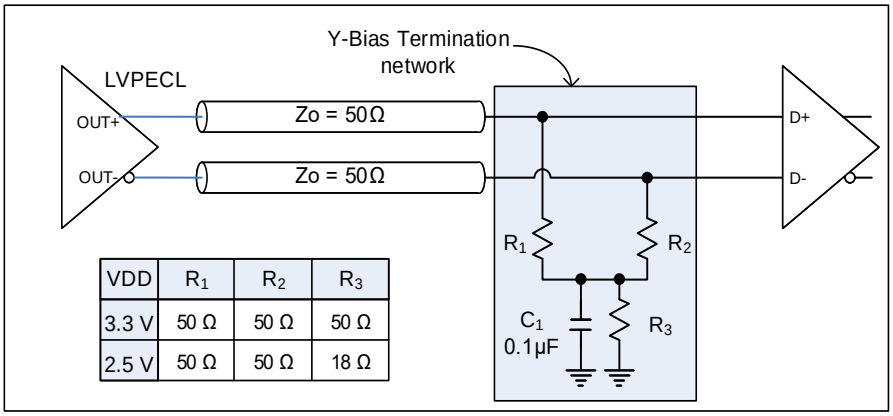


Figure 12. LVPECL and Low-swing LVPECL with Y-Bias Termination

Termination Diagrams (continued)

LVPECL and Low-swing LVPECL (continued)

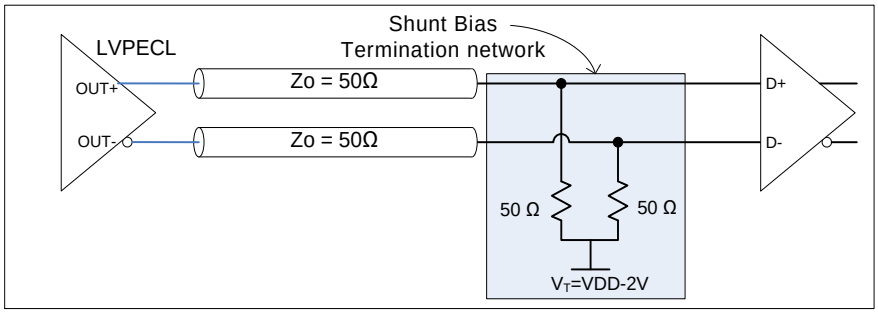


Figure 13. LVPECL and Low-swing LVPECL with DC-coupled Parallel Shunt Load Termination

Termination Diagrams (continued)

LVDS

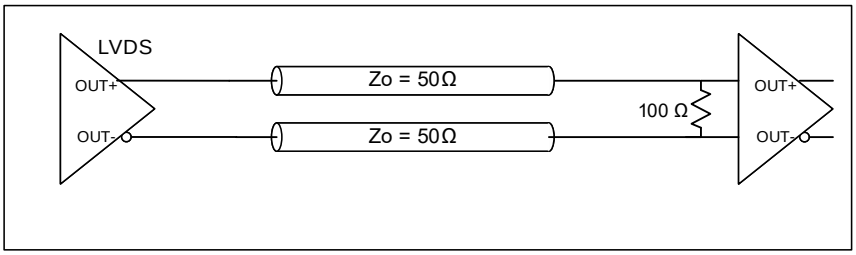


Figure 14. LVDS Single DC Termination at the Load

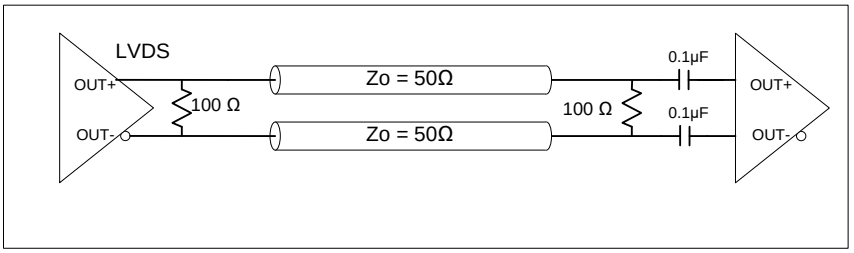


Figure 15. LVDS double AC Termination with Capacitor Close to the Load

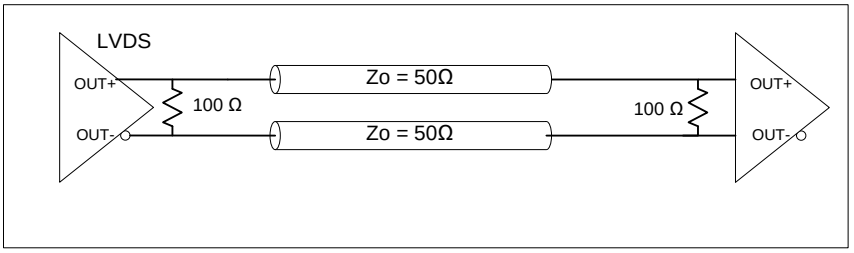


Figure 16. LVDS Double DC Termination

Termination Diagrams (continued)

HCSL

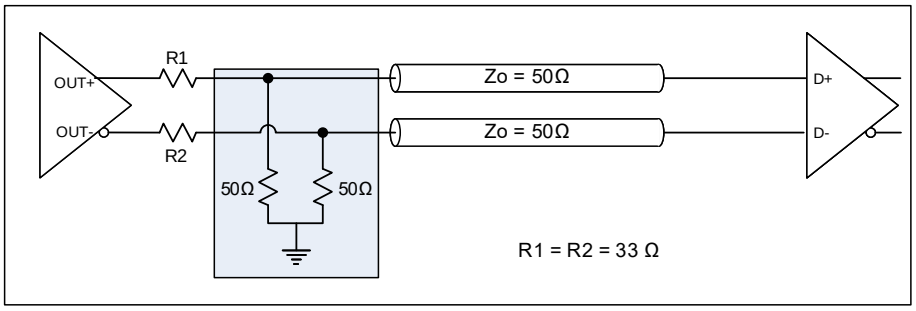
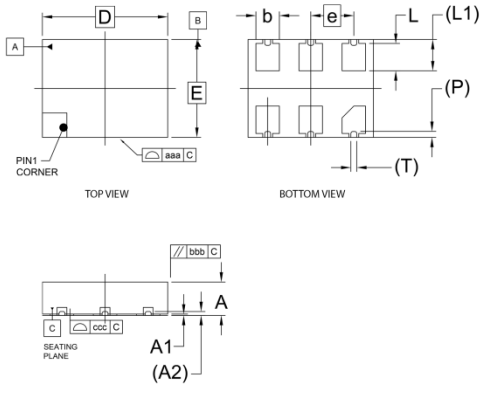


Figure 17. HCSL Interface Termination

Dimensions and Patterns — 3.2 x 2.5 mm²

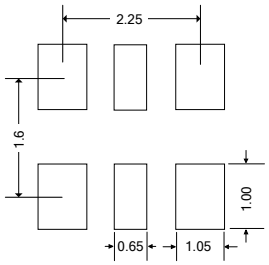
Package Size – Dimensions (Unit: mm)[10]	Recommended Land Pattern (Unit: mm)[11]
3.2 x 2.5 x 0.85 mm	**3.2 x 2.5 x 0.85 mm**



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		3.200 BSC	
	Y	E		2.500 BSC	
LEAD WIDTH		b	0.550	0.600	0.650
LEAD LENGTH		L	0.650	0.700	0.750
		L1		1.000 REF	
LEAD PITCH		e		1.100 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANRITY		ccc		0.080	
DIMPLE WIDTH		T		0.300 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

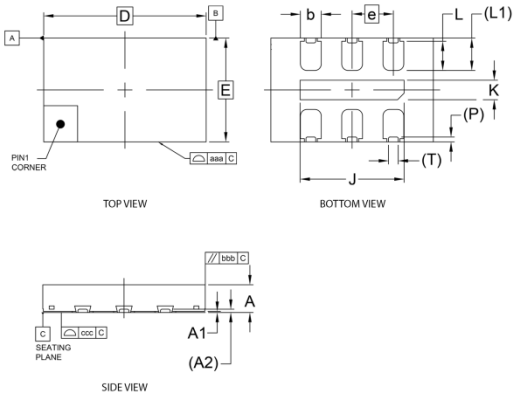
Notes
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters

Package Outline	
6L PQFD	POD-PQFD-006-C03225-038
3.200x2.500x0.850 mm	SiTime
2019/03/13 Rev B00	



Dimensions and Patterns — 5.0 x 3.2 mm²

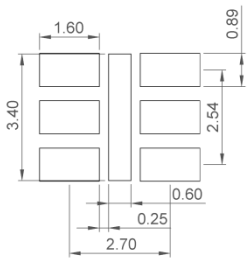
Package Size – Dimensions (Unit: mm)[10]	Recommended Land Pattern (Unit: mm)[11]
5.0 x 3.2 x 0.85 mm[12]	**5.0 x 3.2 x 0.85 mm[12]**



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		5.000 BSC	
	Y	E		3.200 BSC	
EP SIZE	X	J	3.100	3.200	3.300
	Y	K	0.500	0.600	0.700
LEAD WIDTH		b	0.590	0.640	0.690
LEAD LENGTH		L	0.850	0.900	0.950
		L1		1.000 REF	
LEAD PITCH		e		1.270 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANRITY		ccc		0.080	
DIMPLE WIDTH		T		0.300 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

Notes
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters

Package Outline	
6L PQFV	POD-PQFV-006-C05032-039
5.000x3.200x0.850 mm	SiTime
2019/03/13 Rev B00	

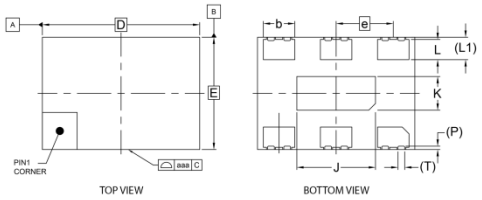


Notes:

10. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
11. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.
12. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Dimensions and Patterns — 7.0 x 5.0 mm^2

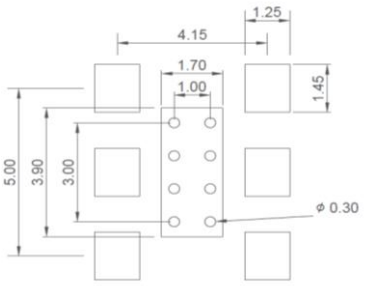
Package Size – Dimensions (Unit: mm)[13]	Recommended Land Pattern (Unit: mm)[14]
7.0 x 5.0 x 0.85 mm[15]	**7.0 x 5.0 x 0.85 mm[15]**



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		7.000 BSC	
	Y	E		5.000 BSC	
EP SIZE	X	J	3.400	3.500	3.600
	Y	K	1.400	1.500	1.600
LEAD WIDTH		b	1.350	1.400	1.450
LEAD LENGTH		L	0.850	0.900	0.950
		L1		1.000 REF	
LEAD PITCH		e		2.540 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANRITY		ccc		0.080	
DIMPLE WIDTH		T		0.300 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

Notes
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters

Package Outline	
6L PQFV	POD-PQFV-006-C07050-037
7.000x5.000x0.850 mm	
2019/03/13 Rev B00	



Note:
Circles in center pad are thermal vias, recommended to improve thermal performance

Notes:

13. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
14. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.
15. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Additional Information

Table 11. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Part number Generator	Tool used to create the part number based on desired features.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/manufacturing-notes
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6085/6EB rev. 3.0, SiT6085EB rev.3.1 and SiT6097EB rev. 2.0 Evaluation Boards for Differential Oscillators User Manual	https://www.sitime.com/support/user-guides

Revision History

Table 12. Revision History

Revision	Release Date	Change Summary
1.0	07/21/17	Initial draft
1.03		Corrected max frequency in ordering information table. Added 5.0 x 3.2 package. Added preliminary IPJ numbers for 5032 package. Will be updated after characterization. Corrected minor errors. Added Additional Information Table.
1.04	05/11/2018	Performed minor edits and updated Ordering Information.
1.05	10/25/2018	Removed “Contact SiTime” for ±10 ppm
1.06	08/17/2019	Updated package Dimensions Drawings Updated Table 8 Thermal Considerations for 5032 package Updated Table 2 specification for First Year Aging Added 5, 10, and 20 year aging specs Added Evaluation Boards SiT6085EB reference in Additional Information Rearranged layout, added Description, Block Diagram and TOC Tightened LVDS minimum VOD specification Added HTS code Added low-swing LVPECL package code and specifications

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439