Si5357 Data Sheet

12-Output Any-Frequency Clock Generator

Based on Silicon Labs proprietary MultiSynth™ flexible frequency synthesis technology, the Si5357 generates any combination of output frequencies with excellent jitter performance. The device's highly flexible architecture enables a single device to generate a wide range of integer and non-integer related frequencies on up to 12 clock outputs with 0 ppm frequency synthesis error. The device offers multiple banks of outputs that can each be tied to independent voltages, enabling usage in mixed-supply applications. Given its frequency, format, and supply voltage flexibility, the Si5357 is ideally suited to replace multiple clock ICs and oscillators with a single device.

The Si5357 is quickly and easily configured using ClockBuilder Pro™ software. ClockBuilder Pro assigns a custom part number for each unique configuration. Devices are factory-programmable free of charge, making it easy to get a custom clock uniquely tailored for each application. Devices can also be in-circuit programmed via an I^2C serial interface.

Applications:

- Servers, Storage
- Print Imaging
- Audio processing
- Broadcast Video
- Test and Measurement
- Industrial, Embedded Computing

KEY FEATURES

- Any-frequency 12-output LVCMOS programmable clock generator
- Offered in 32-pin QFN, up to 12 outputs
- MultiSynth technology enables any-frequency synthesis on any output up to 170 MHz
- Highly configurable output path featuring a cross point mux
  - Up to three independent fractional synthesis output paths
  - Up to five independent integer dividers
- Input frequency range:
  - External crystal: 16 to 50 MHz
  - Differential clock: 10 to 170 MHz
  - LVCMOS clock: 10 to 170 MHz
- Output frequency range: 5 to 170 MHz
- Temperature range: –40 to +85 °C
- RoHS-6 compliant
- Down and center spread spectrum

Table of Contents

1. Features List

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- Output frequency range: 5 to 170 MHz
- Operating temperature range: –40 to +85 °C ambient
- RoHS-6 compliant

2. Ordering Guide

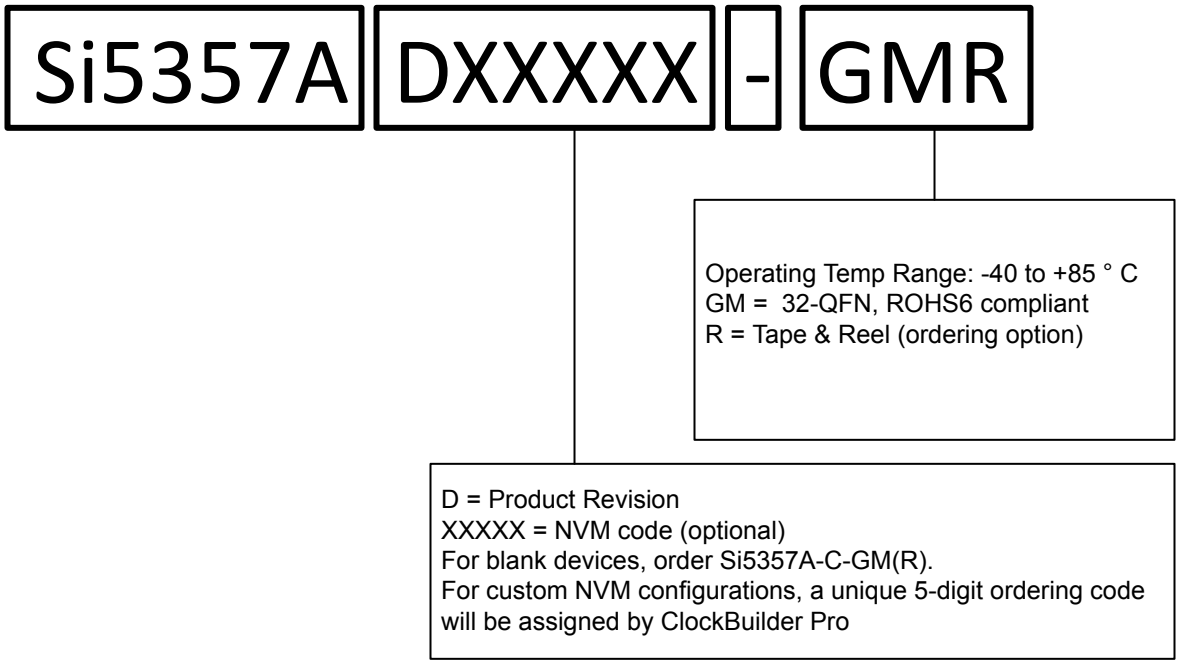


Figure 2.1. Orderable Part Number Guide

3. Functional Description

The Si5357 is a high-performance, low-jitter clock generator capable of synthesizing up to 12 user-programmable clock frequencies up to 170 MHz. The device supports free-run operation using an external crystal, or it can lock to an external clock signal. The output drivers support up to 12 differential clocks or 24 LVCMOS clocks, or a combination of both. VDDO pins are provided for versatility, which can be set to 3.3 V, 2.5 V, 1.8 V, or 1.5 V to power the multi-format output drivers. The core voltage supply (VDD) accepts 3.3 V, 2.5 V, or 1.8 V and is independent from the output supplies (VDDOxs). Using its two-stage synthesis architecture and patented high-resolution low-jitter MultiSynth technology, the Si5357 can generate an entire clock tree from a single device.

The Si5357 combines a wideband PLL with next generation MultiSynth technology to offer the industry's highest output count high performance programmable clock generator, while maintaining excellent jitter performance. The PLL locks to either an external 16–30 MHz crystal (XA/XB) for generating free-running clocks or to an external clock (CLKIN_2/CLKIN_2#) for generating synchronous clocks. In free-run mode, the oscillator frequency is multiplied by the PLL and then divided down either by an integer divider or MultiSynth for fractional synthesis.

The Si5357 features user-defined universal hardware input pins which can be configured in the ClockBuilder Pro software utility. Universal hardware pins can be used for OE, spread spectrum enable, input clock selection, output frequency selection, or I^2C address select.

The device provides the option of storing a user-defined clock configuration in its non-volatile memory (NVM), which becomes the default clock configuration at power-up. To enable in-system programming, a power up mode is available through OTP which powers up the chip in an OTP defined default mode but with no outputs enabled. This allows a host processor to first write a user defined subset of the registers and then restart the power-up sequence to activate the newly programmed configuration without re-downloading the OTP.

3.1 Functional Block Diagram

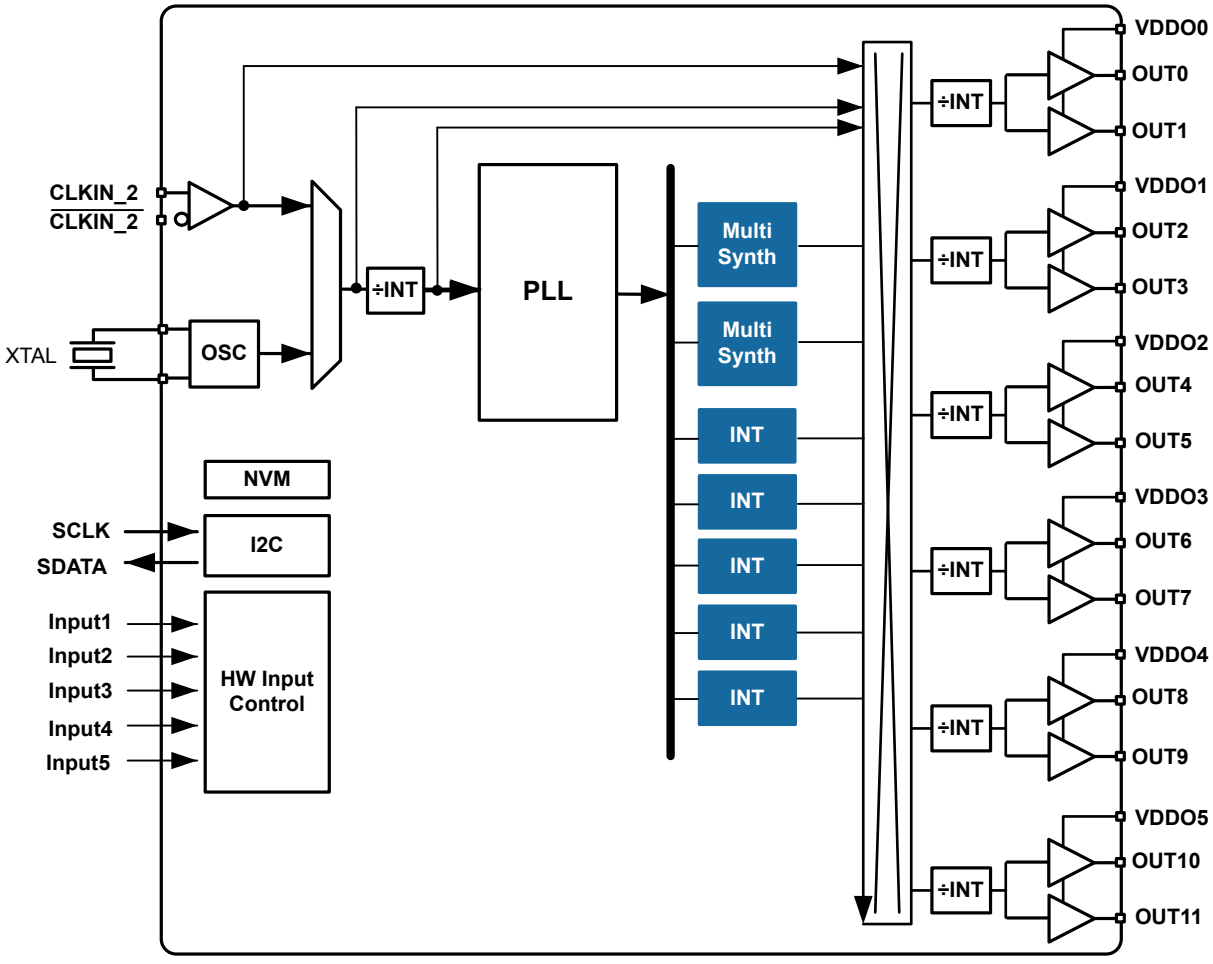


Figure 3.1. Block Diagram for 12-Output Si5357 in 32-QFN

3.2 Modes of Operation

The Si5357 supports both free-run and synchronous modes of operation. The default mode selection is set in ClockBuilder Pro. Alternatively, a universal hardware input pin can be defined as CLKIN_SEL to select between a crystal or clock input. There is also the option to select the input source via the serial interface by writing to the input select register.

3.2.1 Initialization

When power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible when this initialization period is complete. The clock outputs will be squelched until the device initialization is done.

3.3 Frequency Configuration

The phase-locked loop is fully integrated and does not require external loop filter components. Its function is to phase lock to the selected input and provide a common synchronous reference to the high-performance MultiSynth fractional or integer dividers.

A crosspoint mux connects any of the MultiSynth divided frequencies or INT divided frequencies to individual output drivers or banks of output drivers. Additional output integer dividers provide further frequency division by an even integer from 1 to 63. The frequency configuration of the device is programmed by setting the input dividers (P), the PLL feedback fractional divider (Mn/Md), the MultiSynth fractional dividers (Nn/Nd), and the output integer dividers (R). Silicon Labs' Clockbuilder Pro configuration utility determines the optimum divider values for any desired input and output frequency plan

3.4 Inputs

The Si5357 requires an external 16–50 MHz crystal at its XA/XB pins to operate in free-run mode, or an external input clock (CLKIN_2/CLKIN_2#) for synchronous operation. An external crystal is not required in synchronous mode.

3.4.1 External Reference Input (XA/XB)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) on Si5357 to produce a low jitter reference for the PLL when operating in the free-run mode. The Si5357 Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

For free-running operation, the internal oscillator can operate from a low-frequency fundamental mode crystal (XTAL) with a resonant frequency of 16 to 50 MHz. A crystal can easily be connected to pins XA and XB without external components, as shown in the figure below. Internal loading capacitance (CL) values from 2 pf to 30 pf can be selected via register settings or internal CL can be totally disabled allowing for external CL. Alternatively, an external CL can be used along with the internal CL.

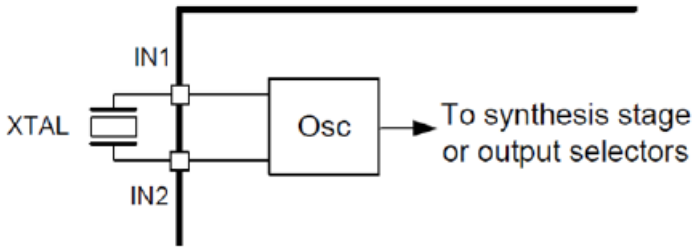


Figure 3.2. External Reference Input (XA/XB)

3.4.2 Input Clocks

An input clock is available to synchronize the PLL when operating in synchronous mode. This input can be configured as LVPECL, LVDS or HCSL differential, or LVCMOS. The recommended input termination schemes are shown in the *Si5357 Family Reference Manual*. Unused inputs can be disabled by register configuration.

3.4.3 Input Selection

The active clock input is selected by register control, or by defining two universal input pins as CLKIN_SEL[1:0] in ClockBuilder Pro. A register bit determines input selection as pin or register selectable. If there is no clock signal on the selected input at power up, the device will not generate output clocks.

In a typical application, the Si5357 reference input is configured immediately after power-up and initialization. If the device is switched to another input more than ±1000 ppm offset from the initial input, the device must be recalibrated manually to the new frequency, temporarily turning off the clock outputs. After the VCO is recalibrated, the device will resume producing clock outputs. If the selected inputs are within ±1000 ppm, any phase error difference will propagate through the device at a rate determined by the PLL bandwidth. Hitless switching and phase build-out are not supported by the Si5357.

3.5 Outputs

The Si5357 supports up to 12 LVCMOS output drivers.

Utilizing the reference clock enables a fan-out buffer function from an input clock source to any bank of outputs.

Individual output integer output dividers (R) allow the generation of additional synchronous frequencies. These integer dividers are configurable as divide by 1 (default) through 63.

3.5.1 LVCMOS Output Terminations

LVCMOS outputs can be dc-coupled, as shown in the figure below.

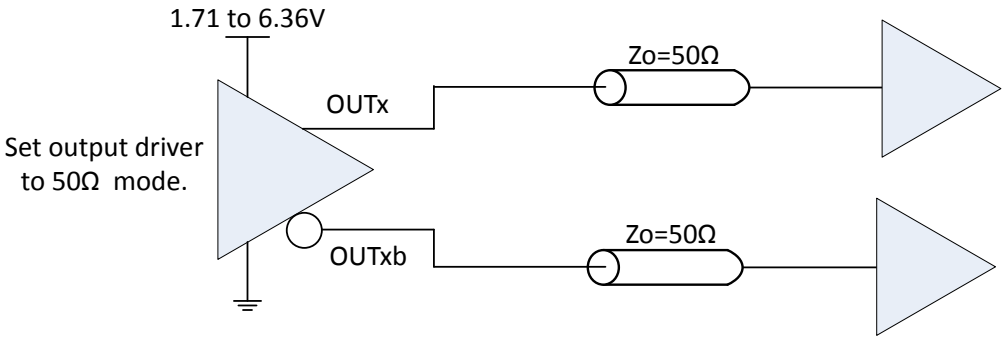


Figure 3.3. LVCMOS Output Termination Example, Option 1

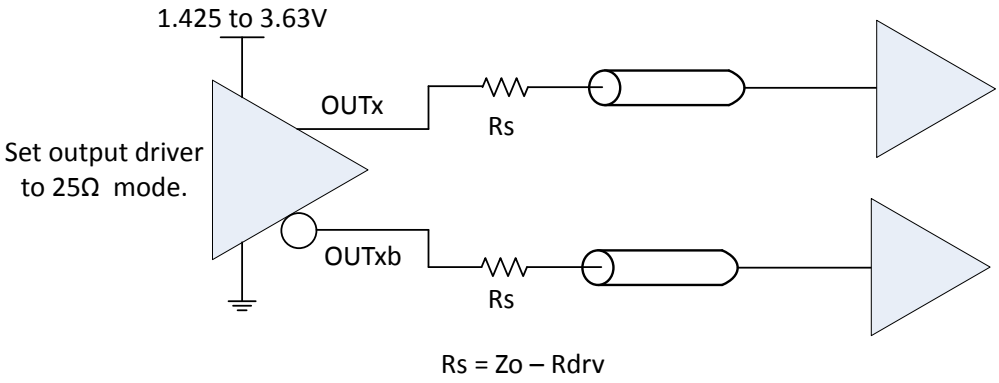


Figure 3.4. LVCMOS Output Termination Example, Option 2

3.5.2 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pin for the respective bank.

3.5.3 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTxb pin is generated with complimentary polarity with the clock on the OUTx pin. The polarity of these clocks is configurable enabling in phase clock generation and/or inverted polarity with respect to other output drivers.

3.5.4 Output Enable/Disable

The universal hardware input pins can be programmed to operate as output enable (OEb), controlling one or more outputs. Pin assignment is done using ClockBuilder Pro. An output enable pin provides a convenient method of disabling or enabling the output drivers. When the output enable pin is held high, all designated outputs will be disabled. When held low, the designated outputs will be enabled. Outputs in the enabled state can be individually disabled through register control.

3.5.5 Synchronous Output Disable Feature

Output clocks are always enabled and disabled synchronously. The output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output.

3.6 Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si5357 supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The Si5357 implements spread spectrum using its patented MultiSynth technology to achieve previously unattainable precision in both modulation rate and spreading magnitude. Spread spectrum can be enabled through I^2C, or by configuring one of the universal hardware input pins using ClockBuilder Pro.

The Si5357 features both center and down spread spectrum modulation capability, from 0.1% to 2.5%. Each MultiSynth is capable of generating an independent spread spectrum clock. The feature is enabled using a user-defined universal hardware input pin or via the device I^2C interface. Spread spectrum can be applied to any output clock derived from a MultiSynth fractional divider, supporting frequencies up to 170 MHz. Since the spread spectrum clock generation is performed in the MultiSynth fractional dividers, the spread spectrum waveform is highly consistent across process, voltage, and temperature. The Si5357 features two independent MultiSynth dividers, enabling the device to provide two independent spread profiles simultaneously to the clock output banks.

3.7 Universal Hardware Input Pins

Universal hardware input pins are user configurable control input pins that can have one or more of the functions listed below assigned to them using ClockBuilder Pro.

If more hardware input pins are needed, the differential input pins can be alternatively configured as two universal hardware input pins. Contact Silicon Labs for further details. Universal hardware input pins can be utilized for the following functions:

Table 3.1. Universal Hardware Input Pins

Description	Function
SSEN_EN0	Spread spectrum enable on MultiSynth0 (N0).
SSEN_EN1	Spread spectrum enable on MultiSynth0 (N1).
FS_INTx	Used to switch an integer output divider frequency from frequency A to frequency B.
FS_MSx	Used to switch a MultiSynth output divider output from frequency and/or change spread spectrum profile.
OE	Output enable for one or more outputs.
I2C address select	Sets the LSB of the I2C address to either 0 or 1.
CLKIN_SEL[1:0]	Selects between crystal or clock inputs.

Spread Spectrum Enable Pins (SSEN[1:0])

SSEN_EN[1:0] pins are active pins that enable/disable spread spectrum on all outputs that correspond to MutliSynth0 or MultiSynth1, respectively. The change in frequency or spread spectrum will be instantaneous and may not be glitch free.

Table 3.2. SPREAD_EN Pin Selection Table

SSEN_ENx	Function
0	Spread Spectrum disabled on MultiSynthx
1	Spread Spectrum enabled on MultiSynthx

Output Frequency Select Pins

There are five integer dividers, one corresponding to each of the five output banks. Using ClockBuilder Pro, a universal hardware input pin can be assigned for each integer divider, providing the capability to select between two different pre-programmed divide values. Divider values of every integer from 8 to 255 are available in ClockBuilder Pro for each integer divider.

Table 3.3. F_{S_INT} Pin Selection Table

F_{S_INTx}	Output Frequency from INTx
0	Frequency A, as defined in ClockBuilder Pro
1	Frequency B, as defined in ClockBuilder Pro

Output Enable

A universal hardware input pin can be defined to control output enable of a differential output, a bank of differential outputs, or as a global output enable pin controlling all outputs. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take < 20 µs for the output to have a clean clock.

Output enabled/disabled for LVCMOS are done in pairs. Each differential buffer True and Compliment output can generate an LVCMOS clock and the OE pin associated with the True and Compliment output buffer will control the respective LVCMOS pair.

For example: If DIFF0 is configured to be SE1 and DIFF0# is configured to be SE2 and OE1 is the associated OE pin, de-asserting the OE1 pin will disable both SE1 and SE2 outputs. The disable and enable of the outputs to a known state is glitch free.

I^2C Address Pin

The AI2C can be assigned as a universal hardware input pin as an I^2C address select function.

CLKIN_SEL[0:1] Pins

These pins are used to set the input source clock between the input clock channels (Crystal, CLK2/CLK#). Upon switching the input clock source, the output will not be glitch free. It is intended for the user to set this pin to a known state before the system is powered up or have the receiver address any unintended output signals when switching to a different input source clock.

3.8 Custom Factory Pre-programmed Parts

Custom pre-programmed parts can be ordered corresponding to a specific configuration file generated using the ClockBuilder Pro software utility. Silicon Labs writes the configuration file prior to shipping. Use the ClockBuilder Pro custom part number wizard (http://www.silabs.com/clockbuilderpro) to quickly and easily request and generate a custom part number for your ClockBuilder Pro configuration file. A factory pre-programmed part will generate clocks at power-up.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Silicon Labs sales representative. Samples of your pre-programmed device will ship within two weeks.

3.9 I^2C Serial Interface

The Si5357 is fully compatible with rev6 of the I^2C specification, including Standard, Fast, and Fast+ modes. Configuration and operation of the Si5357 can be controlled by reading and writing registers using the I^2C . Communication with a 1.8 V to 3.3 V host is supported. See the *Si5357 Family Reference Manual* for details.

3.10 In-Circuit Programming

The Si5332 is in-system configurable using the I^2C interface by the following two methods:

- *In-ciruit configuration of device registers after power-up.* With this method changes to volatile register memory can be done as required to produce the desired outputs. This does not alter internal NVM; therefore, register memory changes are lost at power-down. Refer to the *Si5332 Family Reference Manual* available on our web site for details.
- *In-circuit re-configuration of internal NVM.* Writing to internal NVM requires use of the CBPro Field Programmer (CBPROG-DONGLE) and CBPro software. See *UG286: ClockBuilderPro Field Programmer Kit* user's guide available on our web site for more information. (One important note: The Si5332 core VDDs (VDD_DIG, VDDA, and VDD_XTAL) must be powered by 3.3V during in-circuit NVM programming.)

4. Register Map

Refer to the *Si5357 Family Reference Manual* for a complete list of registers descriptions and settings.

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Ambient Temperature	T_A		–40	25	85	°C
Junction Temperature	TJ_{MAX}		—	—	125	°C
Core Supply Voltage	VDDA, VDD_DIG, VDD-xtal		1.71	—	3.63	V
Output Driver Supply Voltage	V_{DDO}		1.425	—	3.63	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 5.2. DC Characteristics

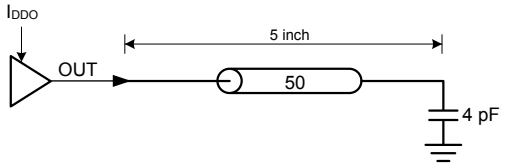
(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Core Supply Current	I_{DD}			—	45	70	mA
Output Buffer Supply Current	I_{DDOx}	3.3 V VDDO LVCMOS[1] output @ 170 MHz		—	16	19	mA
		2.5 V VDDO LVCMOS[1] output @ 170 MHz		—	9	11	mA
		1.8 VDDO LVCMOS[1] output @ 170 MHz		—	7.5	8.5	mA
Total Power Dissipation	P_d	32-pin	Note 1		270	—	mW

Notes:

1. LVCMOS outputs measured into a 5 inch 50 Ω PCB trace with 4 pF load.

LVCMOS Output Test Configuration



2. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available.

Table 5.3. Clock Input Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Clock (AC-coupled Differential Input Clock on CLKIN_2/CLKIN_2#)						
Frequency	F_{IN}	Differential	10	—	250	MHz
Voltage Swing	V_{PP}	Differential AC-coupled < 170 MHz	0.5	—	1.8	V_{PP_diff}
Slew Rate	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Impedance	R_{IN}		10	—	—	kΩ
Input Capacitance	C_{IN}		2	3.5	6	pF
Input Clock (DC-coupled LVCMOS Input Clock on CLKIN_2)						
Frequency	F_{IN}		10	—	170	MHz
Input High Voltage	V_{IH}		0.8 × V_{DD}	—	—	V
Input Low Voltage	V_{IL}		—	—	0.2 × V_{DD}	V
Slew Rate[1,2]	SR/SF	20-80%	0.75	—	—	V/ns
Duty Cycle	DC		40	—	60	%
Input Capacitance	C_{IN}		2	3.5	6	pF

Notes:

1. Imposed for jitter performance.
2. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20}$ = ((0.8 - 0.2) * $V_{IN\_Vpp\_se}$) / SR.

Table 5.4. External Crystal Input Specification

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTAL} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	F_{xtal}			16-50		MHz
Load Capacitance	C_L	16 - 30 MHz	6	12	18	pF
		31 - 50 MHz			10	pF
Shunt Capacitance	C_O	16 - 30 MHz	—	—	7	pF
		31 - 50 MHz	—	—	2	pF
ESR	C_L	16 - 30 MHz	—	—	50	Ω
		31 - 50 MHz	—	—	50	Ω
Max Crystal Drive Level	d_L		250	—	—	µW
Input Capacitance [1]	C_{IN}	Internal cap disabled	—	2.5	—	pF
		Internal cap enabled (per pad)	3	—	29	pF
Input Voltage	V_{XIN}		-0.3	—	1.3	V

Notes:
1. Internal capacitance on the xtal input pads is programmable or can be disabled.

Table 5.5. Control Pins

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTA} = 1.8 V to 3.3 V +10%/-5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Si5357 Control Input Pins (Inputx)						
Input Voltage	V_{IL}		-0.1	—	0.3 × VDD[1]	V
	V_{IH}		0.7 × V_{DD}	—	1.1 × V_{DD}	V
Input Capacitance	C_{IN}		—	—	4	pF
Pull-up/down Resistance	R_{IN}		—	50	—	kΩ

Note:
1. VDD indicates all core voltages VDD_DIG, VDDA, and VDD_XTAL which are required to all be using the same nominal voltage.

Table 5.6. LVCMOS Clock Output Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTA} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency	fout	1.8-3.3 V CMOS	5	—	170	MHz
		1.5 V CMOS	5	—	133.33	MHz
Rise/Fall Time, 3.3 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace, CL = 4 pf	—	0.5	0.8	ns
Rise/Fall Time, 2.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.6	0.95	ns
Rise/Fall Time, 1.8 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.75	1.3	ns
Rise/Fall Time, 1.5 V (20-80%)	t_R/t_F	50 Ω impedance, 5” trace CL = 4 pf	—	0.9	1.3	ns
CMOS Output Resistance (Single Strength)		3.3 V	—	46	—	Ω
		2.5 V	—	48	—	Ω
		1.8 V	—	53	—	Ω
		1.5 V	—	58	—	Ω
CMOS Output Resistance (Double Strength)		3.3 V	—	23	—	Ω
		2.5 V	—	24	—	Ω
		1.8 V	—	27	—	Ω
		1.5 V	—	29	—	Ω
CMOS Output Voltage	V_{OH}	–4 mA load	VDDO-0.3	—	—	V
	V_{OL}	4 mA load	—	—	0.3	V
Duty Cycle	DC	XO and PLL mode	45	—	55	%

Table 5.7. Performance Characteristics

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTA} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Ramp	t_{VDD}	0 V to V_{DDmin}	0.1	—	10	ms
Initialization Time	$t_{initialization}$	Time for I^2C to become operational after core supply exceeds V_{DDmin}	—	—	15	ms
Clock Stabilization from Power-up	t_{STABLE}	Time for clock outputs to appear after POR	—	15	25	ms
Input to Output Propagation Delay	t_{PROP}	Buffer mode (PLL Bypass)	—	2.5	4	ns
Spread Spectrum PP Frequency Deviation	SSDEV		0.1	—	2.5	%
0.5% Spread Frequency Deviation	SSDEV	MultiSynth Output < 250 MHz	0.4	0.45	0.5	%
Spread Spectrum Modulation Rate	SSDEV	MultiSynth Output < 250 MHz	30	31.5	33	kHz

Notes:

1. Outputs at same frequencies and using the same driver format.
2. The maximum step size is only limited by the register lengths; however, the MultiSynth output frequency must be kept between 5 MHz and 170 MHz.
3. Update rate via I2C is also limited by the time it takes to perform a write operation.
4. Default value is ~31.5 kHz.

Table 5.8. Jitter Performance Specifications

(V_{DD} = V_{DDA} = V_{DD_DIG} = V_{DD_XTA} = 1.8 V to 3.3 V +10%/-5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Typ	Max	Units
Jitter Generation, Locked to External 25 MHz Clock	J_{PER}	N = 10, 000 cycles Integer or Fractional Mode. [1,2] Measured in the time domain. Performance is limited by the noise floor of the equipment.	12		ps Pk-Pk
	J_{CC}		11		ps Pk
Jitter Generation, Locked to External 25 MHz Crystal	J_{PER}	N = 10, 000 cycles Integer or Fractional Mode. [1,2] Measured in the time domain. Performance is limited by the noise floor of the equipment.	12		ps Pk-Pk
	J_{CC}		11		ps Pk
Power Supply Noise Rejection[3]	PSNR	25 kHz	–67	—	dBc
		50 kHz	–66	—	
		100 kHz	–69	—	
		500 kHz	–73	—	
		1 MHz	–72	—	

Notes:
1. Integer mode assumes that the output dividers (Nn/Nd) are configured with an integer value.
2. Fractional and DCO modes assume that the output dividers (Nn/Nd) are configured with a fractional value and the feedback divider is integer.
3. Measured at 156.25 MHz carrier frequency. 100 mVpp sine wave noise added and noise spur amplitude measured.

Table 5.9. Thermal Characteristics

Parameter	Symbol	Test Condition[1]	Value	Units
Si5357 — 32 QFN				
Thermal Resistance, Junction to Ambient	θ_{JA}	Still Air	32.8	°C/W
		Air Flow 1 m/s	28.8	
		Air Flow 2 m/s	27.6	
Thermal Resistance, Junction to Case	θ_{JC}		18.5	
Thermal Resistance, Junction to Board	θ_{JB}		15.1	
	Ψ_{JB}		14.9	
Thermal Resistance, Junction to Top Center	Ψ_{JT}		0.5	

Note:
1. Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GND pad: 36, Number of Cu Layers: 4.

Table 5.10. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T_{STG}		–55 to +150	°C
DC Supply Voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	VDD_{xtal}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
Input Voltage Range	V_I	XIN/XOUT	–0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 125	°C
Soldering Temperature (Pb-free profile)	T_{PEAK}		260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)	T_P		20 to 40	sec

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
3. The device is compliant with JEDEC J-STD-020.

6. Pin Descriptions

6.1 Pin Descriptions (32-QFN)

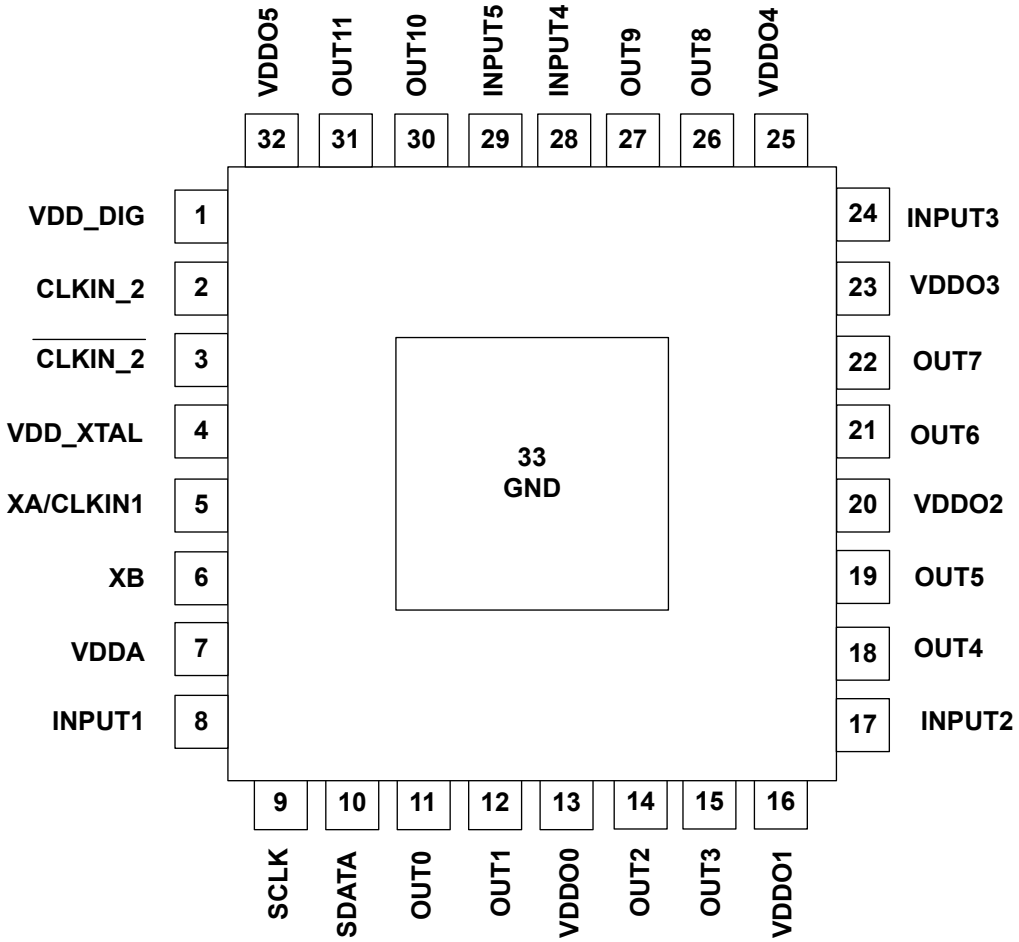


Figure 6.1. 32-QFN

Table 6.1. Si5357 Pin Descriptions, (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	P	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_XTAL.
2	CLKIN_2	I	These pins accept both differential and single-ended clock signals. Refer to Section 3.4.2 Input Clocks for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
3	CLKIN_2b	I	
4	VDD_XTAL	P	Voltage supply for crystal oscillator. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.

Pin Number	Pin Name	Pin Type	Function
5	XA/CLK1IN	I	These pins are used for an optional XTAL input when operating the device in free-run mode.
6	XB	O or P	
7	VDDA	P	Core Supply Voltage. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDD_XTAL and VDD_DIG. See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Must be connected to same voltage as VDD_DIG and VDD_XTAL.
8	INPUT1	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
9	SCLK	I	**Serial Clock Input** SCLK is a digital input internally referenced to VDD_DIG. SCLK must have an external pull-up resistor (I^2C bus pull-up) to same voltage as VDD_DIG. This pin functions as the serial clock input for I^2C.
10	SDATA	I/O	**Serial Data Interface** SDA is a digital open-drain bi-directional internally referenced to VDD_DIG. SDA must have an external pull-up resistor (I^2C bus pull-up) to same voltage as VDD_DIG. This is the bidirectional data pin (SDATA) for the I^2C mode.
11	OUT0	O	**LVCMOS Clock Outputs** Termination recommendations are provided in 3.5.1 LVCMOS Output Terminations. Unused outputs should be left unconnected.
12	OUT1	O	
13	VDDO0	P	**Supply Voltage (1.8–3.3 V or 1.5 V) for OUT0 or OUT1** See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT2	O	**LVCMOS Clock Outputs** Termination recommendations are provided in 3.5.1 LVCMOS Output Terminations. Unused outputs should be left unconnected.
15	OUT3	O	
16	VDDO1	P	**Supply Voltage (1.8–3.3 V or 1.5 V) for OUT2 and OUT3** See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	INPUT2	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
18	OUT4	O	**LVCMOS Clock Outputs** Termination recommendations are provided in 3.5.1 LVCMOS Output Terminations. Unused outputs should be left unconnected.
19	OUT5	O	

Pin Number	Pin Name	Pin Type	Function
20	VDDO2	P	**Supply Voltage (1.8–3.3 V or 1.5 V) for OUT4 and OUT5** See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
21	OUT6	O	**LVCMOS Clock Outputs** Termination recommendations are provided in 3.5.1 LVCMOS Output Terminations. Unused outputs should be left unconnected.
22	OUT7	O	
23	VDDO3	P	**Supply Voltage (1.8–3.3 V or 1.5 V) for OUT6 and OUT7** See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
24	INPUT3	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
25	VDDO4	P	**Supply Voltage (1.8–3.3 V or 1.5 V) for OUT8 and OUT9** See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT8	O	**LVCMOS Clock Outputs** Termination recommendations are provided in 3.5.1 LVCMOS Output Terminations. Unused outputs should be left unconnected.
27	OUT9	O	
28	INPUT4	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
29	INPUT5	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.7 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
30	OUT10	O	**LVCMOS Clock Outputs** Termination recommendations are provided in 3.5.1 LVCMOS Output Terminations. Unused outputs should be left unconnected.
31	OUT11	O	
32	VDDO5	P	**Supply Voltage (1.8–3.3 V or 1.5 V) for OUT10 and OUT11** See the *Si5357 Family Reference Manual* for power supply filtering recommendations. Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
33	GND PAD	P	**Ground Pad** This pad provides electrical and thermal connection to ground and must be connected for proper operation.

7. Package Outline

7.1 Si5357 5x5 mm 32-QFN Package Diagram

The figure below illustrates the package details for the Si5357 32-QFN option. The table below lists the values for the dimensions shown in the illustration.

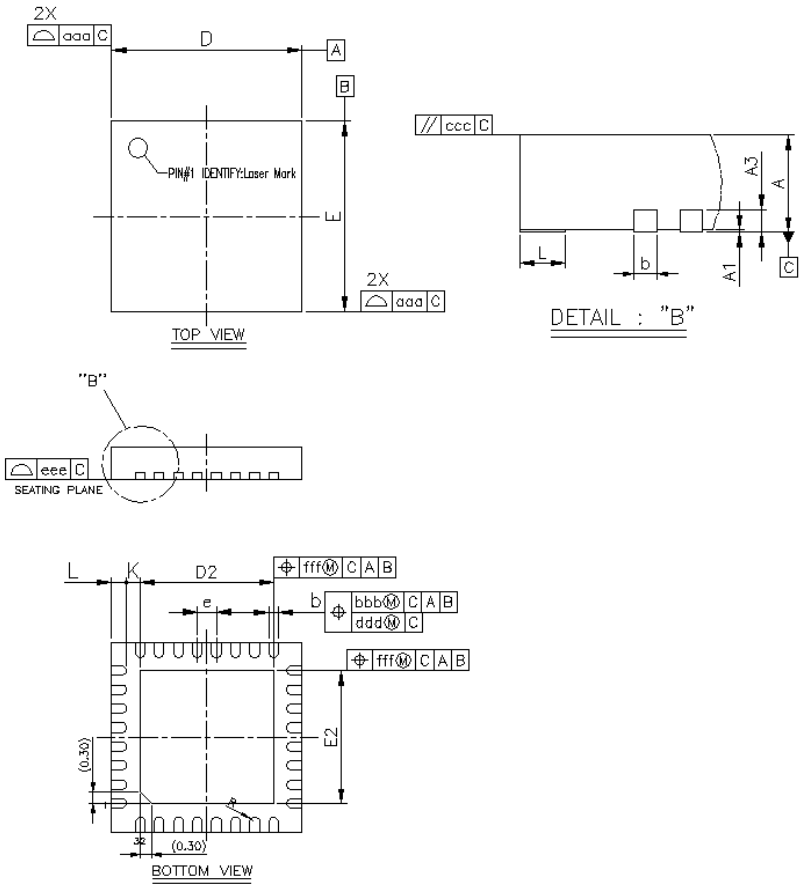


Figure 7.1. 32-Pin Quad Flat No-Lead (QFN)

Table 7.1. Package Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
E		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	---	---
R	0.09	---	0.14
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the Si5357 in the 32-QFN package. The table below lists the values for the dimensions shown in the illustration.

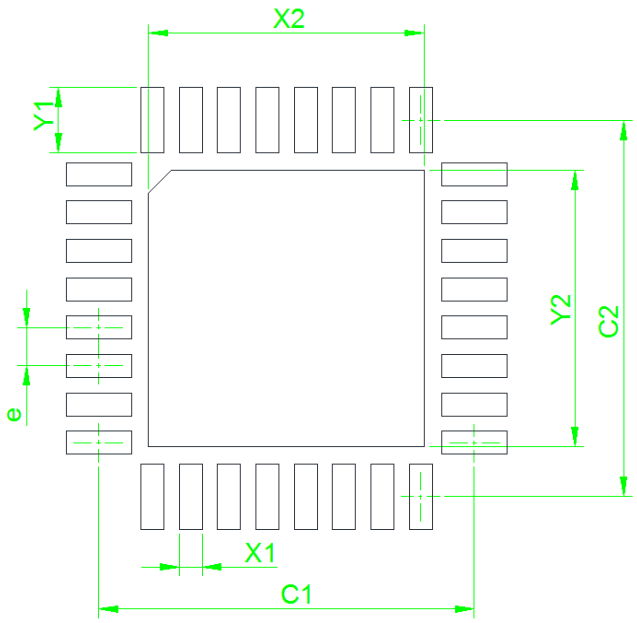


Figure 8.1. PCB Land Pattern

Table 8.1. PCB Land Pattern Dimensions

Dimension	mm
C1	4.90
C2	4.90
e	0.50
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm

Notes:
General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
4. A 3x3 array of 0.85mm square openings on a 1.00mm pitch can be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Top Marking

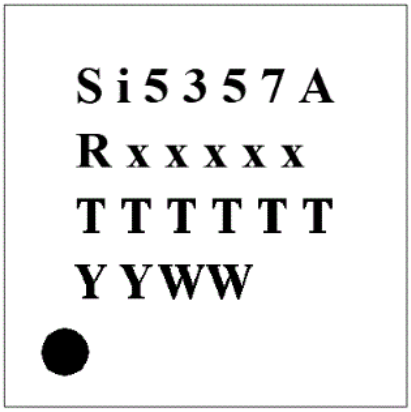


Figure 9.1. Si5357 Top Marking

Table 9.1. Top Marking Explanation

Line	Characters	Description
1	Si5357g	Base part number and device grade g = Device Grade
2	Rxxxxx	R = Produce revision (see ordering guide for current revision) xxxxx = Customer specific NVM sequence number assigned by ClockBuilder Pro
3	TTTTTT	Manufacturing trace code.
4	YYWW	Year (YY) and work week (WW) of package assembly

10. Document Change List

Revision 1.0

August 2018

- Updated Si5332 5x5 mm 32-QFN package diagram for external crystal versions
- Updated Si5332 32-QFN land pattern
- Updated supply current and rise/fall time specifications

Revision 0.7

September 2017

- Initial release.

ClockBuilder Pro

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