X5328, X5329 (Replaces X25328, X25329)

CPU Supervisor with 32Kbit SPI EEPROM

FN8132
Rev 2.00
October 16, 2015

FEATURES

- **Low V_{CC} detection and reset assertion**
  - **Five standard reset threshold voltages**
  - **Re-program low V_{CC} reset threshold voltage using special programming sequence**
  - **Reset signal valid to V_{CC} = 1V**
- **Long battery life with low power consumption**
  - **<1µA max standby current**
  - **<400µA max active current during read**
- **32Kbits of EEPROM**
- **Built-in inadvertent write protection**
  - **Power-up/power-down protection circuitry**
  - **Protect 0, 1/4, 1/2 or all of EEPROM array with Block Lock™ protection**
  - **In circuit programmable ROM mode**
- **2MHz SPI interface modes (0,0 & 1,1)**
- **Minimize EEPROM programming time**
  - **32-byte page write mode**
  - **Self-timed write cycle**
  - **5ms write cycle time (typical)**
- **2.7V to 5.5V and 4.5V to 5.5V power supply operation**
- **Available packages**
  - **14 Ld TSSOP, 8 Ld SOIC, 8 Ld PDIP**
- **Pb-free plus anneal available (RoHS compliant)**

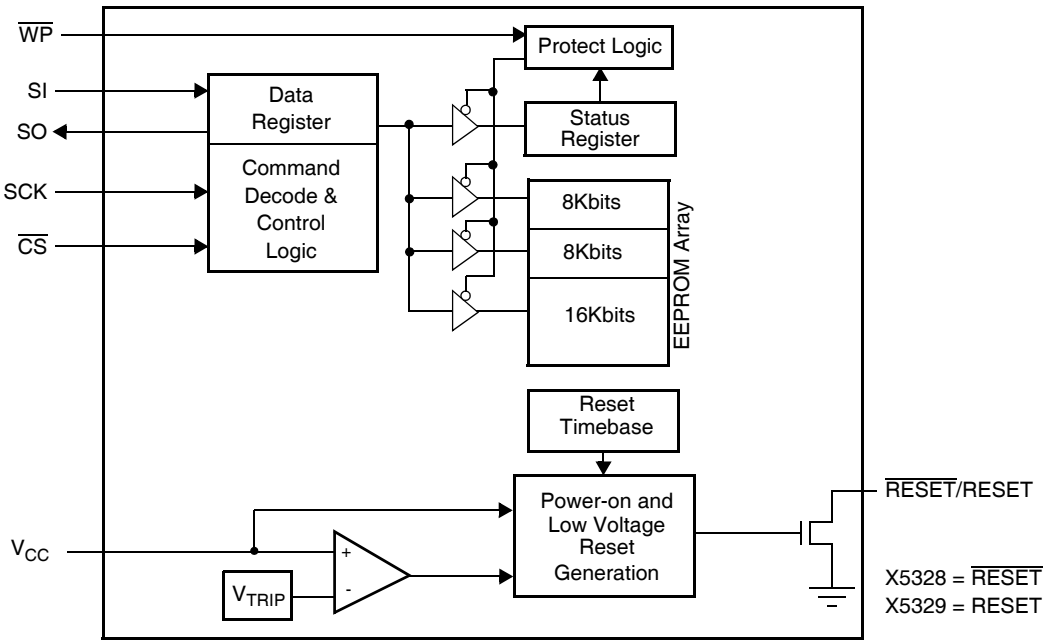
DESCRIPTION

These devices combine three popular functions, Power-on Reset Control, Supply Voltage Supervision, and Block Lock Protect Serial EEPROM Memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions by holding $\overline{\text{RESET}}$/RESET active when V_{CC} falls below a minimum V_{CC} trip point. $\overline{\text{RESET}}$/RESET remains asserted until V_{CC} returns to proper operating level and stabilizes. Five industry standard V_{TRIP} thresholds are available, however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold in applications requiring higher precision.

BLOCK DIAGRAM



Ordering Information

PART NUMBER	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
$\overline{\text{RESET}}$ ACTIVE LOW					
X5328PZ-4.5A (Note) **(No longer available, recommended replacement: X5328S8Z-4.5A)**	X5328P Z AL	4.5-5.5	4.5-4.75	0 to 70	8 Ld PDIP
X5328PIZ-4.5A (Note) **(No longer available, recommended replacement: X5328S8IZ-4.5A)**	X5328P Z AM			-40 to 85	8 Ld PDIP
X5328S8Z-4.5A (Note)	X5328 Z AL			0 to 70	8 Ld SOIC
X5328S8IZ-4.5A (Note)	X5328 Z AM			-40 to 85	8 Ld SOIC
X5328V14Z-4.5A (Note)	X5328V Z AL			0 to 70	14 Ld TSSOP
X5328PZ (Note) **(No longer available, recommended replacement: X5328S8Z)**	X5328P Z	4.5-5.5	4.25-4.5	0 to 70	8 Ld PDIP
X5328PIZ (Note) **(No longer available, recommended replacement: X5328S8IZ)**	X5328P Z I			-40 to 85	8 Ld PDIP
X5328S8Z* (Note)	X5328 Z			0 to 70	8 Ld SOIC
X5328S8IZ* (Note)	X5328 Z I			-40 to 85	8 Ld SOIC
X5328PZ-2.7A (Note) **(No longer available, recommended replacement: X5328S8Z-2.7A)**	X5328P Z AN	2.7-5.5	2.85-3.0	0 to 70	8 Ld PDIP
X5328PIZ-2.7A (Note) **(No longer available, recommended replacement: X5328S8IZ-2.7A)**	X5328P Z AP			-40 to 85	8 Ld PDIP
X5328S8Z-2.7A (Note)	X5328 Z AN			0 to 70	8 Ld SOIC
X5328S8IZ-2.7A (Note)	X5328 Z AP			-40 to 85	8 Ld SOIC
X5328PZ-2.7 (Note) **(No longer available, recommended replacement: X5328S8Z-2.7)**	X5328P Z F	2.7-5.5	2.55-2.7	0 to 70	8 Ld PDIP
X5328PIZ-2.7 (Note) **(No longer available, recommended replacement: X5328S8IZ-2.7)**	X5328P Z G			-40 to 85	8 Ld PDIP
X5328S8Z-2.7* (Note)	X5328 Z F			0 to 70	8 Ld SOIC
X5328S8IZ-2.7* (Note)	X5328 Z G			-40 to 85	8 Ld SOIC
RESET ACTIVE HIGH					
X5329S8Z-4.5A (Note)	X5329 Z AL	4.5-5.5	4.5-4.75	0 to 70	8 Ld SOIC
X5329S8IZ-4.5A (Note)	X5329 Z AM			-40 to 85	8 Ld SOIC
X5329V14Z-4.5A (Note)	X5329V Z AL			0 to 70	14 Ld TSSOP
X5329S8Z* (Note)	X5329 Z	4.5-5.5	4.25-4.5	0 to 70	8 Ld SOIC
X5329S8IZ* (Note)	X5329 Z I			-40 to 85	8 Ld SOIC
X5329S8Z-2.7A (Note)	X5329 Z AN	2.7-5.5	2.85-3.0	0 to 70	8 Ld SOIC
X5329S8IZ-2.7A (Note) **(No longer available, recommended replacement: X5329S8Z-2.7A)**	X5329 Z AP			-40 to 85	8 Ld SOIC
X5329S8Z-2.7* (Note)	X5329 Z F	2.7-5.5	2.55-2.7	0 to 70	8 Ld SOIC
X5329S8IZ-2.7* (Note) **(No longer available, recommended replacement: X5329S8Z-2.7)**	X5329 Z G			-40 to 85	8 Ld SOIC

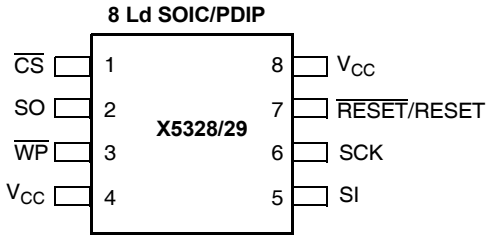
*Add “T1” suffix for tape and reel.

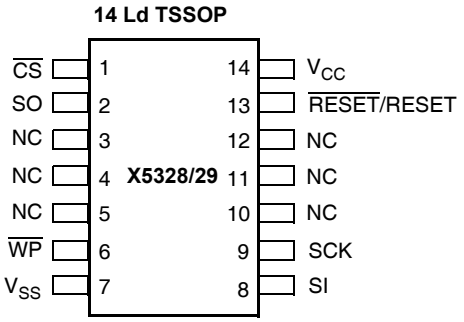
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN DESCRIPTION

Pin (SOIC/PDIP)	Pin TSSOP	Name	Function
1	1	$\overline{CS}$	**Chip Select Input.** $\overline{CS}$ HIGH, deselects the device and the SO output pin is at a high impedance state. Unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. Prior to the start of any operation after power-up, a HIGH to LOW transition on $\overline{CS}$ is required.
2	2	SO	**Serial Output.** SO is a push/pull serial data output pin. A read cycle shifts data out on this pin. The falling edge of the serial clock (SCK) clocks the data out.
5	8	SI	**Serial Input.** SI is a serial data input pin. Input all opcodes, byte addresses, and memory data on this pin. The rising edge of the serial clock (SCK) latches the input data. Send all opcodes (Table 1), addresses and data MSB first.
6	9	SCK	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output. The rising edge of SCK latches in the opcode, address, or data bits present on the SI pin. The falling edge of SCK changes the data output on the SO pin.
3	6	$\overline{WP}$	**Write Protect.** The $\overline{WP}$ pin works in conjunction with a nonvolatile WPEN bit to "lock" the setting of the Watchdog Timer control and the memory write protect bits.
4	7	V_{SS}	Ground
8	14	V_{CC}	Supply Voltage
7	13	$\overline{RESET}$/RESET	**Reset Output**. $\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 200ms. $\overline{RESET}$/RESET goes active on power-up at about 1V and remains active for 200ms after the power supply stabilizes.
	3-5,10-12	NC	No internal connections

PIN CONFIGURATION





PRINCIPLES OF OPERATION

Power-On Reset

Application of power to the X5328/X5329 activates a Power-on Reset Circuit. This circuit goes active at about 1V and pulls the $\overline{\text{RESET}}$/RESET pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When V_{CC} exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{\text{RESET}}$/RESET, allowing the processor to begin executing code.

Low Voltage Monitoring

During operation, the X5328/X5329 monitors the V_{CC} level and asserts $\overline{\text{RESET}}$/RESET if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{\text{RESET}}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{\text{RESET}}$/RESET signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

V_{CC} Threshold Reset Procedure

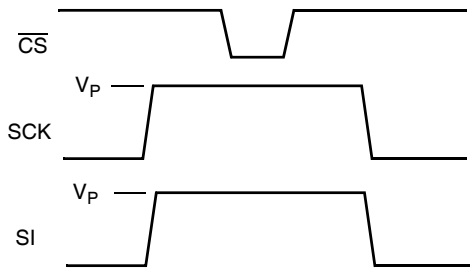
The X5328/X5329 has a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or for higher precision in the V_{TRIP} value, the X5328/X5329 threshold may be adjusted.

Setting the V_{TRIP} Voltage

This procedure sets the V_{TRIP} to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure directly makes the change. If the new setting is lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold to the V_{CC} pin and tie the $\overline{\text{CS}}$ pin and the $\overline{\text{WP}}$ pin HIGH. $\overline{\text{RESET}}$/RESET and SO pins are left unconnected. Then apply the programming voltage V_P to both SCK and SI and pulse $\overline{\text{CS}}$ LOW then HIGH. Remove V_P and the sequence is complete.

Figure 1. Set V_{TRIP} Voltage



Resetting the V_{TRIP} Voltage

This procedure sets the V_{TRIP} to a “native” voltage level. For example, if the current V_{TRIP} is 4.4V and the V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the V_{TRIP} voltage, apply a voltage between 2.7 and 5.5V to the V_{CC} pin. Tie the $\overline{\text{CS}}$ pin, the $\overline{\text{WP}}$ pin, and the SCK pin HIGH. $\overline{\text{RESET}}$/RESET and SO pins are left unconnected. Then apply the programming voltage V_P to the SI pin ONLY and pulse $\overline{\text{CS}}$ LOW then HIGH. Remove V_P and the sequence is complete.

Figure 2. Reset V_{TRIP} Voltage

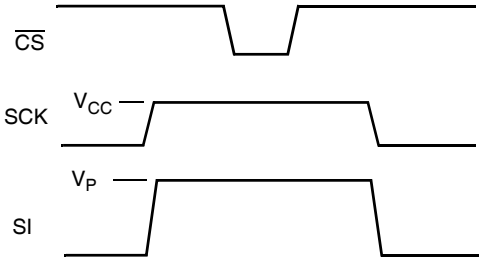


Figure 3. V_{TRIP} Programming Sequence Flow Chart

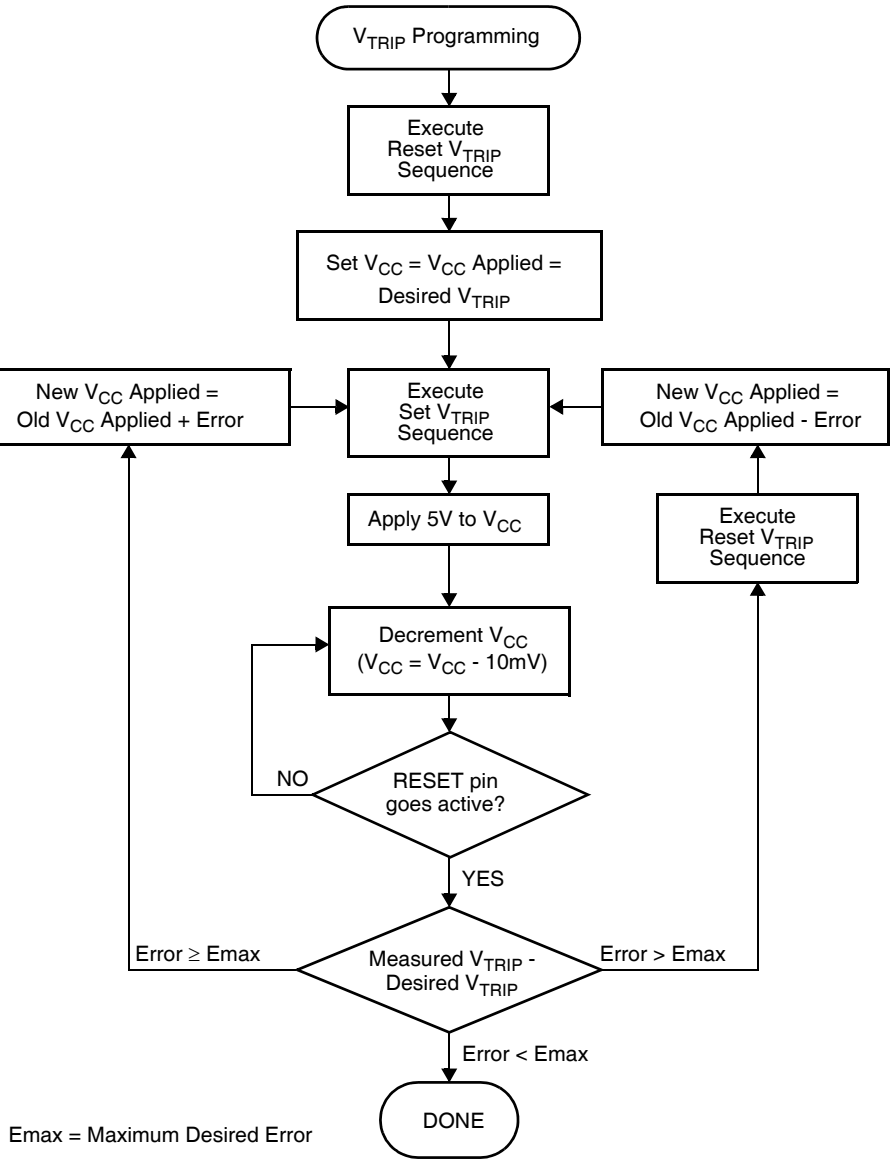
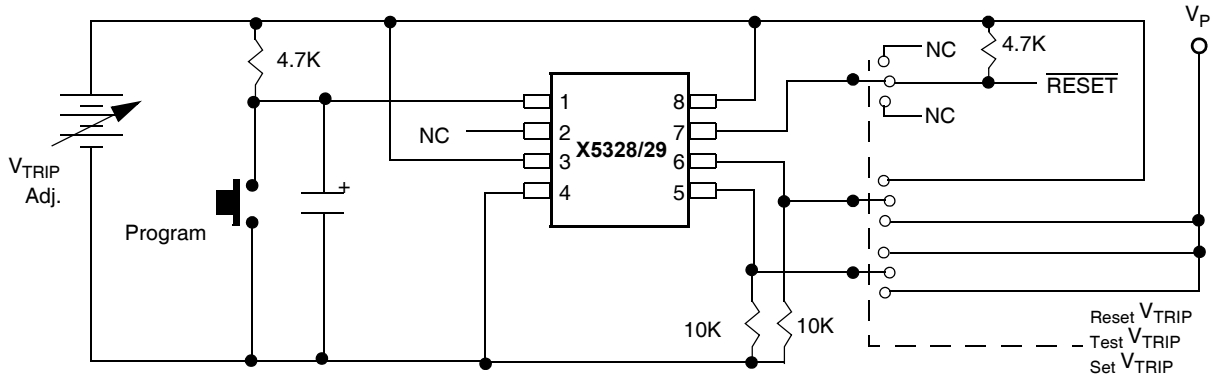


Figure 4. Sample V_{TRIP} Reset Circuit



SPI SERIAL MEMORY

The memory portion of the device is a CMOS Serial EEPROM array with Intersil's block lock protection. The array is internally organized as x 8. The device features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus.

The device utilizes Intersil's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families. It contains an 8-bit instruction register that is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW during the entire operation.

All instructions (Table 1), addresses and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The device contains a Write Enable Latch. This latch must be SET before a Write Operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 3). This latch is automatically reset upon a power-up condition and after the completion of a valid Write Cycle.

Status Register

The RDSR instruction provides access to the Status Register. The Status Register may be read at any time, even during a Write Cycle. The Status Register is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	FLB	1*	1*	BL1	BL0	WEL	WIP

*Bits (5,4) should be written as '1' only.

The Write-In-Progress (WIP) bit is a volatile, read only bit and indicates whether the device is busy with an internal nonvolatile write operation. The WIP bit is read using the RDSR instruction. When set to a "1", a nonvolatile write operation is in progress. When set to a "0", no write is in progress.

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
SFLB	0000 0000	Set Flag Bit
WRDI/RFLB	0000 0100	Reset the Write Enable Latch/Reset Flag Bit
RSDR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Lock, WPEN & Flag Bits)
READ	0000 0011	Read Data from Memory Array Beginning at Selected Address
WRITE	0000 0010	Write Data to Memory Array Beginning at Selected Address

Note: *Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

Table 2. Block Protect Matrix

WREN CMD	Status Register	Device Pin	Block	Block	Status Register
WEL	WPEN	WP#	Protected Block	Unprotected Block	WPEN, BL0, BL1, WD0, WD1
0	X	X	Protected	Protected	Protected
1	1	0	Protected	Writable	Protected
1	0	X	Protected	Writable	Writable
1	X	1	Protected	Writable	Writable

The Write Enable Latch (WEL) bit indicates the Status of the Write Enable Latch. When WEL = 1, the latch is set HIGH and when WEL = 0 the latch is reset LOW. The WEL bit is a volatile, read only bit. It can be set by the WREN instruction and can be reset by the WRDS instruction.

The block lock bits, BL0 and BL1, set the level of block lock protection. These nonvolatile bits are programmed using the WRSR instruction and allow the user to protect one quarter, one half, all or none of the EEPROM array. Any portion of the array that is block lock protected can be read but not written. It will remain protected until the BL bits are altered to disable block lock protection of that portion of memory.

Status Register Bits		Array Addresses Protected
BL1	**BL0**	**X5328/X5329**
0	0	None
0	1	$0C00-$0FFF
1	0	$0800-$0FFF
1	1	$0000-$0FFF

The FLAG bit shows the status of a volatile latch that can be set and reset by the system using the SFLB and RFLB instructions. The Flag bit is automatically reset upon power-up.

The nonvolatile WPEN bit is programmed using the WRSR instruction. This bit works in conjunction with the $\overline{WP}$ pin to provide an In-Circuit Programmable ROM function (Table 2). $\overline{WP}$ is LOW and WPEN bit programmed HIGH disables all Status Register Write Operations.

In Circuit Programmable ROM Mode

This mechanism protects the block lock and Watchdog bits from inadvertent corruption.

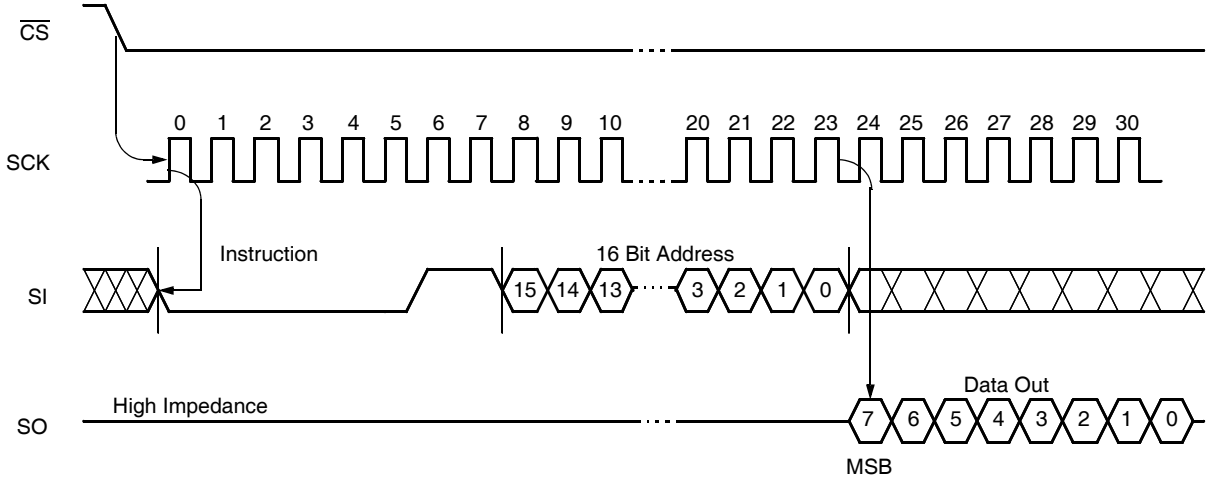
In the locked state (Programmable ROM Mode) the $\overline{WP}$ pin is LOW and the nonvolatile bit WPEN is “1”. This mode disables nonvolatile writes to the device’s Status Register.

Setting the $\overline{WP}$ pin LOW while WPEN is a “1” while an internal write cycle to the Status Register is in progress will not stop this write operation, but the operation disables subsequent write attempts to the Status Register.

When $\overline{WP}$ is HIGH, all functions, including nonvolatile writes to the Status Register operate normally.

Setting the WPEN bit in the Status Register to “0” blocks the $\overline{WP}$ pin function, allowing writes to the Status Register when $\overline{WP}$ is HIGH or LOW. Setting the WPEN bit to “1” while the $\overline{WP}$ pin is LOW activates the Programmable ROM mode, thus requiring a change in the $\overline{WP}$ pin prior to subsequent Status Register changes. This allows manufacturing to install the device in a system with $\overline{WP}$ pin grounded and still be able to program the Status Register. Manufacturing can then load Configuration data, manufacturing time and other parameters into the EEPROM, then set the portion of memory to be protected by setting the block lock bits, and finally set the “OTP mode” by setting the WPEN bit. Data changes now require a hardware change.

Figure 5. Read EEPROM Array Sequence



Read Sequence

When reading from the EEPROM memory array, $\overline{CS}$ is first pulled low to select the device. The 8-bit READ instruction is transmitted to the device, followed by the 16-bit address. After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address $0000 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the Read EEPROM Array Sequence (Figure 1).

To read the Status Register, the $\overline{CS}$ line is first pulled low to select the device followed by the 8-bit RDSR instruction. After the RDSR opcode is sent, the contents of the Status Register are shifted out on the SO line. Refer to the Read Status Register Sequence (Figure 2).

Write Sequence

Prior to any attempt to write data into the device, the “Write Enable” Latch (WEL) must first be set by issuing the WREN instruction (Figure 3). $\overline{CS}$ is first taken LOW, then the WREN instruction is clocked into the device. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the Write Operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the Write Operation will be ignored.

To write data to the EEPROM memory array, the user then issues the WRITE instruction followed by the 16-bit address and then the data to be written. Any unused address bits are specified to be “0’s”. The WRITE operation minimally takes 32 clocks. $\overline{CS}$ must go low and remain low for the duration of the operation. If the address counter reaches the end of a page and the clock continues, the counter will roll back to the first address of the page and overwrite any data that may have been previously written.

For the Page Write Operation (byte or page write) to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed (Figure 4).

To write to the Status Register, the WRSR instruction is followed by the data to be written (Figure 5). Data bits 0 and 1 must be “0”.

While the write is in progress following a Status Register or EEPROM Sequence, the Status Register may be read to check the WIP bit. During this time the WIP bit will be high.

OPERATIONAL NOTES

The device powers-up in the following state:

– The device is in the low power standby state.
– A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
– SO pin is high impedance.
– The Write Enable Latch is reset.
– The Flag Bit is reset.
– Reset Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

– A WREN instruction must be issued to set the Write Enable Latch.
– $\overline{CS}$ must come HIGH at the proper clock count in order to start a nonvolatile write cycle.

Figure 6. Read Status Register Sequence

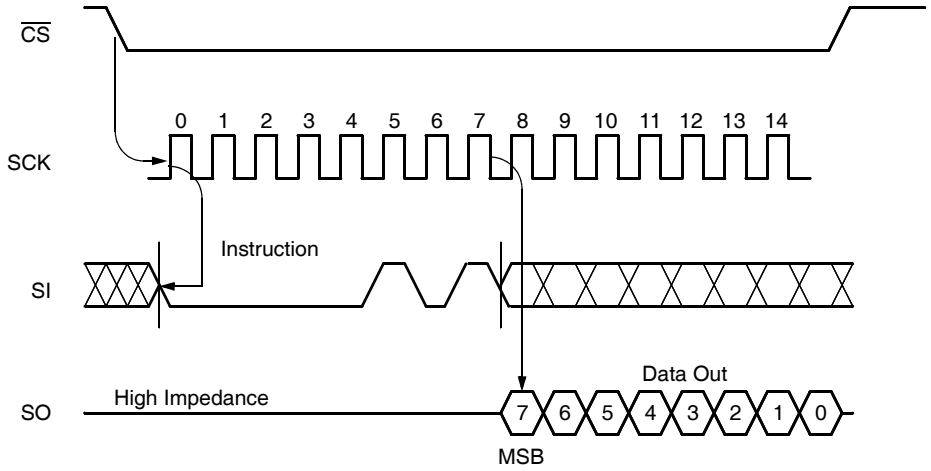


Figure 7. Write Enable Latch Sequence

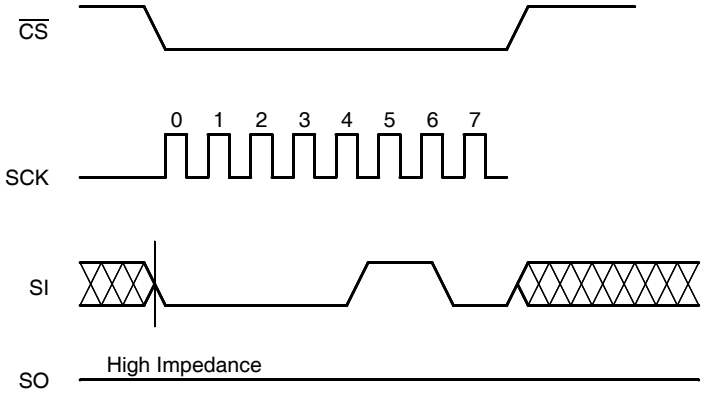


Figure 8. Write Sequence

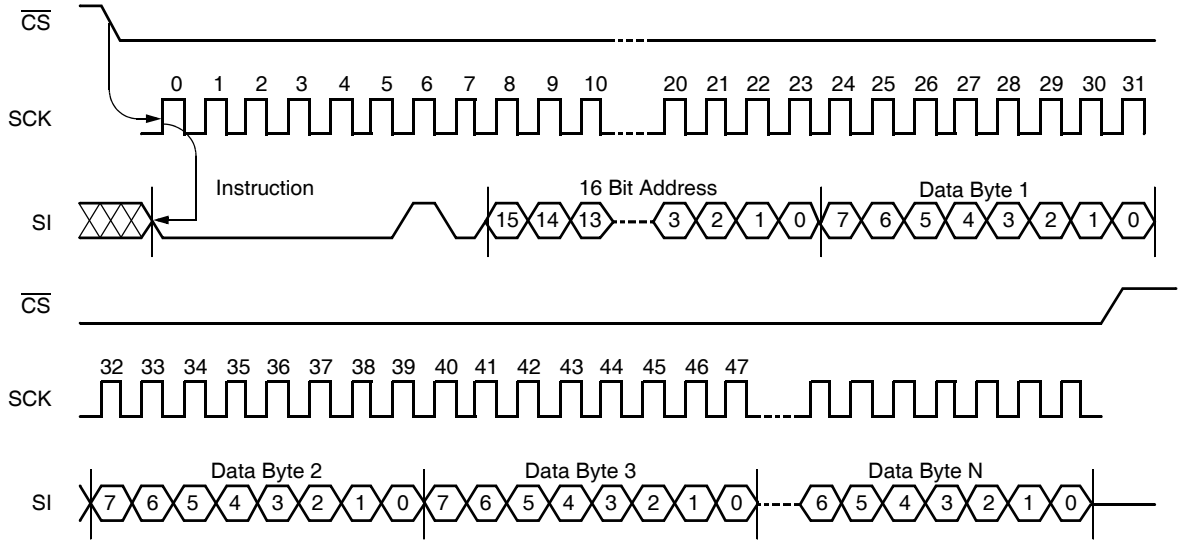
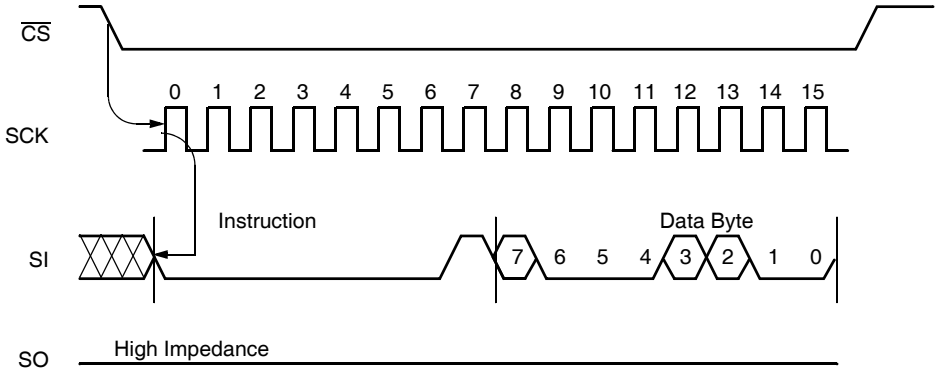


Figure 9. Status Register Write Sequence



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10s) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

Voltage Option	Supply Voltage
-2.7 or -2.7A	2.7V to 5.5V
BLank or -4.5A	4.5V-5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

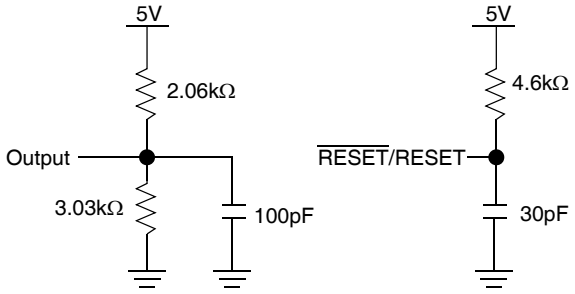
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	V_{CC} Write Current (Active)			5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open
I_{CC2}	V_{CC} Read Current (Active)			0.4	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 2MHz, SO = Open
I_{SB}	V_{CC} Standby Current			1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	-0.5		V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage			0.4	V	V_{CC} > 3.3V, I_{OL} = 2.1mA
V_{OL2}	Output LOW Voltage			0.4	V	2V < V_{CC} ≤ 3.3V, I_{OL} = 1mA
V_{OL3}	Output LOW Voltage			0.4	V	V_{CC} ≤ 2V, I_{OL} = 0.5mA
V_{OH1}	Output HIGH Voltage	V_{CC} - 0.8			V	V_{CC} > 3.3V, I_{OH} = -1.0mA
V_{OH2}	Output HIGH Voltage	V_{CC} - 0.4			V	2V < V_{CC} ≤ 3.3V, I_{OH} = -0.4mA
V_{OH3}	Output HIGH Voltage	V_{CC} - 0.2			V	V_{CC} ≤ 2V, I_{OH} = -0.25mA
V_{OLS}	Reset Output LOW Voltage			0.4	V	I_{OL} = 1mA

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
C_{OUT}(2)	Output Capacitance (SO, $\overline{RESET}$, RESET)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

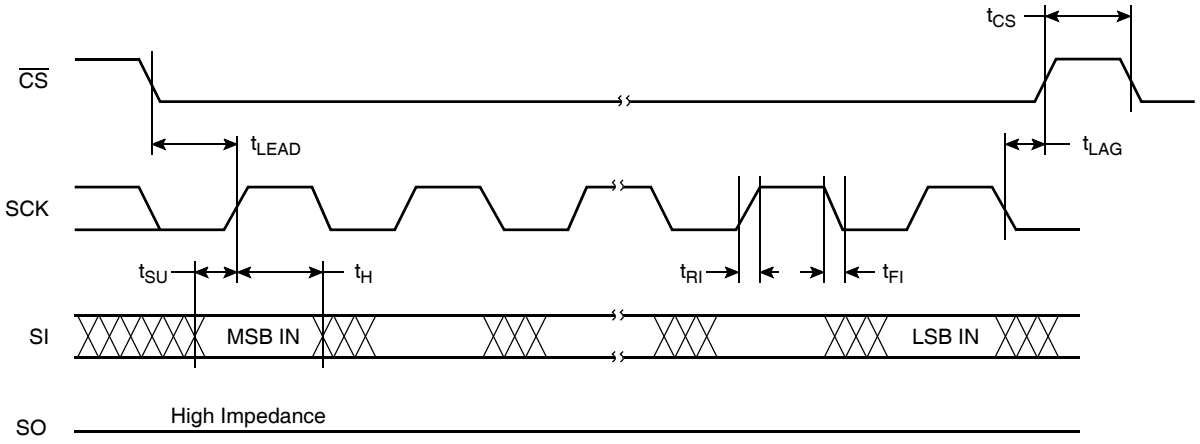
Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x0.5

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Serial Input Timing

Symbol	Parameter	2.7-5.5V		Unit
		Min.	Max.	
f_{SCK}	Clock Frequency	0	2	MHz
t_{CYC}	Cycle Time	500		ns
t_{LEAD}	$\overline{CS}$ Lead Time	250		ns
t_{LAG}	$\overline{CS}$ Lag Time	250		ns
t_{WH}	Clock HIGH Time	200		ns
t_{WL}	Clock LOW Time	250		ns
t_{SU}	Data Setup Time	50		ns
t_H	Data Hold Time	50		ns
t_{RI}(3)	Input Rise Time		100	ns
t_{FI}(3)	Input Fall Time		100	ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(4)	Write Cycle Time		10	ms

Serial Input Timing

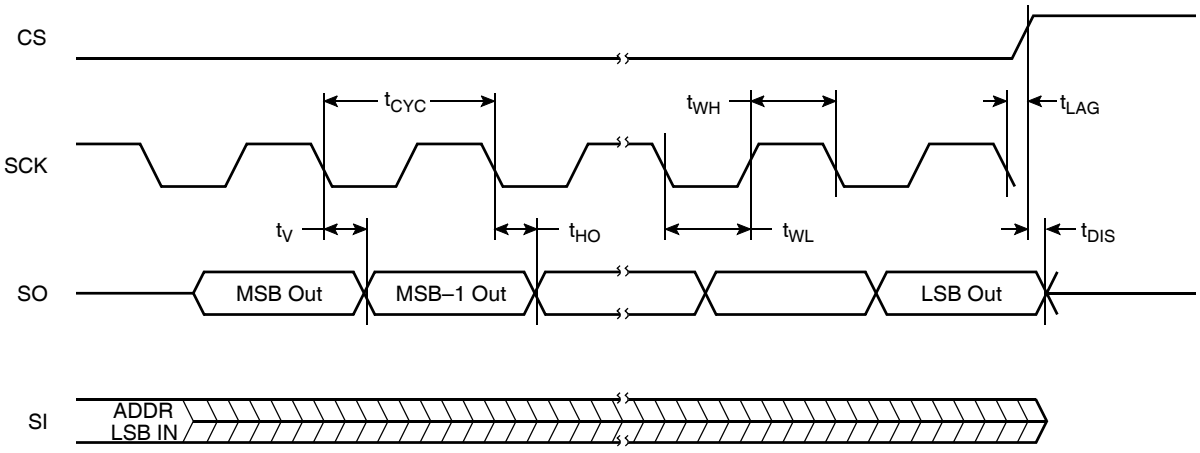


Serial Output Timing

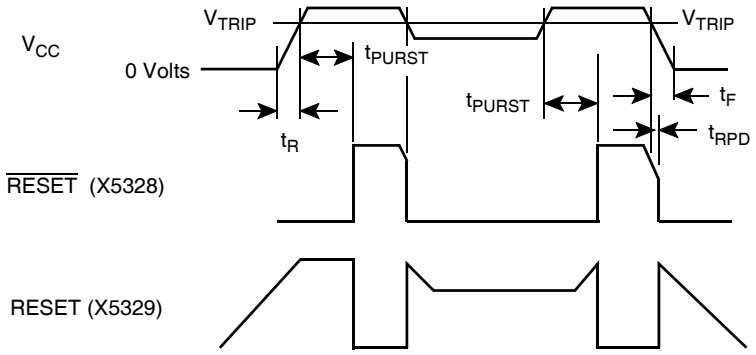
Symbol	Parameter	2.7-5.5V		Unit
		Min.	Max.	
f_{SCK}	Clock Frequency	0	2	MHz
t_{DIS}	Output Disable Time		250	ns
t_V	Output Valid from Clock Low		250	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(3)	Output Rise Time		100	ns
t_{FO}(3)	Output Fall Time		100	ns

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Serial Output Timing



Power-Up and Power-Down Timing

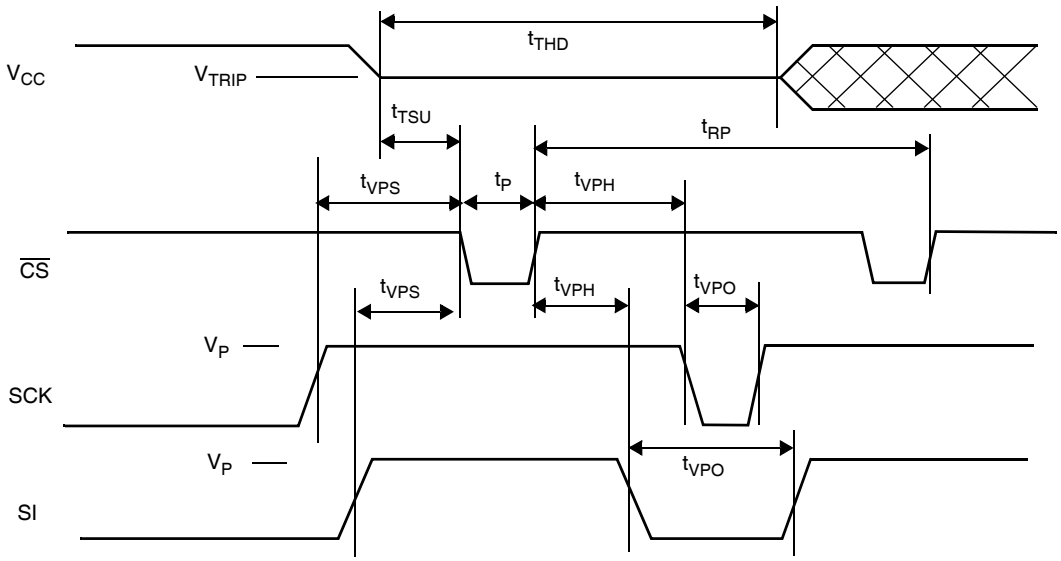


$\overline{RESET}$ Output Timing

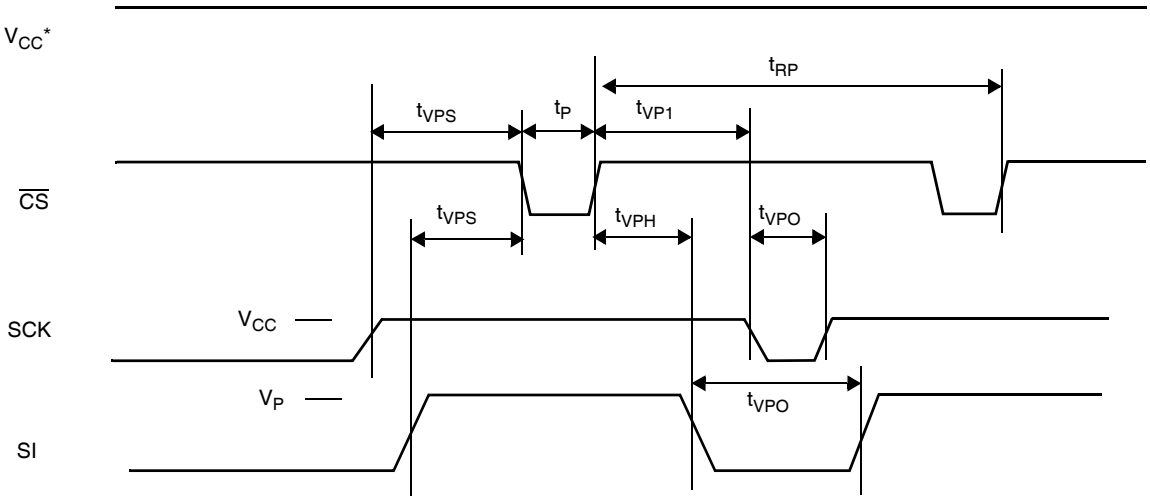
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset Trip Point Voltage, X5328-4.5A, X5328-4.5A Reset Trip Point Voltage, X5328, X5329 Reset Trip Point Voltage, X5328-2.7A, X5329-2.7A Reset Trip Point Voltage, X5328-2.7, X5329-2.7	4.5 4.25 2.85 2.55	4.63 4.38 2.93 2.63	4.75 4.5 3.0 2.7	V
V_{TH}	V_{TRIP} Hysteresis (HIGH to LOW vs. LOW to HIGH V_{TRIP} voltage)		20		mV
t_{PURST}	Power-up Reset Time Out	100	200	280	ms
t_{RPD}(5)	V_{CC} Detect to Reset/Output			500	ns
t_F(5)	V_{CC} Fall Time	100			µs
t_R(5)	V_{CC} Rise Time	100			µs
V_{RVALID}	Reset Valid V_{CC}	1			V

Note: (5) This parameter is periodically sampled and not 100% tested.

V_{TRIP} Set Conditions



V_{TRIP} Reset Conditions



*V_{CC} > Programmed V_{TRIP}

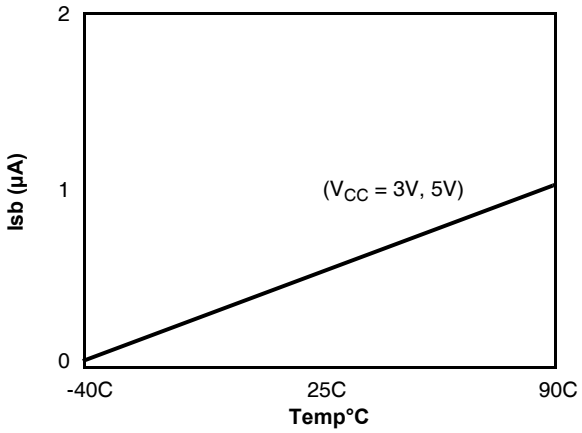
V_{TRIP} Programming Specifications V_{CC} = 1.7-5.5V; Temperature = 0°C to 70°C

Parameter	Description	Min.	Max.	Unit
t_{VPS}	SCK V_{TRIP} Program Voltage Setup time	1		µs
t_{VPH}	SCK V_{TRIP} Program Voltage Hold time	1		µs
t_P	V_{TRIP} Program Pulse Width	1		µs
t_{TSU}	V_{TRIP} Level Setup time	10		µs
t_{THD}	V_{TRIP} Level Hold (stable) time	10		ms
t_{WC}	V_{TRIP} Write Cycle Time		10	ms
t_{RP}	V_{TRIP} Program Cycle Recovery Period (Between successive programming cycles)	10		ms
t_{VPO}	SCK V_{TRIP} Program Voltage Off time before next cycle	0		ms
V_P	Programming Voltage	15	18	V
V_{TRAN}	V_{TRIP} Programed Voltage Range	1.7	5.0	V
V_{ta1}	Initial V_{TRIP} Program Voltage accuracy (V_{CC} applied-V_{TRIP}) (Programmed at 25°C.)	-0.1	+0.4	V
V_{ta2}	Subsequent V_{TRIP} Program Voltage accuracy [(V_{CC} applied-V_{ta1})-V_{TRIP}] (Programmed at 25°C.)	-25	+25	mV
V_{tr}	V_{TRIP} Program Voltage repeatability (Successive program operations.) (programmed at 25°C)	-25	+25	mV
V_{tv}	V_{TRIP} Program variation after programming (0-75°C). (programmed at 25°C)	-25	+25	mV

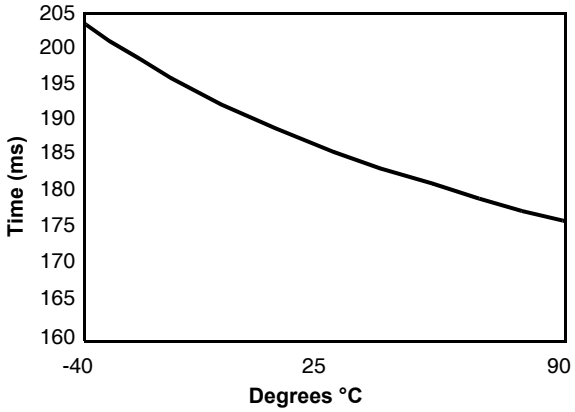
V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

TYPICAL PERFORMANCE

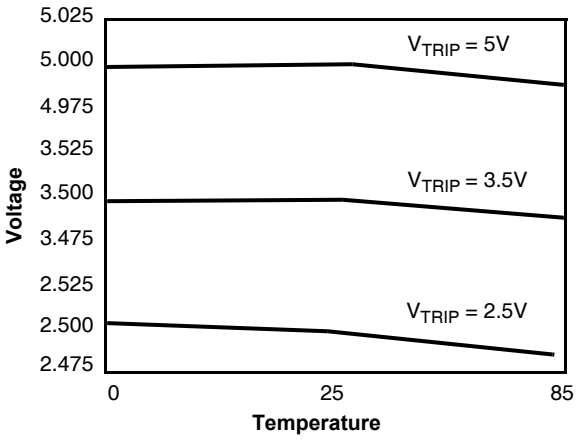
V_{CC} Supply Current vs. Temperature (I_{SB})



t_{PURST} vs. Temperature



V_{TRIP} vs. Temperature (programmed at 25°C)



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 16, 2015	FN8132.2	Updated the Ordering Information table on page 2. Added Revision History and About Intersil sections. Replaced all Package Outline drawings with the most recent versions.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

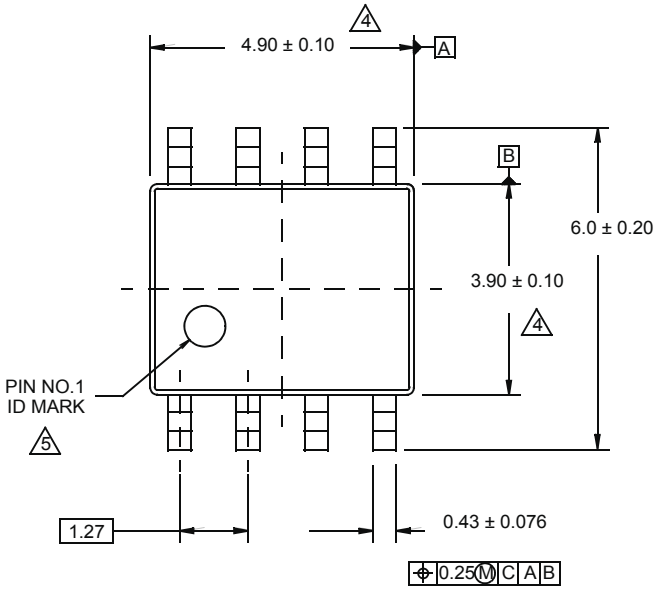
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

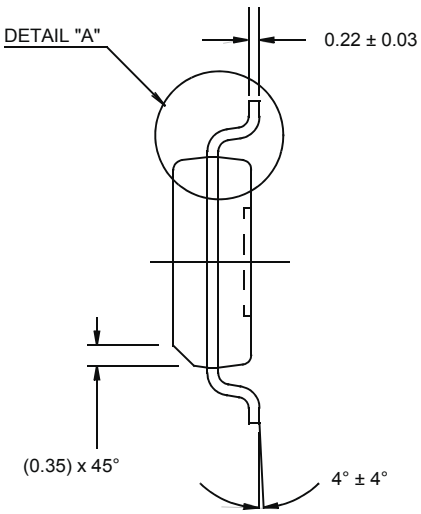
Package Outline Drawing

M8.15E

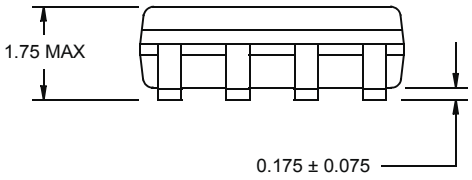
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



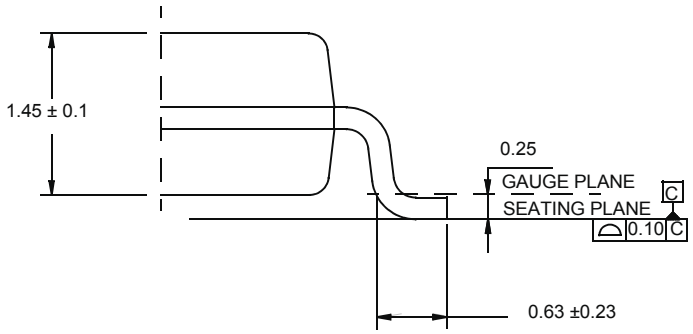
TOP VIEW



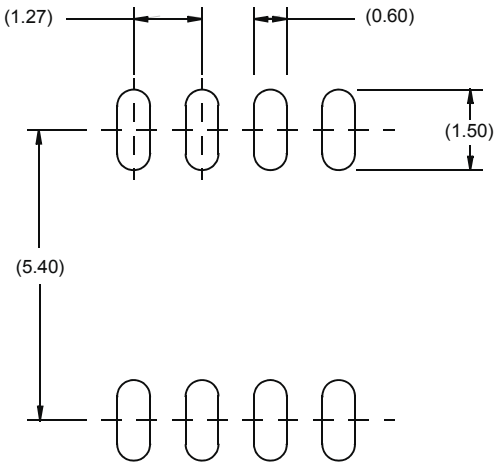
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"

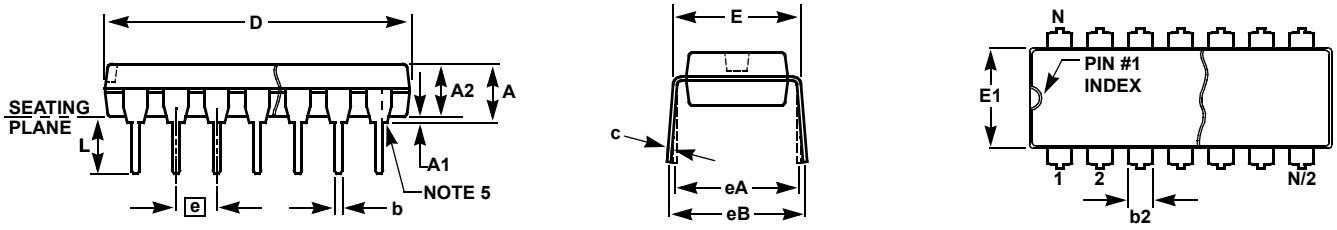


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Plastic Dual-In-Line Packages (PDIP)



MDP0031

PLASTIC DUAL-IN-LINE PACKAGE

SYMBOL	INCHES					TOLERANCE	NOTES
	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20		
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. C 2/07

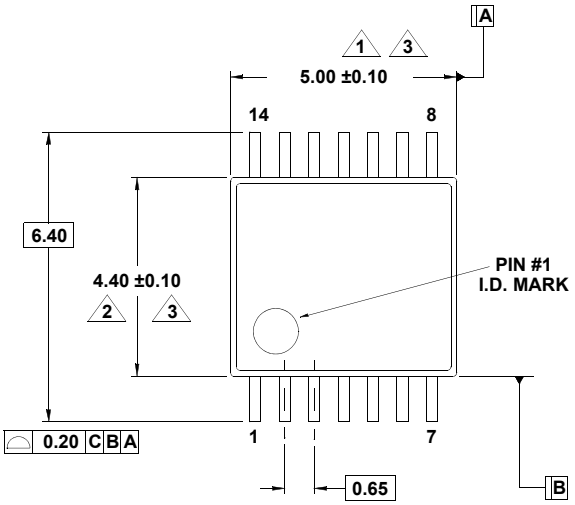
NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

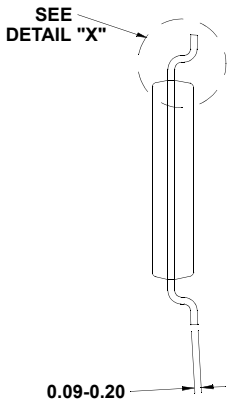
Package Outline Drawing

M14.173

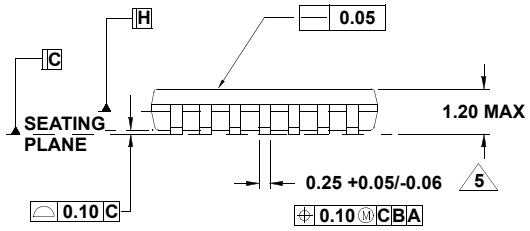
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09



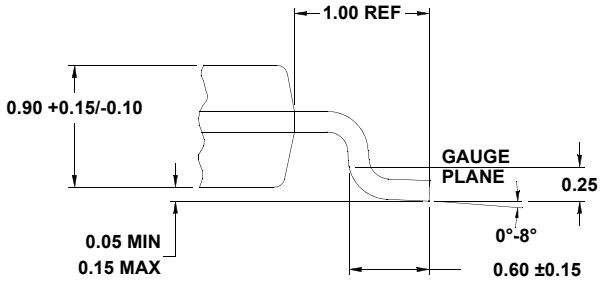
TOP VIEW



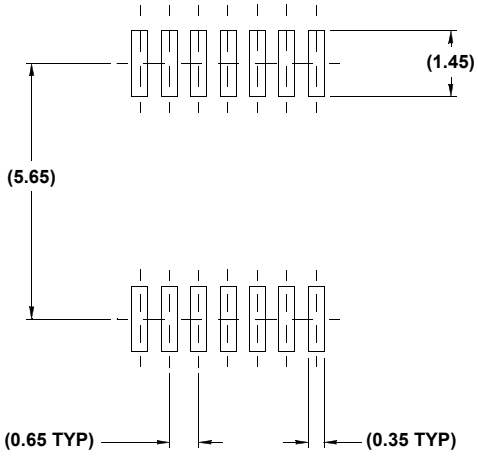
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.