Low Phase Noise, 1-to-8, 3.3V, 2.5V LVPECL Output Fanout Buffer

8SLVP1208

Datasheet

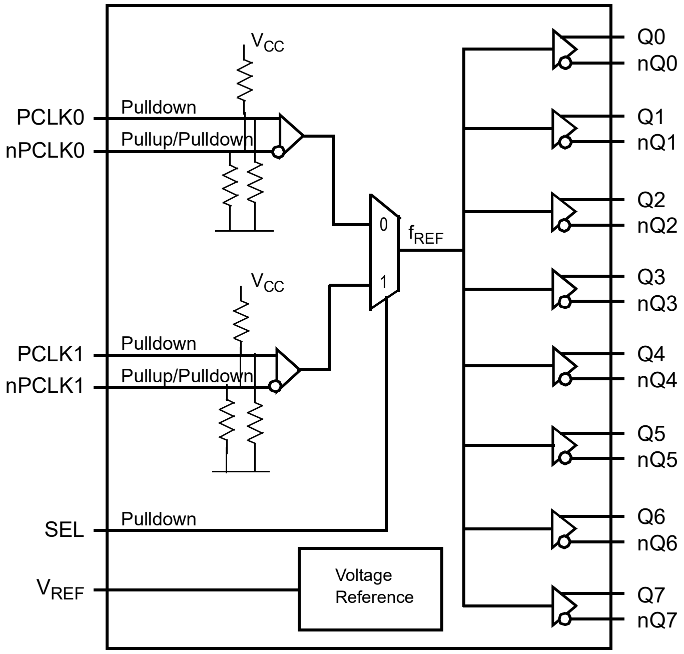
General Description

The 8SLVP1208 is a high-performance differential LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The 8SLVP1208 is characterized to operate from a 3.3V and 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the 8SLVP1208 ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and eight low skew outputs are available. The integrated bias voltage generators enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

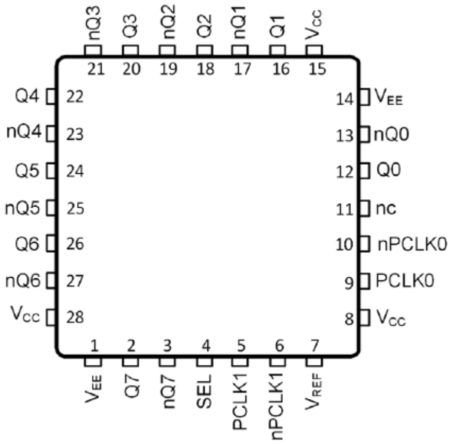
Features

- Eight low skew, low additive jitter LVPECL output pairs
- Two selectable, differential clock input pairs
- Differential pairs can accept the following differential input levels: LVDS, LVPECL, CML
- Maximum input clock frequency: 2GHz
- LVCMOS interface levels for the control input (input select)
- Output skew: 28ps (typical)
- Propagation delay: 410ps (maximum)
- Low additive phase jitter, RMS: 54.1fs (maximum) (f_{REF} = 156.25MHz, V_{PP} = 1V, 12kHz - 20MHz)
- Full 3.3V and 2.5V supply voltage
- Maximum device current consumption (I_{EE}): 141mA
- Available in lead-free (RoHS 6), 28-Lead VFQFN package
- -40°C to 85°C ambient operating temperature
- Supports case temperature ≤ 105°C operations
- Differential PCLK0, nPCLK0 and PCLK1, nPCLK1 pairs can also accept single-ended LVCMOS levels. See Applications section *Wiring the Differential Input to Accept Single-Ended Levels* (*Figure 1A* and *Figure 1B*)

Block Diagram



Pin Assignment



8SLVP1208

28-Lead LFCSP
5mm x 5mm x 0.75mm package body
NB Package

Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions[1]

Number	Name	Type		Description
1, 14	V_{EE}	Power		Negative supply pins.
2, 3	Q7, nQ7	Output		Differential output pair. 7 LVPECL interface levels.
4	SEL	Input	Pulldown	Reference select control. See Table 3 for function. LVCMOS/LVTTL interface levels.
5	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
6	nPCLK1	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. $V_{CC}/2$ default when left floating.
7	V_{REF}	Output		Bias voltage reference for the nPCLK inputs.
8, 15, 28	V_{CC}	Power		Power supply pins.
9	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
10	nPCLK0	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. $V_{CC}/2$ default when left floating.
11	nc	Unused		Do not connect.
12, 13	Q0, nQ0	Output		Differential output pair 0. LVPECL interface levels.
16, 17	Q1, nQ1	Output		Differential output pair 1. LVPECL interface levels.
18, 19	Q2, nQ2	Output		Differential output pair 2. LVPECL interface levels.
20, 21	Q3, nQ3	Output		Differential output pair 3. LVPECL interface levels.
22, 23	Q4, nQ4	Output		Differential output pair 4. LVPECL interface levels.
24, 25	Q5, nQ5	Output		Differential output pair 5. LVPECL interface levels.
26, 27	Q6, nQ6	Output		Differential output pair 6. LVPECL interface levels.

NOTE 1: *Pulldown* and *Pullup* refer to internal input resistors. See *Table 2*, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. SEL Input Selection Function Table[1]

Input	Operation
SEL	
0 (default)	PCLK0, nPCLK0 is the selected differential clock input
1	PCLK1, nPCLK1 is the selected differential clock input

NOTE 1: SEL is an asynchronous control.

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{CC}	3.63V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O (LVPECL) Continuous Current Surge Current	 50mA 100mA
Input Sink/Source, IREF	±2mA
Maximum Junction Temperature, $T_{J,MAX}$	125°C
Storage Temperature, T_{STG}	-65°C to 150°C
ESD - Human Body Model[1]	2000V
ESD - Charged Device Model[1]	1500V

NOTE 1: According to JEDEC/JESD 22-A114/22-C101.

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{CC}	Power Supply Voltage		3.135	3.3V	3.465	V
I_{EE}	Power Supply Current			110	141	mA
I_{CC}	Power Supply Current	Q0 to Q7 terminated 50Ω to V_{CC} – 2V		285	343	mA

Table 4B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{CC}	Power Supply Voltage		2.375	2.5V	2.625	V
I_{EE}	Power Supply Current			102	127	mA
I_{CC}	Power Supply Current	Q0 to Q7 terminated 50Ω to V_{CC} – 2V		285	341	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.465V	2.2		V_{CC} + 0.3	V
			V_{CC} = 2.625V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.465V	-0.3		0.8	V
			V_{CC} = 2.625V	-0.3		0.7	V
I_{IH}	Input High Current	SEL	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input Low Current	SEL	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	-10			µA

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias		I_{REF} = 2mA	V_{CC} – 1.83	V_{CC} – 1.54	V_{CC} – 1.25	V
V_{OH}	Output High Voltage[2]			V_{CC} – 1.23	V_{CC} – 1.16	V_{CC} – 0.80	V
V_{OL}	Output Low Voltage[2]			V_{CC} – 1.97	V_{CC} – 1.90	V_{CC} – 1.70	V

NOTE 1: Input and output parameters vary 1:1 with V_{CC}.

NOTE 2: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 4E. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0 PCLK1, nPCLK1	V_{CC} = V_{IN} = 2.625V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{CC} = 2.625V, V_{IN} = 0V	-150			µA
V_{REF}	Reference Voltage for Input Bias		I_{REF} = 2mA	V_{CC} – 1.64	V_{CC} – 1.36	V_{CC} – 1.09	V
V_{OH}	Output High Voltage[2]			V_{CC} – 1.21	V_{CC} – 1.00	V_{CC} – 0.79	V
V_{OL}	Output Low Voltage[2]			V_{CC} – 1.92	V_{CC} – 1.80	V_{CC} – 1.67	V

NOTE 1: Input and output parameters vary 1:1 with V_{CC}.

NOTE 2: Outputs terminated with 50Ω to V_{CC} – 2V.

AC Electrical Characteristics

Table 5A. AC Electrical Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C[1]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Frequency	PCLK[0:1], nPCLK[0:1]				2	GHz
$\Delta V/\Delta t$	Input Edge Rate	PCLK[0:1], nPCLK[0:1]		1.5			V/ns
t_{PD}	Propagation Delay[2]		PCLK[0:1], nPCLK[0:1] to any Qx, nQx for $V_{PP,IN}$ = 0.1V or 0.3V	160	287	410	ps
*t*sk(o)	Output Skew[3, 4]				28	64	ps
*t*sk(i)	Input Skew[4]				12	65	ps
*t*sk(p)	Pulse Skew		f_{REF} = 100MHz		29	70	ps
*t*sk(pp)	Part-to-Part Skew[4, 5]				55	140	ps
t_R / t_F	Output Rise/ Fall Time		20% to 80%	29	104	200	ps
$MUX_{ISOLATION}$	Mux Isolation[6]				76		dB
V_{PP}	Peak-to-Peak Input Voltage[7, 8]		f < 1.5GHz	0.1		1.5	V
			f > 1.5GHz	0.2		1.5	V
V_{CMR}	Common Mode Input Voltage[7, 8, 9]			1.0		V_{CC} – 0.6	V
$V_{O\ (pp)}$	Output Voltage Swing, Peak-to-Peak		V_{CC} = 3.3V, $f_{REF} \le$ 2GHz	0.5	0.83	1.10	V
			V_{CC} = 2.5V, $f_{REF} \le$ 2GHz	0.5	0.82	1.05	V
V_{DIFF_OUT}	Differential Output Voltage Swing, Peak to Peak		V_{CC} = 3.3V, $f_{REF} \le$ 2GHz	1.0	1.67	2.20	V
			V_{CC} = 2.5V, $f_{REF} \le$ 2GHz	1.0	1.63	2.10	V

NOTE 1: NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 2: Measured from the differential input crossing point to the differential output crossing point.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 6: Qx, nQx outputs measured differentially. See *MUX Isolation* diagram in the *Parameter Measurement Information* section.

NOTE 7: V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.

NOTE 8: For single-ended LVCMOS input applications, please refer to the *Applications Information*, *Wiring the Differential Input to Accept Single-Ended Levels*, *Figure 1A* and *Figure 1B*.

NOTE 9: Common mode input voltage is defined as the crosspoint.

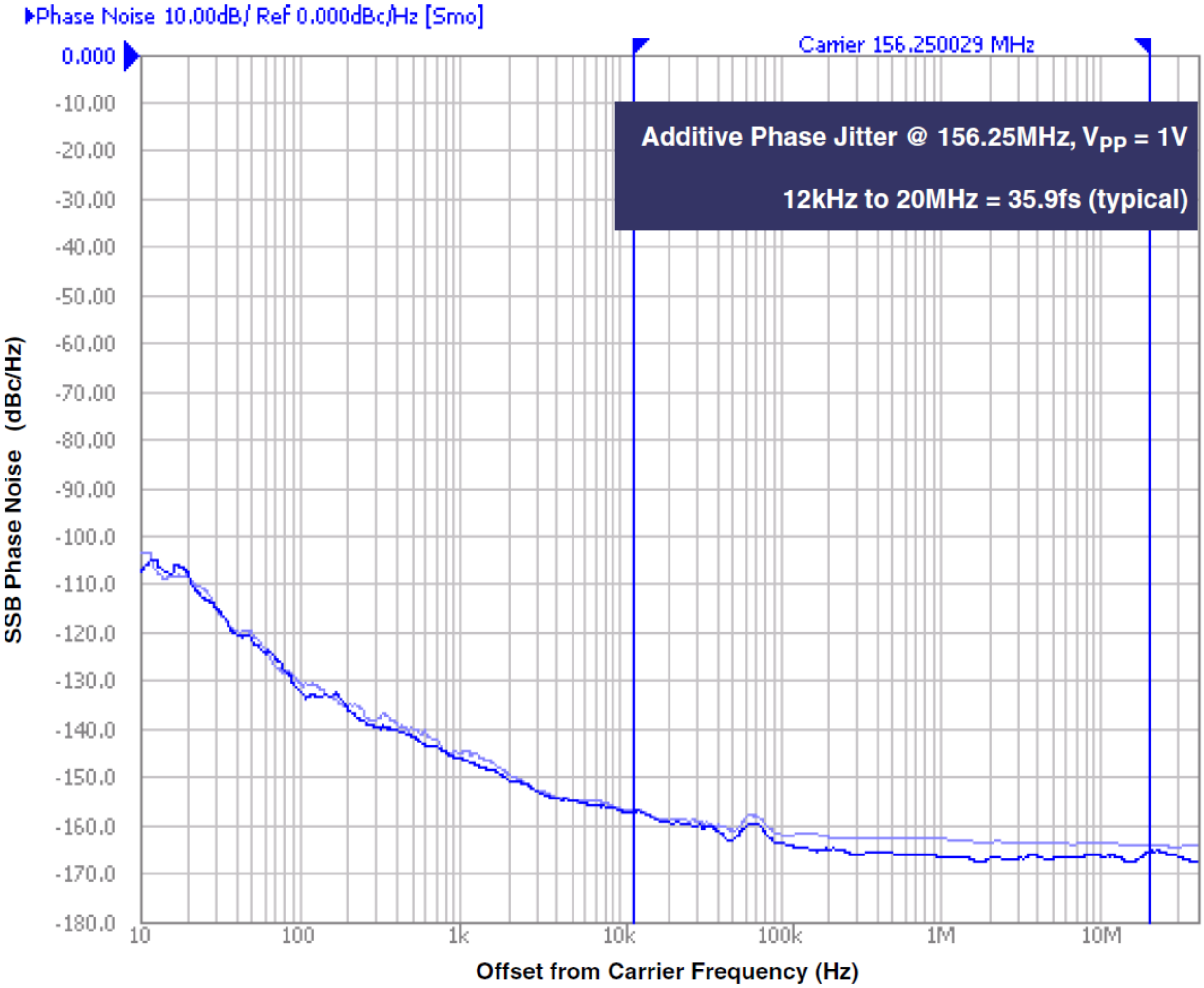
Table 5B. AC Electrical Characteristics, Buffer Additive Phase Jitter, T_{JIT}, T_A = -40°C to 85°C[1]

Symbol	Parameter	Test Condition	V_{CC} = 2.5V ± 5%, V_{EE} = 0V			V_{CC} = 3.3V ± 5%, V_{EE} = 0V			Units
			Min	Typ	Max	Min	Typ	Max	
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	f_{REF} = 122.88MHz, Square Wave, V_{PP} = 1V, Integration Range: 1kHz - 40MHz		56.4	87.4		46.8	79.9	fs
		f_{REF} = 122.88MHz, Square Wave, V_{PP} = 1V, Integration Range: 10kHz - 20MHz		42.5	64.5		38.4	60.5	fs
		f_{REF} = 122.88MHz, Square Wave, V_{PP} = 1V, Integration Range: 12kHz - 20MHz		42.5	64.5		38.4	60.5	fs
		f_{REF} = 156.25MHz, Square Wave, V_{PP} = 1V, Integration Range: 1kHz - 40MHz		51.9	69.5		47.4	71.1	fs
		f_{REF} = 156.25MHz, Square Wave, V_{PP} = 1V, Integration Range: 10kHz - 20MHz		41.4	58.6		35.9	54.2	fs
		f_{REF} = 156.25MHz, Square Wave, V_{PP} = 1V, Integration Range: 12kHz - 20MHz		41.4	58.6		35.9	54.1	fs
		f_{REF} = 156.25MHz, Square Wave, V_{PP} = 0.5V, Integration Range: 1kHz - 40MHz		49.8	76.6		44.9	70.2	fs
		f_{REF} = 156.25MHz, Square Wave, V_{PP} = 0.5V, Integration Range: 10kHz - 20MHz		36.9	53.9		31.1	52.3	fs
		f_{REF} = 156.25MHz, Square Wave, V_{PP} = 0.5V, Integration Range: 12kHz - 20MHz		36.8	53.7		31.1	52.3	fs

NOTE 1: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Additive Phase Jitter

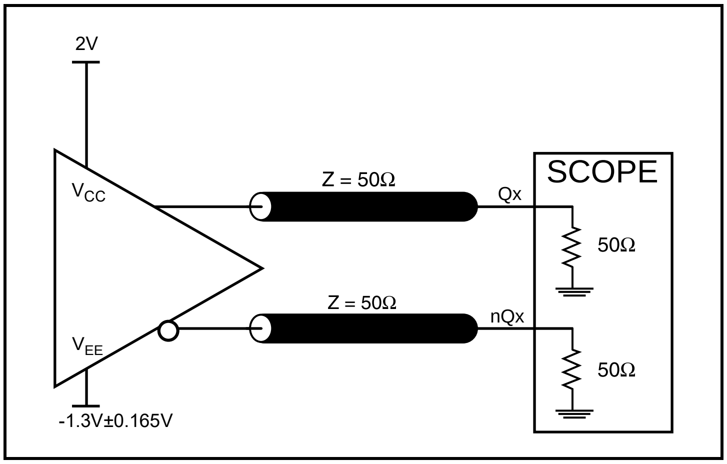
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



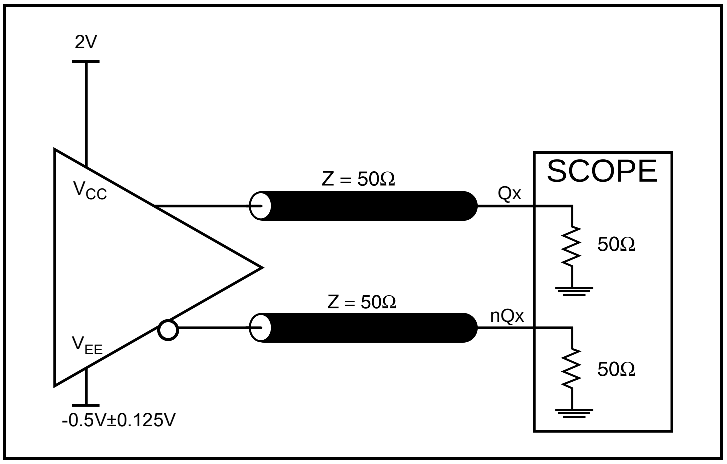
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

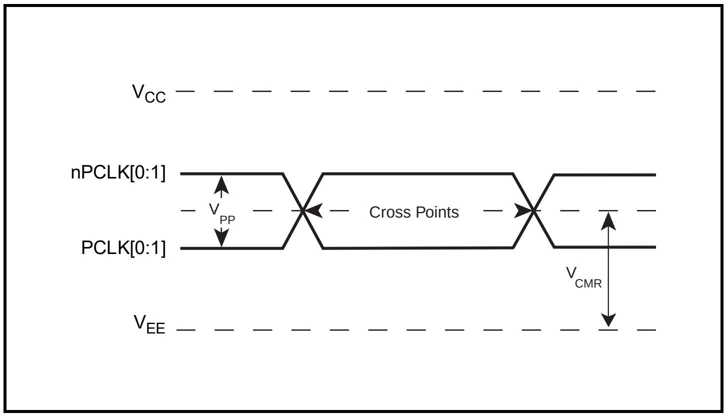
Parameter Measurement Information



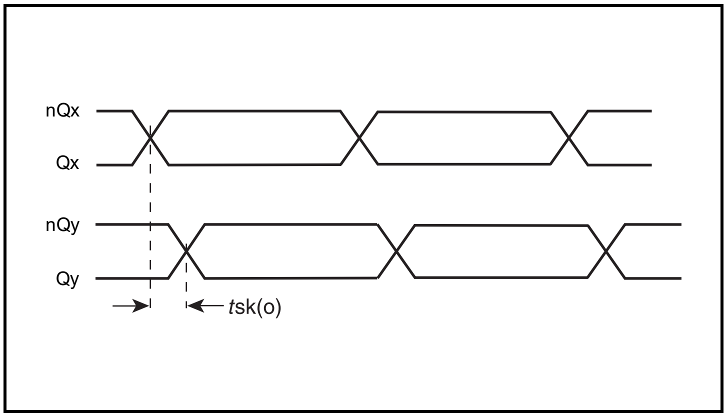
3.3V LVPECL Output Load AC Test Circuit



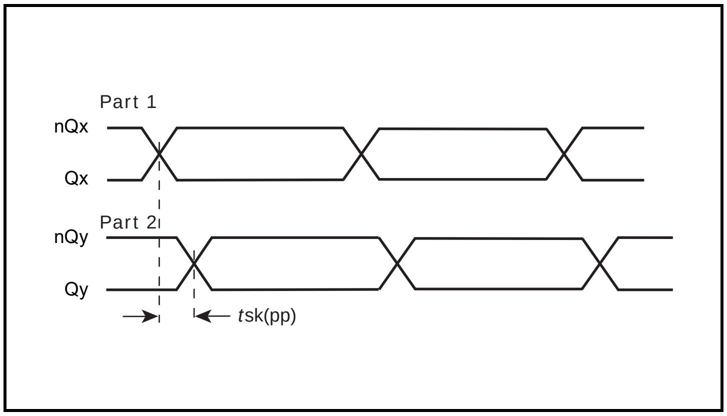
2.5V LVPECL Output Load AC Test Circuit



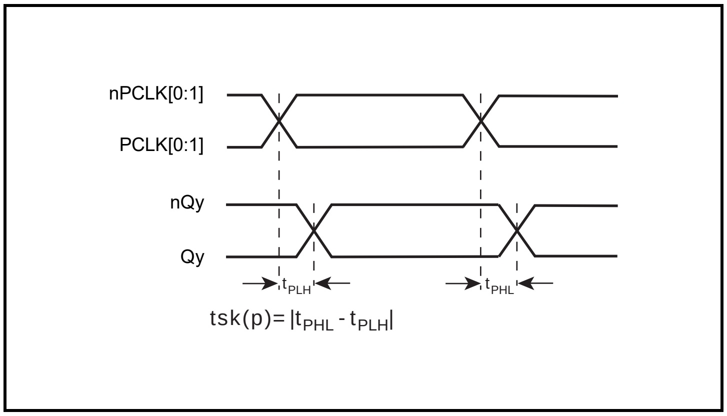
Differential Input Level



Output Skew

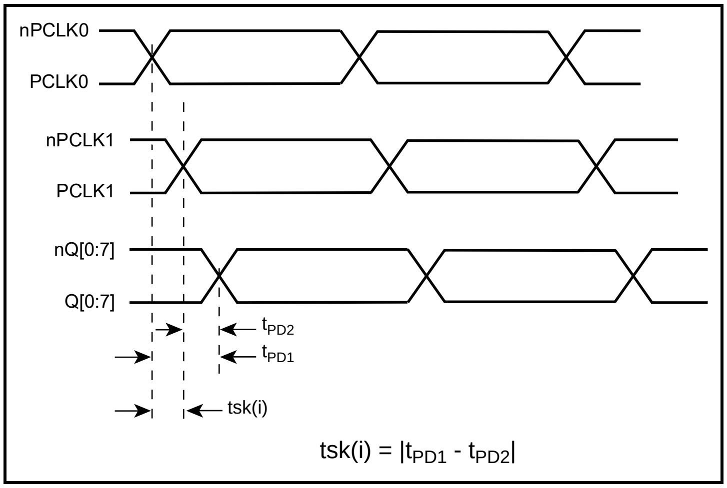


Part-to-Part Skew

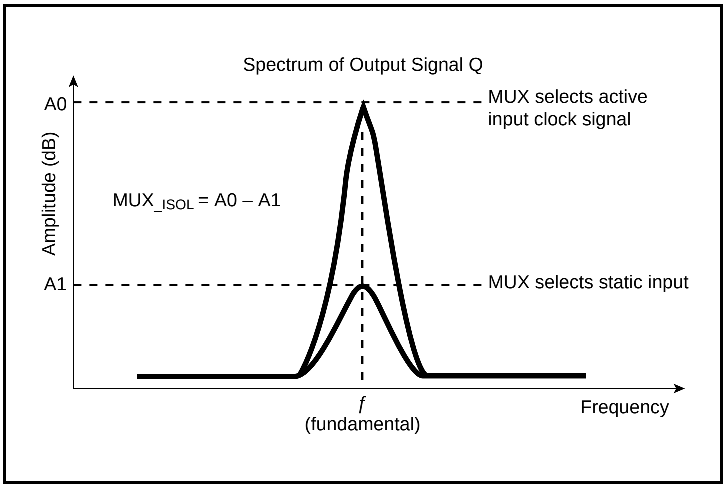


Pulse Skew

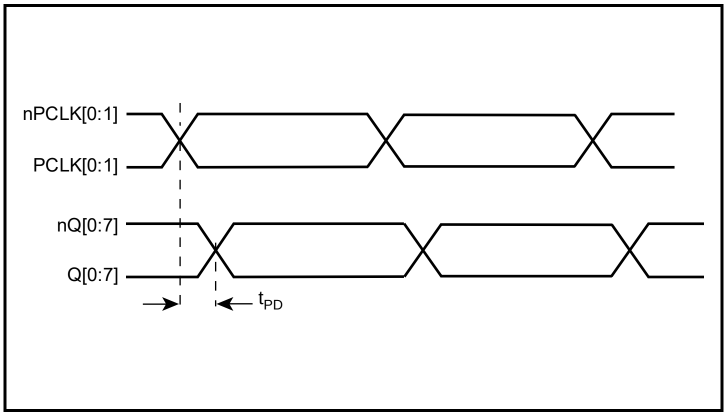
Parameter Measurement Information, continued



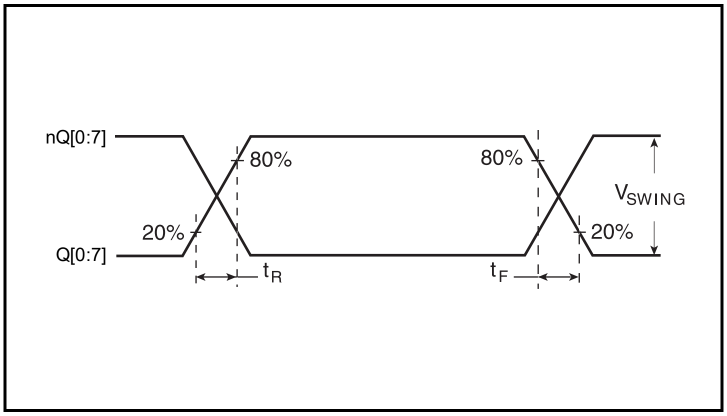
Input Skew



MUX Isolation



Propagation Delay



Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

The 8SLVP1208I inputs can be interfaced to LVPECL, LVDS, CML or LVCMOS drivers. *Figure 1A* illustrates how to DC couple a single LVCMOS input to the 8SLVP1208. The value of the series resistance RS is calculated as the difference between the transmission line impedance and the driver output impedance. This resistor should be placed close to the LVCMOS driver. To avoid cross-coupling of single-ended LVCMOS signals, apply the LVCMOS signals to no more than one PCLK input.

A practical method to implement Vth is shown in *Figure 1B* below. The reference voltage Vth = V1 = $V_{CC}/2$, is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible.

The ratio of R1 and R2 might need to be adjusted to position the V1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V1 at 1.25V. The values below apply when both the single-ended swing and V_{CC} are at the same voltage.

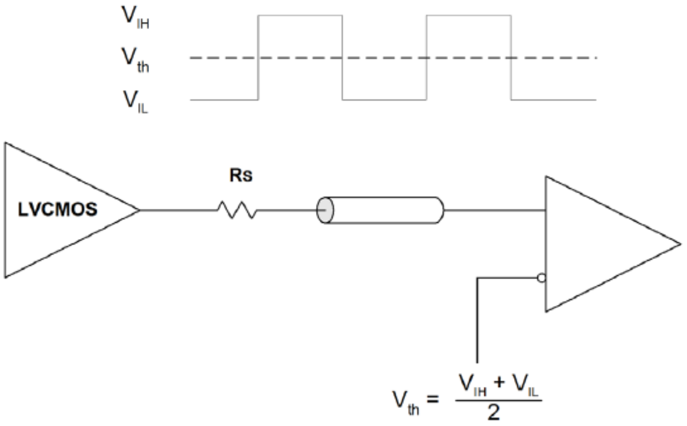


Figure 1A. DC-Coupling a Single LVCMOS Input to the 8SLVP1208

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced, particularly if both input references are LVCMOS to minimize cross talk. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V.

Figure 1B shows a way to attenuate the PCLK input level by a factor of two as well as matching the transmission line between the LVCMOS driver and the 8SLVP1208 at both the source and the load. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. R3 and R4 in parallel should equal the transmission line impedance; for most 50Ω applications, R3 and R4 will be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Though some of the recommended components of Figure 1B might not be used, the pads should be placed in the layout so that they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

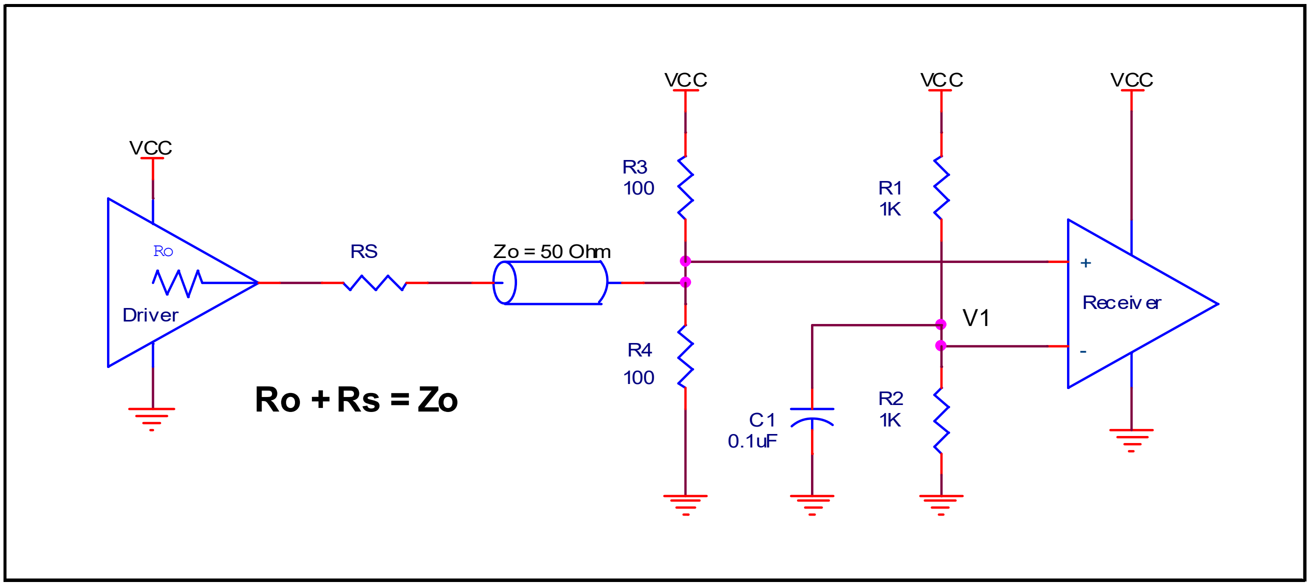


Figure 1B. Alternative DC Coupling a Single LVCMOS Input to the 8SLVP1208

Recommendations for Unused Input and Output Pins

Inputs:

PCLK/nPCLK Inputs

For applications requiring only one differential input, the unused PCLK/nPCLK input can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A* to *Figure 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

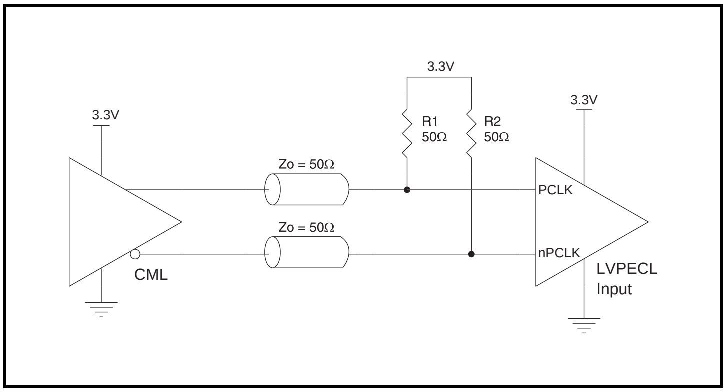


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

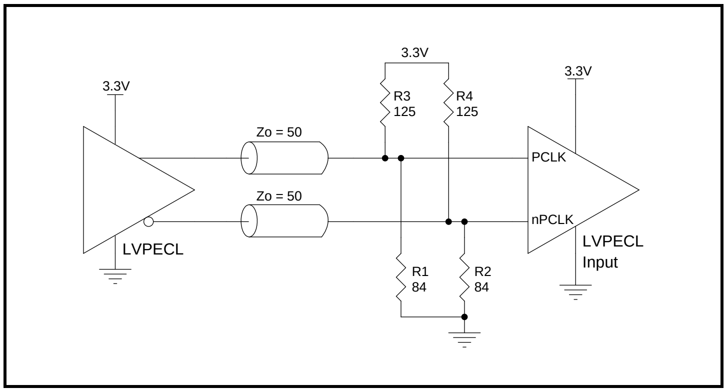


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

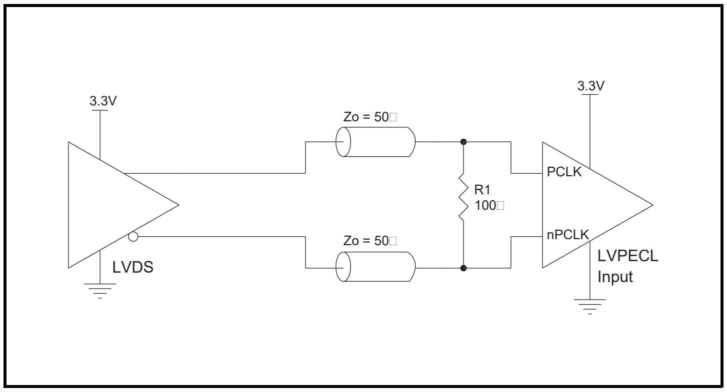


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

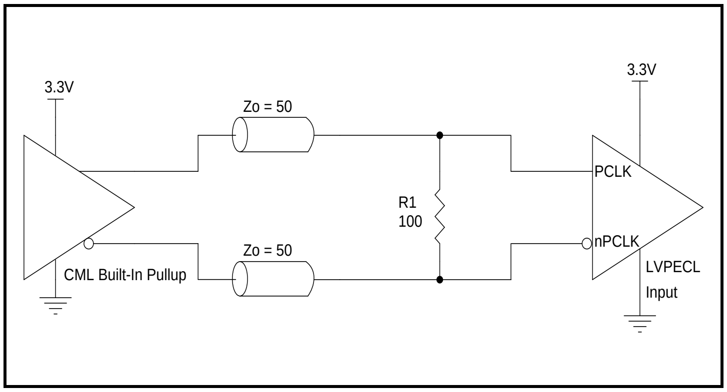


Figure 2D. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

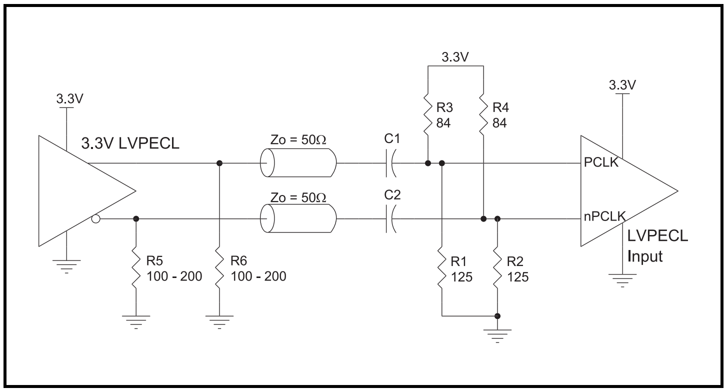


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 3A* to *Figure 3E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

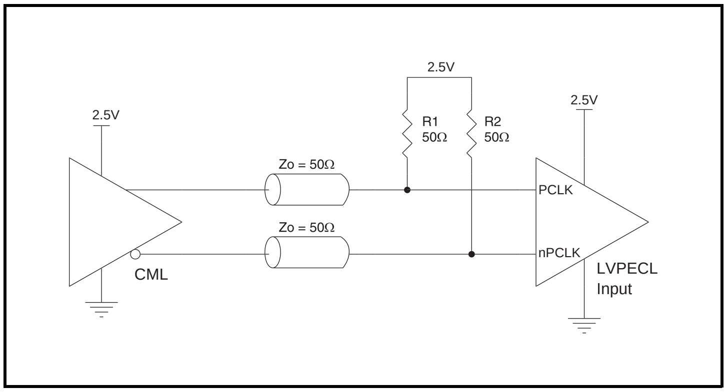


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

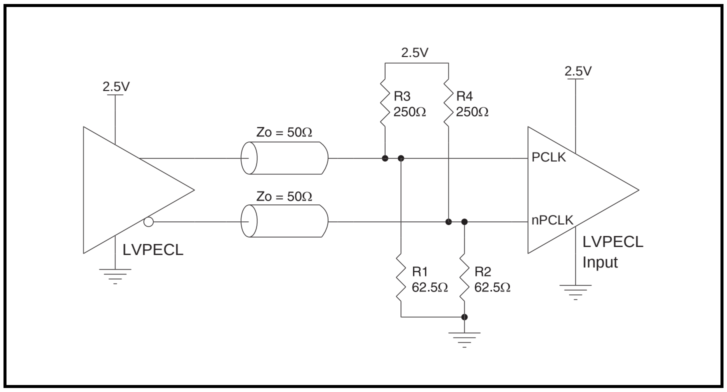


Figure 3B. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

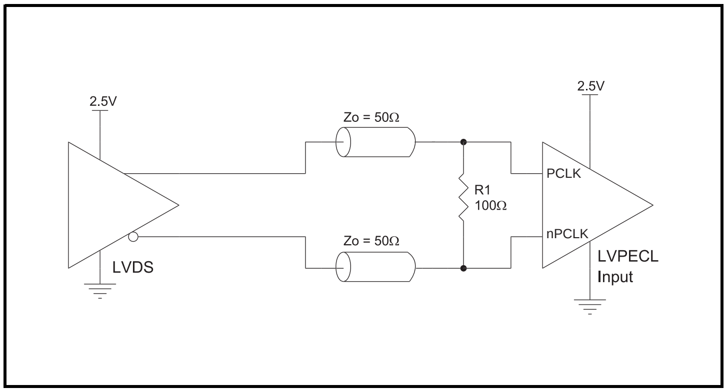


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

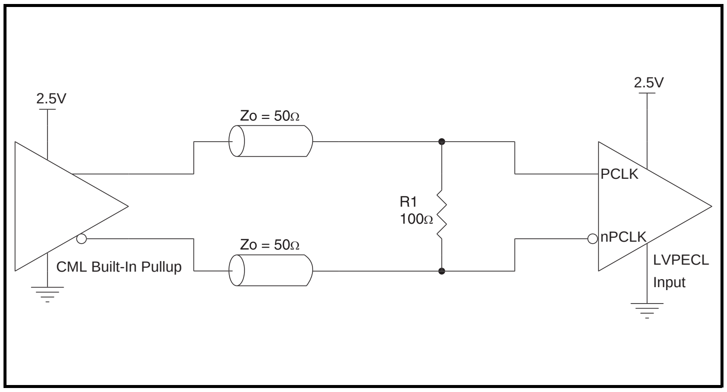


Figure 3D. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

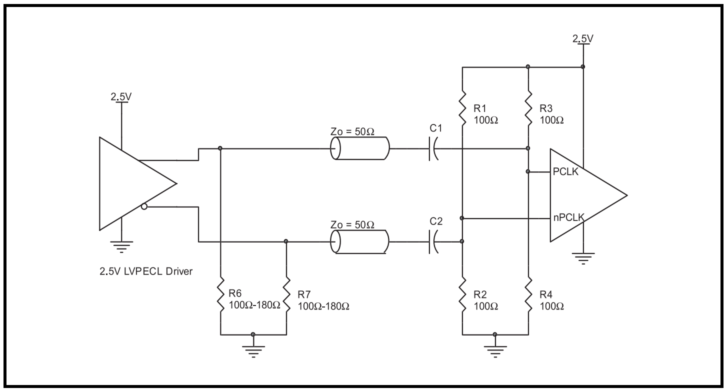


Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts. While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

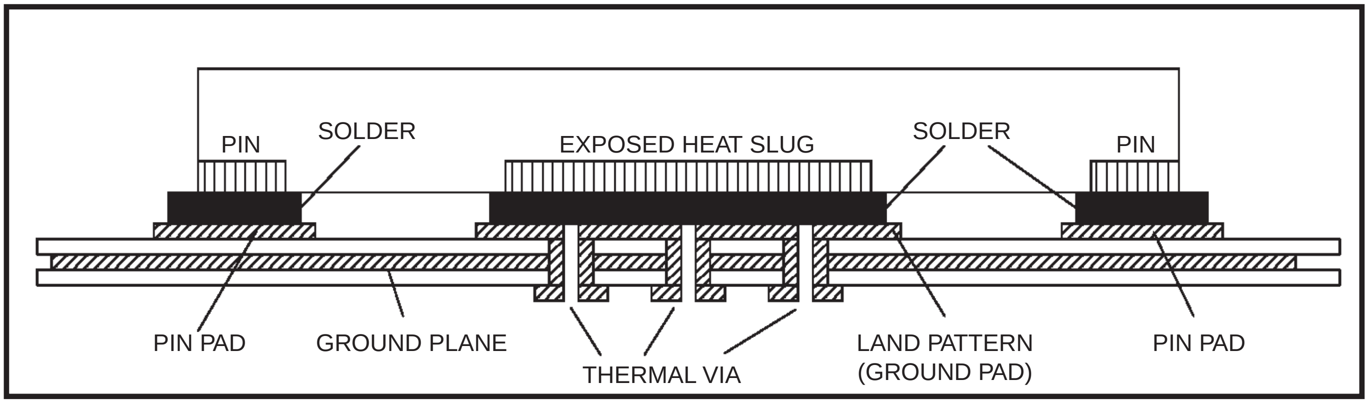


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 5A* and *Figure 5B*show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

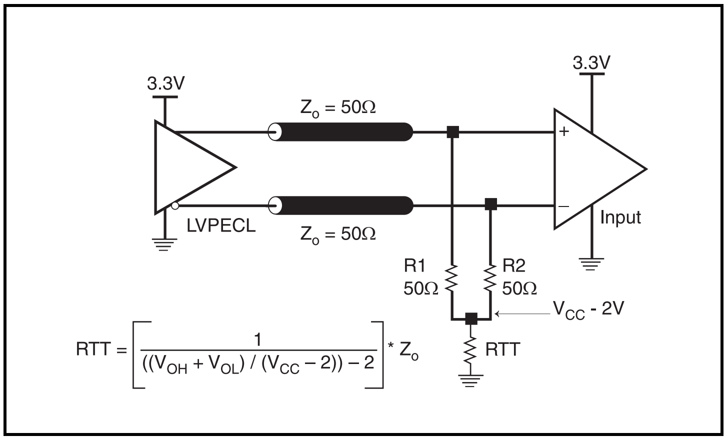


Figure 5A. 3.3V LVPECL Output Termination

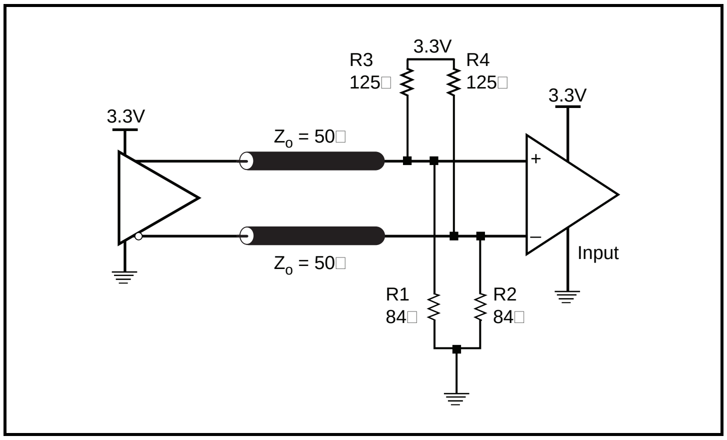


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and *Figure 6B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in *Figure 6B* can be eliminated and the termination is shown in *Figure 6C.*

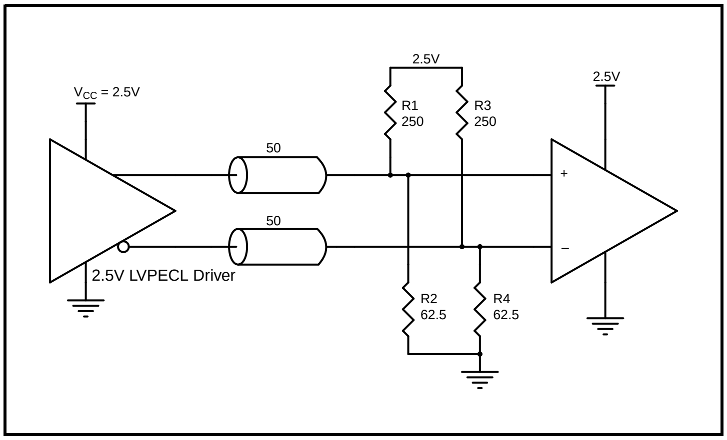


Figure 6A. 2.5V LVPECL Driver Termination Example

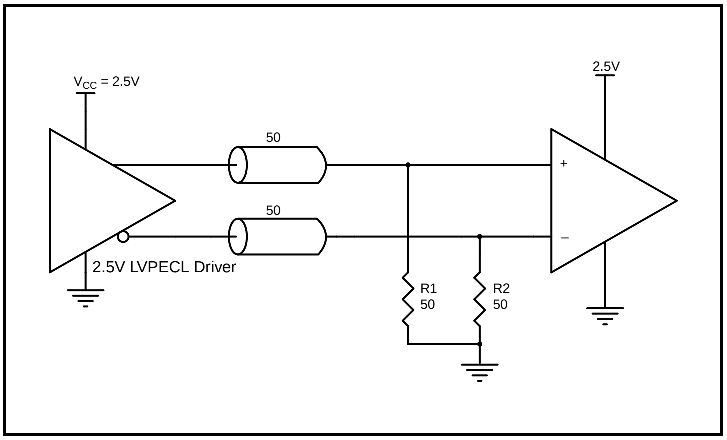


Figure 6C. 2.5V LVPECL Driver Termination Example

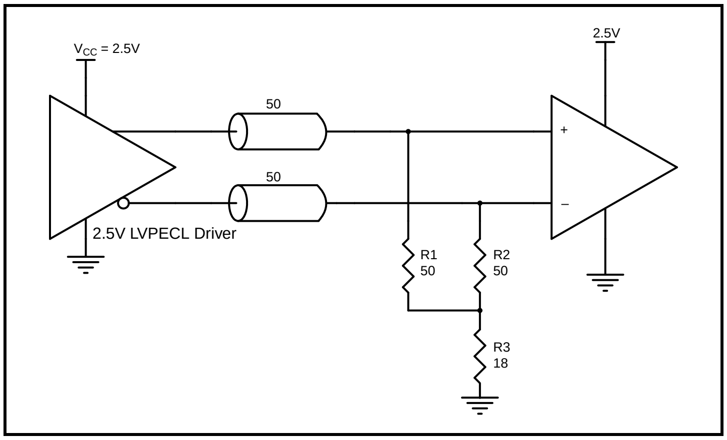


Figure 6B. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8SLVP1208.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8SLVP1208 is the sum of the core power plus the power dissipated at the output(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated at the outputs.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 141mA = **488.57mW**
- Power $(outputs)_{MAX}$ = **29.4mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 29.4mW = **235.2mW**

Total Power$\__{MAX}$ (3.465V, with all outputs switching) = 488.57mW + 235.2mW = **723.77mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 46.2°C/W per *Table 6* below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.724W * 46.2°C/W = 118.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 28-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.4°C/W	37.1°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Table 7*.

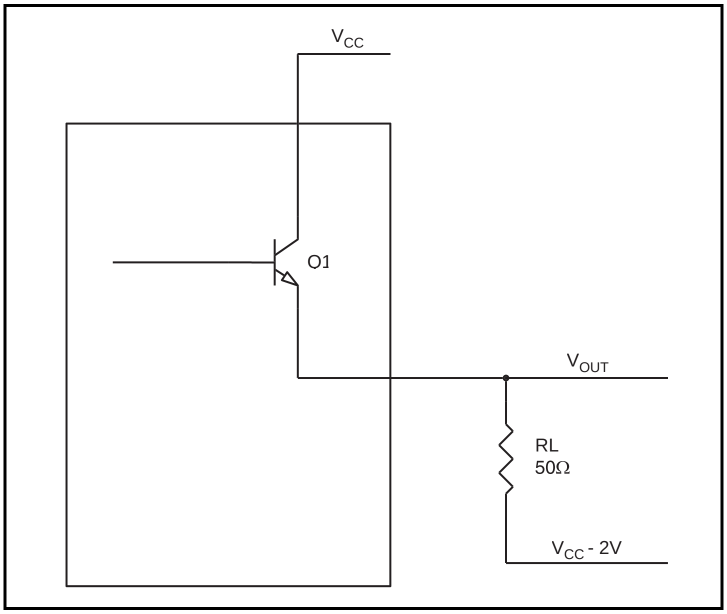


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation at the output(s), use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} – 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.8V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = 0.8$ **V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$
  $(V_{CC\_MAX} – V_{OL\_MAX})$ = **1.7V**

Pd_H is the power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = $[(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$ $[(2V – 0.8V)/50\Omega] * 0.8V$ = **19.2mW**

Pd_L = $[(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$ $[(2V – 1.7V)/50\Omega] * 1.7V$ = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **29.4mW**

Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter Ψ_{JB} (Psi-JB) to calculate the junction temperature (T_J) and ensure it does not exceed the maximum allowed junction temperature in Absolute Maximum Ratings.

The junction-to-board thermal characterization parameter, Ψ_{JB}, is calculated using the following equation:

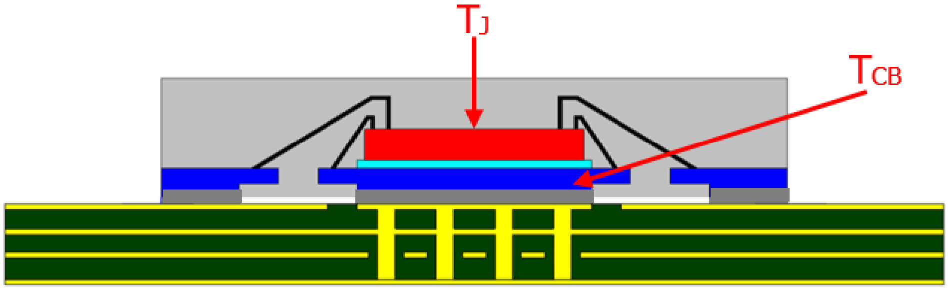
$\mathbf{T_J = T_{CB} + \Psi_{JB} \times P_d}$, where

$\mathbf{T_J}$ = Junction temperature at steady state condition in (^{o}C).

$\mathbf{T_{CB}}$ = Case temperature (Bottom) at steady state condition in (^{o}C).

$\mathbf{\Psi_{JB}}$ **=** Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

$\mathbf{P_d}$ = Power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. Its critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature (T_{CB}). A good connection ensures that temperature at the exposed pad (T_{CB}) and the board temperature (T_B) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption, and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example calculation for junction temperature (T_J): $T_J = T_{CB} + \Psi_{JB} \times P_d$

Package type:	28-Lead VFQFN
Ψ_{JB}	1.0 C/W
T_{CB}	105^{o}C
P_d	0.724 W

For the variables above, the junction temperature is equal to 105.7^{o}C. Since this is below the maximum junction temperature of 125^{o}C, there are no long-term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 118.4^{o}C, this device can function without the degradation of the specified AC or DC parameters.

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 28-Lead VFQFN

θ_{JA} **at 0 Air Flow**			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.4°C/W	37.1°C/W

Transistor Count

The transistor count for the 8SLVP1208 is: 304

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/nbnbg28-package-outline-50-x-50-mm-body-050-mm-pitch-qfn

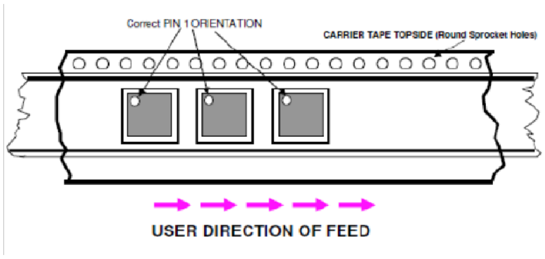
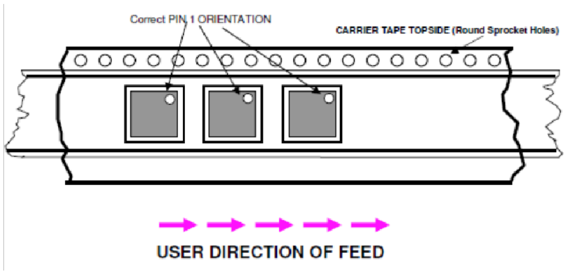
Ordering Information

Table 8. Ordering Information[1]

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVP1208ANBGI	LVP1208ANBGI	“Lead-Free” 28-Lead VFQFN	Tray	-40°C to 85°C
8SLVP1208ANBGI8	LVP1208ANBGI	“Lead-Free” 28-Lead VFQFN	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40°C to 85°C
8SLVP1208ANBGI/W	LVP1208ANBGI	“Lead-Free” 28-Lead VFQFN	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40°C to 85°C

NOTE 1:Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

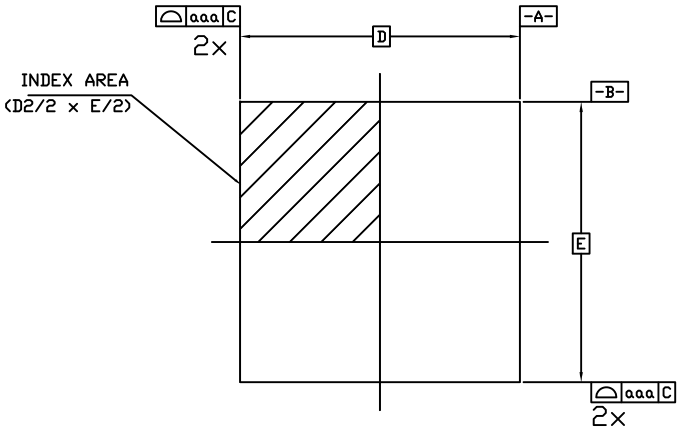
Table 9. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

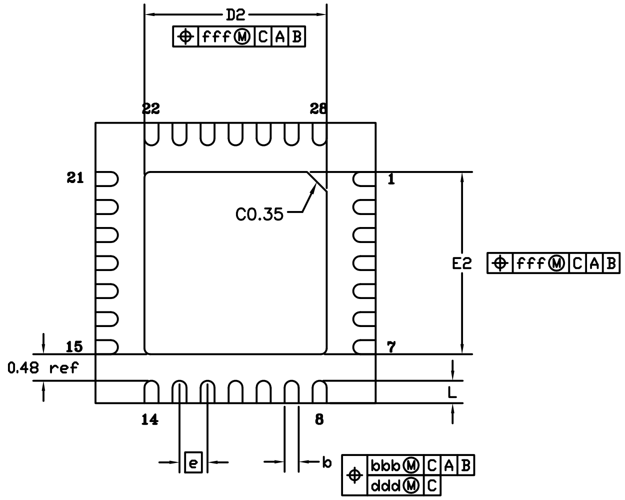
Revision History

Revision Date	Description of Change
May 8, 2020	Added Absolute Maximum Ratings
August 28, 2014	Fixed typo: V_{DIFF_OUT}, Test Conditions - V_{CC} = 3.3V, $f_{REF} \leq$ 2GHz. Updated contact information. Updated format.
March 25, 2014	Corrected page layout formatting.
January 27, 2014	Changed NOTE 6 to read: V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC}.
January 30, 2013	Added Features Bullet: Differential PCLKA, nPCLKA and PCLKB, nPCLKB pairs can also accept single-ended LVCMOS levels. Added NOTE 8 to V_{PP}, V_{CMR}. Updated the “Wiring the Differential Input to Accept Single-Ended Levels” note.
August 2, 2012	Ordering Information Table - added additional row. Added Orientation Packaging Table.
April 23, 2012	Additive Phase Noise Plot label, corrected units from 35.9ps to 35.9fs. Corrected page headers from 1:8, LVPECL Output Fanout Buffer to 2:8, LVPECL.

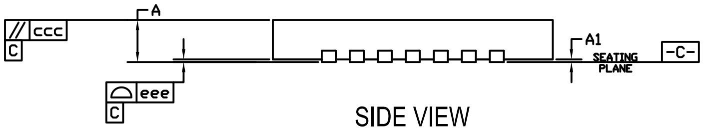
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	06/04/10	KS
01	CORRECTION ON L	09/22/10	DP
02	COMBINE POD & LAND PATTERN	1/22/14	J.H



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	3.15	3.25	3.35
E2	3.15	3.25	3.35
L	0.30	0.40	0.50
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

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TITLE NB/NBG28 PACKAGE OUTLINE
5.0 x 5.0 mm BODY
0.50 mm PITCH QFN

SIZE C
DRAWING No. PSC-4312
REV 02

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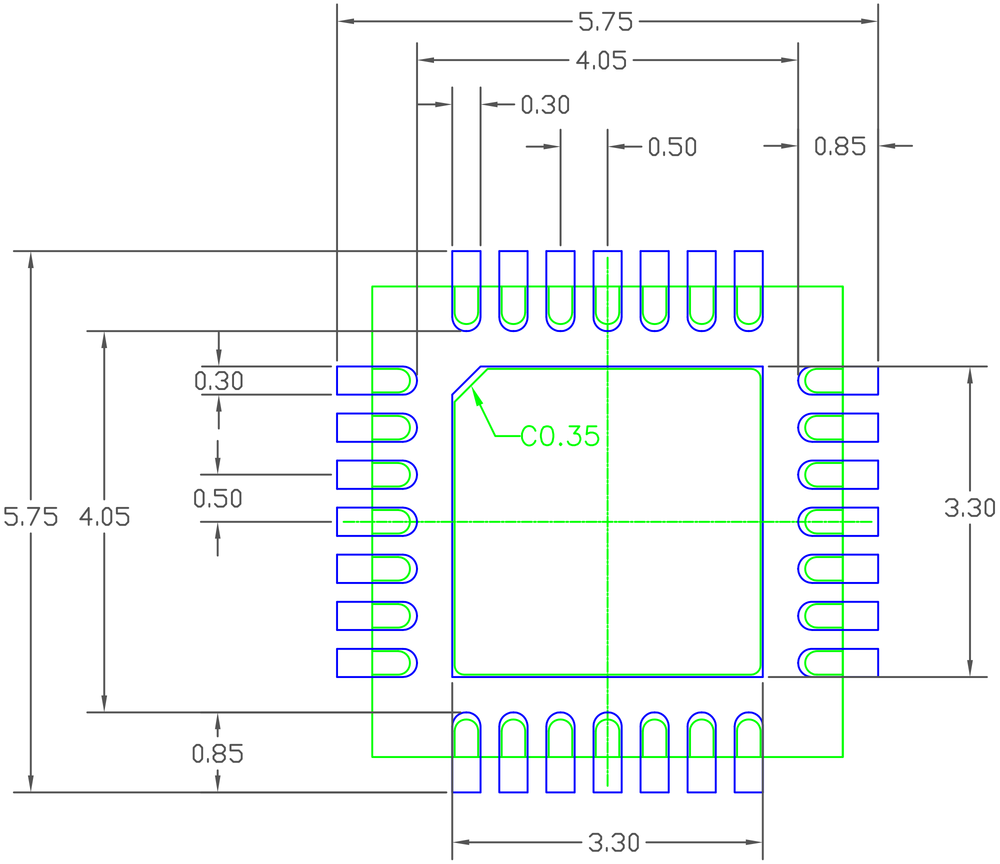
SHEET 1 OF 2

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	06/04/10	KS
01	CORRECTION ON L	09/22/10	DP
02	COMBINE POD & LAND PATTERN	1/22/14	J.H



NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
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XX± .05
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