2020

MotorComm SZ18201 Datasheet

FAST ETHERNET TRANSCEIVER

REV V1.10

Revision History

Revision	Release Date	Summary
0.1		Draft
0.2	2019/05/26	Modify pin assignment
1.0	2019/07/11	Add POS, WOL description Update Register table
1.01	2019/09/04	Update Electrical Characteristics
1.02	2019/09/11	Modify RBIAS resistor to 2.49k ohm
1.03	2019/10/16	Modify errors
1.04	2019/11/05	Update Register
1.05	2019/11/12	Update Block diagram
1.06	2020/01/13	Add EPAD description
1.07	2020/03/16	Modify package information, ordering information Add thermal resistance
1.08	2020/03/23	Add Copyright Statement and Disclaimer Add Reg ext 0x200a Modify Rbias pin description
1.09	2020/03/26	Add Packaging Type Release
1.10	2020/07/20	Change company logo and name

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1. GENERAL DESCRIPTION

The SZ18201 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted pair cables transceiver. Additionally, the SZ18201 provides flexibility to connect to a MAC through a standard MII and RMII interface.

The SZ18201 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5 twisted-pair cable.

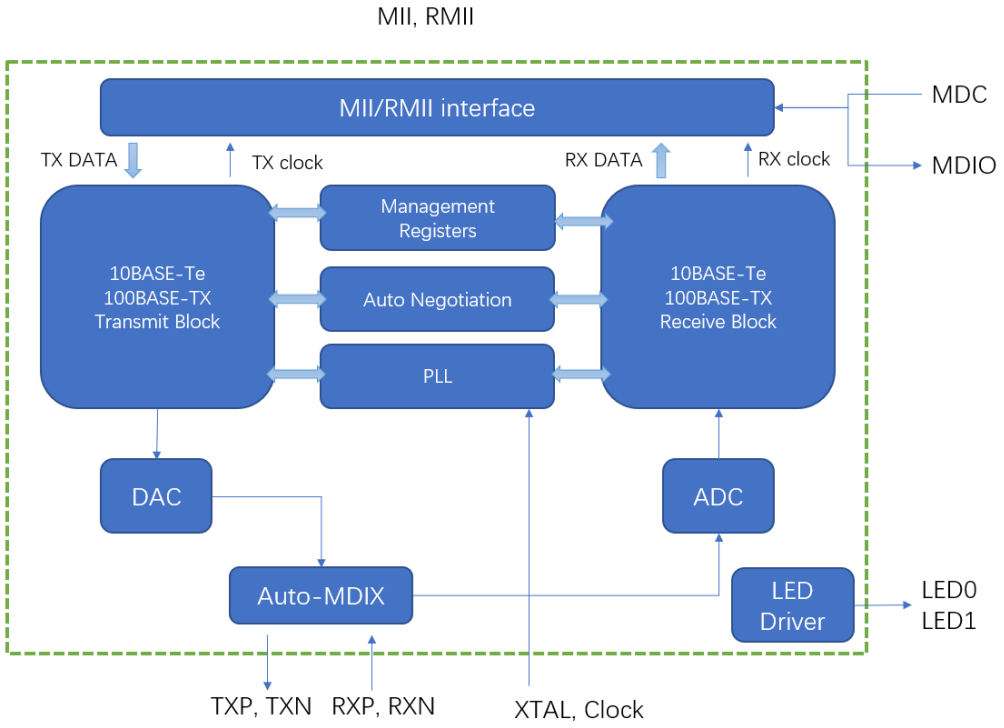
The SZ18201 offers integrated built-in self-test and loopback capabilities for ease of use.

The SZ18201 offers innovative and robust approach for reducing power consumption through EEE, WoL and other programmable energy savings modes.

TARGET APPLICATIONS

- General Embedded Applications
- Video Surveillance
- Industrial Controls
- Factory Automation

BLOCK DIAGRAM



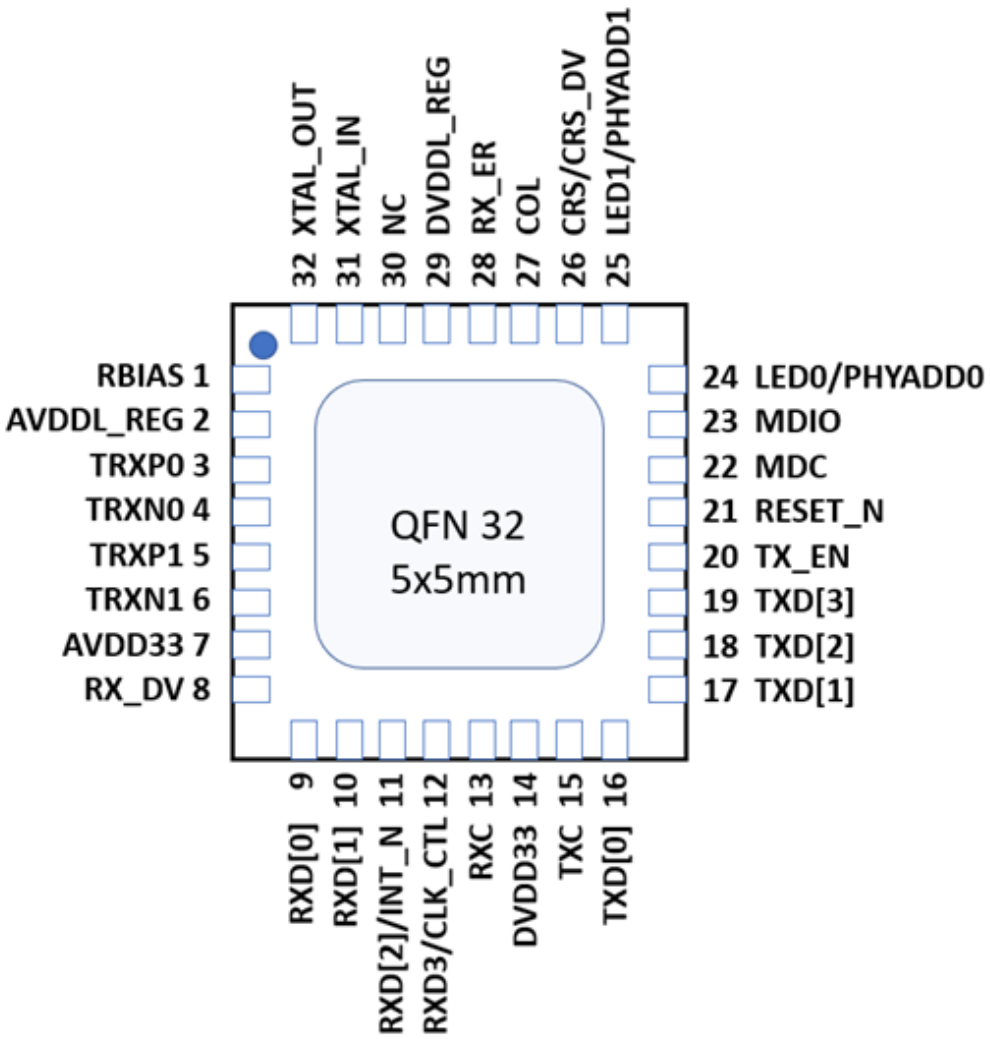
2. FEATURE

- EEE 802.3az, EEE
- 100Base-TX
- 10Base-Te
- MII mode
- RMII mode
- Full/Half duplex
- Auto-negotiation
- Power down mode
- Base Line Wander (BLW) compensation
- Auto MDIX
- Interrupt function
- WOL, Wake on Lan
- Automatic Polarity correction
- 2 sets LED indicator
- 25 MHz crystal or OSC
- Provide 50Mhz clock source for MAC
- Single Power supply, internal LDO
- Package QFN 32, 5x 5mm

3. PIN ASSIGMENT

3.1 SZ18201

3.2 QFN32 5X5MM



3.2 PIN DESCRIPTIONS

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open-drain output
- OT = Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR = Sample on reset
- XT = Crystal inputs/outputs pin type
- PWR= Power related

No.	Name	Type	Description
1	RBIAS	I	Bias Resistor. An external 2.49 kΩ±1% resistor must be connected between the RBIAS pin and GND
2	AVDDL_REG	PWR/O	Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
3	TRXP0	IO	Transmit/Receive Pairs for channel 0. Differential data from copper media is transmitted and received on the single TRD± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center-tap power supply.
4	TRXN0	IO	
5	TRXP1	IO	Transmit/Receive Pairs for channel 1. Differential data from copper media is transmitted and received on the single TRD± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center-tap power supply.
6	TRXN1	IO	
7	AVDD33	PWR	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
8	RX_DV	O/PD	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. Power On Strapping for MII/RMII selection. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin.
9	RXD[0]	O/PD	Receive Data [0]
10	RXD[1]	O/PD	Receive Data [1] An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function.
11	RXD[2]/INT_N	O/OD/PD	Receive Data [2] When in RMII mode, this pin is used for the interrupt

			function.
12	RXD[3]/CLK_CTL	O/PD	Receive Data [3] RXD[3]/CLK_CTL pin is the Power On Strapping in RMII Mode. 1: REF_CLK input mode, RMII1 mode 0: REF_CLK output mode, RMII2 mode Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).
13	RXC	O/PD	Receive Clock. This pin provides a continuous clock reference for RX_DV and RXD [0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
14	DVDD33	PWR	3.3V Digital Power Input. 3.3V power supply for digital circuit.
15	TXC	IO/PD	MII Mode Transmit Clock. This pin provides a continuous clock as a timing reference for TXD [3:0] and TXEN signals. TXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode RMII Mode Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The default direction is reference clock output mode if RXD[3]/CLK_CTL pin floating.
16	TXD[0]	I/PD	Transmit Data [0]
17	TXD[1]	I/PD	Transmit Data [1]
18	TXD[2]	I/PD	Transmit Data [2]
19	TXD[3]	I/PD	Transmit Data [3]
20	TX_EN	I/PD	MII/RMII Mode Transmit Enable. The input signal indicates the presence of valid nibble data on TXD [3:0]. An internal weakly pulled low resistor prevents the bus floating.
21	RESET_N	I/HZ	RESET. Active-low, reset pin for chip.
22	MDC	I/PU	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.

23	MDIO	IO/PU	Management Data Input/Output. This pin provides the bi-directional signal used to transfer management information
24	LED0/ PHYAD[0]	O/OD/ PD	LED 0, Link 10Mbps On, Active blink. PHY address 0 selection
25	LED1/ PHYAD[1]	O/PD	LED 1, Link 100Mbps On, Active blink. PHY address 1 selection
26	CRS/CRS_DV	O/PD	MI mode: Carrier Sense. This pin's signal is asserted high if the media is not in Idle state. RMII mode: Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non-idle.
27	COL	O/PD	Collision Detect. COL is asserted high when a collision is detected on the media.
28	RXER	O/PD	Receive Error.
29	DVDDL_REG	PWR/O	DVDDL Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
30	NC		NC
31	XTAL_IN	I/XT	25 MHz Crystal Oscillator Input Pin.
32	XTAL_OUT	O/XT	25 MHz Crystal Oscillator Output Pin. A continuous 25 MHz reference clock must be supplied to the chip by connecting a 25 MHz crystal between these two pins or by driving XTAL_IN with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTAL_OUT unconnected.
EPAD	EPAD	GND	Exposed ground pad on back of the chip, tie to ground

3.3 POWER ON STRAPPING

No.	Name	POS	Internal Pull/Down	Description
24	LED0/ PHYAD[0]	phy_address[0]	Pull Down	The power-on strapping value of PAD RXD1, wol_led_sel, determines the PAD LED0 working as LED0 or PMEB. Wol_led_sel=0, this PAD works as LED0, it could be external PU or PD, Wol_led_sel=1, this PAD works as PMEB, it shall be external pull-up, then phy_address[0] always =1;
25	LED1/ PHYAD[1]	phy_address[1]	Pull Down	The PHY address is 00000~00011 config by phy_address[1:0]
10	RXD[1]	Wol_led_sel (Wake on LAN selection)	Pull Down	The power-on strapping value of PAD RXD1, Wol_led_sel, determines the PAD LED0 working as LED0 or PMEB. 1, LED0 works as PMEB (WOL interrupt) 0, LED0 works as LED0.
12	RXD[3]/CLK_CTL	Clock control	Pull Down	The power-on strapping value of {RX_DV, RXD3} determines the xMII mode: {RX_DV, RXD3}=2'b00 means MII mode; {RX_DV, RXD3}=2'b01 means ReMII mode; {RX_DV, RXD3}=2'b10 means RMII2 mode; TXC 50Mhz reference clock is output {RX_DV, RXD3}=2'b11 means RMII1 mode; TXC 50Mhz reference clock is
8	RX_DV	MII mode selection	Pull Down	

				input

MODE CONFIG

Pin 8 RX_DV (PD)	Pin 12 RXD3 (PD)	Mode
0	0	MII
0	1	ReMII, Reverse MII Mode
1	0	RMII2, TXC 50Mhz reference clock is output by default
1	1	RMII1, TXC 50Mhz reference clock is input

PHY ADDRESS

Pin 24 LED0/ PHYAD[0] (PD)	Pin 25 LED1/ PHYAD[1] (PD)	PHY address
0	0	00000
0	1	00010
1	0	00001
1	1	00011

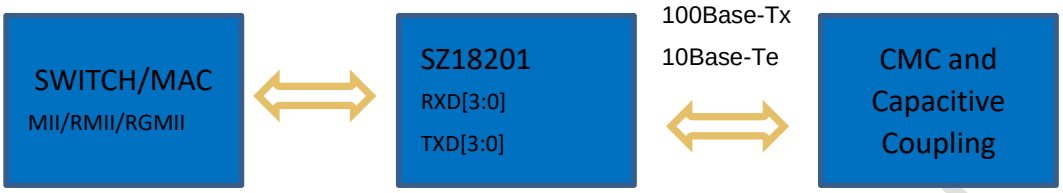
WAKE ON LAN SELECTION

Pin 10 RXD1 (PD)	Function	Mote
0	LED Mode	Pin 24 is LED0
1	WOL Mode	Pin 24 is PMEB, Must external pull up

4 FUNCTION DESCRIPTION

APPLICATION DIAGRAM

100BASE-TX/10BASE-TE APPLICATION



MII INTERFACE

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE-Te, 100BASE-TX,. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the SZ18201 supports a subset of MII signals. This subset includes all MII signals except TX_ER.

RMII INTERFACE

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock frequency.

MANAGEMENT INTERFACE

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

DAC

The digital-to-analog converter (DAC) transmits MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that reduces electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

ADC

Receive channel has its own analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital data path.

ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference (ISI) created by the channel. The equalizer accepts sampled data from the analog-to-digital converter (ADC) on channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

AUTO- NEGOTIATION

The SZ18201 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

a) Speed: 10/100Mbps

b) Duplex mode: full duplex and/or half duplex

c) Pause

Auto negotiation is initialized when the following scenarios happen:

a) Power-up/Hardware/Software reset

b) Auto negotiation restart

c) Transition from power-down to power up

d) Link down

Auto negotiation is enabled for SZ18201 by default, and can be disable by software control.

POLARITY DETECTION AND AUTO CORRECTION

SZ18201 can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

For 10BASE-Te/100BASE-TX, SZ18201 can handle both cable errors at the same time.

EEE

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

5 OPERATIONAL DESCRIPTION

RESET

SZ18201 have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. After RESET_N is released , SZ18201 latches input value on POS related pins are used as configuration information which provides flexibility in application without mdio access.

SZ18201 also provides a software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table.

PHY ADDRESS

For SZ18201, phy_address[1:0] is used to generate phy address.

Please refer to the POS setting as below. PHY address

Pin 24 LED0/ PHYAD[0] (PD)	Pin 25 LED1/ PHYAD[1] (PD)	PHY address
0	0	00000
0	1	00010
1	0	00001
1	1	00011

XMII INTERFACE

SZ18201 support 4 kinds of MII related interfaces: MII, RMII1, RMII2 and REMII.

MII

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE-Te, 100BASE-TX, The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the SZ18201 supports a subset of MII signals. This subset includes all MII signals except TX_ER. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz. TXC and RXC are output in this case.

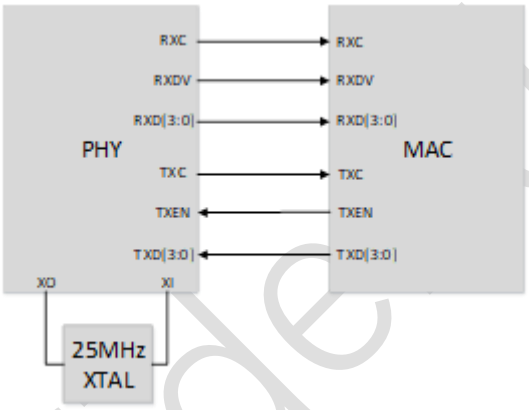


Figure . connection diagram of MII

RMII

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock speed compared to MII. It has 7 signals: REF_CLK, TX_EN, TXD[1:0], RX_DV and RXD[1:0]. In SZ18201, we use TXC as REF_CLK. For 100M application, REF_CLK is 50MHz; for 10M application, REF_CLK is still 50MHz, data will be duplicated for 10 times in 20ns cycles. SZ18201 supports two types of connection method;

1. RMII1 mode: This is fully conforming to RMII standard. SZ18201 can use clock from TXC as reference clock for pll. In this case, 25MHz crystal at XI/XO is not needed. Configure bit 6 of extended register(address 0h50) to 1 to enable this feature.

2. RMII2 mode: TXC will be 50MHz output to MAC, this can save one 50MHz clock source.

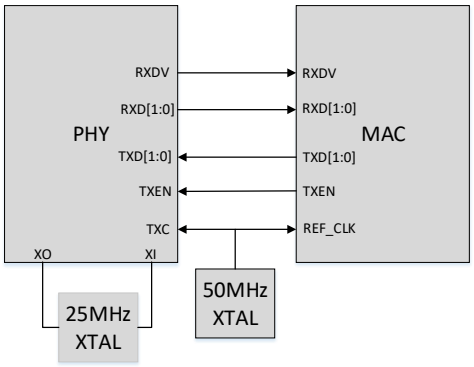


Figure .connection diagram of RMII1(with 25MHz and 50MHz clock)

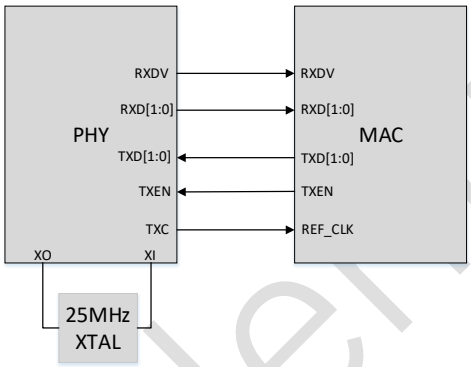


Figure .connection diagram of RMII2

REMII INTERFACE

Reverse media independent interface is the opposite of MII interface. The only difference is the direction of tx clock and rx clock. For MII, tx clock and rx clock are output; for REMII, tx clock and rx clock are input. REMII interface are used for back to back connection of two phys.

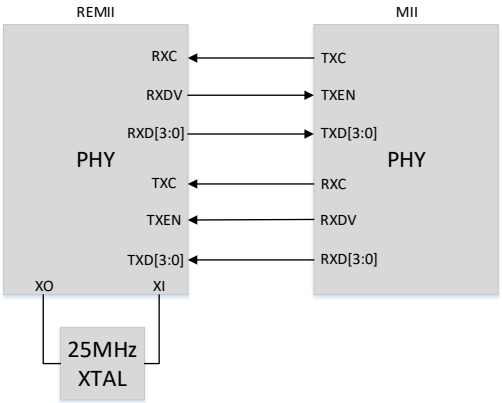


Figure .connection diagram of REMII

LOOPBACK MODE

There are three loopback modes in SZ18201.

INTERNAL LOOPBACK:

In Internal loopback mode, SZ18201 feed transmit data to receive path in chip.

Configure bit 14 of mii register(address 0h0) to enable internal loopback mode. For 10Base-Te and 100Base-Tx, SZ18201 feeds digital DAC data to ADC directly.

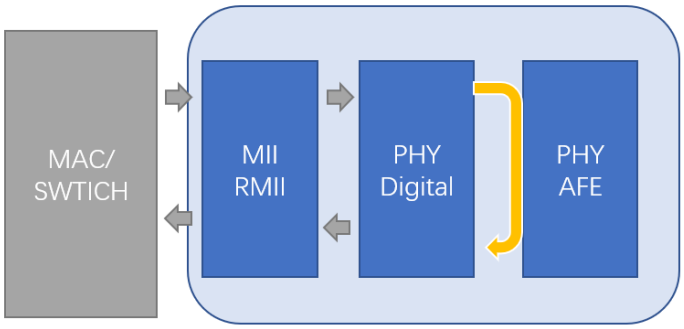


Figure . Internal loopback

EXTERNAL LOOPBACK

In external loopback mode, SZ18201 feed transmit data to receive path out of chip. For 10Base-Te and 100Base-Tx, just connect TRX_P0/N0 to TRX_P1/N1.

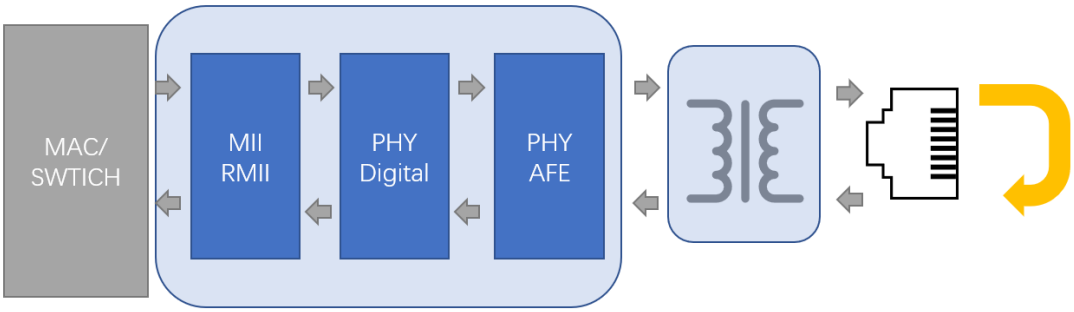


Figure . external loopback

REMOTE LOOPBACK

In remote loopback mode, SZ18201 feed MII receive data to transmit path in chip. Configure bit 11 of extended register(address 0h4000) and for TRX interface, just connect to link partner normally.

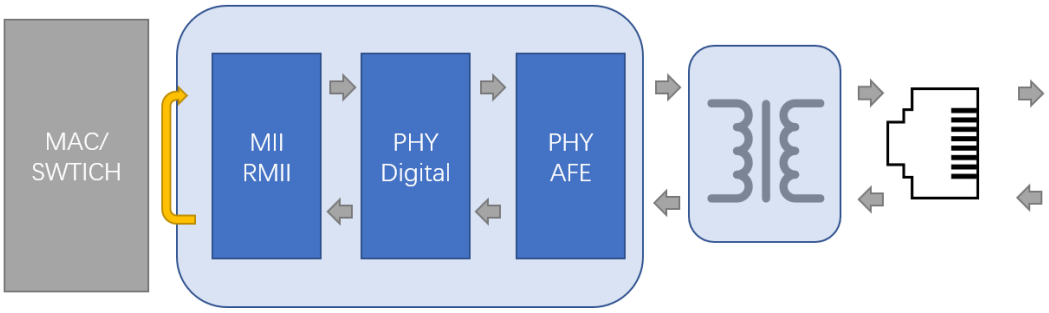


Figure . remote loopback

WOL WAKE ON LAN

WOL

Wake-on-LAN (WOL) is a mechanism to manage and regulate the total network power consumption.

WOL MECHANISM

SZ18201 supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin or general PHY interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waked up. The 48-bit MAC address is written in EXT 0x4004, 0x4005, 0x4006 registers.

For example, to write a specific MAC address (0xAAAABBBBCCCC) to PHY, write EXT 0x4004 = 0xAAAA, 0x4005 = 0xBBBB, and 0x4006 = 0xCCCC. The PHY internal MAC address can be set to any value.

NOTE: The MAC address is not a real MAC address and is only a symbol to indicate the content of the frame.

The WOL mechanism is enabled via EXT 0x4000 bit2. POS RXD[1] can't control enable or disable the WOL mechanism but only control pad LED0 working as WOL interrupt.

WOL INTERRUPT

SZ18201 support dedicated WOL interrupt pin. For 32-pin, when the pad RXD[1] is externally PULL UP, pad LED0 will work as WOL interrupt.

If EXT 0x4003 bit7 is 0, the dedicated WOL interrupt is programmed to a level, otherwise, it's programed to a pulse; either is active low. When it's programmed to a pulse, the pulse width can be programmed via EXT 0x4003 bit9:8.

WOL interrupt is also wire-and to general PHY interrupt RXD[2]_INTN (32-pin) when the bit6 INT_WOL in Interrupt enable register (MII Register 0x12) is set to 1. If the general PHY interrupt is triggered by WOL, it can be cleared by reading MII register 0x13 bit6.

NOTE:

When general PHY interrupt is used to monitor WOL interrupt, EXT 0x4003 bit7 should be 1, otherwise, the general PHY interrupt can't be read cleared.

Because PHY requires to receive packets from the line side, PHY cannot be powered down. If the link partner supports Energy Efficient Ethernet function, both ends can use EEE mode to save more power.

MII register 0x0 bit10 ISOLATE: When this bit is set to 1, the xMII output pins are HighZ. The xMII inputs are ignored.

6 REGISTER OVERVIEW

MII MANAGEMENT INTERFACE CLAUSE 22 REGISTER PROGRAMMING

The SZ18201 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 12.5 MHz must drive the MDC pin of the SZ18201. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

Notation	Description
RW	Read and write
SC	Self-clear
RO	Read only
LH	Latch high
LL	Latch Low
RC	Read clear
SWC	Software reset clear

MII REGISTERS

MII REGISTER 00H: BASIC CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	1'b0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	1'b0	Internal loopback control 1'b0: disable loopback 1'b1: enable loopback
13	Speed Selection(LSB)	RW	1'b0	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	1'b1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.

11	Power_down	RW SWC	1’b0	=1: Power down =0: Normal operation When the port is switched from power down to normal operation, software reset and Auto- Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW SWC	1’b0	Isolate phy from MII/RMII: PHY will not respond to xMII TXD/TX_EN, and present high impedance on RXD/RX_DV. 1’b0: Normal mode 1’b1: Isolate mode
9	Re_Autoneg	RW SWS SC	1’b0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART. =1: Restart Auto-Negotiation Process =0: Normal operation
8	Duplex_Mode	RW	1’b1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. =1: Full Duplex =0: Half Duplex
7	Collision_Test	RW SWC	1’b0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. =1: Enable COL signal test =0: Disable COL signal test
6	Speed_ Selection(MSB)	RW	1’b1	See bit13.

5:0	Reserved	RO	5'b0	Reserved. Write as 0, ignore on read

MII REGISTER 01H: BASIC STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	1'b0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	1'b1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	1'b1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	1'b1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	1'b1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	1'b0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	1'b0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	1'b1	Whether support extended status register in 0Fh 0: Not supported 1: Supported
7	Unidirect_Ability	RO	1'b0	1'b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1'b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	1'b1	1'b0: PHY will not accept management frames with preamble suppressed 1'b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	1'b0	1'b0: Auto-negotiation process not completed 1'b1: Auto-negotiation process completed

4	Remote_Fault	RO RC SWC LH	1'b0	1'b0: no remote fault condition detected 1'b1: remote fault condition detected
3	Autoneg_Ability	RO	1'b1	1'b0: PHY not able to perform Auto-negotiation 1'b1: PHY able to perform Auto-negotiation
2	Link_Status	RO LL SWC	1'b0	Link status 1'b0: Link is down 1'b1: Link is up
1	Jabber_Detect	RO RC LH SWC	1'b0	10BaseTe jabber detected 1'b0: no jabber condition detected 1'b1: Jabber condition detected
0	Extended_Capability	RO	1'b1	To indicate whether support EXTs, to access from address register 1Eh and data register 1Fh 1'b0: Not supported 1'b1: Supported

MII REGISTER 02H: PHY IDENTIFICATION REGISTER1

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	16'b0	Bits 3 to 18 of the Organizationally Unique Identifier

MII REGISTER 03H: PHY IDENTIFICATION REGISTER2

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	6'b0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	6'h12	
3:0	Revision_No	RO	4'h8	4 bits manufacturer's revision number

MII REGISTER 04H: AUTO-NEGOTIATION ADVERTISEMENT

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1'b0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed. =1: Advertise =0: Not advertised
14	Reserved	RO	1'b0	Reserved
13	Remote_Fault	RW	1'b0	=1: Set Remote Fault bit =0: Do not set Remote Fault bit
12	Extended_Next_Page	RW	1'b1	Extended next page enable control bit =1: Local device supports transmission of extended next pages =0: Local device does not support transmission of extended next pages.
11	Asymmetric_Pause	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Asymmetric Pause

				=0: No asymmetric Pause
10	Pause	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: MAC PAUSE implemented =0: MAC PAUSE not implemented
9	100BASE-T4	RO	1'b0	=1: Able to perform 100BASE-T4 =0: Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_ Full_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
7	100BASE-TX_ Half_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11]

				• Link goes down =1: Advertise =0: Not advertised
6	10BASE-Te_Full_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
5	10BASE-Te_Half_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
4:0	Selector_Field	RW	5'b00001	Selector Field mode. 00001 = IEEE 802.3

MII REGISTER 05H: AUTO-NEGOTIATION LINK PARTNER ABILITY

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	1'b0	Received Code Word Bit 15 =1: Link partner is capable of next page =0: Link partner is not capable of next page

14	ACK	RO SWC	1'b0	Acknowledge. Received Code Word Bit 14 =1: Link partner has received link code word =0: Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	1'b0	Remote Fault. Received Code Word Bit 13 =1: Link partner has detected remote fault =0: Link partner has not detected remote fault
12	RESERVED	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 11 =1: Link partner requests asymmetric pause =0: Link partner does not request asymmetric pause
10	PAUSE	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 10 =1: Link partner supports pause operation =0: Link partner does not support pause operation
9	100BASE-T4	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 9 =1: Link partner supports 100BASE-T4 =0: Link partner does not support100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 8 =1: Link partner supports 100BASE-TX full-duplex =0: Link partner does not support 100BASE-TX full-duplex
7	100BASE-TX_HALF_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 7 =1: Link partner supports 100BASE-TX

				half-duplex =0: Link partner does not support 100BASE-TX half-duplex
6	10BASE-Te_FULL_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 6 =1: Link partner supports 10BASE-Te full-duplex =0: Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 5 =1: Link partner supports 10BASE-Te half-duplex =0: Link partner does not support 10BASE-Te half-duplex
4:0	SELECTOR_FIELD	RO SWC	5'h0	Selector Field Received Code Word Bit 4:0

MII REGISTER 06H: AUTO-NEGOTIATION EXPANSION REGISTER

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	11'h0	Always 0
4	Parallel_Detection_fault	RO RC LH SWC	1'b0	=1: Fault is detected =0: No fault is detected
3	Link_partner_next_page able	RO LH SWC	1'b0	=1: Link partner supports Next page =0: Link partner does not support next page
2	Local_Next_Page_able	RO	1'b1	=1: Local Device supports Next Page =0: Local Device does not Next Page
1	Page_received	RO RC LH	1'b0	=1: A new page is received =0: No new page is received
0	Link_Partner_Auto_negotiation	RO	1'b0	=1: Link partner supports

	_able			auto-negotiation =0: Link partner does not support auto-negotiation

MII REGISTER 07H: AUTO-NEGOTIATION NEXT PAGE REGISTER

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1'b0	Transmit Code Word Bit 15 =1: The page is not the last page =0: The page is the last page
14	Reserved	RO	1'b0	Transmit Code Word Bit 14
13	Message_page_mode	RW	1'b1	Transmit Code Word Bit 13 =1: Message Page =0: Unformatted Page
12	Ack2	RW	1'b0	Transmit Code Word Bit 12 =1: Comply with message =0: Cannot comply with message
11	Toggle	RO	1'b0	Transmit Code Word Bit 11 =1: This bit in the previously exchanged Code Word is logic 0 =0: The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatte D_Field	RW	11'h1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

MII REGISTER 08H: AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER

Bit	Symbol	Access	Default	Description
15	Next_Page	RO	1'b0	Received Code Word Bit 15

				=1: This page is not the last page =0: This page is the last page
14	Reserved	RO	1'b0	Received Code Word Bit 14
13	Message_page_mode	RO	1'b0	Received Code Word Bit 13 =1: Message Page =0: Unformatted Page
12	Ack2	RO	1'b0	Received Code Word Bit 12 =1: Comply with message =0: Cannot comply with message
11	Toggle	RO	1'b0	Received Code Word Bit 11 =1: This bit in the previously exchanged Code Word is logic 0 =0: The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatte D_Field	RO	11'b0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

MII REGISTER 0AH: MASTER-SLAVE STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	Master_Slave_Config uration_Fault	RO RC SWC LH	1'b0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. =1: Master/Slave configuration fault detected =0: No fault detected
14	Master_Slave_Config uration_Resolution	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Local PHY configuration resolved to Master =0: Local PHY configuration resolved to Slave
13	Local_Receiver_Stat us	RO	1'b0	=1: Local Receiver OK =0: Local Receiver not OK

				Always 0.
12	Remote_Receiver_Status	RO	1'b0	=1: Remote Receiver OK =0: Remote Receiver not OK Always 0.
11	Link Partner_ 1000Base-T_Full_Duplex_Capability	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Link Partner supports 1000BASE-T half duplex =0: Link Partner does not support 1000BASE-T half duplex
10	Link_Partner_1000Base-T_Half_Duplex_Capability	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Link Partner supports 1000Base-T full duplex =0: Link Partner does not support 1000Base-T full duplex
9:8	Reserved	RO	2'b0	Always 0
7:0	Idle_Error_Count	RO SC	8'b0	Counter for Idle errors

MII REGISTER 0DH: MMD ACCESS CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15:14	Function	RW	2'b0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	9'b0	Always 0
4:0	DEVAD	RW	5'b0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

MII REGISTER 0EH: MMD ACCESS DATA REGISTER

Bit	Symbol	Access	Default	Description

15:0	Address_data	RW	16'b0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

MII REGISTER 0FH: EXTENDED STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO	1'b0	PHY not able to support 1000Base-X_Fd
14	1000Base-X_Hd	RO	1'b0	PHY not able to support 1000Base-X_Hd
13	1000Base-T_Fd	RO	1'b0	PHY not able to support 1000Base-T_Fd
12	1000Base-T_Hd	RO	1'b0	PHY not able to support 1000Base-T_Hd
11:8	Reserved	RO	1'b0	Reserved
7	100Base-T1	RO	1'b1	Reserved
6	1000Base-T1	RO	1'b0	Reserved
5:0	Reserved	RO	6'b0	Reserved

MII REGISTER 10H: PHY SPECIFIC FUNCTION CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	9'b0	Always 0.
6:5	Cross_md	RW	2'b11	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Int_polar_sel	RW	1'b0	No use.
3	Crs_on_tx	RW	1'b0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode:

				=1: Assert CRS on transmitting or receiving =0: Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	1'b0	=1: SQE test enabled =0: SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	1'b1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. =1: Polarity Reversal Enabled =0: Polarity Reversal Disabled
0	Dis_jab	RW	1'b0	Jabber takes effect only in 10BASE-Te =1: Disable jabber function =0: Enable jabber function

MII REGISTER 11H: PHY SPECIFIC STATUS REGISTER

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	2'b00	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	1'b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. =1: Full-duplex =0: Half-duplex
12	Page_Received_	RO	1'b0	=1: Page received

	real-time			=0: Page not received
11	Speed_and_Duplex_Resolved	RO	1’b0	This bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled =1: Resolved =0: Not resolved
10	Link_status_real-time	RO	1’b0	=1: Link up =0: Link down
9:7	Reserced	RO	3’b111	Always 3’b111.
6	MDI_Crossover_Status	RO	1’b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 “PHY specific function control register” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. =1: MDIX =0: MDI
5	Wirespeed_downgrade	RO	1’b0	=1: Downgrade =0: No Downgrade
4:2	Reserved	RO	3’b0	Always 0.
1	Polarity_Real_Time	RO	1’b0	=1: Reverted polarity =0: Normal polarity
0	Jabber_Real_Time	RO	1’b0	=1: Jabber is asserted. =0: No jabber

MII REGISTER 12H: INTERRUPT MASK REGISTER

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation_Error_int _mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
14	Speed_Changed_int_mask	RW	1’b0	=1: Interrupt enable

				=0: Interrupt disable
13	Duplex_changed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
12	Page_Received_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
11	Link_Failed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
10	Link_Succeed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
9	Reserved	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
8	Reserved	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
7	Reserved	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
6	WOL_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
5	Wirespeed_downgraded_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
4:2	Reserved	RW	3'b0	No used.
1	Polarity_changed_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable
0	Jabber_Happened_int_mask	RW	1'b0	=1: Interrupt enable =0: Interrupt disable

MII REGISTER 13H: INTERRUPT STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation_	RO RC	1'b0	Error can take place when any of the

	Error_INT			following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state =1: Auto-Negotiation Error takes place =0: No Auto-Negotiation Error takes place
14	Speed_Changed_INT	RO RC	1'b0	=1: Speed changed =0: Speed not changed
13	Duplex_changed_INT	RO RC	1'b0	=1: duplex changed =0: duplex not changed
12	Page_Received_INT	RO RC	1'b0	=1: Page received =0: Page not received
11	Link_Failed_INT	RO RC	1'b0	=1: Link down takes place =0: No link down takes place
10	Link_Succeed_INT	RO RC	1'b0	=1: Link up takes place =0: No link up takes place
9	Reserved	RO	1'b0	Always 0.
8	Reserved	RO	1'b0	Always 0.
7	Reserved	RO	1'b0	Always 0.
6	WOL_INT	RO RC	1'b0	=1: PHY received WOL magic frame. =0: PHY didn't receive WOL magic frame.
5	Wirespeed_downgraded_INT	RO RC	1'b0	=1: speed downgraded. =0: Speed didn't downgrade.

4:2	Reserved	RO	3'b0	Always 0.
1	Polarity_changed_INT	RO RC	1'b0	=1: PHY revered MDI polarity =0: PHY didn't revert MDI polarity
0	Jabber_Happened_INT	RO RC	1'b0	=1: 10BaseTe TX jabber happened =0: 10BaseTe TX jabber didn't happen

MII REGISTER 14H: SPEED AUTO DOWNGRADE CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	4'b0	Always 0.
11	En_mdio_latch	RW	1'b1	=1: To latch MII/MMD register's read out value during MDIO read =0: Do not latch MII/MMD register's read out value during MDIO read
10	Reserved	RW SC	1'b0	Reserved
9	Reserved	RW	1'b0	Reserved
8	Reserved	RW	1'b0	Reserved
7	Reserved	RW	1'b0	Reserved
6	Reserved	RW	1'b0	Reserved
5	En_speed_downgrade	RW	1'b1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre-downgrade	RW	3'b011	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits.
1	Bp_autospd_timer	RW	1'b0	=1: the wirespeed downgrade FSM will bypass the timer used for link stability check; =0: not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1.

0	Reserved	RO	1'b0	Always 0.

MII REGISTER 15H: RX ERROR COUNTER REGISTER

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	16'b0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over. If speed mode is 2'b01, it counts for fe_100 RX_ER; Else, it's 0.

MII REGISTER 1EH: DEBUG REGISTER'S ADDRESS OFFSET REGISTER

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Address _Offset	RW	16'h0	It's the address offset of the EXT that will be Write or Read

MII REGISTER 1FH: DEBUG REGISTER'S DATA REGISTER

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Datas	RW	16'b0	It's the data to be written to the EXT indicated by the address offset in register 0x1E, or the data read out from that debug register.

EXTENDED REGISTER

EXT 200AH: 10BT POWER CONTROL, REGISTER

Bit	Symbol	Access	Default	Description
15	Reserved	RW	1'b1	Reserved
14	Reserved	RW	1'b1	Reserved
13:12	Reserved	RW	2'boo	Reserved
11	Reserved	RW	1'b1	Reserved
10	En_10bt_idl	RW	1'b1	=1: In 10BT mode , if there's no data or NLP to transmit, shut off DAC; otherwise turn on the DAC; =0: In 10BT, DAC will not be turn off.
9	Reserved	RW	1'b1	Reserved
8:4	Reserved	RO	5'bo	Always 0.
3	Reserved	RW SWS	1'b1	Reserved
2:0	Reserved	RW SWC	3'bo	Reserved

EXT 4000H: EXTENDED COMBO CONTROL1

Bit	Symbol	Access	default	Description
15:13	Reserved	RO	3'b000	
12	Reserved	RW	1'b0	Reserved
11	Remote_Loopback	RW	1'b0	Remote loopback control 1'b0: disable 1'b1: enable
10:9	Reserved	RW	2'b0	Reserved
8	Reserved	RW	1'b0	Reserved
7:6	Reserved	RW	2'b00	Reserved

5	Jumbo_Enable	RW	1'b0	Enable Jumbo frame reception up to 18KB frame, when disabled only up to 4.5KB frame supported 0: disable jumbo frame reception 1: enable jumbo frame reception
4	Rmii_RX_DV_sel	RW	1'b0	Drive PAD CRS_DV of RMII by CRS_DV or RX_DV. 0: by CRS_DV 1: by RX_DV
3	Reserved	RW	1'b0	Reserved
2	Wol_en	RW	1'b0	1: enable WOL mechanism. 0: disable WOL.
1	Rmii_en	RW	1'b0	Its default value is determined by power on strapping. 1: enable RMII mode; 0: disable RMII mode.
0	Clk_sel	RW	1'b0	Its default value is determined by power on strapping. 1: input TXC/RXC; 0: output TXC/RXC. {rmii_en, clk_sel}: 2'b00: MII mode; 2'b01: REMII mode; 2'b10: RMII2 mode; 2'b11: RMII1 mode.

EXT 4001H: EXTENDED PAD CONTROL

Bit	Symbol	Access	default	Description
15	Output_int_or_wol	RW	1'b1	SZ18201, control to output general INTn or WOL INTn to PAD LED0_INTN_PMEB, when power on strapping value of RXD[1] is 1.

				1’b1: output general INTn; 1’b0: output WOL INTn.
14:8	Reserved	RW	7’b0	Reserved
7:6	Reserved	RW	2’b11	Reserved
5:4	Xmii_Dr	RW	2’b10	Xmii interface driver strength control in non-scan mode.
3:2	Mdio_Dr	RW	2’b11	Mdio pin driver strength control in non-scan mode.
1:0	Reserved	RW	2’b11	Reserved

EXT 4003H: EXTENDED COMBO CONTROL2

Bit	Symbol	Access	default	Description
15	Reserved	RW	1’b0	Reserved
14	Slave_jitter_test	RW	1’b0	Mux clk_dac to rxc in slave jitter test mode 1: enable 0: disable
13:10	Reserved	RW	4’b0	Reserved
9:7	Wol_lth_sel	RW	3’b100	Wol_lth_sel[0] control WOL INTn to be a level or a pulse. 1’b1: a pulse; 1’b0: a level. Wol_lth_sel[2:1] control WOL INTn pulse width when Wol_lth_sel[0] is 1. 2’b00: 10us; 2’b01: 100us; 2’b10: 1ms; 2’b11: 10ms.
6	En_isolate_txc	RW	1’b1	When isolate (mii.0.10) is 1, control to make TXC input or not. 1’b1: input; 1’b0: keep TXC previous direction.
5	En_isolate_rxc	RW	1’b1	When isolate (mii.0.10) is 1, control to make RXC input or not. 1’b1: input; 1’b0: keep RXC previous direction.
4:0	Reserved	RW	5’b01111	Reserved

EXT 4004H: WOL MAC ADDRESS

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[47:32]	RW	16'b0	

EXT 4005H: WOL MAC ADDRESS

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[31:16]	RW	16'b0	

EXT 4006H: WOL MAC ADDRESS

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[15:0]	RW	16'b0	

EXT 40A0H: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15	Pkg_chk_en	RW	1'b0	1: to enable RX/TX package checker. RX checker checks the MII data at transceiver's PCS RX; TX checker checks the MII data at mii_bridge's TX.
14	Pkg_en_gate	RW	1'b1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0; 0: not gate the clocks.
13	Bp_pkg_gen	RW	1'b1	1: normal mode, to send xMII TX data from PAD; 0: test mode, to send out the MII data generated by pkg_gen module.
12	Pkg_gen_en	RW SC	1'b0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1'b0. If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0; Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared.

11:8	Pkg_prm_lth	RW	4'd8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
7:4	Pkg_ipg_lth	RW	4'd12	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	1'b0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	Pkg_corrupt_crc	RW	1'b0	1: to make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.
1:0	Pkg_payload	RW	2'b0	Control the payload of the generated packages. 00: increased Byte payload; 01: random payload; 10: fix pattern 0x5AA55AA5… 11: reserved.

EXT 40A1H: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:0	Pkg_length	RW	16'd64	To set the length of the generated packages.

EXT 40A2H: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:0	Pkg_burst_size	RW	16'b0	To set the number of packages in a burst of package generation. 0: continuous packages will be generated.

EXT 40A3H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description

15:0	Pkg_ib_valid_high	RO	16'b0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

EXT 40A4H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_low	RO	16'b0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

EXT 40A5H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_high	RO	16'b0	Pkg_ib_os_good[31:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

EXT 40A6H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_low	RO	16'b0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

EXT 40A7H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_high	RO	16'b0	Pkg_ib_us_good[31:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

EXT 40A8H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description

15:0	Pkg_ib_us_good_low	RO	16'b0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

EXT 40A9H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_err	RO	16'b0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

EXT 40AAH: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_bad	RO	16'b0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.

EXT 40ABH: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_frag	RO	16'b0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

EXT 40ACH: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_nosfd	RO	16'b0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

EXT 40ADH: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_high	RO	16'b0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

EXT 40AEH: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_low	RO	16'b0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

EXT 40AFH: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_high	RO	16'b0	Pkg_ob_os_good[31:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

EXT 40B0H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_low	RO	16'b0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

EXT 40B1H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_high	RO	16'b0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

EXT 40B2H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_low	RO	16'b0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

EXT 40B3H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description

15:0	Pkg_ob_err	RO	16'b0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

EXT 40B4H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_bad	RO	16'b0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

EXT 40B5H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_frag	RO	16'b0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

EXT 40B6H: PKG_SELFTEST STATUS

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_nosfd	RO	16'b0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

EXT 40B7H: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:1	Reserved	RO	15'b0	
1	Pkgchk_txsrc_sel	RW	1'b0	Control the source of packages for pkg checker in TX direction to check. 1'b1: from pkg_gen; 1'b0: from xMII TX interface.
0	Pkgen_en_az	RW	1'b0	To send AZ LPI pattern during IPG of the packages sent by pkg_gen.

EXT 40B8H: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description

15:11	Reserved	RW	5'b0	No use.
10:0	Pkgen_pre_az_t	RW	11'b0	Control the IDLE time after traffic and before sending LPI_IDLE, in unit us. For Giga mode, only Pkgen_pre_az_t[8:0] is valid.

EXT 40B9H: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5'b0	No use.
10:0	Pkgen_in_az_t	RW	11'b0	Control the time sending LPI_IDLE, in unit us. For Giga mode, only Pkgen_in_az_t[8:0] is valid.

EXT 40BAH: PKG_SELFTEST CONTROL

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5'b0	No use.
10:0	Pkgen_aft_az_t	RW	11'b0	Control the IDLE time from end of LPI_IDLE to the beginning of next package. For Giga mode, only Pkgen_in_az_t[8:0] is valid.

EXT 40C0H: LED0 CONTROL

Bit	Symbol	Access	default	Description
15	Led_force_en	RW	1'b0	To enable LED force mode.

14:13	Led_force_mode	RW	2'b0	Valid when bit15 led_force_en is set. 00 = force LED OFF; 01 = force LED ON; 10 = force LED to blink at Blink Mode1; 11 = force LED to blink at Blink Mode2. There are 4 Blink Mode, which are different at blink frequency.
12	Led_act_blk_ind	RW	1'b0	When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON. when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status, =1: LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0; =0: LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.
11	Led_fdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up and duplex mode is full duplex, =1: make LED ON; =0: don't make LED ON;
10	Led_hdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up and duplex mode is half duplex, =1: make LED ON; =0: don't make LED ON;

9	Led_txact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
8	Led_rxact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
7	Led_txact_on_en	RW	1'b0	=1: if BLINK status is not activated, when PHY link up and TX is active, make LED ON at least 10ms;
6	Led_rxact_on_en	RW	1'b0	=1: if BLINK status is not activated, when PHY link up and RX is active, make LED ON at least 10ms;
5	Led_ht_on_en	RW	1'b0	=1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED ON;
4	Led_bt_on_en	RW	1'b1	=1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED ON;
3	Led_col_blk_en	RW	1'b0	=1: if PHY link up and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;
2	Led_ht_blk_en	RW	1'b0	=1: if PHY link up and speed mode is 100Mbps, make LED BLINK at Blink mode 2;
1	Led_bt_blk_en	RW	1'b0	=1: if PHY link up and speed mode is 10Mbps, make LED BLINK at Blink mode 3;
0	Dis_led_an_try	RW	1'b1	when PHY is active and auto-negotiation is at LINK_GOOD_CHECK status, =1: LED will be on; =0: LED will be off.

EXT 40C1H: LED0/1 CONTROL

Bit	Symbol	Access	default	Description
15:10	Reserved	RO	6'b0	Always 0.
9	Invert_led_duty	RW	1'b0	=1: to invert the duty cycle of ON and OFF, namely make LED ON time short and OFF time long.
8	Lpbk_led_dis	RW	1'b0	=1: In internal loopback mode, LED will not blink; =0: In internal loopback mode, LED will still blink if it's configured to blink on activity.
7	Jabber_led_dis	RW	1'b1	=1: when 10Mbps Jabber happens, LED will not blink; =0: when 10Mbps Jabber happens, LED will still blink if it's configured to blink on TX.
6	Col_blk_sel	RW	1'b1	=1: when collision happens, LED blink at Blink Mode2 with higher frequency; =0: when collision happens, LED blink at Blink Mode1 with lower frequency;
5	En_led_act_level	RW	1'b0	=1: to make LED blink at different frequency (Blink mode 0) when traffic weight is high. =0: to make LED blink always at Blink mode 1 no matter what the traffic weight is.
4:0	Led_act_level_th	RW	5'd12	Traffic is heavy or not's threshold. RX/TX traffic is monitored separately. In 1s interval, if RX or TX traffic active time > Led_act_level_th*42ms, then the traffic is heavy; otherwise, traffic is not heavy.

EXT 40C2H: LED0/1 CONTROL

Bit	Symbol	Access	default	Description

15:12	Freq_sel_c0	RW	4'd14	Control the LED blink frequency in Blink mode 0. ON/OFF duty cycle could be reverted by 40C1h bit9 invert_led_duty. Below description is the default ON/OFF cycle, that is invert_led_duty=0. 4'd0=LED blink once every 10s, 6% OFF; 4'd1=LED blink once every 9.4s, 7% OFF; 4'd2=LED blink once every 8s, 8% OFF; 4'd3=LED blink once every 7.4s, 9% OFF; 4'd4=LED blink once every 6s, 11% OFF; 4'd5=LED blink once every 5s, 6% OFF; 4'd6=LED blink once every 4s, 8% OFF; 4'd7=LED blink once every 3s, 11% OFF; 4'd8=LED blink once every 2s, 16% OFF; 4'd9=LED blink once every 1s, 16% OFF; 4'd10=LED blink at 2Hz, 50% OFF; 4'd11=LED blink at 3Hz, 50% OFF; 4'd12=LED blink at 4Hz, 50% OFF; 4'd13=LED blink at 6Hz, 50% OFF; 4'd14=LED blink at 8Hz, 50% OFF; 4'd15=LED blink at 10Hz, 50% OFF;
11:8	Freq_sel_c1	RW	4'd12	Control the LED blink frequency in Blink mode 1. See description in bit15~12 Freq_sel_c0 for detail.
7:4	Freq_sel_c2	RW	4'd7	Control the LED blink frequency in Blink mode 2. See description in bit15~12 Freq_sel_c0 for detail.
3:0	Freq_sel_c3	RW	4'd5	Control the LED blink frequency in Blink mode 3. See description in bit15~12 Freq_sel_c0 for detail.

EXT 40C3H: LED1 CONTROL

Bit	Symbol	Access	default	Description

15	Led_force_en	RW	1'b0	To enable LED force mode.
14:13	Led_force_mode	RW	2'b0	Valid when bit15 led_force_en is set. 00 = force LED OFF; 01 = force LED ON; 10 = force LED to blink at Blink Mode1; 11 = force LED to blink at Blink Mode2. There are 4 Blink Mode, which are different at blink frequency.
12	Led_act_blk_ind	RW	1'b0	When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON. when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status, =1: LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0; =0: LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.
11	Led_fdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up at FE and duplex mode is full duplex, =1: make LED ON; =0: don't make LED ON;
10	Led_hdx_on_en	RW	1'b0	If BLINK status is not activated, when PHY link up at FE and duplex mode is half duplex, =1: make LED ON; =0: don't make LED ON;

9	Led_txact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up at either AE or FE and TX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
8	Led_rxact_blk_en	RW	1'b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up at either AE or FE and RX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don't make LED BLINK.
7	Led_txact_on_en	RW	1'b0	=1: if BLINK status is not activated, when PHY link up at either AE or FE and TX is active, make LED ON at least 10ms;
6	Led_rxact_on_en	RW	1'b0	=1: if BLINK status is not activated, when PHY link up at either AE or FE and RX is active, make LED ON at least 10ms;
5	Led_ht_on_en	RW	1'b1	=1: if BLINK status is not activated, when PHY link up at AE or FE and speed mode is 100Mbps, make LED ON;
4	Led_bt_on_en	RW	1'b0	=1: if BLINK status is not activated, when PHY link up at AE or FE and speed mode is 10Mbps, make LED ON;
3	Led_col_blk_en	RW	1'b0	=1: if PHY link up at FE and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;
2	Led_ht_blk_en	RW	1'b0	=1: if PHY link up at AE or FE and speed mode is 100Mbps, make LED BLINK at Blink mode 2;
1	Led_bt_blk_en	RW	1'b0	=1: if PHY link up at AE or FE and speed mode is 10Mbps, make LED BLINK at Blink mode 3;
0	Reserved	RO	1'b0	Always 0.

7 TIMING AND ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Unit
DVDD33	3.3 V power supply	-0.3	3.70	V
AVDD33	3.3 V power supply	-0.3	3.70	V
AVDDL	1.2 V power supply	-0.2	1.50	V
DVDDL	1.2 V power supply	-0.2	1.50	V

RECOMMENDED OPERATING CONDITION

Description	Pins	Min	Typ	Max	Unit
Power supply	DVDD33	2.97	3.30	3.63	V
	AVDD33	2.97	3.30	3.63	V
	AVDDL	1.08	1.20	1.32	V
	DVDDL	1.08	1.20	1.32	V
SZ18201 Ambient Operation Temperature Ta		0	-	70	℃
Maximum Junction Temperature				125	℃

CRYSTAL REQUIREMENT

Symbol	Description	Min	Typ	Max	Unit
F ref	Crystal Reference Frequency	-	25	-	MHz
F ref Tolerance	Crystal Reference Frequency tolerance	-50	-	50	ppm
Duty Cycle	Reference clock input duty cycle	40	-	60	%
ESR	Equivalent Series Resistance	-		50	ohm
DL	Drive Level	-	-	0.5	mW
Vih	Crystal output high level	1.4	-	-	V
Vil	Crystal output low level	-	-	0.4	V

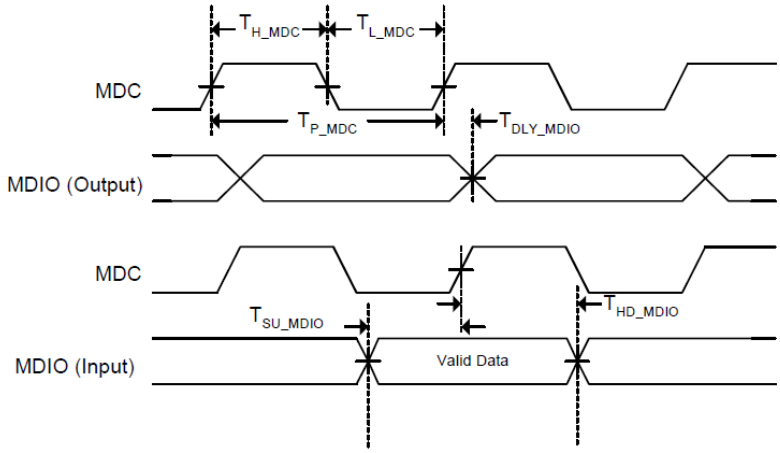
OSCILLATOR/EXTERNAL CLOCK REQUIREMENT

Parameter	Condition	Min	Typ	Max	Unit
Frequency			25		MHz
Frequency tolerance	Ta= -40~85 C	-50		50	PPM
Duty Cycle		40	-	60	%
Peak to Peak Jitter				200	ps
Vih		1.4		AVDD33+0.3	V
Vil				0.4	V
Rise Time	10%~90%			10	ns
Fall Time	10%~90%			10	ns
Temperature Range		0		70	℃

DC CHARACTERISTICS

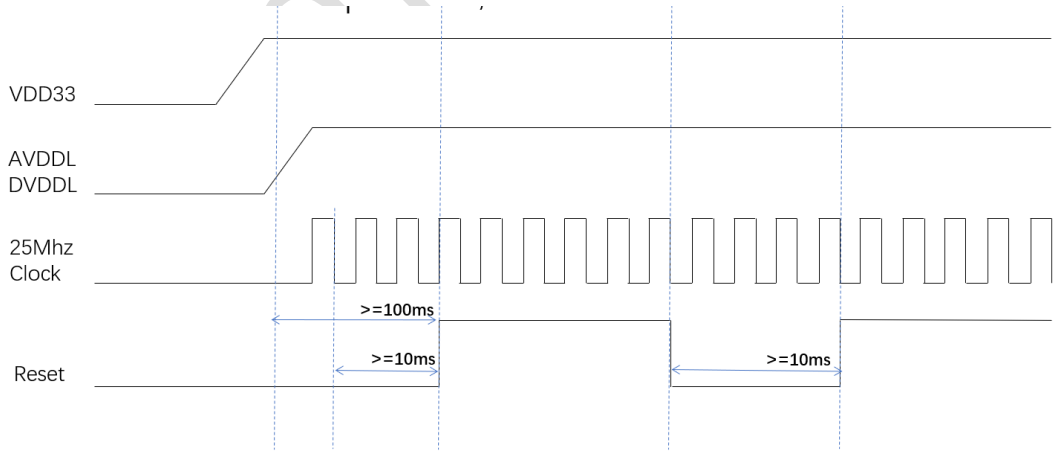
Symbol	Description	Min	Typ	Max	Unit
DVDD33	3.3V power supply	2.97	3.3	3.63	V
AVDD33	3.3V power supply	2.97	3.3	3.63	V
DVDDL	1.2V power supply	1.08	1.2	1.32	V
AVDDL	1.2V power supply	1.08	1.2	1.32	V
Voh 3.3V	Minimum High Level Voltage Output Voltage	2.4	-	3.6	V
Vol 3.3V	Minimum Low Level Voltage Output Voltage	-0.3	-	0.4	V
Vih 3.3V	Maximum High Level Input Voltage	2	-	-	V
Vil 3.3V	Maximum Low Level Input Voltage	-	-	0.8	V

MDC/MDIO TIMING



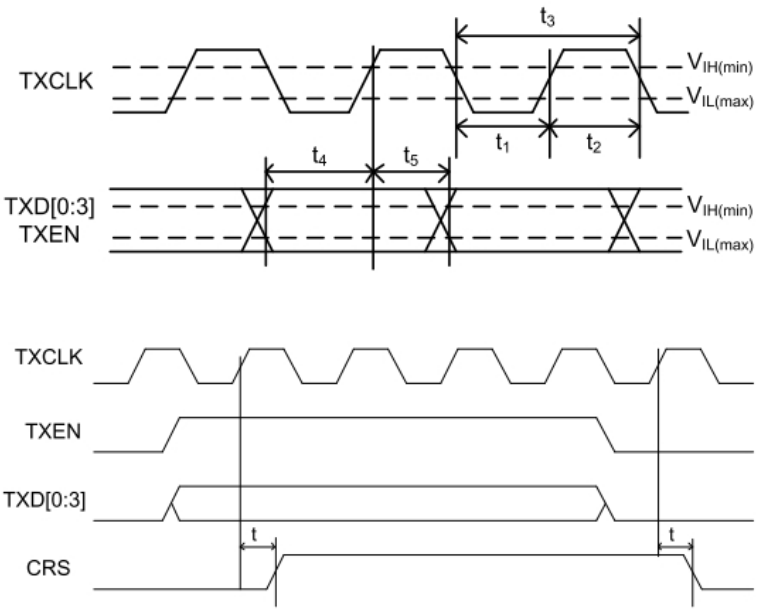
Symbol	Description	Min	Typ	Max	Unit
T DLY_MDIO	MDC to MDIO Output Delay Time			20	ns
T SU_MDIO	MDIO Input to MDC Setup Time	10			ns
T HD_MDIO	MDIO Input to MDC Hold Time	10			ns
T P_MDC	MDC Period	80			ns
T H_MDC	MDC High	30			ns
T L_MDC	MDC Low	30			ns
Maximum Frequency = 12.5M Hz					

POWER ON SEQUENCE/CLOCK/RESET



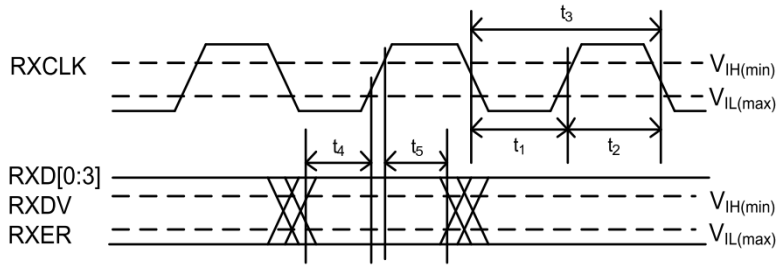
When using crystal, the clock is generated internally after power is stable. For a reliable power on reset, suggest to keep asserting the reset low long enough (100ms) to ensure the clock is stable and clock-to-reset 10ms requirement is satisfied.

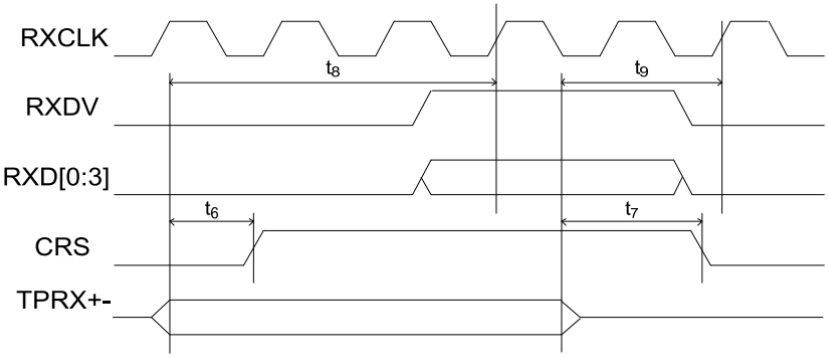
MII TRANSMISSION CYCLE TIMING



Symbol	Description		Minimum	Typical	Maximum	Unit
t1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	5	-	-	ns
t5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	-	-	ns
		10Mbps	0	-	-	ns
t6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns

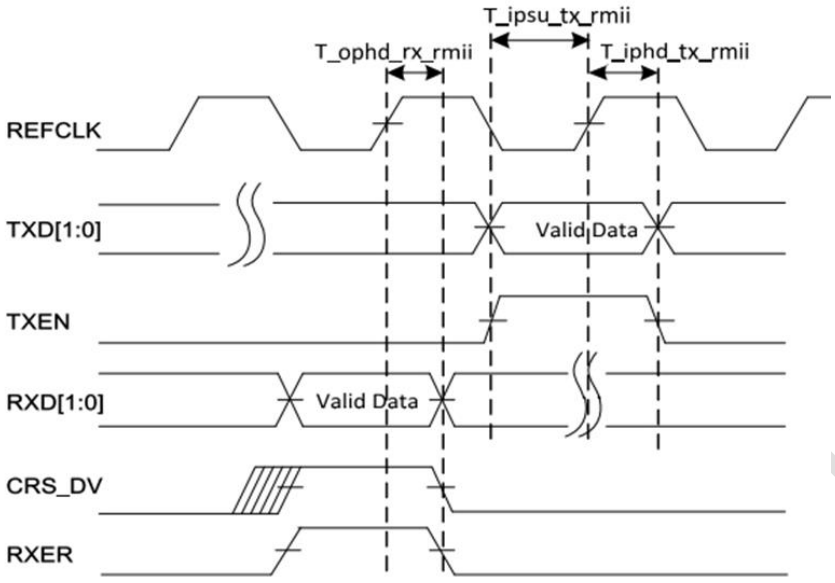
MII RECEPTION CYCLE TIMING





Symbol	Description		Minimum	Typical	Maximum	Unit
t1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	14 0	200	260	ns
t2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	14 0	200	260	ns
t3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	RXER, RX_DV,RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t5	RXER, RX_DV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t8	Receive Frame to Sampled Edge of RX_DV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t9	End of Receive Frame to Sampled Edge of RX_DV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

RMII TRANSMISSION AND RECEPTION CYCLE TIMING



Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	2	-	-	ns

8 POWER REQUIREMENTS

POWER CONSUMPTION

MII MODE

Condition		3.3V(Pull up)	AVDD33	DVDD33	3.3V total(mA)
Reset		0	5.2	0	5.2
Power down		0	5.4	0.1	5.5
Hibernation		0	6	0.1	6.1
Active		0	44.3	0.7	45
Link	10M	4.2	19.3	0.6	24.1
	100M	3.9	56.6	4.9	65.4
Traffic	10M	1.9	37.9	0.8	40.6
	100M	1.8	56.7	6	65.5

RMII MODE

Condition		3.3V(Pull up)	AVDD33	DVDD33	3.3V total(mA)
Reset		0	5.2	0	5.2
Power down		0	5.4	0.1	5.5
Hibernation		0	6	0	6
Active		0	44.3	0	44.3
Link	10M	4.1	19.4	0.1	23.6
	100M	3.9	56.6	0.2	60.7
Traffic	10M	2.2	37.2	0.3	39.7
	100M	2.1	56.8	1.1	60.9

Unit is mA

9 PACKAGE INFORMATION

ROHS-COMPLIANT PACKAGING

Motor-comm offers an RoHS package that is compliant with RoHS

Part Number	Status	Package Qty	Op temp (℃)	Note
SZ18201	Active	3000; Tape & Reel, Tray	0 to 70	

THERMAL RESISTANCE

θ_{JA} = 37.8 ℃/W (T_A =25 ℃)

θ_{JA} = 33.3 ℃/W (T_A =100 ℃)

θ_{JB} = 16.3 ℃/W

θ_{JC} = 35 ℃/W

Terminology:

(1) θ_{JA} , Junction-to-ambient thermal resistance

$$\theta_{JA} = (T_J - T_A)/ P_H$$

where θ_{JA} = thermal resistance from junction-to-ambient (°C/W)

T_J = junction temperature when the device has achieved a steady-state after application of P_H (°C)

T_a = ambient temperature (°C)

P_H = power dissipation that produced change in junction temperature (W)

(2) θ_{JB}, junction-to-board thermal resistance

$$\theta_{JB} = (T_J - T_B)/ P_H$$

where θ_{JB}=thermal resistance from junction-to-board as described by this specification(°C/W)

T_J = junction temperature when the device has achieved a steady-state after application of P_H (°C)

T_B = board temperature at steady state(°C)

P_H = power dissipation that produced change in junction temperature (W)

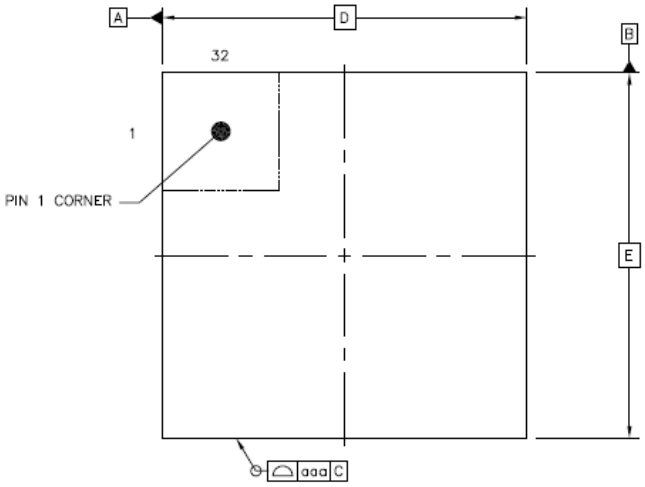
(3) θ_{JC}, junction-to-case thermal resistance

$$\theta_{JC} = (T_J - T_C)/ P_H$$

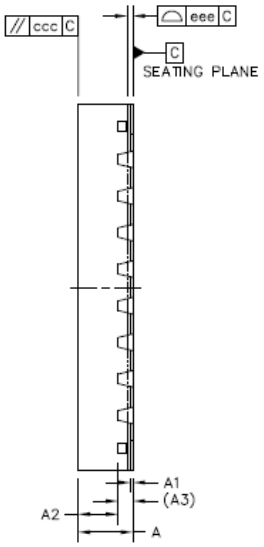
where T_C = case temperature attached with a cold plate

θ_{JC} represents the resistance to the heat flows from the chip to package top case. θJC is important when external heat sink is attached on package top.

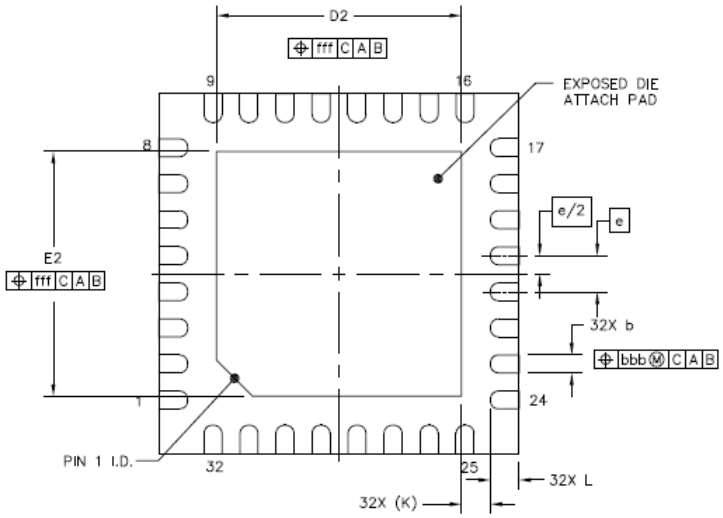
10 MECHANICAL INFORMATION



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

11 ORDERING INFORMATION

Part Number	Grade	Package	Packaging	Status	Operation temp(℃)
SZ18201	Consumer	QFN 32 5x5mm	Tape & Reel, Tray	Mass Production	0 to 70 ℃