

DS0134
Datasheet
SmartFusion2 SoC FPGA and IGLOO2 FPGA
Automotive Grade 2



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SmartFusion2 and IGLOO2 Automotive Grade 2 AC/DC Electrical Characteristics

1. Introduction

Microsemi's automotive grade SmartFusion[®]2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO[®]2 FPGA families offer the best-in-class security, industry leading high reliability and lowest static power in a flash-based fabric. With a strong heritage of supplying to Military and Aviation customers, Microsemi automotive grade devices are ideally suited to meet the demands of the automotive industry providing the lowest total-cost-of-ownership. These next-generation devices integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, high-performance SERDES communications interfaces on a single chip with extended temperature support.

Automotive grade SmartFusion2 and IGLOO2 devices offer up to 90 K Logic Elements, up to 5 MB of embedded RAM, up to 4 SERDES lanes, up to 2 PCIe endpoints and integrated hard DDR3 memory controllers with single error correct and double error detect. IGLOO2 automotive grade devices integrate a high-performance memory subsystem (HPMS) with on-chip flash, 32 kbyte embedded SRAM, and multiple DMA controllers. SmartFusion2 automotive grade SoC FPGAs provide a low-power real time microcontroller subsystem (MSS) with an embedded ARM Cortex-M3 encapsulating the benefits of HPMS along with a rich set of industry standard peripherals including Ethernet, USB, and CAN.

SmartFusion2 and IGLOO2 FPGAs are the best alternative to ASICs and SRAM based FPGAs with their advantages of Zero FIT reliability, tamper-free advanced security, industry's lowest static power and supply assurance for long product lifetime support.

2. Device Status

The following SmartFusion2 and IGLOO2 devices are available. For more information on device status, refer to the "[Datasheet Categories](#)".

Table 1 • IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status

Design Security Device Densities	Status
005S	Production
010TS	Production
025TS	Production
060TS	Production
090TS	Production

3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

- [PB0135: Automotive Grade IGLOO2 FPGAs Product Brief](#)
- [DS0124: IGLOO2 Pin Descriptions](#)
- [PB0136: Automotive Grade SmartFusion2 SoC FPGAs Product Brief](#)
- [DS0115: SmartFusion2 Pin Descriptions](#)

4. General Specifications

4.1 Operating Conditions

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in [Table 2](#) is not implied.

Table 2 • Absolute Maximum Ratings

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC core supply voltage. Must always power this pin.	-0.3	1.32	V	-
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	-0.3	3.63	V	-
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	-0.3	3.63	V	-
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	-0.3	3.63	V	-
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	-0.3	3.63	V	-
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	-0.3	3.63	V	-
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	-0.3	3.63	V	-
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	-0.3	3.63	V	-
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	-0.3	3.63	V	-
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	-0.3	2.75	V	-
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	-0.3	1.32	V	-
SERDES_[01]_VDD	PCIe/PCS power supply	-0.3	1.32	V	-
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	-0.3	3.63	V	-
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	-0.3	2.75	V	-
VI	I/O Input voltage for MSIO I/O Bank	-0.3	3.63	V	-
	I/O Input voltage for MSIOD/DDRIO I/O Bank	-0.3	2.75	V	-
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	-0.3	3.63	V	-
T _{STG}	Storage temperature	-65	150	°C	*
T _J	Junction temperature	-	145	°C	-

Note: * For flash programming and retention maximum limits, refer to [Table 4 on page 5](#). For recommended operating conditions, refer to [Table 3 on page 3](#).

Table 3 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Tj	Operating Junction Temperature	Automotive Grade 2	-40	25	125	°C	–
	Programming Junction Temperature	–	0	25	85	°C	–
		–	-40	25	100	°C	1
VDD	DC core supply voltage. Must always power this pin.	–	1.14	1.2	1.26	V	–
VPP	Power Supply for Charge Pumps (for Normal Operation and Programming) for 010, 025, and 060 Devices	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
	Power Supply for Charge Pumps (for Normal Operation and Programming) for 090 devices	3.3 V Range	3.15	3.3	3.45	V	–
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0-5	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V Range	2.375	2.5	2.625	V	2
		3.3 V Range	3.15	3.3	3.45	V	2

Table 3 • Recommended Operating Conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lanes 0-3. It is a +2.5 V SERDES internal PLL supply.	–	2.375	2.5	2.625	V	–
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. It is a +1.2 V SERDES PMA supply.	–	1.14	1.2	1.26	V	–
SERDES_[01]_VDD	PCIe/PCS Power supply	–	1.14	1.2	1.26	V	–
VDDIx	1.2 V DC supply voltage	–	1.14	1.2	1.26	V	–
	1.5 V DC supply voltage	–	1.425	1.5	1.575	V	–
	1.8 V DC supply voltage	–	1.71	1.8	1.89	V	–
	2.5 V DC supply voltage	–	2.375	2.5	2.625	V	–
	3.3 V DC supply voltage (3.3 V only available in MSIO)	–	3.15	3.3	3.45	V	–
	LVDS differential I/O	–	2.375	2.5	3.45	V	–
	BLVDS, MLVDS, Mini-LVDS, RSDS differential I/O	–	2.375	2.5	2.625	V	–
	LVPECL differential I/O	–	3.15	3.3	3.45	V	–
VREFx	Reference Voltage Supply for FDDR (Bank0) and MDDR(Bank5)	–	0.49 × VDDIx	0.5 × VDDIx	0.51 × VDDIx	V	–
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–

Notes:

1. Programming at this temperature range is available only with VPP in 3.3 V Range
2. Power supply ramps must all be strictly monotonic, without plateaus.
3. PLL supply voltages should be either 2.5 V or 3.3 V. Mixed voltages are not allowed.

Table 4 • FPGA Operating Limits

Product Grade	Element	Programming Temperature	Operating Temperature	Programming Cycles	Digest Temperature	Digest Cycle	Retention (Biased/Unbiased)
Automotive Grade 2 ^{1,2}	FPGA	Min T _J = 0°C Max T _J = 85°C	Min T _J = -40°C Max T _J = 125°C	500	Min T _J = -40°C Max T _J = 100°C	2000	10 Years
		Min T _J = -40°C Max T _J = 100°C	Min T _J = -40°C Max T _J = 125°C	500	Min T _J = -40°C Max T _J = 100°C	2000	10 Years

1. The retention specification is defined as the total number of programming and digest cycles. For example, 10 years of retention after 500 programming cycles. If your product qualification requires accelerated programming cycles, see Microsemi SoC Products Quality and Reliability Report about recommended methodologies.
2. Programming at Industrial temperature range is available only with VPP in 3.3V Range

Table 5 • Embedded Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Automotive Grade 2	Embedded flash	Min T _J = -40°C Max T _J = 125°C	Min T _J = -40°C Max T _J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • Device Storage Temperature and Retention

Product Grade	Storage Temperature (T _{stg})	Retention
Automotive Grade 2	Min T _J = -40°C Max T _J = 125°C	10 Years

Table 7 • High Temperature Data Retention (HTR) Lifetime

T _J (C)	HTR Lifetime* (Years)
90	20.0
95	20.0
100	20.0
105	17.0
110	15.0
115	13.0
120	11.5
125	10.0
130	8.0
135	6.0
140	4.5
145	3.0
150	1.5

Note: * HTR Lifetime is the period during which a verify failure is not expected due to flash leakage.

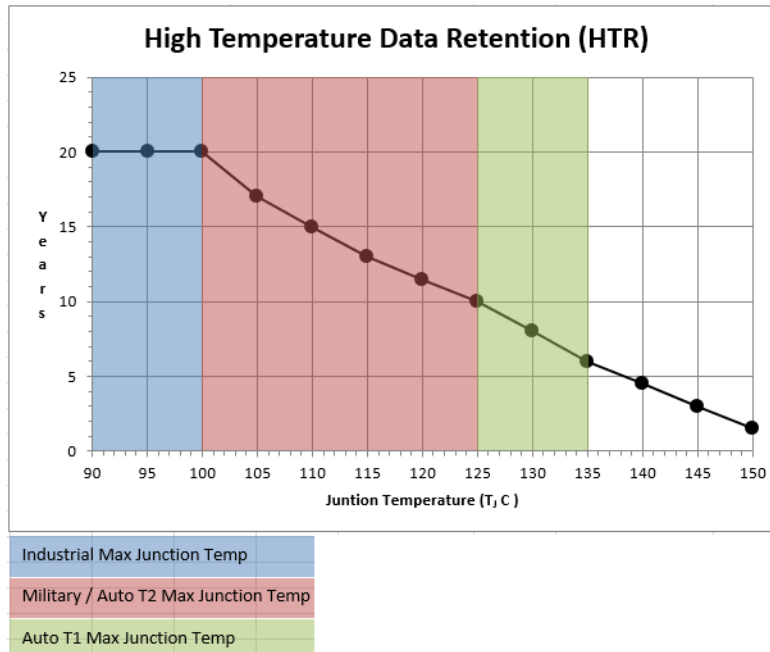


Figure 1 • High Temperature Data Retention (HTR)

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to V_{CCI} + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3 Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad \text{EQ 1}$$

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad \text{EQ 2}$$

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{EQ 3}$$

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)
- T_C = Case temperature
- P = Total power dissipated by the device

Table 8 • Package Thermal Resistance

Product M2GL/M2S	θ_{JA}			θ_{JB}	θ_{JC}	Units
	Still Air	1.0 m/s	2.5 m/s			
005						
FGG484	19.36	15.81	14.63	9.74	5.27	°C/W
VFG256	41.30	38.16	35.30	28.41	3.94	°C/W
VFG400	20.19	16.94	15.41	8.86	4.95	°C/W
010						
FGG484	18.22	14.83	13.62	8.83	4.92	°C/W
VFG256	37.36	34.26	31.45	24.84	7.89	°C/W
VFG400	19.40	15.75	14.22	8.11	4.22	°C/W
025						
FGG484	17.03	13.66	12.45	7.66	4.18	°C/W
VFG256	33.85	30.59	27.85	21.63	6.13	°C/W
VFG400	18.36	14.89	13.36	7.12	3.41	°C/W
060						
FGG484	15.40	12.06	10.85	6.14	3.15	°C/W
VFG400	17.45	14.01	12.47	6.22	2.69	°C/W
FGG676	15.49	12.21	11.06	7.07	3.87	°C/W
090						
FGG484	14.64	11.37	10.16	5.43	2.77	°C/W
FGG676	14.52	11.19	10.37	6.17	3.24	°C/W

4.3.2 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using [EQ 4](#).

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 125°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL060TS-1FGG484 package at Automotive Grade 2 temperature and in still air, where:

$$\theta_{JA} = 15.4^{\circ}\text{C/W (taken from Table 8 on page 7).}$$

$$T_A = 105^{\circ}\text{C}$$

$$\text{Maximum Power Allowed} = \frac{125^{\circ}\text{C} - 105^{\circ}\text{C}}{15.4^{\circ}\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

4.3.3 Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

4.3.4 Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition.

This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

5. Power Consumption

5.1 Quiescent Supply Current

Table 9 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze Mode	Flash*Freeze Mode	
FPGA Core	On	Off	–
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	–
MDDR_PLL_VDDA CCC_XX[01]_PLL_VDDA PLL0_PLL1_MDDR_VDDA FDDR_PLL_VDDA	0 V	0 V	–
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIIO	On	On	3
VDDix	On	On	2, 4
VREFx	On	On	–

Table 9 • Quiescent Supply Current Characteristics (continued)

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze Mode	Flash*Freeze Mode	
MSSDDR CLK	32 kHz	32 kHz	–
RAM	On	Sleep state	–
HPMS Controller	50 MHz	50 MHz	–
50 MHz Oscillator (enable/disable)	Enabled	Disabled	–
1 MHz Oscillator (enable/disable)	Disabled	Disabled	–
Crystal Oscillator (enable/disable)	Disabled	Disabled	–

Notes:

- SERDES_[01]_VDD Power Supply is shorted to VDD.
- VDDix has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the “Recommendation for Unused Bank Supplies” table in the AC393: SmartFusion2 and IGLOO2 Board Design Guidelines Application Note.
- SERDES and DDR blocks to be unused.
- No Differential (that is to say, LVDS) I/O's or ODT attributes to be used.

Table 10 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process

Parameter	Modes	Conditions	005	010	025	060	090	Units
			VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	
IDC1	Non-Flash*Freeze	Typical (T _J = 25°C)	6.2	6.9	8.9	15.3	15.4	mA
		Automotive Grade 2 (T _J = 125°C)	60.9	73.0	106.4	215.4	217.5	mA
IDC2	Flash*Freeze	Typical (T _J = 25°C)	1.4	2.6	3.7	5.0	5.1	mA
		Automotive Grade 2 (T _J = 125°C)	33.5	55.6	74.2	98.5	99.5	mA

Table 11 • SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process

Parameter	Modes	Conditions	005	010	025	060	090	Units
			VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	VDD=1.26 V	
IDC1	Non-Flash*Freeze	Automotive Grade 2 (T _J = 125°C)	114.9	151.5	227.4	438.8	443.1	mA
IDC2	Flash*Freeze	Automotive Grade 2 (T _J = 125°C)	81.1	127.2	144.2	193.1	195.0	mA

5.2. Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 12 • Currents During Program Cycle, $0^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$, Typical Process

Power Supplies	Voltage (V)	005	010	025	060	090	Units
VDD	1.26	46	53	55	30	42	mA
VPP	3.46	8	11	6	9	12	mA
VPPNVM	3.46	1	2	2	3	3	mA
VDDI	2.62	31	16	17	12	12	mA
	3.46	62	31	36	12	17	mA
Number of banks		7	8	8	10	9	–

Table 13 • Currents During Verify Cycle, $0^{\circ}\text{C} \leq T_J \leq 85^{\circ}\text{C}$, Typical Process

Power Supplies	Voltage (V)	005	010	025	060	090	Units
VDD	1.26	44	53	55	33	41	mA
VPP	3.46	6	5	3	8	11	mA
VPPNVM	3.46	1	0	0	0	1	mA
VDDI	2.62	31	16	17	12	11	mA
	3.46	61	32	36	12	17	mA
Number of banks		7	8	8	10	9	–

Table 14 • Inrush Currents at Power up, $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$, Typical Process

Power Supplies	Voltage (V)	005	010	025	060	090	Units
VDD	1.26	36	53	78	54	98	mA
VPP	3.46	35	57	50	14	36	mA
VDDI	2.62	134	141	161	106	283	mA
Number of banks		7	8	8	10	9	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 15 • Average Temperature and Voltage Derating Factors for Fabric Timing Delays (Normalized to $T_J = 125^{\circ}\text{C}$, Worst-Case VDD = 1.14 V)

Core Voltage VDD (V)	Junction Temperature ($^{\circ}\text{C}$)							
	-55°C	-40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

7. Timing Model

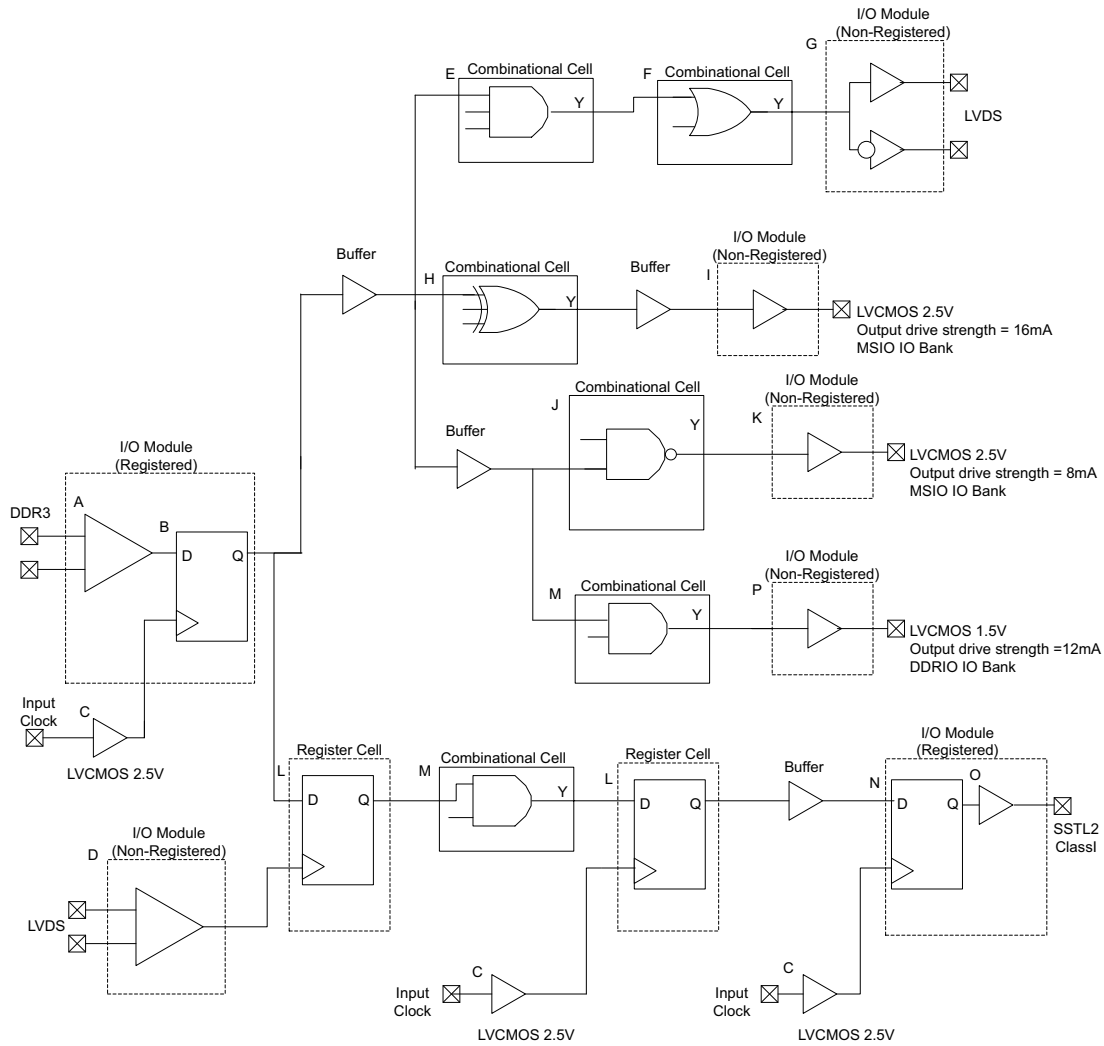


Figure 2 • Timing Model

Table 16 • Timing Model Parameters

Index	Parameter	Description	Speed Grade -1	Units	Notes
A	t_{PY}	Propagation Delay of DDR3 Receiver	1.672	ns	Refer to page 43 for more information
B	t_{CLKQ}	Clock-to-Q of the Input Data Register	0.165	ns	Refer to page 59 for more information
	t_{SUD}	Setup Time of the Input Data Register	0.369	ns	Refer to page 59 for more information
C	t_{RCKH}	Input High Delay for Global Clock	1.55	ns	Refer to page 71 - 71 for more information
	t_{RCKL}	Input Low Delay for Global Clock	0.861	ns	Refer to page 71 - 71 for more information
D	t_{PY}	Input Propagation Delay of LVDS Receiver	3.061	ns	Refer to page 50 for more information
E	t_{DP}	Propagation Delay of a three input AND Gate	0.217	ns	Refer to page 68 for more information
F	t_{DP}	Propagation Delay of a OR Gate	0.17	ns	Refer to page 68 for more information
G	t_{DP}	Propagation Delay of a LVDS Transmitter	2.299	ns	Refer to page 50 for more information
H	t_{DP}	Propagation Delay of a three input XOR Gate	0.236	ns	Refer to page 68 for more information
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16mA on the MSIO Bank	2.717	ns	Refer to page 22 for more information
J	t_{DP}	Propagation Delay of a two input NAND Gate	0.17	ns	Refer to page 68 for more information
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8mA on the MSIO Bank	2.594	ns	Refer to page 22 for more information
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.112	ns	Refer to page 59 for more information
	t_{SUD}	Setup Time of the Data Register	0.262	ns	Refer to page 59 for more information
M	t_{DP}	Propagation Delay of a two input AND gate	0.17	ns	Refer to page 68 for more information
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.272	ns	Refer to page 61 for more information
	t_{OSUD}	Setup Time of the Output Data Register	0.196	ns	Refer to page 61 for more information

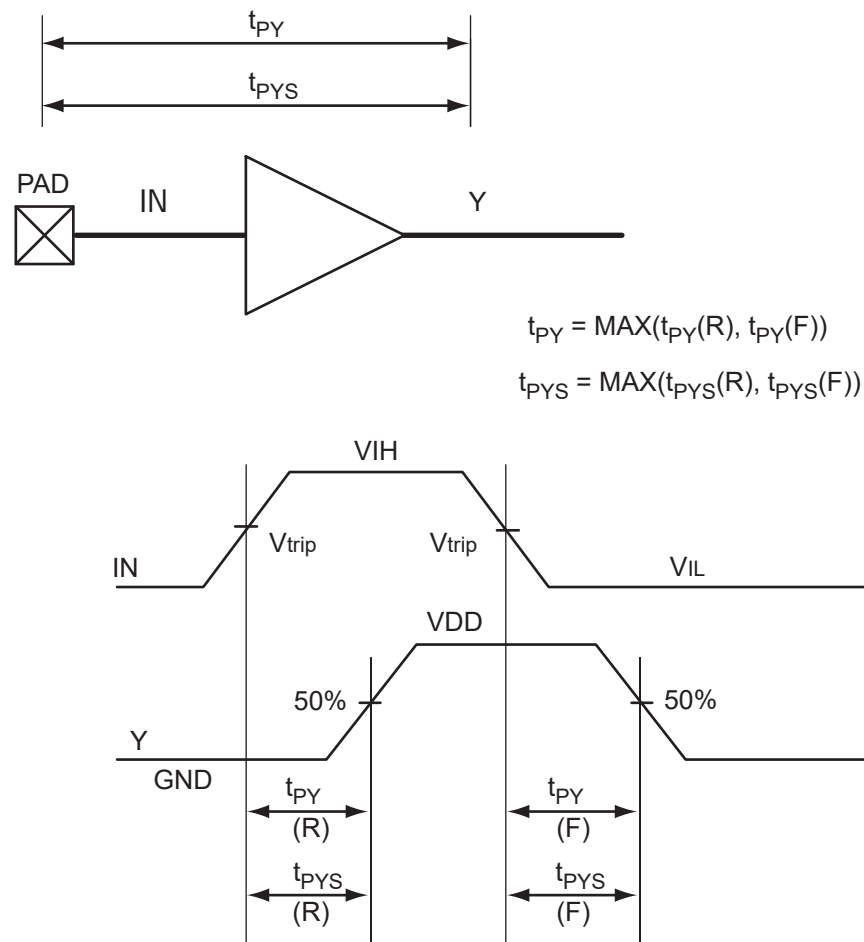
Table 16 • Timing Model Parameters (continued)

Index	Parameter	Description	Speed Grade -1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 39 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 29 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

8.1 Input Buffer and AC Loading


Figure 3 • Input Buffer AC Loading

8.2. Output Buffer and AC Loading

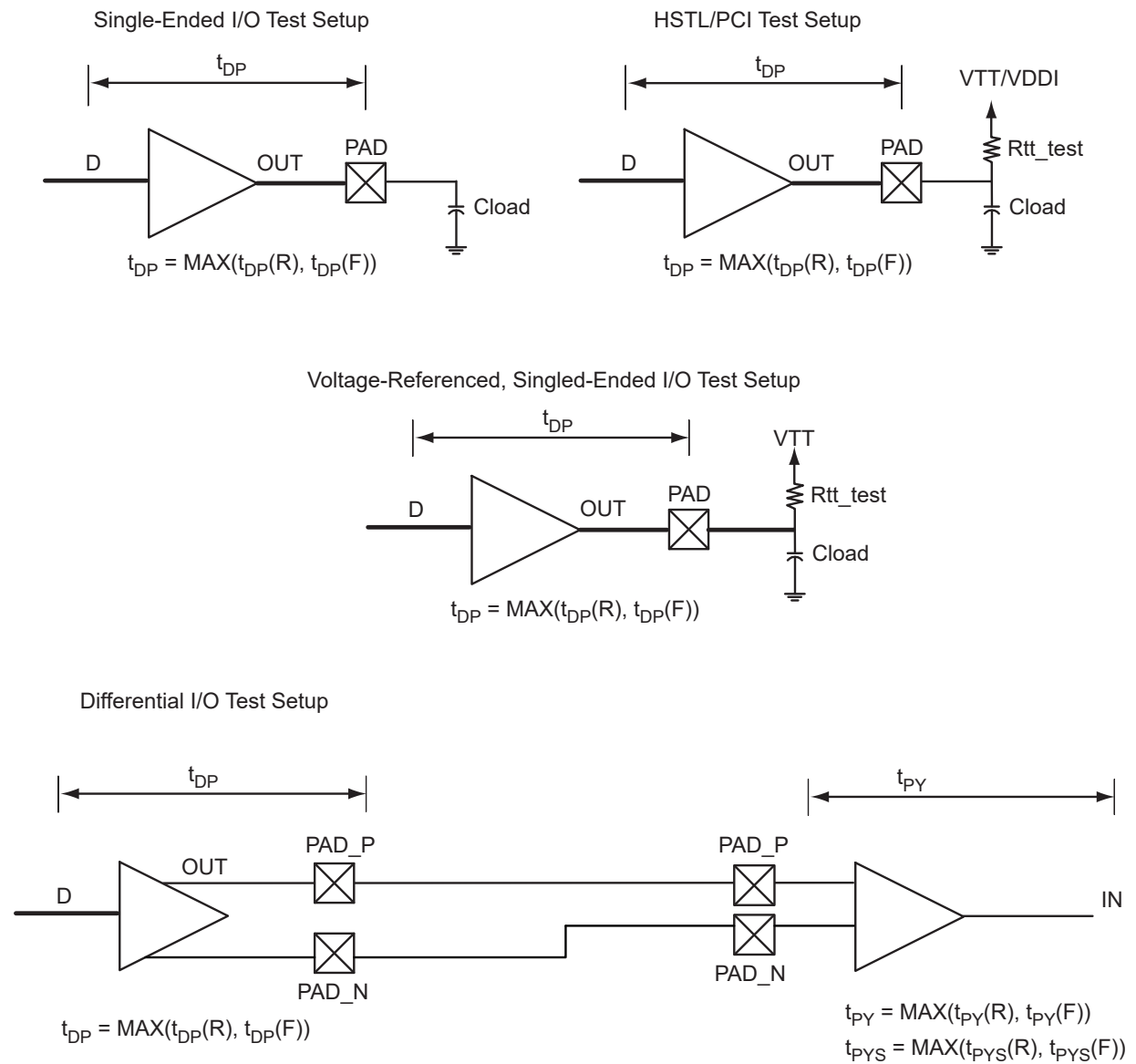


Figure 4 • Output Buffer AC Loading

8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 5.

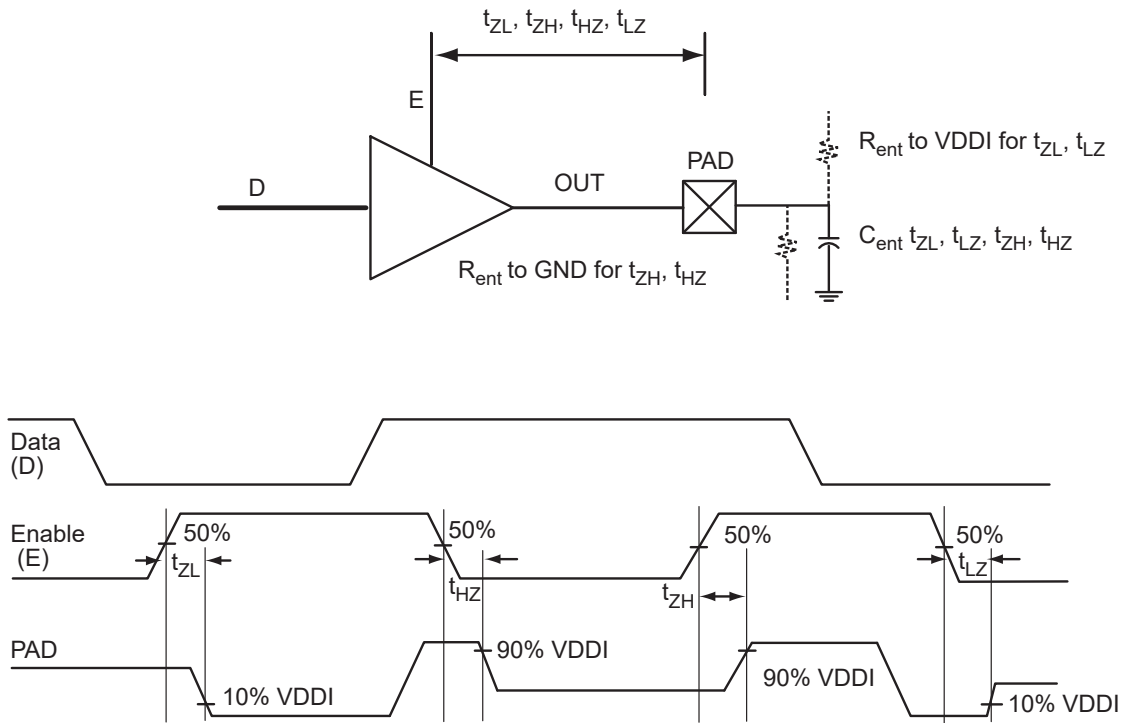


Figure 5 • Tristate Buffer for Enable Path Test Point

8.4 I/O Speeds

Table 17 • Maximum Data Rate Summary for Worst-Case Automotive Grade 2 Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	560	–	–	Mbps
LVTTTL 3.3 V	540	–	–	Mbps
LVC MOS 3.3 V	540	–	–	Mbps
LVC MOS 2.5 V	360	370	360	Mbps
LVC MOS 1.8 V	260	360	360	Mbps
LVC MOS 1.5 V	140	190	210	Mbps
LVC MOS 1.2 V	100	140	180	Mbps
LPDDR – LVC MOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL 1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RS DS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps

Table 18 • Maximum Frequency Summary for Worst-Case Automotive Grade 2 Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	280	–	–	MHz
LVTTL 3.3 V	270	–	–	MHz
LVC MOS 3.3 V	270	–	–	MHz
LVC MOS 2.5 V	180	185	180	MHz
LVC MOS 1.8 V	130	180	180	MHz
LVC MOS 1.5 V	70	95	105	MHz
LVC MOS 1.2 V	50	70	90	MHz
LPDDR - LVC MOS 1.8 V mode	–	–	180	MHz
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	180	MHz
HSTL 1.5 V	–	–	180	MHz
SSTL 2.5 V	225	240	180	MHz
SSTL 1.8 V	–	–	300	MHz
SSTL 1.5 V	–	–	300	MHz
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	405	–	–	MHz
LVDS 3.3 V	240	240	–	MHz
LVDS 2.5 V	240	240	–	MHz
RS DS	230	240	–	MHz
BLVDS	225	–	–	MHz
MLVDS	225	–	–	MHz
Mini-LVDS	230	240	–	MHz

8.5 Detailed I/O Characteristics

Table 19 • Input Capacitance

Symbol	Definition	Conditions	Min	Max	Units
CIN	Input Capacitance		–	10	pF
IIL (dc)	Input Current LOW (Applicable to HSTL/SSTL inputs only) ¹	VDDI = 2.5 V		400	μA
		VDDI = 1.8 V		500	μA
		VDDI = 1.5 V		600	μA
	Input Current LOW (Applicable to all other digital inputs)			10	μA
IIH (dc)	Input Current HIGH (Applicable to HSTL/SSTL inputs only) ¹	VDDI = 2.5 V		400	μA
		VDDI = 1.8 V		500	μA
		VDDI = 1.5 V		600	μA
	Input Current HIGH (Applicable to all other digital inputs)			10	μA
T _{RAMPIN} ²	Input Ramp Time (Applicable to all digital inputs)			50	ns

1. Applicable when IO pair is programmed with HSTL/SSTL IO type on IOP and an un-terminated IO type (LVCMOS, and so on) on ION pad.

2. Voltage ramp must be monotonic.

**Table 20 • I/O Weak Pull-Up/Pull-Down Resistance Values for DDRIO, MSIO, and MSIOD Banks
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level**

VDDI Domain	DDRIO I/O Bank				MSIO I/O Bank				MSIOD I/O Bank				Notes
	R _(WEAK PULL-UP) at VOH (Ω)		R _(WEAK PULL-DOWN) at VOL (Ω)		R _(WEAK PULL-UP) at VOH (Ω)		R _(WEAK PULL-DOWN) at VOL (Ω)		R _(WEAK PULL-UP) at VOH (Ω)		R _(WEAK PULL-DOWN) at VOL (Ω)		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3 V	N/A	N/A	N/A	N/A	9.9K	17.1K	9.98K	17.5K	N/A	N/A	N/A	N/A	
2.5 V	10K	17.8K	9.98K	18K	10K	17.6K	10.1K	18.4K	9.6K	16.6K	9.5K	16.4K	1, 2
1.8 V	10.3K	19.1K	10.3K	19.5K	10.4K	19.1K	10.4K	20.4K	9.7K	17.3K	9.7K	17.1K	1, 2
1.5 V	10.6K	20.2K	10.6K	21.1K	10.7K	20.4K	10.8K	22.2K	9.9K	18K	9.8K	17.6K	1, 2
1.2 V	11.1K	22.7K	11.2K	24.6K	11.3K	23.2K	11.5K	26.7K	10.3K	19.6K	10K	19.1K	1, 2

Notes:

- $R_{(WEAK PULL-DOWN)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN MAX)}$
- $R_{(WEAK PULL-UP)} = (VDDI_{max} - VOH_{spec}) / I_{(WEAK PULL-UP MIN)}$

Table 21 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL / LVCMOS / PCI / PCI-X	$0.05 \times V_{DDI}$ (Worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (Worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (Worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

8.6 Single-Ended I/O Standards

8.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

8.6.2 3.3 V LVCMOS/LVTTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 22 • LVTTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTTL/LVCMOS 3.3 V Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
LVTTTL/LVCMOS 3.3 V DC Input Voltage Specification						
V _{IH} (DC)	DC input logic High		2.0	–	3.45	V
V _{IL} (DC)	DC input logic Low		–0.3	–	0.8	V
I _{IH} (DC) ¹	Input current High		–	–		
I _{IL} (DC) ¹	Input current Low		–	–		
LVCMOS 3.3 V DC Output Voltage Specification						
V _{OH} ²	DC output logic High		2.4	–	–	V
V _{OL} ²	DC output logic Low		–	–	0.4	V
LVTTTL 3.3 V DC Output Voltage Specification						
V _{OH}	DC output logic High		2.4	–	–	V
V _{OL}	DC output logic Low		–	–	0.4	V

1. For more information about input current high (I_{IH}) and input current low (I_{IL}), see Table 19.

2. The V_{OH}/V_{OL} test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 23 • LVTTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTTL/LVCMOS 3.3 V Maximum Switching Speed						
D _{max}	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 24 • LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 25 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications (Applicable to MSIO Bank* Only)

Output Drive Selection	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
2 mA	2.4	0.4	2	2
4 mA	2.4	0.4	4	4
8 mA	2.4	0.4	8	8
12 mA	2.4	0.4	12	12
16 mA	2.4	0.4	16	16
20 mA	2.4	0.4	18	18

Note: * Software Configurator GUI displays the Commercial/Industrial numeric values. The actual drive capability at temperature is defined in Table 25.

8.6.2.2 AC Switching Characteristics

Worst-case Automotive Grade 2 conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 26 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics for MSIO I/O Banks (Input Buffers)

Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVTTTL/LVCMOS 3.3 V (for MSIO I/O Bank)	None	2.416	2.443	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 27 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics for MSIO I/O Bank (Output and Tristate Buffers)

Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
2 mA	slow	3.515	3.826	3.242	2.024	3.636	ns
4 mA	slow	2.565	2.948	2.774	3.339	4.896	ns
8 mA	slow	2.349	2.568	2.528	5.013	5.329	ns
12 mA	slow	2.261	2.324	2.386	6.389	6.05	ns
16 mA	slow	2.274	2.287	2.369	6.671	6.256	ns
20 mA	slow	2.372	2.206	2.306	6.976	6.541	ns

8.6.3 2.5 V LVCMOS

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 FPGA and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

8.6.3.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 28 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Min	Typ	Max	Units
LVCMOS 2.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
LVCMOS 2.5 V DC Input Voltage Specification					
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Bank)	1.7	–	2.625	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)	1.7	–	2.75	V
VIL (DC)	DC input logic Low	–0.3	–	0.7	V
IIH (DC) ¹	Input current High	–	–		
IIL (DC) ¹	Input current Low	–	–		
LVCMOS 2.5 V DC Output Voltage Specification					
VOH ²	DC output logic High	VDDI – 0.4	–	–	V
VOL ²	DC output logic Low	–	–	0.4	V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.
2. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

Table 29 • LVCMOS 2.5 V Maximum AC Switching Speeds

Symbol	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	370	Mbps

Table 30 • LVCMOS 2.5 V AC Test Parameters and Driver Impedance Specifications

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 2.5 V Calibrated Impedance Option					
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	75, 60, 50, 33, 25, 20	–	Ω
LVCMOS 2.5 V AC Test Parameters Specifications					
Vtrip	Measuring/trip point for data path	–	1.2	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})	–	5	–	pF
Cload	Capacitive loading for data path (t _{DP})	–	5	–	pF

Table 31 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (With Software Default Fixed Code)				
2 mA	2 mA	2 mA	1.7	0.7	2	2
4 mA	4 mA	4 mA	1.7	0.7	4	4
6 mA	6 mA	6 mA	1.7	0.7	6	6
8 mA	8 mA	8 mA	1.7	0.7	8	8
12 mA	12 mA	12 mA	1.7	0.7	12	12
16 mA	N/A	16 mA	1.7	0.7	16	16

Note: For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at:
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.

8.6.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 32 • LVCMOS 2.5 V AC Switching Characteristics for Receiver (Input Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVCMOS 2.5 V (for DDRIO I/O Bank)	None	1.903	2.021	ns
LVCMOS 2.5 V (for MSIO I/O Bank)	None	2.689	2.698	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)	None	2.447	2.46	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 33 • LVCMOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 2.5 V (for DDRIO I/O Bank with Fixed Code)							
2 mA	slow	3.967	3.664	3.986	4.172	3.811	ns
	medium	3.625	3.38	3.647	3.882	3.458	ns
	medium_fast	3.485	3.259	3.507	3.747	3.327	ns
	fast	3.458	3.253	3.48	3.74	3.31	ns
4 mA	slow	3.371	2.942	3.362	5.148	4.71	ns
	medium	3.063	2.701	3.059	4.874	4.381	ns
	medium_fast	2.925	2.566	2.92	4.686	4.248	ns
	fast	2.91	2.559	2.905	4.683	4.238	ns

Table 33 • LVC MOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	3.189	2.716	3.169	5.56	5.092	ns
	medium	2.886	2.473	2.876	5.273	4.752	ns
	medium_fast	2.749	2.355	2.738	5.127	4.167	ns
	fast	2.731	2.345	2.72	5.115	4.6	ns
8 mA	slow	3.132	2.646	3.109	5.686	5.207	ns
	medium	2.832	2.407	2.82	5.402	4.864	ns
	medium_fast	2.698	2.292	2.685	5.262	4.732	ns
	fast	2.684	2.282	2.671	5.252	4.724	ns
12 mA	slow	3.013	2.504	2.984	5.918	5.416	ns
	medium	2.72	2.284	2.707	5.657	5.074	ns
	medium_fast	2.592	2.176	2.578	5.537	4.949	ns
	fast	2.58	2.166	2.566	5.529	4.946	ns
16 mA	slow	2.936	2.415	2.902	6.136	5.577	ns
	medium	2.66	2.206	2.645	5.901	5.261	ns
	medium_fast	2.536	2.102	2.519	5.815	5.142	ns
	fast	2.523	2.093	2.506	5.81	5.137	ns
LVC MOS 2.5 V (for MSIO I/O Bank)							
2 mA	slow	3.933	4.352	4.22	2.358	3.838	ns
4 mA	slow	2.905	3.423	3.508	4.681	5.262	ns
6 mA	slow	2.687	2.995	3.155	5.561	5.73	ns
8 mA	slow	2.594	2.877	3.07	6.602	6.248	ns
12 mA	slow	2.623	2.732	2.944	6.974	6.478	ns
16 mA	slow	2.717	2.617	2.84	7.455	6.824	ns
LVC MOS 2.5 V (for MSIOD I/O Bank)							
2 mA	slow	2.403	2.922	2.89	5.397	5.202	ns
4 mA	slow	1.998	2.446	2.468	5.936	5.665	ns
6 mA	slow	1.861	2.329	2.375	6.391	6.068	ns
8 mA	slow	1.781	2.145	2.208	6.884	6.44	ns
12 mA	slow	1.804	2.039	2.108	7.23	6.685	ns

8.6.4 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

8.6.4.1 Minimum and Maximum AC/DC Input and Output Levels

Table 34 • LVCMOS 1.8 V DC Voltage Specification

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply Voltage	1.710	1.8	1.89	V
LVCMOS 1.8 V DC Input Voltage Specification					
VIH(DC)	DC input Logic HIGH (for MSIOD and DDRIO I/O Banks)	0.65 x VDDI	–	1.89	V
VIH(DC)	DC input Logic HIGH (for MSIO I/O Bank)	0.65 x VDDI	–	2.75	V
VIL(DC)	DC input Logic LOW	-0.3	–	0.35 x VDDI	V
IIH(DC) ¹	Input Current HIGH	–	–		
IIL(DC) ¹	Input Current LOW	–	–		
LVCMOS 1.8 V DC Output Voltage Specification					
VOH	DC output Logic HIGH	VDDI - 0.45	–	–	V
VOL	DC output Logic LOW	–	–	0.45	V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.

Table 35 • LVCMOS 1.8 V Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.8 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	260	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	360	Mbps
<i>Note: * Maximum data rate applies for drive strength 8mA and above, all slews</i>						

Table 36 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection		VOH (V)		VOL (V)	
MSIO I/O Bank	MSIOD I/O Bank	Min	Max	IOH (at VOH) mA	IOL (at VOL) mA
2 mA	2 mA	VDDI – 0.45	0.45	2	2
4 mA	4 mA	VDDI – 0.45	0.45	4	4
6 mA	6 mA	VDDI – 0.45	0.45	6	6
8 mA	8 mA	VDDI – 0.45	0.45	8	8
10 mA	10 mA	VDDI – 0.45	0.45	10	10
12 mA	N/A	VDDI – 0.45	0.45	12	12

Table 37 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection	VOH (V)	VOL (V)			
DDRIO Bank*	Min	Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	**
8 mA	VDDI – 0.45	0.45	6	6	**
10 mA	VDDI – 0.45	0.45	8	8	–
12 mA	VDDI – 0.45	0.45	10	10	–
16 mA	VDDI – 0.45	0.45	12	12	–

Notes:

* Software Configurator GUI will display the Commercial/Industrial numeric values. The actual drive capability at temperature is defined by Table 37.

** DDRIO has two 6mA drive strength settings. The setting that corresponds to Output Drive Selection value of 8mA has a shorter propagation delay.

Table 38 • LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications

LVCMOS 1.8 V AC Calibrated Impedance Option					
Symbols	Parameters	Min	Typ	Max	Units
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	75, 60, 50, 33, 25, 20	–	Ω
LVCMOS 1.8 V AC Test Parameters Specifications					
Vtrip	Measuring/trip point for data path	–	0.9	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})	–	5	–	pF

8.6.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1		Units
		t_{pY}	t_{pYS}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns
	50	3.185	3.171	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	50	3.394	3.397	ns
	75	3.322	3.316	ns
	150	3.252	3.239	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.827	2.813	ns
	50	3.043	3.053	ns
	75	2.968	2.963	ns
	150	2.898	2.886	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 40 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns

Table 40 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns
LVCMOS 1.8 V (for MSIO I/O Bank)							
2 mA	slow	3.957	4.784	5.023	5.643	5.866	ns
4 mA	slow	3.668	4.162	4.485	6.543	6.382	ns
6 mA	slow	3.586	3.994	4.358	7.622	6.941	ns
8 mA	slow	3.616	3.782	4.162	7.988	7.161	ns
10 mA	slow	3.662	3.732	4.121	8.396	7.423	ns
12 mA	slow	3.75	3.615	4.006	8.576	7.543	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)							
2 mA	slow	3.048	3.692	3.898	5.818	5.609	ns
4 mA	slow	2.5	3.088	3.288	6.421	6.121	ns
6 mA	slow	2.225	2.747	2.937	7.18	6.753	ns
8 mA	slow	2.233	2.72	2.904	7.49	6.992	ns
10 mA	slow	2.263	2.577	2.759	7.851	7.253	ns

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 41 • LVCMOS 1.5 V Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 1.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification					
V _{IH} (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)	$0.65 \times V_{DDI}$	–	1.575	V
V _{IH} (DC)	DC input logic High (for MSIO I/O Bank)	$0.65 \times V_{DDI}$	–	2.75	V
V _{IL} (DC)	DC input logic Low	–0.3	–	$0.35 \times V_{DDI}$	V
I _{IH} (DC) ¹	Input current High	–	–		
I _{IL} (DC) ¹	Input current Low	–	–		
LVCMOS 1.5 V DC Output Voltage Specification					
V _{OH}	DC output logic High	$V_{DDI} \times 0.75$	–	–	V
V _{OL}	DC output logic Low	–	–	$V_{DDI} \times 0.25$	V

1. For more information about input current high (I_{IH}) and input current low (I_{IL}), see Table 19.

Table 42 • LVC MOS 1.5 V Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVC MOS 1.5 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	210	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	140	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	190	Mbps

Table 43 • LVC MOS 1.5 V AC Test Parameters and Driver Impedance Specifications

Symbols	Parameters	Min	Typ	Max	Units
LVC MOS 1.5 V AC Calibrated Impedance Option					
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)	–	75, 60, 50, 40	–	Ω
LVC MOS 1.5 V AC Test Parameters Specifications					
Vtrip	Measuring/trip point for data path	–	0.75	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})	–	5	–	pF

Table 44 • LVC MOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	$VDDI \times 0.75$	$VDDI \times 0.25$	2	2
4 mA	4 mA	4 mA	$VDDI \times 0.75$	$VDDI \times 0.25$	4	4
6 mA	6 mA	6 mA	$VDDI \times 0.75$	$VDDI \times 0.25$	6	6
8 mA	N/A	8 mA	$VDDI \times 0.75$	$VDDI \times 0.25$	8	8
N/A	N/A	10 mA	$VDDI \times 0.75$	$VDDI \times 0.25$	10	10
N/A	N/A	12 mA	$VDDI \times 0.75$	$VDDI \times 0.25$	12	12

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 45 • LVC MOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVC MOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	None	2.19	2.216	ns
LVC MOS 1.5 V (for MSIO I/O Bank)	None	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVC MOS 1.5 V (for MSIOD I/O Bank)	None	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 46 • LVC MOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVC MOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

Table 46 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
8 mA	slow	4.603	3.691	4.585	7.397	6.553	ns
	medium	4.081	3.242	4.062	7.064	6.189	ns
	medium_fast	3.827	3.015	3.804	6.912	6.051	ns
	fast	3.804	2.994	3.781	6.903	6.051	ns
10 mA	slow	4.519	3.612	4.499	7.578	6.676	ns
	medium	4.026	3.177	4.005	7.264	6.335	ns
	medium_fast	3.775	2.948	3.75	7.11	6.198	ns
	fast	3.747	2.929	3.721	7.103	6.19	ns
12 mA	slow	4.456	3.562	4.433	7.704	6.795	ns
	medium	3.965	3.13	3.943	7.388	6.425	ns
	medium_fast	3.731	2.912	3.704	7.278	6.303	ns
	fast	3.703	2.893	3.676	7.275	6.294	ns
LVCMOS 1.5 V (for MSIO I/O Bank)							
2 mA	slow	5.118	6.263	6.53	6.524	6.388	ns
4 mA	slow	4.657	5.178	5.65	8.57	7.55	ns
6 mA	slow	4.693	4.89	5.389	8.928	7.766	ns
8 mA	slow	4.876	4.663	5.183	9.59	8.173	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)							
2 mA	slow	3.085	3.795	4.086	6.838	6.477	ns
4 mA	slow	2.731	3.365	3.631	7.663	7.165	ns
6 mA	slow	2.742	3.162	3.417	8.126	7.52	ns

8.6.6 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

8.6.6.1 Minimum and Maximum Input and Output Levels Specification

Table 47 • LVCMOS 1.2 V Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V Recommended DC Operating Conditions						
VDDI	Supply voltage		1.140	1.2	1.26	V
LVCMOS 1.2 V DC Input Voltage Specification						
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O Banks)		$0.65 \times VDDI$	–	1.26	V
VIH (DC)	DC input logic High (for MSIO I/O Bank)		$0.65 \times VDDI$	–	2.75	V
VIL (DC)	DC input logic Low		–0.3	–	$0.35 \times VDDI$	V
IIH (DC) ¹	Input current High		–	–		
IIL (DC) ¹	Input current Low		–	–		
LVCMOS 1.2 V DC Output Voltage Specification						
VOH	DC output logic High		$VDDI \times 0.75$	–	–	V
VOL	DC output logic Low		–	–	$VDDI \times 0.25$	V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.

Table 48 • LVCMOS 1.2 V Maximum AC Switching Speeds

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	180	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	100	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	140	Mbps

Table 49 • LVCMOS 1.2 V AC Calibrated Impedance and Test Parameters Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVCMOS 1.2 V AC Calibrated Impedance Option						
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)		–	75, 60, 50, 40	–	Ω
LVCMOS 1.2 V AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.6	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 50 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
N/A	N/A	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

8.6.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, VDD=1.14 V, VDDI= 1.14 V

	ODT (On Die Termination) in Ω	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Codes)	None	2.539	2.556	ns
LVCMOS 1.2 V (for MSIO I/O Bank)	None	4.888	4.845	ns
	50	6.683	6.605	ns
	75	5.923	5.847	ns
	150	5.29	5.235	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)	None	4.281	4.235	ns
	50	6.806	6.721	ns
	75	5.643	5.564	ns
	150	4.813	4.753	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 52 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, VDD=1.14 V, VDDI= 1.14 V

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Code)							
2 mA	slow	6.938	5.599	6.948	7.568	6.612	ns
	medium	6.11	4.814	6.114	7.201	6.234	ns
	medium_fast	5.675	4.409	5.676	6.971	6.048	ns
	fast	5.633	4.379	5.634	6.958	6.037	ns
4 mA	slow	6.328	4.892	6.316	8.339	7.306	ns
	medium	5.538	4.192	5.521	7.961	6.923	ns
	medium_fast	5.119	3.832	5.097	7.76	6.741	ns
	fast	5.072	3.085	5.051	7.752	6.725	ns

Table 52 • LVC MOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.14\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	6.092	4.681	6.075	8.685	7.589	ns
	medium	5.342	4.016	5.32	8.33	7.19	ns
	medium_fast	4.949	3.66	4.922	8.139	7.022	ns
	fast	4.903	3.622	4.876	8.107	7.006	ns
LVC MOS 1.2 V (for MSIO I/O Bank)							
2 mA	slow	7.051	7.856	8.541	10.387	8.768	ns
4 mA	slow	7.385	7.027	7.815	11.547	9.444	ns
LVC MOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 53 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
IIH(DC) ¹	Input current High		–	–		
IIL(DC) ¹	Input current Low		–	–		
PCI/PCIX DC Output Voltage Specification						
VOH	DC output logic High		Per PCI Specification			V
VOL	DC output logic Low		Per PCI Specification			V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.

Table 54 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
Dmax	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	–	–	560	Mbps
PCI/PCI-X AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path (falling edge)		–	$0.615 \times VDDI$	–	V
Vtrip	Measuring/trip point for data path (rising edge)		–	$0.285 \times VDDI$	–	V
Rtt_test	Resistance for data test path		–	25	–	Ω
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	10	–	pF

8.6.7.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 55 • PCI/PCIX AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 3.15\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
PCI/PCIX (for MSIO I/O Bank)	None	2.379	2.387	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 56 • PCI/PCIX AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 3.15\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
PCI/PCIX (for MSIO I/O Bank)	2.394	2.274	2.316	6.876	6.242	ns

8.7. Memory Interface and Voltage Referenced I/O Standards

8.7.1 High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

8.7.1.1 Minimum and Maximum Input and Output Levels Specification

Table 57 • HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL Recommended DC Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
VTT	Termination voltage		0.698	0.750	0.803	V
VREF	Input reference voltage		0.698	0.750	0.803	V
HSTL DC Input Voltage Specification						
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V
IIH (DC) ¹	Input current High		–	–		
IIL (DC) ¹	Input current Low		–	–		
HSTL DC Output Voltage Specification						
HSTL Class I						
VOH	DC output logic High		VDDI – 0.4	–	–	V
VOL	DC output logic Low		–	–	0.4	V
IOH at VOH	Output minimum source DC current		–7.0	–	–	mA
IOL at VOL	Output minimum sink current		7.0	–	–	mA
HSTL Class II						
VOH	DC output logic High		VDDI – 0.4	–	–	V
VOL	DC output logic Low		–	–	0.4	V
IOH at VOH	Output minimum source DC current		–15.0	–	–	mA
IOL at VOL	Output minimum sink current		15.0	–	–	mA
HSTL DC Differential Voltage Specifications						
VID (DC)	DC input differential voltage		0.2	–	–	V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.

Table 58 • HSTL AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL AC Differential Voltage Specifications						
V _{DIFF}	AC input differential voltage		0.4	–	–	V
V _x	AC differential cross point voltage		0.68	–	0.9	V
HSTL Maximum AC Switching Speed						
D _{max}	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps
HSTL Impedance Specification						
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ω	–	25.5, 47.8	–	Ω
R _{TT}	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ω	–	47.8	–	Ω
HSTL AC Test Parameters Specification						
V _{trip}	Measuring/trip point for data path		–	0.75	–	V
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF
R _{tt_test}	Reference resistance for data test path for HSTL15 Class I (t _{DP})		–	50	–	Ω
R _{tt_test}	Reference resistance for data test path for HSTL15 Class II (t _{DP})		–	25	–	Ω
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF

8.7.1.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 59 • HSTL15 AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	ODT (On Die Termination) in Ω	t _{py}	Units
		Speed Grade –1	
HSTL (for DDRIO I/O Bank with Fixed Code)			
Pseudo-Differential	None	1.673	ns
True-Differential	None	1.693	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 60 • HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
HSTL Class I (for DDRIO I/O Bank)						
Single Ended	2.922	2.91	2.904	3.225	3.218	ns
Differential	2.907	2.757	2.755	2.662	2.66	ns
HSTL Class II (for DDRIO I/O Bank)						
Single Ended	2.817	2.735	2.735	2.644	2.644	ns
Differential	2.827	2.81	2.803	3.205	3.197	ns

8.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

8.7.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.3.1 Minimum and Maximum DC Input and Output Levels Specification

Table 61 • DDR1/SSTL2 Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
VTT	Termination voltage	1.164	1.250	1.339	V
VREF	Input reference voltage	1.164	1.250	1.339	V
SSTL2 DC Input Voltage Specification					
VIH (DC)	DC input logic High	VREF + 0.15	–	2.625	V
VIL (DC)	DC input logic Low	–0.3	–	VREF – 0.15	V
IIH (DC) ¹	Input current High	–	–		
IIL (DC) ¹	Input current Low	–	–		
SSTL2 DC Output Voltage Specification					
SSTL2 Class I (DDR Reduced Drive)					
VOH	DC output logic High	VTT + 0.608	–	–	V
VOL	DC output logic Low	–	–	VTT – 0.608	V
IOH at VOH	Output minimum source DC current	8.1	–	–	mA
IOL at VOL	Output minimum sink current	–8.1	–	–	mA
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks Only					
VOH	DC output logic High	VTT + 0.81	–	–	V
VOL	DC output logic Low	–	–	VTT – 0.81	V
IOH at VOH	Output minimum source DC current	16.2	–	–	mA
IOL at VOL	Output minimum sink current	–16.2	–	–	mA
SSTL2 DC Differential Voltage Specification					
VID (DC)	DC input differential voltage	0.3	–	–	V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.

Table 62 • DDR1/SSTL2 AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL2 Maximum AC Switching Speeds						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17pF load	–	–	450	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17pF load	–	–	480	Mbps
SSTL2 AC Differential Voltage Specifications						
VDIFF	AC Input Differential Voltage		0.7	–	–	V
Vx	AC Differential Cross Point Voltage		$0.5 \times VDDI - 0.2$	–	$0.5 \times VDDI + 0.2$	V
SSTL2 Impedance Specifications						
	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
SSTL2 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	1.25	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 2.375\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t_{pY}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1	Units
		t_{py}	
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 64 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.4.1 Minimum and Maximum Input and Output Levels Specification

Table 65 • DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	1.71	1.8	1.89	V
VTT	Termination voltage	0.838	0.900	0.964	V
VREF	Input reference voltage	0.838	0.900	0.964	V
SSTL18 DC Input Voltage Specification					
VIH (DC)	DC input logic High	VREF + 0.125	–	1.89	V
VIL (DC)	DC input logic Low	–0.3	–	VREF – 0.125	V
IIH (DC) ¹	Input current High	–	–		
IIL (DC) ¹	Input current Low	–	–		
SSTL18 DC Output Voltage Specification					
SSTL18 Class I (DDR2 Reduced Drive)					
VOH	DC output logic High	VTT + 0.603	–	–	V
VOL	DC output logic Low	–	–	VTT – 0.603	V
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)	6.0	–	–	mA
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)	–6.0	–	–	mA
SSTL18 Class II (DDR2 Full Drive)²					
VOH	DC output logic High	VTT + 0.603	–	–	V
VOL	DC output logic Low	–	–	VTT – 0.603	V
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)	12.0	–	–	mA
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)	–12.0	–	–	mA
SSTL18 DC Differential Voltage Specification					
VID (DC)	DC input differential voltage	0.3	–	–	V
<i>Note:</i>					

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.
2. To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

Table 66 • DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL18 AC Differential Voltage Specification						
V _{DIFF} (AC)	AC input differential voltage		0.5	–	–	V
V _x (AC)	AC differential cross point voltage		$0.5 \times V_{DDI} - 0.175$	–	$0.5 \times V_{DDI} + 0.175$	V
SSTL18 Maximum AC Switching Speed						
D _{max}	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specification	–	–	600	Mbps
SSTL18 Impedance Specifications						
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
R _{TT}	Effective impedance value (ODT)	Reference resistor = 150 Ω	–	50, 75, 150	–	Ω
SSTL18 AC Test Parameters Specifications						
V _{trip}	Measuring/trip point for data path		–	0.9	–	V
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF
R _{tt_test}	Reference resistance for data test path for SSTL18 Class I (t _{DP})		–	50	–	Ω
R _{tt_test}	Reference resistance for data test path for SSTL18 Class II (t _{DP})		–	25	–	Ω
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF

8.7.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 67 • DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t _{py}	
SSTL18 (for DDRIO I/O Bank with Fixed Codes)			
Pseudo differential	None	1.633	ns
True differential	None	1.65	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Table 68 • DDR2/SSTL18 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
SSTL18 Class I (for DDRIO I/O Bank)						
Single Ended	2.67	3.078	3.072	2.489	2.484	ns
Differential	2.645	2.431	2.434	2.396	2.398	ns
SSTL18 Class II (for DDRIO I/O Bank)						
Single Ended	2.564	2.973	2.965	2.45	2.444	ns
Differential	2.532	2.401	2.398	2.368	2.365	ns

8.7.5 Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification
Table 69 • DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		1.425	1.5	1.575	V
VTT	Termination voltage		0.698	0.750	0.803	V
VREF	Input reference voltage		0.698	0.750	0.803	V
SSTL15 DC Input Voltage Specification						
$V_{IH}(\text{DC})$	DC input logic High		$V_{REF} + 0.1$	–	1.575	V
$V_{IL}(\text{DC})$	DC input logic Low		–0.3	–	$V_{REF} - 0.1$	V
$I_{IH}(\text{DC})^1$	Input current High		–	–		
$I_{IL}(\text{DC})^1$	Input current Low		–	–		
SSTL15 DC Output Voltage Specification						
DDR3/SSTL15 Class I (DDR3 Reduced Drive)						
VOH	DC output logic High		$0.8 \times V_{DDI}$	–	–	V
VOL	DC output logic Low		–	–	$0.2 \times V_{DDI}$	V
IOH at VOH	Output minimum source DC current		6.5	–	–	mA
IOL at VOL	Output minimum sink current		–6.5	–	–	mA
SSTL15 Class II (DDR3 Full Drive)²						
VOH	DC output logic High		$0.8 \times V_{DDI}$	–	–	V
VOL	DC output logic Low		–	–	$0.2 \times V_{DDI}$	V
IOH at VOH	Output minimum source DC current		7.6	–	–	mA

Table 69 • DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only) (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
IOL at VOL	Output minimum sink current		-7.6	-	-	mA
SSTL15 Differential Voltage Specification						
VID	DC input differential voltage		0.2	-	-	V
<i>Note:</i>						

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.
2. To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.

Table 70 • DDR3/SSTL15 AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 AC Differential Voltage Specification						
VDIFF	AC input differential voltage		0.3	-	-	V
Vx	AC differential cross point voltage		$0.5 \times VDDI$ - 0.150	-	$0.5 \times VDDI +$ 0.150	V
SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	-	-	600	Mbps
SSTL15 AC Calibrated Impedance Option						
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ω	-	34, 40	-	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 240 Ω	-	20, 30, 40, 60, 120	-	Ω
SSTL15 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		-	0.75	-	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		-	2k	-	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		-	5	-	pF
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})		-	50	-	Ω
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		-	25	-	Ω
Cload	Capacitive loading for data path (t_{DP})		-	5	-	pF

8.7.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 71 • DDR3/SSTL15 AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 1.425\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1	Units
		t_{PY}	
DDR3/SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only			
Pseudo-Differential	None	1.672	ns
True-Differential	None	1.694	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Table 72 • DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)						
Single Ended	2.832	2.766	2.767	2.658	2.659	ns
Differential	2.848	3.401	3.393	3.173	3.166	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)						
Single Ended	2.832	2.76	2.759	2.655	2.655	ns
Differential	2.845	3.397	3.387	3.179	3.171	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

8.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification
Table 73 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions						
VDDI	Supply voltage	1.71	1.8	1.89	V	–
VTT	Termination voltage	0.838	0.900	0.964	V	–
VREF	Input reference voltage	0.838	0.900	0.964	V	–
LPDDR DC Input Voltage Specification						
VIH (DC)	DC input logic High	$0.7 \times V_{DDI}$	–	1.89	V	–
VIL (DC)	DC input logic Low	–0.3	–	$0.3 \times V_{DDI}$	V	–
IIH (DC)	Input current High	–	–	10	μA	–
IIL (DC)	Input current Low	–	–	10	μA	–
LPDDR DC Output Voltage Specification						
LPDDR Reduced Drive						
VOH	DC output logic High	$0.9 \times V_{DDI}$	–	–	V	–
VOL	DC output logic Low	–	–	$0.1 \times V_{DDI}$	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR Full Drive						
VOH	DC output logic High	$0.9 \times V_{DDI}$	–	–	V	–
VOL	DC output logic Low	–	–	$0.1 \times V_{DDI}$	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–

Table 73 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Min	Typ	Max	Units	Notes
IOL at VOL	Output minimum sink current	-0.1	-	-	mA	-
LPDDR DC Differential Voltage Specification						
VID (DC)	DC input differential voltage	$0.4 \times VDDI$	-	-	V	-
<i>Note: *To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.</i>						

Table 74 • LPDDR Maximum AC Switching Speeds (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Dmax	Maximum data rate	AC loading: per JEDEC specifications	-	-	360	Mbps

Table 75 • LPDDR AC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR AC Differential Voltage Specification						
VDIFF (AC)	AC Input differential voltage	-	$0.6 \times VDDI$	-	-	V
Vx (AC)	AC Differential Cross Point Voltage	-	$0.4 \times VDDI$	-	$0.6 \times VDDI$	V
LPDDR Impedance Specifications						
Rref	Supported Output Driver Calibrated Impedance	Reference Resistor = 150 Ω	-	20,42	-	Ω
RTT	Effective impedance Value - ODT	Reference Resistor = 150 Ω	-	50, 75, 150	-	Ω
LPDDR AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	-	-	0.9	-	V
Rent	Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	-	-	2k	-	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	-	-	5	-	pF
Rtt_test	Reference resistance for Data Test Path for LPDDR (t_{DP})	-	-	50	-	Ω
Cload	Capacitive Loading for Data Path (t_{DP})	-	-	5	-	pF

8.7.6.2 AC Switching Characteristics

Table 76 • LPDDR AC Switching Characteristics for Receiver (Input Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^\circ\text{C}$, $VDD=1.14\text{ V}$, $VDDI=1.71\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1	Units
		t_{PY}	
LPDDR (for DDRIO I/O Bank with Fixed Codes)			
Pseudo-Differential	None	1.633	ns
True-Differential	None	1.65	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Table 77 • LPDDR AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.71\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{zL}	t_{zH}	t_{HZ}	t_{LZ}	
LPDDR Reduced Drive (for DDRIO I/O Bank)						
Single Ended	2.645	2.431	2.434	2.396	2.398	ns
Differential	2.652	3.044	3.038	2.46	2.455	ns
LPDDR Full Drive (for DDRIO I/O Bank)						
Single Ended	2.532	2.401	2.398	2.368	2.365	ns
Differential	2.546	2.509	2.503	2.852	2.845	ns

8.7.6.3 Minimum and Maximum AC/DC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode
Table 78 • LPDDR-LVCMOS 1.8 V Mode, Minimum and Maximum DC Input and Output Levels (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8 V Recommended DC Operating Conditions						
VDDI	Supply Voltage	–	1.710	1.8	1.89	V
LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification						
$V_{IH}(\text{DC})$	DC input Logic HIGH for (MSIOD and DDRIO I/O Banks)	–	$0.65 \times V_{DDI}$	–	1.89	V
$V_{IH}(\text{DC})$	DC input Logic HIGH (for MSIO I/O Bank)	–	$0.65 \times V_{DDI}$	–	3.45	V
$V_{IL}(\text{DC})$	DC input Logic LOW	–	-0.3	–	$0.35 \times V_{DDI}$	V
$I_{IH}(\text{DC})^1$	Input current HIGH	–	–	–		
$I_{IL}(\text{DC})^1$	Input current LOW	–	–	–		
LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification						
VOH	DC output Logic HIGH	–	$V_{DDI} - 0.45$	–	–	V
VOL	DC output Logic LOW	–	–	–	0.45	V

 1. For more information about input current high (I_{IH}) and input current low (I_{IL}), see Table 19.

Table 79 • LPDDR-LVCMOS 1.8 V Maximum AC Switching Speeds (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
D_{max}	Maximum Data Rate (for DDRIO I/O Bank)	AC Loading: 17pF Load, 8mA Drive and Above/All Slew	–	–	360	Mbps

Table 80 • LPDDR-LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR - LVCMOS 1.8 V Calibrated Impedance Option						
Rodt_cal	Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	5	–	pF
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

Table 81 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)

Output Drive Selection	VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	–
8 mA	VDDI – 0.45	0.45	8	8	–
10 mA	VDDI – 0.45	0.45	10	10	–
12 mA	VDDI – 0.45	0.45	12	12	–
16 mA	VDDI – 0.45	0.45	16	16	*

*Note: * 16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance*

8.7.6.4 AC Switching Characteristics

Table 82 • LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Table 83 • LPDDR - LVCMOS 1.8 V AC Switching Characteristics for Transmitter DDRIO I/O Bank (Output and Tristate Buffers)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t_{DP}	t_{zL}	t_{zH}	t_{HZ}	t_{LZ}	
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns

8.8. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.8.1.1 Minimum and Maximum Input and Output Levels

Table 84 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V
LVDS DC Input Voltage Specification						
VI	DC Input voltage	2.5 V range	0	–	2.925	V
VI	DC input voltage	3.3 V range	0	–	3.45	V
IIH (DC) ¹	Input current High		–	–		
IIL (DC) ¹	Input current Low		–	–		
LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		250	350	450	mV
VOCM	Output common mode voltage		1.125	1.25	1.375	V
VICM	Input common mode voltage		0.05	1.25	2.35	V
VID ²	Input differential voltage		100	350	600	mV

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.
2. When VID is < 300 mV, the input signal is delayed by up to an additional 450 ps for LVDS25 and 280 ps for LVDS33. This delay is not accounted in the timing model. Clock insertion delays, propagation delays, and I/O to FF delays are marginally affected. Adding a parallel termination resistor of 200 Ω +/- 5% across the receiver pins can mitigate this additional delay when VID is < 300 mV.

Table 85 • LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ω differential load	–	–	480	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
LVDS Impedance Specification						
Rt	Termination resistance	–	–	100	–	Ω

Table 85 • LVDS AC Specifications (continued)

LVDS AC Test Parameters Specifications					
Vtrip	Measuring/trip point for data path	–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	5	–	pF

8.8.1.2 LVDS25 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 86 • LVDS25 Receiver Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{pY}	
LVDS (for MSIO I/O Bank)	None	3.061	ns
	100	3.057	ns
LVDS (for MSIOD I/O Bank)	None	2.792	ns
	100	2.787	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 87 • LVDS25 Transmitter Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS (for MSIO I/O Bank)	2.299	2.602	2.589	2.305	2.32	ns
LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.656	1.845	1.838	1.992	1.969	ns
Min pre-emphasis	1.583	1.868	1.866	2.018	1.998	ns
Med pre-emphasis	1.559	1.893	1.886	2.045	2.021	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 88 • LVDS33 Receiver Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{pY}	
LVDS33 (for MSIO I/O Bank)	None	2.763	ns
	100	2.76	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Table 89 • LVDS33 Transmitter Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS33 (for MSIO I/O Bank)	2.069	2.112	2.106	2.078	2.09	ns

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multi-point bus applications. Multi-drop and multi-point bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification
Table 90 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC) ¹	Input current High		–	–		
IIL (DC) ¹	Input current Low		–	–		
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

1. For more information about input current high (IIH) and input current low (IIL), see Table 19.

Table 91 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.2.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 92 • B-LVDS AC Switching Characteristics for Receiver (Input Buffers)
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{pY}	
Bus-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 93 • B-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
Bus-LVDS (for MSIO I/O Bank)	2.78	2.632	2.617	2.448	2.436	ns

8.8.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.3.1 Minimum and Maximum Input and Output Levels

Table 94 • M-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Recommended DC Operating Conditions						
V_{DDI}^1	Supply voltage		2.375	2.5	2.625	V
M-LVDS DC Input Voltage Specification						
V_I	DC input voltage		0	–	2.925	V
$I_{IH}(\text{DC})^2$	Input current High		–	–		
$I_{IL}(\text{DC})^2$	Input current Low		–	–		
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)						
V_{OH}	DC output logic High		1.25	1.425	1.6	V
V_{OL}	DC output logic Low		0.9	1.075	1.25	V
M-LVDS Differential Voltage Specification						
V_{OD}	Differential output voltage Swing (for MSIO I/O Bank only)		300	–	650	mV
V_{OCM}	Output common mode voltage (for MSIO I/O Bank only)		0.3	–	2.1	V
V_{ICM}	Input common mode voltage		0.3	–	1.2	V
V_{ID}	Input differential voltage		50	–	2400	mV

1. Only M-LVDS TYPE I is supported.

2. For more information about input current high (I_{IH}) and input current low (I_{IL}), see Table 19.

Table 95 • M-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speeds						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance	–	–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 96 • M-LVDS AC Switching Characteristics for Receiver (Input Buffers)

 Worst-case Automotive Grade 2 conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{pY}	
M-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
M-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 97 • M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-case Automotive Grade 2 conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
M-LVDS (for MSIO I/O Bank)	2.78	2.632	2.616	2.447	2.436	ns

8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 98 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.925	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		300	–	600	mV
VOCM	Output common mode voltage		1	–	1.4	V
VICM	Input common mode voltage		0.3	–	1.2	V
VID	Input differential voltage		100	–	600	mV

Table 99 • Mini-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
Mini-LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
Mini-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.4.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 100 • Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade -1	Units
		t_{pY}	
Mini-LVDS (for MSIO I/O Bank)	None	3.112	ns
	100	2.995	ns
Mini-LVDS (for MSIOD I/O Bank)	None	2.612	ns
	100	2.612	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 101 • Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
Mini-LVDS (for MSIO I/O Bank)	2.3	2.602	2.59	2.306	2.32	ns
Mini-LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.652	1.84	1.833	1.988	1.965	ns
Min pre-emphasis	1.652	1.84	1.833	1.988	1.965	ns
Med pre-emphasis	1.577	1.868	1.86	2.02	1.994	ns
Max pre-emphasis	1.555	1.894	1.883	2.048	2.019	ns

8.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

8.8.5.1 Minimum and Maximum Input and Output Levels

Table 102 • RSDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
RSDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
RSDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
RSDS Differential Voltage Specification						
VOD	Differential output voltage swing		100	–	600	mV
VOCM	Output common mode voltage		0.5	–	1.5	V

Table 102 • RSDS DC Voltage Specification (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
VICM	Input common mode voltage		0.3	–	1.5	V
VID	Input differential voltage		100	–	600	mV

Table 103 • RSDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
RSDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
RSDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
RSDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 104 • RSDS AC Switching Characteristics for Receiver (Input Buffers)

 Worst-case Automotive Grade 2 conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{pY}	
RSDS (for MSIO I/O Bank)	None	3.112	ns
	100	3.108	ns
RSDS (for MSIOD I/O Bank)	None	2.832	ns
	100	2.821	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Table 105 • RSDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
RSDS (for MSIO I/O Bank)	2.256	2.484	2.472	2.111	2.096	ns
RSDS (for MSIOD I/O Bank)						
No pre-emphasis	1.661	1.648	1.645	1.675	1.665	ns
Min pre-emphasis	1.651	1.84	1.833	1.988	1.964	ns
Med pre-emphasis	1.577	1.868	1.859	2.019	1.993	ns
Max pre-emphasis	1.555	1.894	1.883	2.047	2.018	ns

8.8.6 LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

8.8.6.1 Minimum and Maximum Input and Output Levels

Table 106 • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
LVPECL DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
LVPECL Differential Voltage Specification						
VICM	Input common mode voltage		0.3		2.8	V
VIDIFF	Input differential voltage		100	300	1,000	mV

Table 107 • LVPECL Maximum AC Switching Speeds (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVPECL AC Specifications						
Fmax	Maximum data rate (for MSIO I/O Bank)		–	–	810	Mbps

8.8.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 108 • LVPECL Receiver Characteristics

 Worst-case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.15\text{ V}$

	On-Die Termination (ODT) in Ω	t_{py}	Units
		Speed Grade -1	
LVPECL (for MSIO I/O Bank)	None	2.71	ns
	100	2.71	ns

8.9 I/O Register Specifications

8.9.1 Input Register

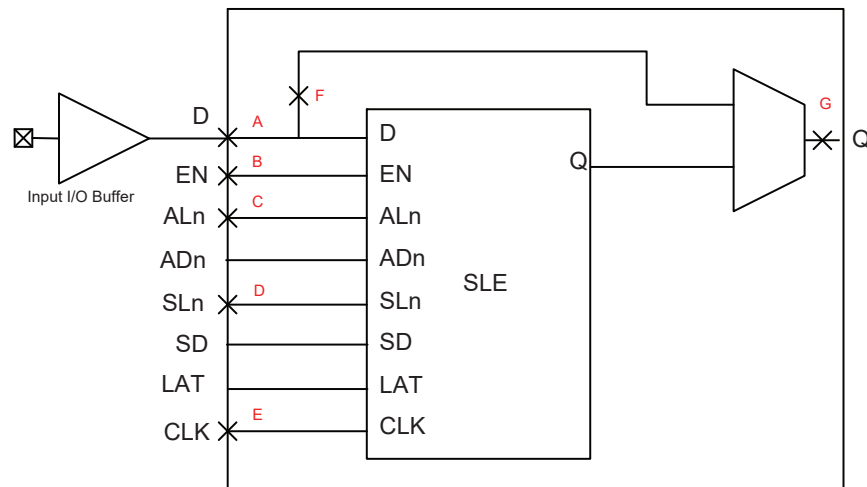


Figure 6 • Timing Model for Input Register

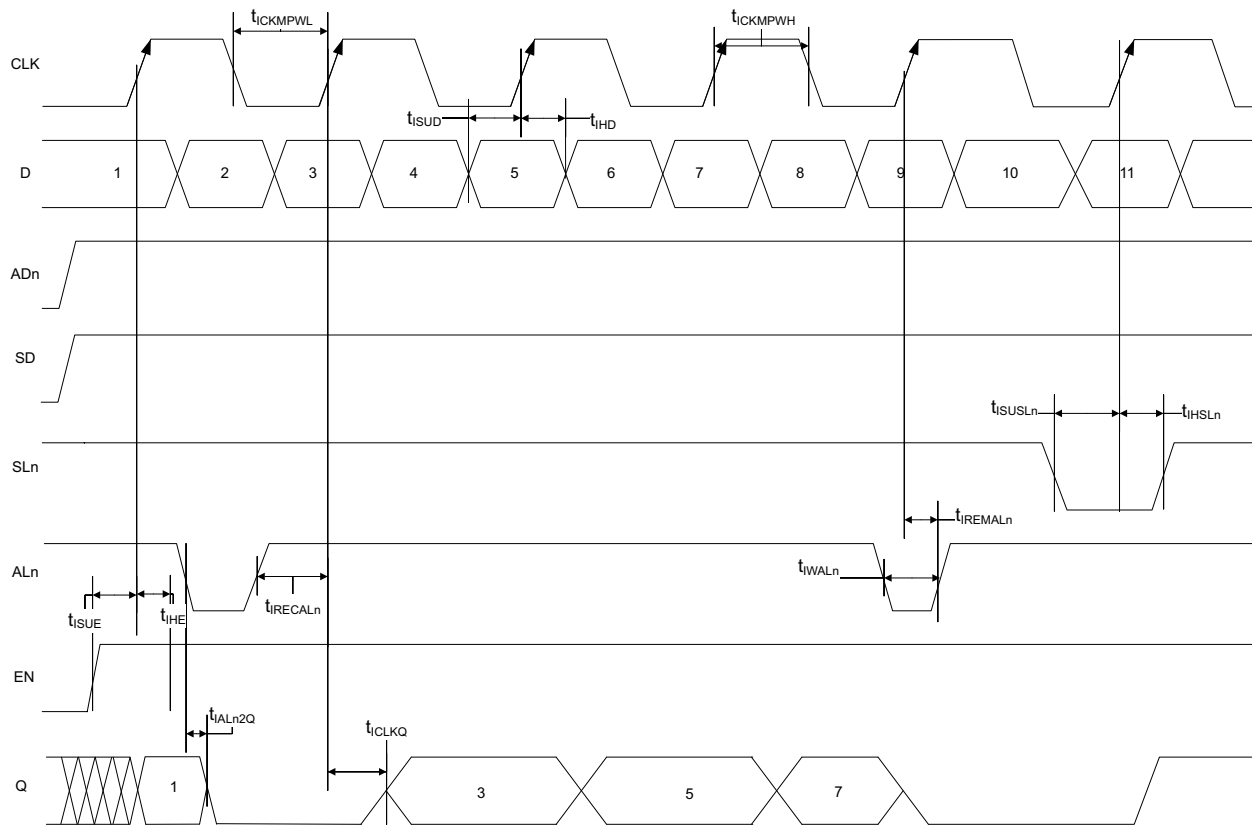


Figure 7 • I/O Register Input Timing Diagram

Table 109 • Input Data Register Propagation Delays
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
t_{BYP}	Bypass Delay of the Input Register	F,G	Note 1	ns
t_{CLKQ}	Clock-to-Q of the Input Register	E,G	0.13	ns
t_{SUD}	Data Setup Time for the Input Register	A,E	Note 1	ns
t_{IHD}	Data Hold Time for the Input Register	A,E	Note 1	ns
t_{SUE}	Enable Setup Time for the Input Register	B,E	0.821	ns
t_{IHE}	Enable Hold Time for the Input Register	B,E	0.016	ns
t_{SUSL}	Synchronous Load Setup Time for the Input Register	D,E	1.726	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D,E	0.062	ns
t_{ALn2Q}	Asynchronous Clear-to-Q of the Input Register ($\text{ADn}=1$)	C,G	0.502	ns
	Asynchronous Preset-to-Q of the Input Register ($\text{ADn}=0$)	C,G	0.459	ns
t_{IREMALn}	Asynchronous Load Removal Time for the Input Register	C,E	0.127	ns
t_{IRECALn}	Asynchronous Load Recovery Time for the Input Register	C,E	0.213	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input Register	C,C	0.444	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Input Register	E,E	0.101	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Input Register	E,E	0.223	ns

1. These timing parameters are dependent on die and I/O location. Use SmartTime tool in Libero for accurate timing data.

8.9.2 Output/Enable Register

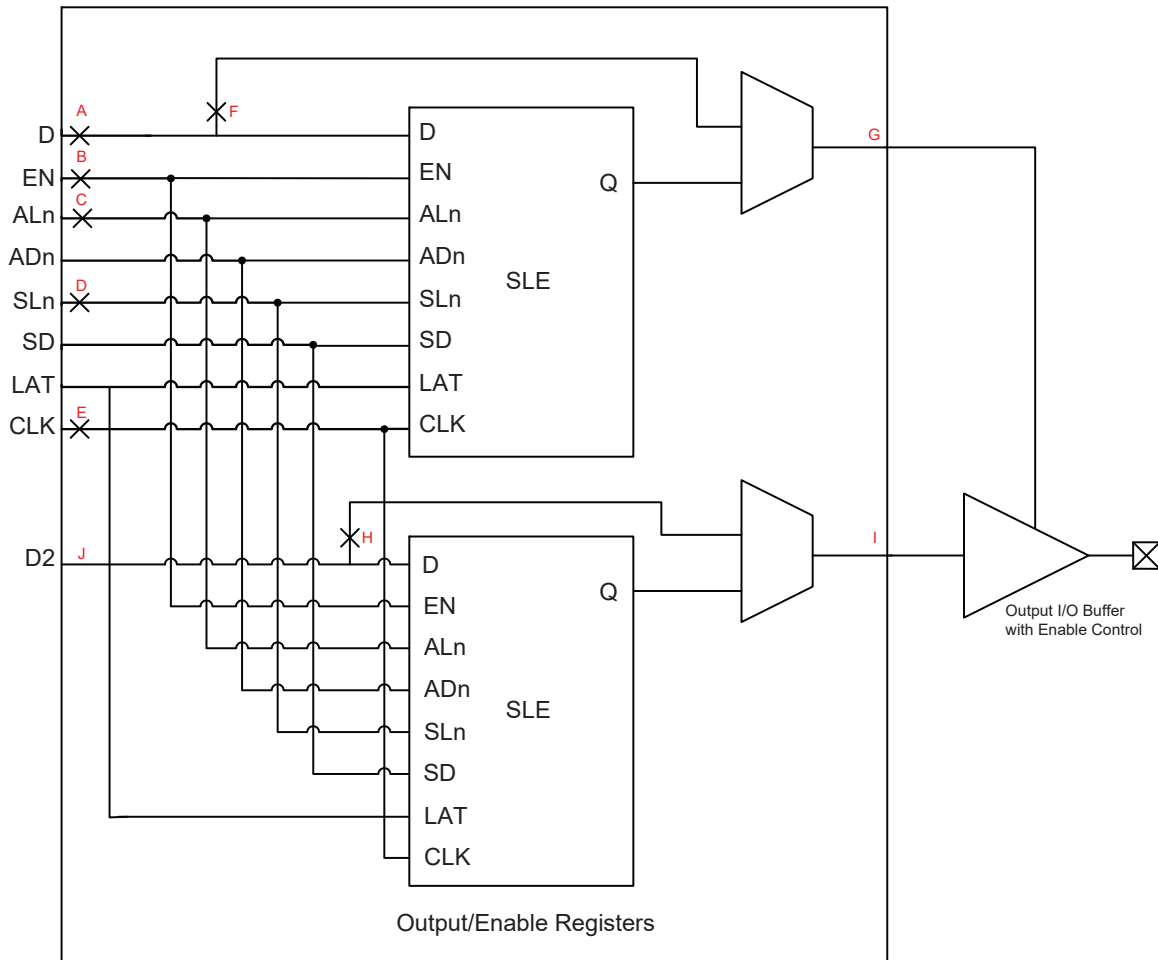
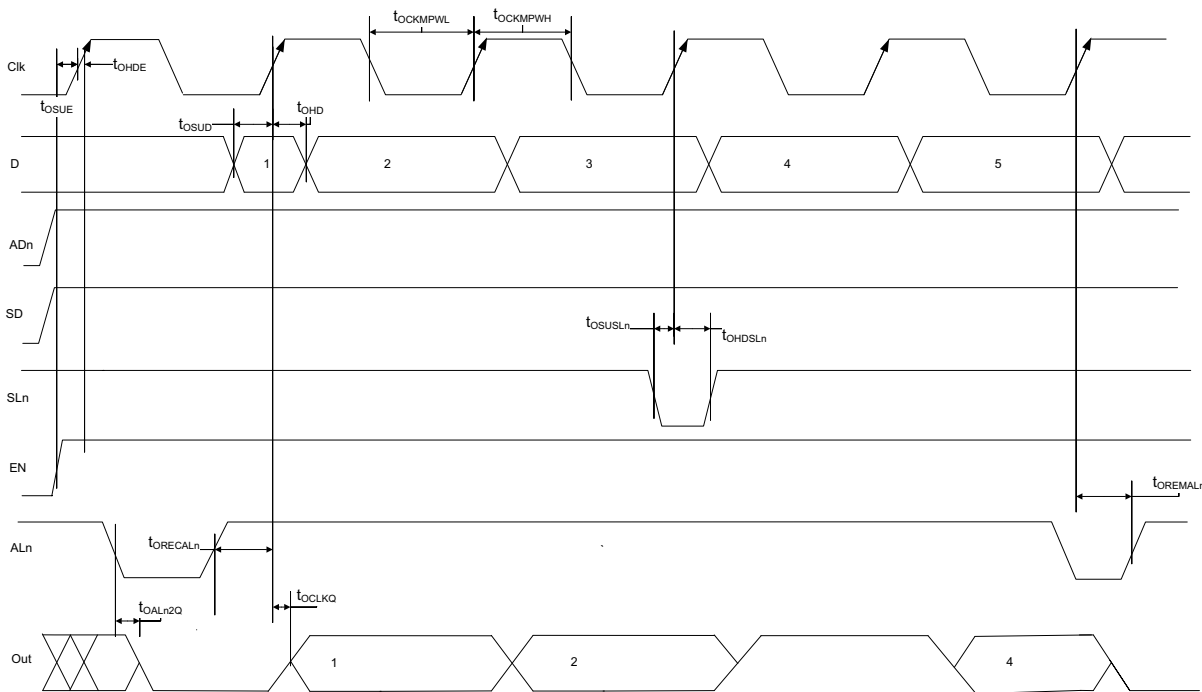


Figure 8 • Timing Model for Output/Enable Register


Figure 9 • I/O Register Output Timing Diagram
Table 110 • Output/Enable Data Register Propagation Delays
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
t_{OBYP}	Bypass Delay of the Output/Enable Register	F,G or H,I	0.342	ns
t_{OCLKQ}	Clock-to-Q of the Output/Enable Register	E,G or E,I	0.254	ns
t_{OSUD}	Data Setup Time for the Output/Enable Register	A,E or J,E	0.268	ns
t_{OHD}	Data Hold Time for the Output/Enable Register	A,E or J,E	0.037	ns
t_{OSUE}	Enable Setup Time for the Output/Enable Register	B,E	0.821	ns
t_{OHE}	Enable Hold Time for the Output/Enable Register	B,E	0.029	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable Register	D,E	1.824	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable Register	D,E	0.062	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable Register (ADn=1)	C,G or C,I	0.558	ns
	Asynchronous Preset-to-Q of the Output/Enable Register (ADn=0)	C,G or C,I	0.526	ns
t_{OREMALn}	Asynchronous Load Removal Time for the Output/Enable Register	C,E	0.134	ns
t_{ORECALn}	Asynchronous Load Recovery Time for the Output/Enable Register	C,E	0.236	ns

Table 110 • Output/Enable Data Register Propagation Delays
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C,C	0.444	ns
t_{OCKMPWH}	Clock Minimum Pulse Width High for the Output/Enable Register	E,E	0.101	ns
t_{OCKMPWL}	Clock Minimum Pulse Width Low for the Output/Enable Register	E,E	0.223	ns

8.10 DDR Module Specification

8.10.1 Input DDR Module

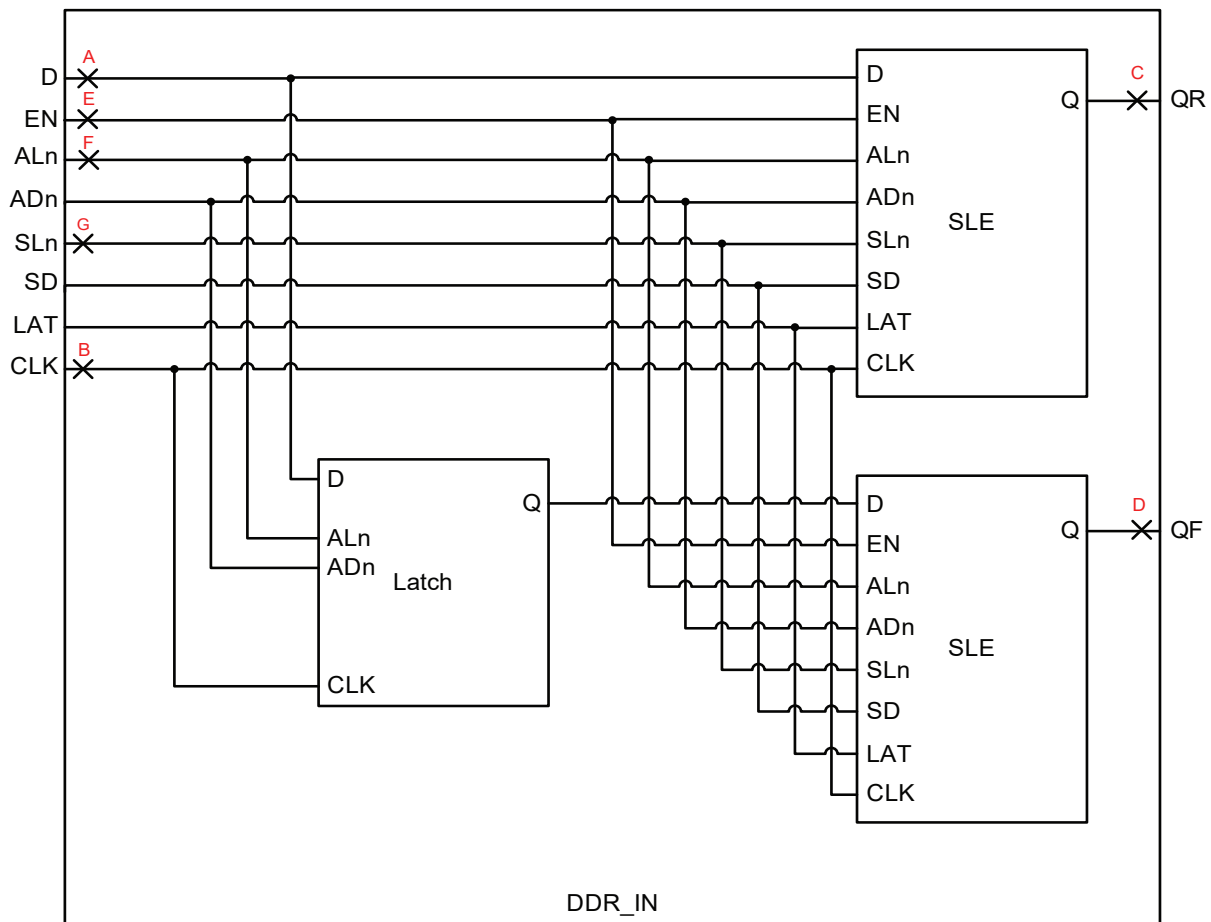


Figure 10 • Input DDR Module

8.10.2 Input DDR Timing Diagram

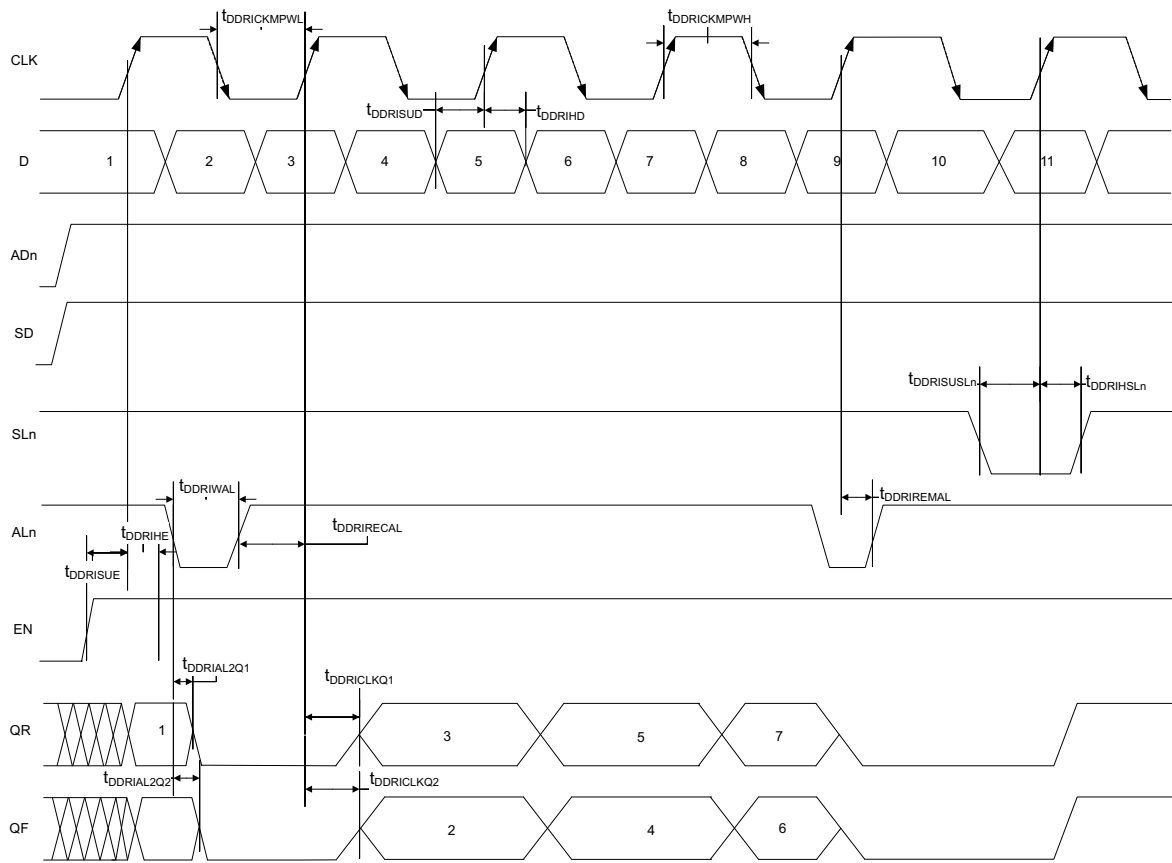


Figure 11 • Input DDR Timing Diagram

8.10.3 Timing Characteristics

Table 111 • Input DDR Propagation Delays

 Worst-Case Automotive Grade 2 Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
$t_{\text{DDRICKLQ1}}$	Clock-to-Out Out_QR for Input DDR	B,C	0.13	ns
$t_{\text{DDRICKLQ2}}$	Clock-to-Out Out_QF for Input DDR	B,D	0.131	ns
t_{DDRISUD}	Data Setup for Input DDR	A,B	Note 1	ns
t_{DDRIHD}	Data Hold for Input DDR	A,B	Note 1	ns
t_{DDRISUE}	Enable Setup for Input DDR	E,B	0.821	ns
t_{DDRIHE}	Enable Hold for Input DDR	E,B	0.016	ns
t_{DDRISUSL_n}	Synchronous Load Setup for Input DDR	G,B	1.726	ns
t_{DDRIHSL_n}	Synchronous Load Hold for Input DDR	G,B	0.062	ns
$t_{\text{DDRIAL2Q1}}$	Asynchronous Load-to-Out QR for Input DDR	F,C	0.459	ns
$t_{\text{DDRIAL2Q2}}$	Asynchronous Load-to-Out QF for Input DDR	F,D	0.416	ns
t_{DDRIREML}	Asynchronous Load Removal time for Input DDR	F,B	0.127	ns
$t_{\text{DDRIRECAL}}$	Asynchronous Load Recovery time for Input DDR	F,B	0.213	ns
t_{DDRIWAL}	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.444	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	B,B	0.101	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	B,B	0.223	ns

1. These timing parameters are dependent on die and I/O location. Use SmartTime tool in Libero for accurate timing data.

8.10.4 Output DDR Module

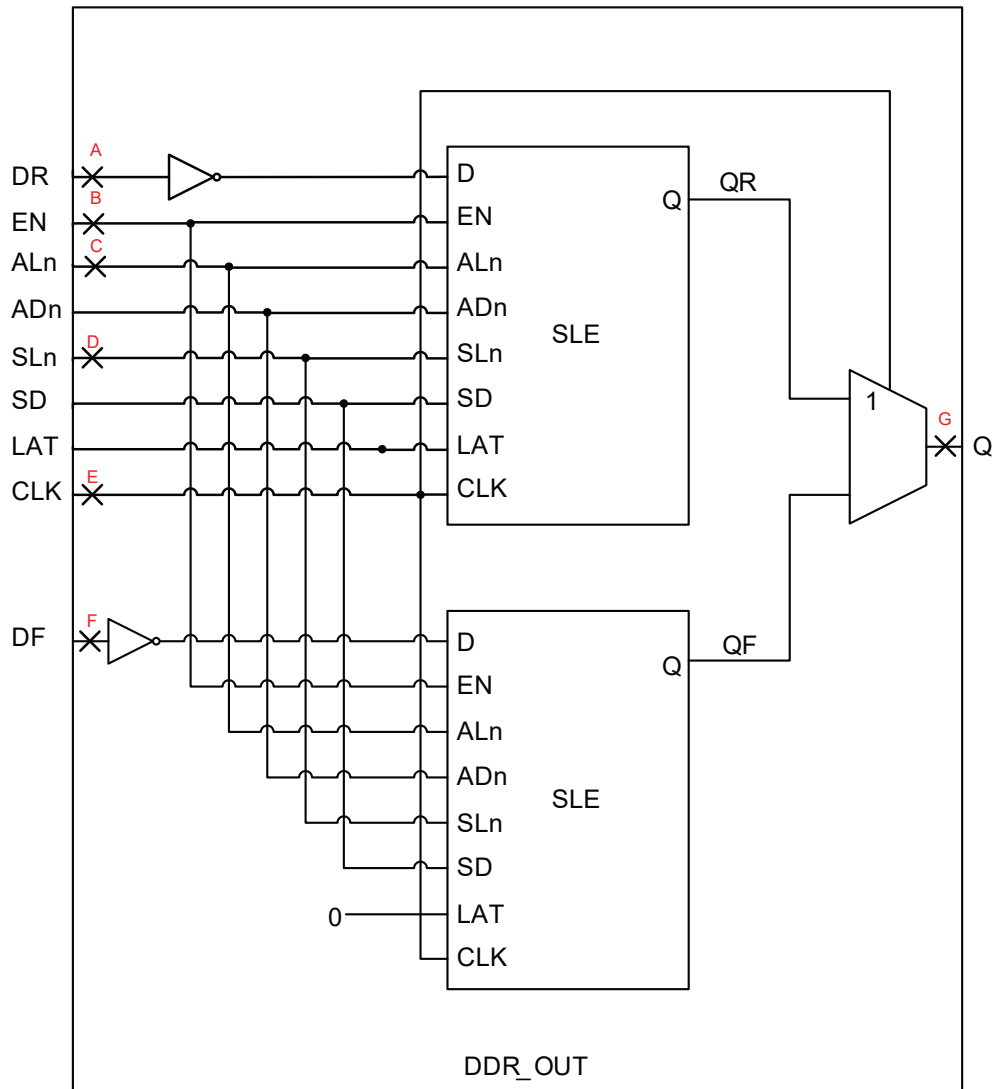
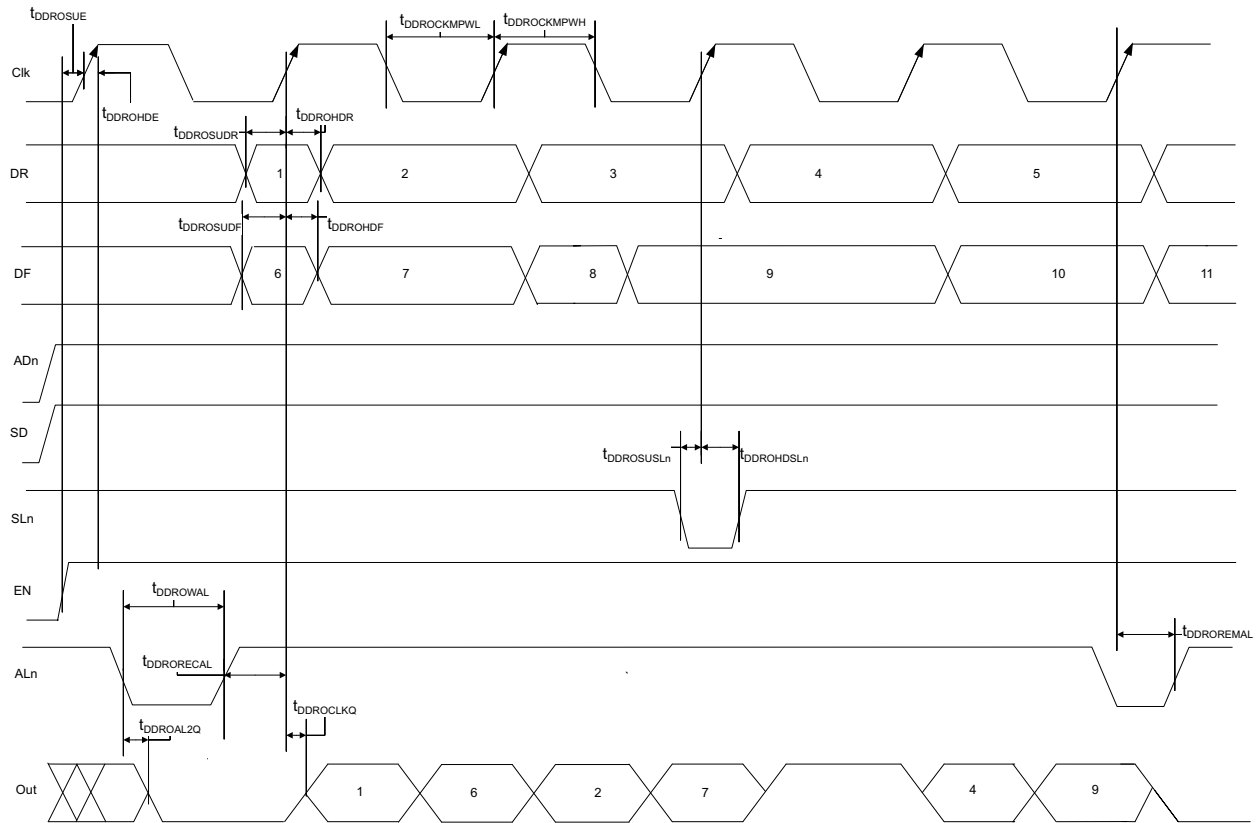


Figure 12 • Output DDR Module


Figure 13 • Output DDR Timing Diagram

8.10.5 Timing Characteristics

Table 112 • Output DDR Propagation Delays

 Worst-Case Automotive Grade 2 Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	Speed Grade -1	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	E,G	0.258	ns
t_{DDROSUDF}	DF Data Setup for Output DDR	F,E	0.278	ns
t_{DDROSUDR}	DR Data Setup for Output DDR	A,E	0.288	ns
t_{DDROHDF}	DF Data Hold for Output DDR	F,E	0.088	ns
t_{DDROHDR}	DR Data Hold for Output DDR	A,E	0.077	ns
t_{DDROSUE}	Enable Setup for Output DDR	B,E	0.829	ns
t_{DDROHE}	Enable Hold for Output DDR	B,E	0.031	ns
t_{DDROSUSL_n}	Synchronous Load Setup for Output DDR	D,E	1.831	ns
t_{DDROHSL_n}	Synchronous Load Hold for Output DDR	D,E	0.042	ns
t_{DDROAL2Q}	Asynchronous Load-to-Out for Output DDR	C,G	0.549	ns
$t_{\text{DDROREMAL}}$	Asynchronous Load Removal time for Output DDR	C,E	0.134	ns
$t_{\text{DDRORECAL}}$	Asynchronous Load Recovery time for Output DDR	C,E	0.238	ns
t_{DDROWAL}	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.377	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	E,E	0.101	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.223	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [SmartFusion2 and IGLOO2 Macro Library Guide](#).

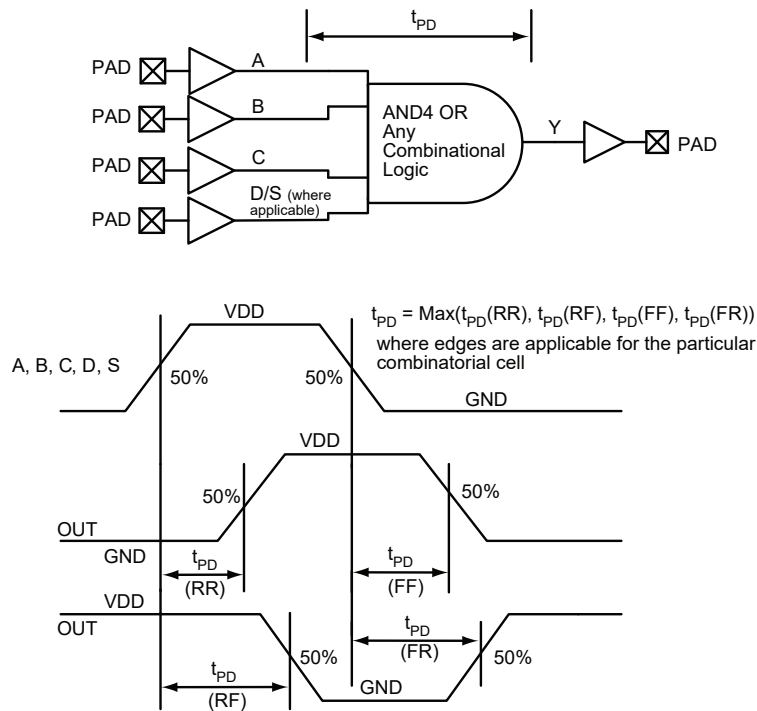


Figure 14 • LUT-4

9.1.1 Timing Characteristics

Table 113 • Combinatorial Cell Propagation Delays

Worst-Case Automotive Grade 2 Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Speed Grade -1	Units
INV	$Y = !A$	t_{PD}	0.104	ns
AND2	$Y = A \cdot B$	t_{PD}	0.17	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.152	ns
OR2	$Y = A + B$	t_{PD}	0.17	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.152	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.17	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.233	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.217	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.298	ns

9.2 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

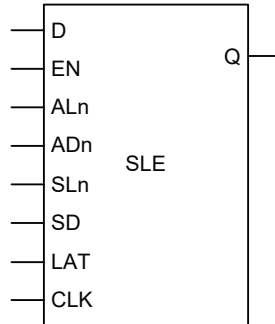


Figure 15 • Sequential Module

Figure 16 shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

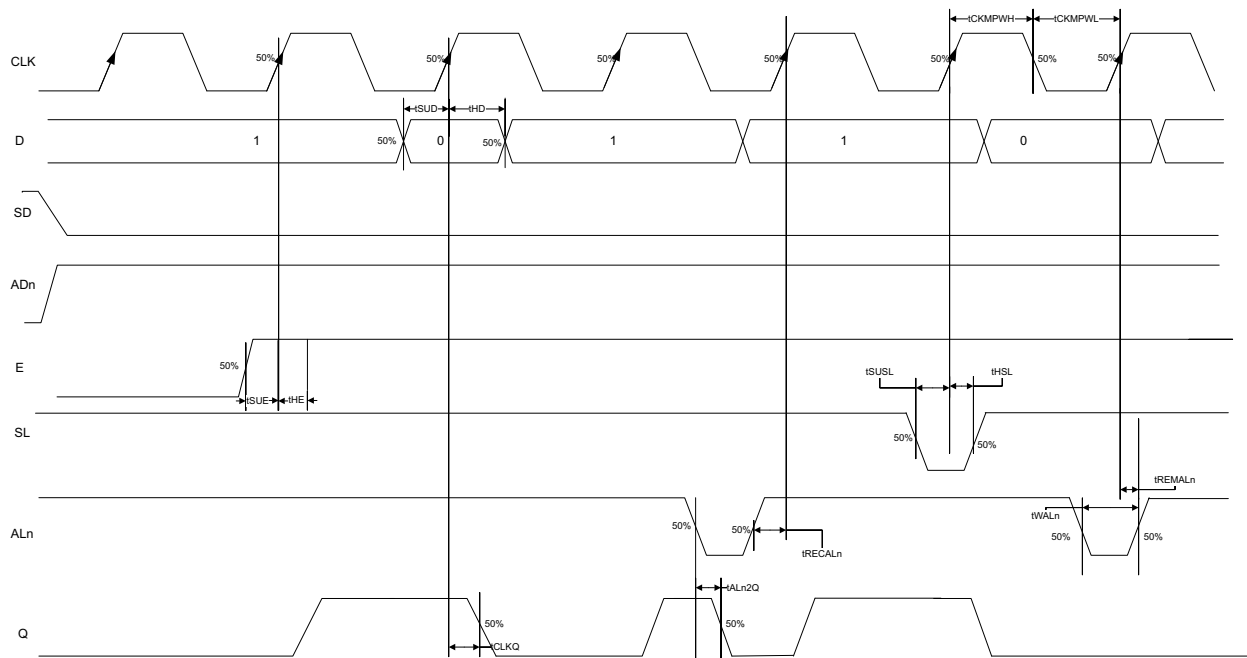


Figure 16 • Sequential Module Timing Diagram

9.2.1 Timing Characteristics

Table 114 • Register Delays

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.114	ns
t_{SUD}	Data Setup Time for the Core Register	0.262	ns
t_{HD}	Data Hold Time for the Core Register	0	ns
t_{SUE}	Enable Setup Time for the Core Register	0.318	ns
t_{HE}	Enable Hold Time for the Core Register	0	ns
t_{SUSL}	Synchronous Load Setup Time for the Core Register	0.565	ns
t_{HSL}	Synchronous Load Hold Time for the Core Register	0	ns
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core Register ($ADn=1$)	0.495	ns
	Asynchronous Preset-to-Q of the Core Register ($ADn=0$)	0.47	ns
t_{REMAIn}	Asynchronous Load Removal Time for the Core Register	0	ns
t_{RECALn}	Asynchronous Load Recovery Time for the Core Register	0.366	ns
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core Register	0.266	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.065	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.139	ns

10. Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the [UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide](#) for the positions of various global routing resources.

Table 115 • M2S090T Device Global Resource

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.793	0.847	ns
t_{RCKH}	Input High Delay for Global Clock	1.412	1.498	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.086	ns

Table 116 • M2S025T Device Global Resource

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.713	0.762	ns
t_{RCKH}	Input High Delay for Global Clock	1.306	1.391	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.085	ns

Table 117 • M2S010T Device Global Resource

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.598	0.639	ns
t_{RCKH}	Input High Delay for Global Clock	1.116	1.192	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.076	ns

Table 118 • M2S005T Device Global Resource

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.736	0.789	ns
t_{RCKH}	Input High Delay for Global Clock	0.927	0.995	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.068	ns

11. FPGA Fabric SRAM

Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

11.1 FPGA Fabric Large SRAM (LSRAM)

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
t_{ADDRSU}	Address Setup Time	0.455	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.352	–	ns
t_{DHD}	Data Hold Time	0.11	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.463	–	ns
t_{RDEHD}	Read Enable Hold Time	0.173	–	ns
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.402	–	ns
t_{WEHD}	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
t_{ADDRSU}	Address Setup Time	0.49	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.346	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.5	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.569	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t_{PLRSTREM}	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
t_{PLRSTREC}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t_{PLRSTMPW}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.428	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
t_{CLKMPWH}	Clock Minimum Pulse Width High	1.5	–	ns
t_{CLKMPWL}	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{\text{PLCLKMPWH}}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{\text{PLCLKMPWL}}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register		0.334	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.56	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.345	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.532	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		
		Min	Max	Units
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.473	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.631	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.34	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.546	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns
t_{RDPLESU}	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
t_{RDPLEHD}	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.583	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t_{PLRSTREM}	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
t_{PLRSTREC}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t_{PLRSTMPW}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.504	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 123 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
t_{CLKMPWH}	Clock Minimum Pulse Width High	1.5	–	ns
t_{CLKMPWL}	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{\text{PLCLKMPWH}}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{\text{PLCLKMPWL}}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns

Table 123 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t _{CLK2Q}	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.342	ns
	Access Time with Feed-Through Write Timing	–	1.559	ns
t _{ADDRSU}	Address Setup Time	0.646	–	ns
t _{ADDRHD}	Address Hold Time	0.282	–	ns
t _{DSU}	Data Setup Time	0.332	–	ns
t _{DHD}	Data Hold Time	0.084	–	ns
t _{BLKSU}	Block Select Setup Time	0.214	–	ns
t _{BLKHD}	Block Select Hold Time	0.223	–	ns
t _{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.559	ns
t _{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t _{RDESU}	Read Enable Setup Time	0.547	–	ns
t _{RDEHD}	Read Enable Hold Time	0.073	–	ns
t _{RDPLESU}	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
t _{RDPLEHD}	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t _{R2Q}	Asynchronous Reset to Output Propagation Delay		1.603	ns
t _{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t _{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t _{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t _{PLRSTREM}	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
t _{PLRSTREC}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t _{PLRSTMPW}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t _{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t _{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t _{WESU}	Write Enable Setup Time	0.468	–	ns
t _{WEHD}	Write Enable Hold Time	0.05	–	ns
F _{max}	Maximum Frequency	–	300	MHz

Table 124 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.322	ns
t_{ADDRSU}	Address Setup Time	0.323	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.348	–	ns
t_{DHD}	Data Hold Time	0.114	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.208	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.322	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.463	–	ns
t_{RDEHD}	Read Enable Hold Time	0.173	–	ns
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.402	–	ns
t_{WEHD}	Write Enable Hold Time	0.25	–	ns
F_{max}	Maximum Frequency	–	300	MHz

11.2 FPGA Fabric Micro SRAM (uSRAM)

Table 125 • uSRAM (RAM64x18) in 64x18 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.869	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.119	–	ns

Table 125 • uSRAM (RAM64x18) in 64x18 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{DINCHD}	Write Input Data hold Time	0.155	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.132	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

Table 126 • uSRAM (RAM64x16) in 64x16 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns

Table 126 • uSRAM (RAM64x16) in 64x16 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.866	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.119	–	ns
t_{DINCHD}	Write Input Data hold Time	0.155	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.132	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
Fmax	Maximum Frequency	–	250	MHz

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns

Table 127 • uSRAM (RAM128x9) in 128x9 Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t _{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t _{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t _{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
t _{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t _{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t _{R2Q}	Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled)	–	0.865	ns
t _{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t _{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t _{CCY}	Write Clock Period	4	–	ns
t _{CCLKMPWH}	Write Clock Minimum Pulse Width High	1.8	–	ns
t _{CCLKMPWL}	Write Clock Minimum Pulse Width Low	1.8	–	ns
t _{BLKCSU}	Write Block Setup Time	0.417	–	ns
t _{BLKCHD}	Write Block Hold Time	0.007	–	ns
t _{DINCSU}	Write Input Data setup Time	0.104	–	ns
t _{DINCHD}	Write Input Data hold Time	0.142	–	ns
t _{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t _{ADDRCHD}	Write Address Hold Time	0.24	–	ns
t _{WECSU}	Write Enable Setup Time	0.41	–	ns
t _{WECHD}	Write Enable Hold Time	-0.027	–	ns
F _{max}	Maximum Frequency	–	250	MHz

Table 128 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t _{CY}	Read Clock Period	4	–	ns
t _{CLKMPWH}	Read Clock Minimum Pulse Width High	1.8	–	ns
t _{CLKMPWL}	Read Clock Minimum pulse Width Low	1.8	–	ns
t _{PLCY}	Read Pipe-line clock period	4	–	ns
t _{PLCLKMPWH}	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
t _{PLCLKMPWL}	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t _{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
t _{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
t _{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
t _{RDENSU}	Read Enable Setup Time	0.287	–	ns
t _{RDENHD}	Read Enable Hold Time	0.059	–	ns
t _{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t _{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t _{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
t _{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t _{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t _{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.865	ns
t _{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t _{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t _{CCY}	Write Clock Period	4	–	ns
t _{CCLKMPWH}	Write Clock Minimum Pulse Width High	1.8	–	ns
t _{CCLKMPWL}	Write Clock Minimum Pulse Width Low	1.8	–	ns
t _{BLKCSU}	Write Block Setup Time	0.417	–	ns
t _{BLKCHD}	Write Block Hold Time	0.007	–	ns
t _{DINCSU}	Write Input Data setup Time	0.104	–	ns
t _{DINCHD}	Write Input Data hold Time	0.142	–	ns

Table 128 • uSRAM (RAM128x8) in 128x8 Mode

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t_{ADDRCHD}	Write Address Hold Time	0.24	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

Table 129 • uSRAM (RAM256x4) in 256x4 Mode

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
t_{CLKMPWH}	Read Clock Minimum Pulse Width High	1.8	–	ns
t_{CLKMPWL}	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{\text{PLCLKMPWH}}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{\text{PLCLKMPWL}}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.812	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.993	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.669	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.166	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.863	ns

Table 129 • uSRAM (RAM256x4) in 256x4 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.104	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.253	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.824	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.023	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.599	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns

Table 130 • uSRAM (RAM512x2) in 512x2 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
t_{CCLKMPWH}	Write Clock Minimum Pulse Width High	1.8	–	ns
t_{CCLKMPWL}	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.104	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
t_{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t_{ADDRCHD}	Write Address Hold Time	0.255	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

Table 131 • uSRAM (RAM1024x1) in 1024x1 Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
t_{CLKMPWH}	Read Clock Minimum Pulse Width High	1.8	–	ns
t_{CLKMPWL}	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{\text{PLCLKMPWH}}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{\text{PLCLKMPWL}}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns

Table 131 • uSRAM (RAM1024x1) in 1024x1 Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t _{CLK2Q}	Read Access Time with Pipeline Register	–	0.274	ns
	Read Access Time without Pipeline Register	–	1.839	ns
t _{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.041	–	ns
t _{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.623	–	ns
t _{RDENSU}	Read Enable Setup Time	0.287	–	ns
t _{RDENHD}	Read Enable Hold Time	0.059	–	ns
t _{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t _{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t _{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.236	ns
t _{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t _{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t _{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t _{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t _{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t _{CCY}	Write Clock Period	4	–	ns
t _{CCLKMPWH}	Write Clock Minimum Pulse Width High	1.8	–	ns
t _{CCLKMPWL}	Write Clock Minimum Pulse Width Low	1.8	–	ns
t _{BLKCSU}	Write Block Setup Time	0.417	–	ns
t _{BLKCHD}	Write Block Hold Time	0.007	–	ns
t _{DINCSU}	Write Input Data setup Time	0.003	–	ns
t _{DINCHD}	Write Input Data hold Time	0.142	–	ns
t _{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t _{ADDRCHD}	Write Address Hold Time	0.255	–	ns
t _{WECSU}	Write Enable Setup Time	0.41	–	ns
t _{WECHD}	Write Enable Hold Time	-0.027	–	ns
F _{max}	Maximum Frequency	–	250	MHz

12. Embedded NVM (eNVM) Characteristics

Table 132 • eNVM Read Performance

Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
		-55°C to 125°C		-40°C to 100°C		0°C to 85°C		
T _J	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	–
F _{MAXREAD}	eNVM Maximum Read Frequency	25	25	25	25	25	25	MHz

Table 133 • eNVM Page Programming

Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
		-55°C to 125°C		-40°C to 100°C		0°C to 85°C		
T _J	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	–
t _{PAGEPGM}	eNVM Page Programming Time	40	40	40	40	40	40	ms

13. Crystal Oscillator

Table 134 describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 134 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

 Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	20	–	MHz
ACCXTAL	Accuracy	–	–	0.006	%
CYCXTAL	Output duty cycle	–	49-51	47-53	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	200	300	ps
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	200	550	ps
IDYNXTAL	Operating current	–	1.5	–	mA
VIHXTAL	Input logic level High	0.9 × VPP	–	–	V
VILXTAL	Input logic level Low	–	–	0.1 × VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	1	ms

Table 135 • Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	2	–	MHz
ACCXTAL	Accuracy	–	–	0.003	%
CYCXTAL	Output duty cycle	–	49–51	47–53	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	1	5	ns
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	1	5	ns
IDYNXTAL	Operating current	–	0.3	–	mA
VIHXTAL	Input logic level High	$0.9 \times V_{PP}$	–	–	V
VILXTAL	Input logic level Low	–	–	$0.1 \times V_{PP}$	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	4.5	ms

Table 136 • Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	32	–	kHz
ACCXTAL	Accuracy	–	–	0.006	%
CYCXTAL	Output duty cycle	–	49–51	45.5–54.5	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	150	300	ns
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	150	300	ns
IDYNXTAL	Operating current	–	0.044	–	mA
VIHXTAL	Input logic level High	$0.9 \times V_{PP}$	–	–	V
VILXTAL	Input logic level Low	–	–	$0.1 \times V_{PP}$	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	120	ms

14. On-Chip Oscillator

Table 137 and Table 138 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 137 • Electrical Characteristics of the 50 MHz RC Oscillator

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter	–	200	500	ps
		Cycle-to-Cycle Jitter	–	320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 138 • Electrical Characteristics of the 1 MHz RC Oscillator

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	μs

15. Clock Conditioning Circuits (CCC)

Table 139 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032	–	200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	$f_{IN} \geq 1\text{ MHz}$	–	70	100	μs	–
	$f_{IN} = 32\text{ kHz}$	–	1	16	ms	–

Table 139 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification (continued)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Input Duty Cycle (Reference Clock)	Internal Feedback					
	$1\text{ MHz} \leq f_{\text{IN_CCC}} \leq 25\text{ MHz}$	10	–	90	%	–
	$25\text{ MHz} \leq f_{\text{IN_CCC}} \leq 100\text{ MHz}$	25	–	75	%	–
	$100\text{ MHz} \leq f_{\text{IN_CCC}} \leq 150\text{ MHz}$	35	–	65	%	–
	$150\text{ MHz} \leq f_{\text{IN_CCC}} \leq 200\text{ MHz}$	45	–	55	%	–
	External Feedback (CCC, FPGA, Off-chip)					
	$1\text{ MHz} \leq f_{\text{IN_CCC}} \leq 25\text{ MHz}$	25	–	75	%	–
	$25\text{ MHz} \leq f_{\text{IN_CCC}} \leq 35\text{ MHz}$	35	–	65	%	–
	$35\text{ MHz} \leq f_{\text{IN_CCC}} \leq 50\text{ MHz}$	45	–	55	%	–
Output duty cycle	005, 010, and 025 Devices	46	–	52	%	–
	060 and 090 Devices	44	–	52	%	–
Spread Spectrum Characteristics						
Modulation frequency range	–	25	35	50	kHz	–
Modulation depth range	–	0	–	1.5	%	–
Modulation depth control	–	–	0.5	–	%	–
Notes:						
1. The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide .						
2. The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.						

Table 140 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Conditions/Package Combinations					Units	Notes
CCC Output Peak-to-Peak Period Jitter $f_{\text{OUT_CCC}}$	–	–	–	–	–	–	–
010 FGG484 Packages	SSO = 0	$0 < \text{SSO} \leq 2$	$\text{SSO} \leq 4$	$\text{SSO} \leq 8$	$\text{SSO} \leq 16$	–	*
20 MHz to 100 MHz	$\text{Max}(110, \pm 1\% \times (1/f_{\text{OUT_CCC}}))$	$\text{Max}(150, \pm 1\% \times (1/f_{\text{OUT_CCC}}))$				ps	–
100 MHz to 400 MHz	120	150		170		ps	–
025 FGG484 Package	$0 < \text{SSO} \leq 16$						*
20 MHz to 74 MHz	$\pm 1\% \times (1/f_{\text{OUT_CCC}})$					ps	–
74 MHz to 400 MHz	210					ps	–
005 FGG484 Package	$0 < \text{SSO} \leq 16$						*
20 MHz to 53 MHz	$\pm 1\% \times (1/f_{\text{OUT_CCC}})$					ps	–
53 MHz to 400 MHz	270					ps	–
090 FGG484 and FGG676	$0 < \text{SSO} \leq 16$						*
20 MHz to 100 MHz	$\pm 1\% \times (1/f_{\text{OUT_CCC}})$					ps	–

Table 140 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Conditions/Package Combinations	Units	Notes
100 MHz to 400 MHz	150	ps	–
<i>Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.</i>			

Table 141 • Programming Time—Typical Automotive Grade 2 Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 1.2\text{ V}$ ¹

	Device	Image Size Bytes	JTAG		2 Step IAP			MSS/Cortex-M3 ISP (SmartFusion2 Only)			Auto Programming	Auto Update	Programming Recovery	Units
			Program	Verify	Authenticate	Program	Verify	Authenticate	Program	Verify	SPI CLK = 100 KHz	SPI CLK = 25 Mhz	SPI CLK = 12.5 Mhz	
Fabric Only	M2S010/M2GL010	568,784	28	18	7	23	12	10	26	14	77	35	35	sec
	M2S025/M2GL025	1,223,504	51	26	14	33	23	21	39	29	150	42	41	sec
	M2S060/M2GL060	2,418,896	77	54	39	61	50	44	65	54	291	83	82	sec
	M2S090/M2GL090	3,645,968	113	126	60	84	73	66	90	79	427	109	108	sec
eNVM Only	M2S010/M2GL010	274,816	78	9	4	76	11	4	82	7	86	87	87	sec
	M2S025/M2GL025	274,816	78	9	4	78	10	4	82	8	87	85	86	sec
	M2S060/M2GL060	268,480	76	8	5	76	22	6	80	8	78	86	86	sec
	M2S090/M2GL090	544,496	154	15	10	152	43	10	157	15	154	162	162	sec
Fabric + eNVM	M2S010/M2GL010	842,688	107	20	11	100	21	15	107	21	161	113	113	sec
	M2S025/M2GL025	1,497,408	120	35	19	113	32	26	121	35	229	120	121	sec
	M2S060/M2GL060	2,686,464	158	70	43	137	70	48	143	60	368	161	158	sec
	M2S090/M2GL090	4,190,208	266	147	68	236	115	75	244	91	582	261	260	sec

1. External SPI flash part# AT25DF641-s3H was used during this measurement.

Table 142 • Programming Time—Worst-case Conditions Grade 2 Conditions: T_j = 100°C, VDD = 1.14 V¹

			JTAG		2 Step IAP			MSS/Cortex-M3 ISP (SmartFusion2 Only)			Auto Programming	Auto Update	Programming Recovery	
			Program	Verify	Authenticate	Program	Verify	Authenticate	Program	Verify	SPI CLK = 100 KHz	SPI CLK = 25 Mhz	SPI CLK = 12.5 Mhz	
	Device	Image Size Bytes	Program	Verify	Authenticate	Program	Verify	Authenticate	Program	Verify	Program	Program	Program	Units
Fabric Only	M2S010/ M2GL010	568,784	50	18	7	45	12	10	48	14	99	57	57	sec
	M2S025/ M2GL025	1,223,504	73	26	14	55	23	21	61	29	150	64	63	sec
	M2S060/ M2GL060	2,418,896	99	54	39	83	50	44	87	54	313	105	104	sec
	M2S090/ M2GL090	3,645,968	135	126	60	106	73	66	112	79	449	131	130	sec
eNVM Only	M2S010/ M2GL010	274,816	100	9	4	98	11	4	104	7	108	109	109	sec
	M2S025/ M2GL025	274,816	100	9	4	100	10	4	104	8	109	107	108	sec
	M2S060/ M2GL060	268,480	98	8	5	98	22	6	102	8	100	108	108	sec
	M2S090/ M2GL090	544,496	176	15	10	174	43	10	179	15	176	184	184	sec
Fabric + eNVM	M2S010/ M2GL010	842,688	129	20	11	122	21	15	129	21	183	135	135	sec
	M2S025/ M2GL025	1,497,408	142	35	19	135	32	26	143	35	251	142	143	sec
	M2S060/ M2GL060	2,686,464	180	70	43	159	70	48	165	60	390	183	180	sec
	M2S090/ M2GL090	4,190,208	288	147	68	258	115	75	266	91	604	283	282	sec

1. External SPI flash part# AT25DF641-s3H was used during this measurement.

16. JTAG

Table 143 • JTAG 1532

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

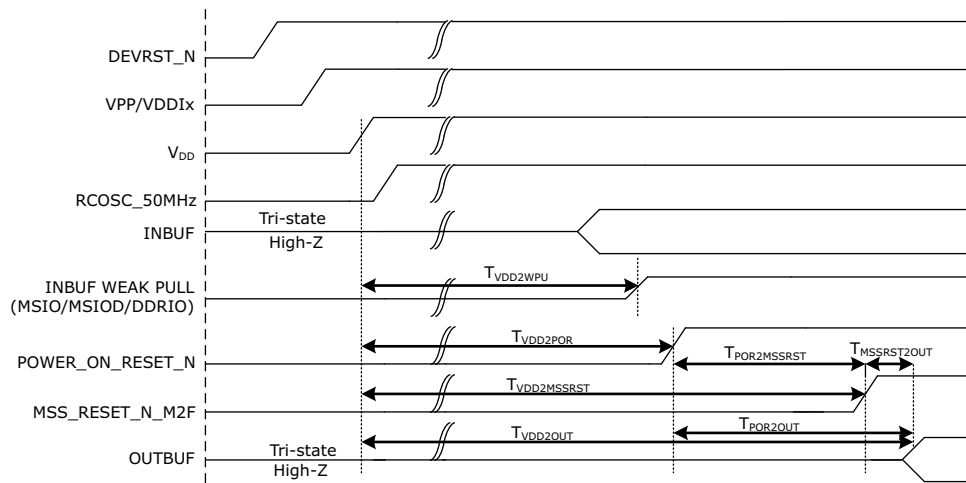
Parameter	Description	-1 Speed Grade					Units
		005	010	025	060	090	
t_{TCK2Q}	Clock to Q (data out)	7.71	7.91	7.95	8.54	9.21	ns
t_{RSTB2Q}	Reset to Q (data out)	7.91	6.54	6.27	8.70	7.94	ns
t_{DISU}	Test Data Input Setup Time	-1.07	-0.70	-0.70	-1.20	-1.33	ns
t_{DIHD}	Test Data Input Hold Time	2.43	2.38	2.47	2.55	2.71	ns
t_{TMSSU}	Test Mode Select Setup Time	-0.75	-0.86	-1.13	-0.99	-1.03	ns
t_{TMDHD}	Test Mode Select Hold Time	1.41	1.48	1.98	1.71	1.69	ns
t_{TRSTREM}	ResetB Removal Time	-0.81	-1.1	-1.38	-1.24	-0.8	ns
t_{TRSTREC}	ResetB Recovery Time	-0.81	-1.1	-1.38	-1.23	-0.8	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	25	MHz

17. Power-up to Functional Times

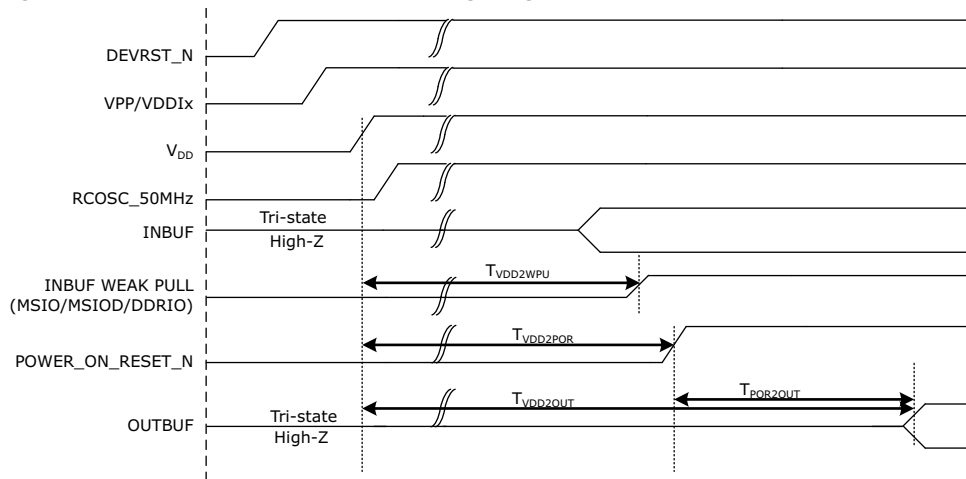
This section describes the maximum power-up to functional time in worst-case automotive Grade 2 conditions, $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 144 • Maximum Power-up to Functional Time When MSS/HPMS is Used (uS)

Parameter	From	To	Description	005	010	025	060	090
T_{POR2OUT}	POWER_ON_RESET_N	Output available at I/O	Fabric to output	647	500	531	474	524
$T_{\text{POR2MSSRST}}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	644	497	528	468	518
$T_{\text{MSSRST2OUT}}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.6	3.6	3.6	4.9	4.8
T_{VDD2OUT}	VDD	Output available at I/O	VDD at its minimum threshold level to output	3096	2975	3012	2869	2992
T_{VDD2POR}	VDD	POWER_ON_RESET_N	VDD at its minimum threshold level to Fabric	2476	2487	2496	2406	2563
$T_{\text{VDD2MSSRST}}$	VDD	MSS_RESET_N_M2F	VDD at its minimum threshold level to MSS	3093	2972	3008	2864	2987
T_{VDD2WPU}	VDD	DDRIO Inbuf Weak Pull	VDD to Inbuf Weak Pull	2500	2487	2509	2507	2519
	VDD	MSIO Inbuf Weak Pull	VDD to Inbuf Weak Pull	2504	2491	2510	2517	2525
	VDD	MSIOD Inbuf Weak Pull	VDD to Inbuf Weak Pull	2479	2468	2493	2486	2499

Figure 17 • Power-up to Functional Timing Diagram When MSS/HPMS is Used

Table 145 • Maximum Power-up to Functional Time When MSS/HPMS is not Used (uS)

Parameter	From	To	Description	005	010	025	060	090
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	114	114	114	114
$T_{VDD2OUT}$	VDD	Output available at I/O	VDD at its minimum threshold level to output	2587	2600	2607	2591	2600
$T_{VDD2POR}$	VDD	POWER_ON_RESET_N	VDD at its minimum threshold level to Fabric	2474	2486	2493	2477	2486
$T_{VDD2WPU}$	VDD	DDRIO Inbuf Weak Pull	VDD to Inbuf Weak Pull	2500	2487	2509	2507	2519
		MSIO Inbuf Weak Pull	VDD to Inbuf Weak Pull	2504	2491	2510	2517	2525
		MSIOD Inbuf Weak Pull	VDD to Inbuf Weak Pull	2479	2468	2493	2486	2499

Figure 18 • Power-up to Functional Timing Diagram When MSS/HPMS is not Used


18. DEVRST_N Characteristics

Table 146 • DEVRST_N Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

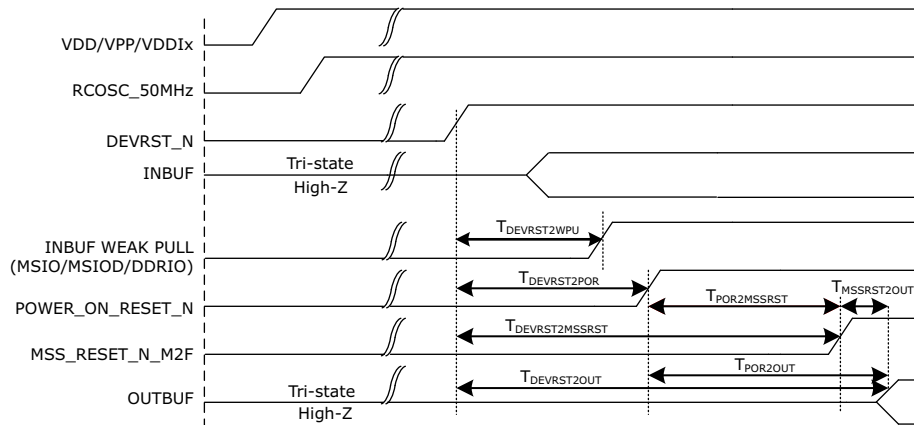
Symbol	Description	All Devices/Speed Grades			Units	Notes
		Min	Typ	Max		
TRAMPDEVRSTN	DEVRST_N ramp time	–	–	1	μs	
FMAXPDEVRSTN	DEVRST_N cycling rate	–	–	100	kHz	

19. DEVRST_N to Functional Times

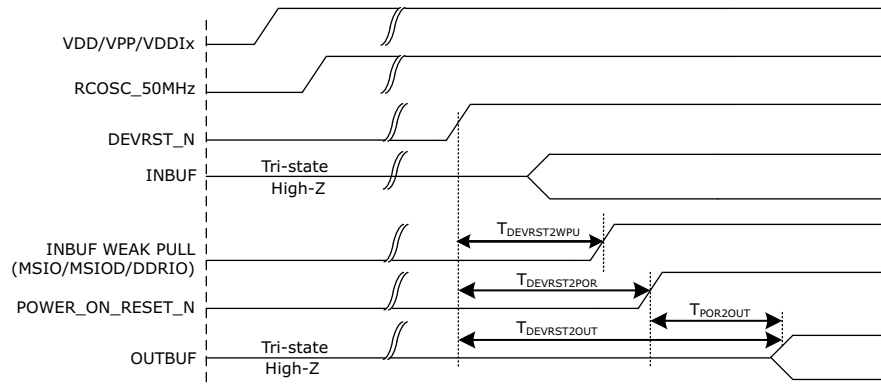
 This section describes the maximum DEVRST_N to functional time in worst-case automotive Grade 2 conditions, $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 147 • Maximum Power-up to Functional Time When MSS/HPMS is Used (μs)

Parameter	From	To	Description	005	010	025	060	090
T_{POR2OUT}	POWER_ON_RESET_N	Output available at I/O	Fabric to output	518	501	527	422	419
$T_{\text{POR2MSSRST}}$	POWER_ON_RESET_N	MSS_RESET_N_M2F	Fabric to MSS	515	497	524	417	414
$T_{\text{MSSRST2OUT}}$	MSS_RESET_N_M2F	Output available at I/O	MSS to output	3.5	3.5	3.5	4.8	4.8
$T_{\text{DEVRST2OUT}}$	DEVRST_N	Output available at I/O	VDD at its minimum threshold level to output	706	768	715	641	635
$T_{\text{DEVRST2POR}}$		POWER_ON_RESET_N	VDD at its minimum threshold level to Fabric	233	289	216	237	234
$T_{\text{DEVRST2MSSRST}}$		MSS_RESET_N_M2F	VDD at its minimum threshold level to MSS	702	765	712	636	630
$T_{\text{DEVRST2WPU}}$		DDRIO Inbuf Weak Pull	DEVRST_N to Inbuf Weak Pull	208	202	197	216	215
		MSIO Inbuf Weak Pull	DEVRST_N to Inbuf Weak Pull	208	202	197	216	215
		MSIOD Inbuf Weak Pull	DEVRST_N to Inbuf Weak Pull	208	202	197	216	215

Figure 19 • DEVRST_N to Functional Timing Diagram When MSS/HPMS is Used

Table 148 • Maximum Power-up to Functional Time when MSS/HPMS is not Used (uS)

Parameter	From	To	Description	005	010	025	060	090
$T_{POR2OUT}$	POWER_ON_RESET_N	Output available at I/O	Fabric to output	114	116	113	115	115
$T_{DEVRST2OUT}$	DEVRST_N	Output available at I/O	VDD at its minimum threshold level to output	314	353	314	343	341
$T_{DEVRST2POR}$		POWER_ON_RESET_N	VDD at its minimum threshold level to Fabric	200	238	201	230	229
$T_{DEVRST2WPU}$		DDRIO Inbuf Weak Pull	DEVRST_N to Inbuf Weak Pull	208	202	197	216	215
		MSIO Inbuf Weak Pull	DEVRST_N to Inbuf Weak Pull	208	202	197	216	215
	MSIOD Inbuf Weak Pull	DEVRST_N to Inbuf Weak Pull	208	202	197	216	215	

Figure 20 • DEVRST_N to Functional Timing Diagram when MSS/HPMS is not used


20. System Controller SPI Characteristics

Table 149 • System Controller SPI Characteristics
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units
			Min	Typ	Max	
SPIFMAX	Maximum operating frequency of SPI interface				20	MHz
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns
sp4 ¹	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.23 9	–	ns
sp5 ¹	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.24 5	–	ns
SPI Master Configuration ²						
SPI Master Configuration (Applicable to 005, 010, 025 Devices)						
sp6m	SPI_[0 1]_DO setup time		(SPI_x_CLK_period/2) - 8.0			ns
sp7m	SPI_[0 1]_DO hold time		(SPI_x_CLK_period/2) - 2.5			ns
sp8m	SPI_[0 1]_DI setup time		12			ns
sp9m	SPI_[0 1]_DI hold time		2.5			ns
SPI Slave Configuration (Applicable to 005, 010, 025 Devices)						
sp6s	SPI_[0 1]_DO setup time		(SPI_x_CLK_period/2) - 17.0			ns
sp7s	SPI_[0 1]_DO hold time		(SPI_x_CLK_period/2) + 3.0			ns
sp8s	SPI_[0 1]_DI setup time		2			ns
sp9s	SPI_[0 1]_DI hold time		7			ns
SPI Master Configuration (Applicable to 060, 090 Devices)						
sp6m	SPI_[0 1]_DO setup time		(SPI_x_CLK_period/2) - 7.0			ns
sp7m	SPI_[0 1]_DO hold time		(SPI_x_CLK_period/2) - 9.5			ns
sp8m	SPI_[0 1]_DI setup time		15			ns
sp9m	SPI_[0 1]_DI hold time		-2.5			ns

Table 149 • System Controller SPI Characteristics
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

SPI Slave Configuration (Applicable to 060, 090 Devices)					
sp6s	SPI_[0 1]_DO setup time		$(\text{SPI}_x_CLK_period/2) - 16.0$		ns
sp7s	SPI_[0 1]_DO hold time		$(\text{SPI}_x_CLK_period/2) - 3.5$		ns
sp8s	SPI_[0 1]_DI setup time		3		ns
sp9s	SPI_[0 1]_DI hold time		2.5		ns

- For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>. Use the supported I/O Configurations for the System Controller SPI in Table 150.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion2 ARM Cortex-M3 and Microcontroller Subsystem User's Guide.

Table 150 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

21. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 151 • Mathblocks With All Registers Used
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With All Registers Used		Speed Grade -1		Units
Parameter	Description	Min	Max	
t_{MISU}	Input, Control Register Setup time	0.149	–	ns
t_{MIHD}	Input, Control Register Hold time	0.08	–	ns
$t_{MOCINSU}$	CDIN Input Setup time	1.68	–	ns
$t_{MOCINHD}$	CDIN Input Hold time	-0.419	–	ns
$t_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	0.185	–	ns
$t_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	0.011	–	ns
$t_{MARSTREM}$	Asynchronous Reset Removal time	0	–	ns
$t_{MARSTREC}$	Asynchronous Reset Recovery time	0.088	–	ns
t_{MOCQ}	Output Register Clock to Out delay	–	0.232	ns
t_{MCLKMP}	CLK Minimum period	2.245	–	ns

Table 152 • Mathblock With Input Bypassed and Output Registers Used
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input Bypassed and Output Registers Used		Speed Grade -1		Units
		Min	Max	
Parameter	Description	Min	Max	Units
t_{MOSU}	Output Register Setup time	2.294	–	ns
t_{MOHD}	Output Register Hold time	-0.444	–	ns
t_{MOCDINSU}	CDIN Input Setup time	1.68	–	ns
t_{MOCDINH}	CDIN Input Hold time	-0.419	–	ns
$t_{\text{MSRSTENSU}}$	Synchronous Reset/Enable Setup time	0.115	–	ns
$t_{\text{MSRSTENHD}}$	Synchronous Reset/Enable Hold time	0.011	–	ns
t_{MARSTREM}	Asynchronous Reset Removal time	0	–	ns
t_{MARSTREC}	Asynchronous Reset Recovery time	0.014	–	ns
t_{MOCQ}	Output Register Clock to Out delay	–	0.232	ns
t_{MCLKMP}	CLK Minimum period	2.179	–	ns

Table 153 • Mathblock With Input Register Used and Output in Bypass Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade -1		Units
		Min	Max	
Parameter	Description	Min	Max	Units
t_{MISU}	Input Register Setup time	0.149	–	ns
t_{MIHD}	Input Register Hold time	0.08	–	ns
$t_{\text{MSRSTENSU}}$	Synchronous Reset/Enable Setup time	0.185	–	ns
$t_{\text{MSRSTENHD}}$	Synchronous Reset/Enable Hold time	-0.012	–	ns
t_{MARSTREM}	Asynchronous Reset Removal time	-0.005	–	ns
t_{MARSTREC}	Asynchronous Reset Recovery time	0.088	–	ns
t_{MICQ}	Input Register Clock to Output delay	–	2.52	ns
t_{MCDIN2Q}	CDIN to Output delay	–	1.951	ns

Table 154 • Mathblock With Input and Output in Bypass Mode
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input and Output in Bypass Mode		Speed Grade -1		Units
		Min	Max	
Parameter	Description	Min	Max	Units
t_{MIQ}	Input to Output delay	–	2.568	ns
t_{MCDIN2Q}	CDIN to Output delay	–	1.951	ns

22. Flash*Freeze Timing Characteristics

Table 155 • Flash*Freeze Entry and Exit Times

 Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$

Symbols	Parameters	Conditions	Entry/Exit Timing		Units	Notes
			FCLK = 100 MHz	FCLK = 3 MHz		
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	320	μs	
		eNVM and MSS/HPMS PLL = OFF	215	430	μs	
TFF_EXIT	Exit Time with respect to MSS PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	100	140	μs	
		eNVM = ON and MSS/HPMS PLL = OFF during F*F and MSS/HPMS PLL turned back on at exit	136	190	μs	
		eNVM and MSS PLL = OFF during F*F and both are turned back on at exit	200	285	μs	
		eNVM = OFF and MSS PLL = ON during F*F and eNVM turned back on at exit	200	285	μs	
	Exit Time with respect to Fabric PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	1.5	1.5	ms	1
		eNVM and MSS PLL = OFF during F*F and both are turned back on at exit	1.5	1.5	ms	1
	Exit Time with respect to Fabric buffer output	eNVM and MSS/HPMS PLL = ON during F*F	21	21	μs	
		eNVM and MSS PLL = OFF during F*F and both are turned back on at exit	65	65	μs	

Notes:

1. PLL Lock Delay set to 1024 cycles (default)

23. DDR Memory Interface Characteristics

Table 156 • DDR Memory Interface Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Standard	Supported Data Rate			Unit
	Min	Typ	Max	
DDR3		667		Mbps
DDR2		667		Mbps
LPDDR	50	—	400	Mbps

24. SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SerDes complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. Table 157 provides the electrical characteristics.

Table 157 • SFP Transceiver Electrical Characteristics

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Pin	Direction	Differential Peak-Peak Voltage			Unit	Note
		Min	Typ	Max		
RD+/-	Output	1600	–	2400	mV	1
TD+/-	Input	350	–	2400	mV	2

Notes:

1. Based on default SERDES transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

25. PCIe Electrical and Timing AC and DC Characteristics

PCIe is a high-speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 158 • Transmitter Parameters

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	μs

Table 159 • Receiver Parameters

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	μs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
RX-CID ¹	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	200	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

 1. AC-coupled, $BER = e^{-12}$.

Table 160 • SERDES Reference Clock AC Specifications

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, Worst-Case $V_{DD} = 1.14\text{ V}$

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	-300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

Table 161 • HCSL Minimum and Maximum DC Input Levels (Applicable to SERDES REFCLK Only)

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply Voltage	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
VI	DC Input voltage	0	–	2.625	V
HCSL Differential Voltage Specification					
VICM	Input common mode voltage	0.05	–	2.4	V
VIDIFF	Input differential voltage	100	–	1100	mV

Table 162 • HCSL Maximum AC Switching Speeds (Applicable to SERDES REFCLK Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HCSL AC Specifications						
Fmax	Maximum Data Rate (for MSIO IO Bank)	–	–	–	350	Mbps
HCSL Impedance Specifications						
Rt	Termination Resistance	–	–	100	–	Ω

26. SmartFusion2 Specifications

26.1 MSS Clock Frequency

Table 163 • Maximum Frequency for MSS Main Clock
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Speed Grade –1	Units
M3_CLK	Maximum frequency for the MSS Main Clock (FCLK)	133	MHz

26.2 SmartFusion2 Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to [Figure 21 on page 106](#).

Table 164 • I²C Characteristics
 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VIL	Input low voltage	Refer to the "Single-Ended I/O Standards" section on page 19 for more information. I/O standard used for illustration: MSIO bank– LVTTTL 8 mA low drive.	–0.3	–	0.8	V	–
VIH	Input high voltage	Refer to the "Single-Ended I/O Standards" section on page 19 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	2	–	3.45	V	–
VHYS	Hysteresis of Schmitt triggered inputs for $V_{DDI} > 2\text{ V}$	Refer to Table 21 on page 19 for more information.	0.05 x V_{DDI}	–	–	V	–
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 19 for more information.	–	–	10	μA	–
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 19 for more information.	–	–	10	μA	–
Tir	Input rise time	Standard Mode	–	–	1000	ns	–
		Fast Mode	–	–	300	ns	–
Tif	Input fall time	Standard Mode	–	–	300	ns	–
		Fast Mode	–	–	300	ns	–

Table 164 • I2C Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VOL	Maximum output voltage low (open drain) at 3 mA sink current for $V_{DDI} > 2\text{ V}$	Refer to the "Single-Ended I/O Standards" section on page 19 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	–	–	0.4	V	–
Cin	Pin capacitance	$V_{IN} = 0$, $f = 1.0\text{ MHz}$	–	–	10	pF	–
t_{OF}	Output fall time from V_{IHMin} to V_{ILMax}	V_{IHmin} to V_{ILMax} , $C_{load} = 400\text{ pF}$	–	21.04	–	ns	1
		V_{IHmin} to V_{ILMax} , $C_{load} = 100\text{ pF}$	–	5.556	–	ns	–
t_{OR}	Output rise time from V_{ILMax} to V_{IHMin}	V_{ILMax} to V_{IHmin} , $C_{load} = 400\text{ pF}$	–	19.887	–	ns	1
		V_{ILMax} to V_{IHmin} , $C_{load} = 100\text{ pF}$	–	5.218	–	ns	–
Rpull-up	Output buffer maximum pull-down resistance	–	–	–	50	Ω	2, 3
Rpull-down	Output buffer maximum pull-up resistance	–	–	–	131.25	Ω	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	–
		Standard mode	–	–	100	Kbps	–
t_{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	–

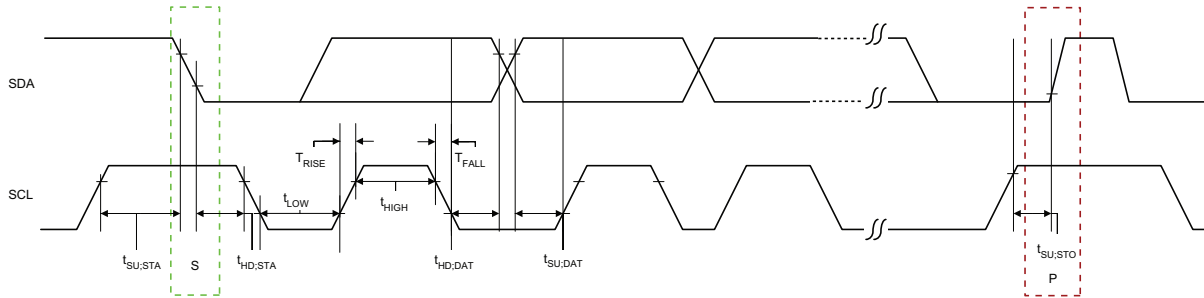
Notes:

1. These values are provided for MSIO Bank - LVTTTL 8 mA Low Drive at 25°C , typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIx} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
3. $R(\text{PULL-DOWN-MAX}) = (V_{OLspec}) / I_{OLspec}$
4. $R(\text{PULL-UP-MAX}) = (V_{DDImax} - V_{OHspec}) / I_{OHspec}$

Table 165 • I2C Switching Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Definition	Conditions	Speed Grade –1		Units
			Min	Max	
t_{LOW}	Low period of I2C_x_SCL	–	1	–	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	1	–	pclk cycles
$t_{HD;STA}$	START hold time	–	1	–	pclk cycles
$t_{SU;STA}$	START setup time	–	1	–	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	1	–	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	1	–	pclk cycles
$t_{SU;STO}$	STOP setup time	–	1	–	pclk cycles


Figure 21 • I²C Timing Parameter Definition

26.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to [Figure 22 on page 108](#).

Table 166 • SPI Characteristics

Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	48.2	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	0.1	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/32	0.19	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/64	0.39	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/128	0.77	–	–	μs	–
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	0.05	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/32	0.095	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/64	0.195	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/128	0.385	–	–	μs	–

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: <http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the [UG0331: SmartFusion2 Microcontroller Subsystem User Guide](#).

Table 166 • SPI Characteristics (continued)

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	All Devices/Speed Grades			Unit	Notes		
		Min	Typ	Max				
sp3	SPI_[0 1]_CLK minimum pulse width low							
	SPI_[0 1]_CLK = PCLK/2	6	–	–	ns	–		
	SPI_[0 1]_CLK = PCLK/4	12.05	–	–	ns	–		
	SPI_[0 1]_CLK = PCLK/8	24.1	–	–	ns	–		
	SPI_[0 1]_CLK = PCLK/16	0.05	–	–	μs	–		
	SPI_[0 1]_CLK = PCLK/32	0.095	–	–	μs	–		
	SPI_[0 1]_CLK = PCLK/64	0.195	–	–	μs	–		
	SPI_[0 1]_CLK = PCLK/128	0.385	–	–	μs	–		
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	–	2.77	–	ns	1		
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	–	2.906	–	ns	1		
SPI Master Configuration								
sp6m	SPI_[0 1]_DO setup time	$(\text{SPI}_x_CLK_period/2) - 3.0$			–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	$(\text{SPI}_x_CLK_period/2) - 2.5$			–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	8	–	–	ns	2		
sp9m	SPI_[0 1]_DI hold time	2.5	–	–	ns	2		
SPI Slave Configuration								
sp6s	SPI_[0 1]_DO setup time	$(\text{SPI}_x_CLK_period/2) - 12.0$			–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	$(\text{SPI}_x_CLK_period/2) + 3.0$			–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	2	–	–	ns	2		
sp9s	SPI_[0 1]_DI hold time	3	–	–	ns	2		
Notes:								
1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models .								
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.								

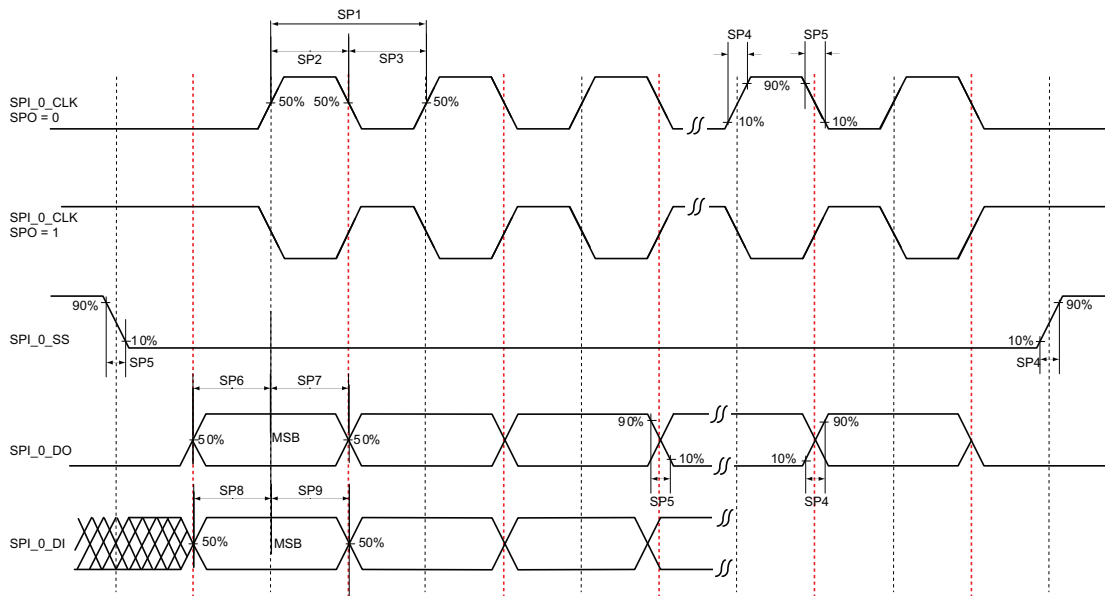


Figure 22 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

27. SRAM PUF

This section describes the SRAM PUF in worst-case automotive Grade 2 conditions, $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$. For more about on-static random-access memory (SRAM) physical unclonable functions (PUF) services, see [AC434: Using SRAM PUF System Service in SmartFusion2 Application Note](#).

Table 167 • SRAM PUF

Service	PUF OFF		PUF ON		Units
	Type	Maximum	Type	Maximum	
Create Activation Code	709.1	770.8	796.0	865.3	ms
Delete Activation Code	1329.3	1444.9	1303.0	1416.3	ms
Create Intrinsic KeyCode	656.6	713.7	643.6	699.5	ms
Create Extrinsic KeyCode	656.6	713.7	643.6	699.5	ms
Get Number of Keys	1.3	1.5	1.3	1.4	ms
Export (KC0, KC1)	998.0	1084.8	978.2	1063.3	ms
Export 2 KeyCodes	2020.2	2195.9	1980.2	2152.4	ms
Export 4 KeyCodes	3065.7	3332.2	3005.0	3266.3	ms
Export 8 KeyCodes	5101.0	5544.6	5000.0	5434.8	ms
Export 16 KeyCodes	9212.1	10013.2	9029.7	9814.9	ms
Import (KC0, KC1)	39.7	43.1	38.9	42.3	ms
Import 2 KeyCodes	50.1	54.5	49.1	53.4	ms
Import 4 KeyCodes	60.6	65.9	59.4	64.6	ms
Import 8 KeyCodes	80.9	87.9	79.3	86.2	ms
Import 16 KeyCodes	123.8	134.6	121.4	131.9	ms

Table 167 • SRAM PUF (continued)

Service	PUF OFF		PUF ON		Units
	Type	Maximum	Type	Maximum	
Delete KeyCode	552.5	600.6	541.6	588.7	ms
Fetch Key	31.4	34.1	11.5	12.5	ms
Fetch ECC Key	20.0	21.7	1.9	2.1	ms
Get Seed	2.0	2.2	0.9	1.0	ms

28. Non-deterministic Random Bit Generator Characteristics

This section describes the NRBG characteristics in worst-case automotive Grade 2 conditions, $T_J = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$. For more information about NRBG, see [AC407: Using NRBG Services in SmartFusion2 and IGLOO2 Devices Application Note](#).

Table 168 • Non-deterministic Random Bit Generator Characteristics

Service	Conditions		Timing	Units	Notes
	Prediction Resistance	Additional Input			
Instantiate	OFF	X	85	ms	
Generate (after Instantiate)	OFF	0	$4.5\text{ ms} + (7\text{ us/byte} \times \text{No. of Bytes})$		1
	OFF	64	$6.0\text{ ms} + (7\text{ us/byte} \times \text{No. of Bytes})$		
	OFF	128	$7.0\text{ ms} + (7\text{ us/byte} \times \text{No. of Bytes})$		
	ON	X	47	ms	
Generate (subsequent)	OFF	0	$0.5\text{ ms} + (7\text{ us/byte} \times \text{No. of Bytes})$		1
	OFF	64	$2.0\text{ ms} + (7\text{ us/byte} \times \text{No. of Bytes})$		
	OFF	128	$3.0\text{ ms} + (7\text{ us/byte} \times \text{No. of Bytes})$		
	ON	X	43	ms	
Reseed			40	ms	
Uninstantiate			0.16	ms	
Reset			0.10	ms	
Self Test	First time after power up		20	ms	
	Subsequent		6	ms	

1. If PUF_OFF, generate would incur additional PUF Delay time for consecutive service calls.

29. Cryptographic Block Characteristics

This section describes the Cryptographic block characteristics in worst-case automotive Grade 2 conditions, $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$. For more information about Cryptographic block and associated services, see [AC410: Using AES System Services in SmartFusion2 and IGLOO2 Devices Application Note](#) and [AC432: Using SHA-256 System Services in SmartFusion2 and IGLOO2 Devices Application Note](#).

Table 169 • Cryptographic Block Characteristics

Service	Conditions	Timing	Units
Any Service	First certificate check penalty at boot	11.5	ms
AES128/256 (Encoding / Decoding) ¹	Up to 100 blocks	200	kbps
	100 blocks up to 64k blocks	650	kbps
SHA256	512 bits	530	kbps
	1024 bits	770	kbps
	2048 bits	940	kbps
	24 kbits	1130	kbps
HMAC	512 bytes	810	kbps
	1024 bytes	880	kbps
	2048 bytes	920	kbps
	24 kbytes	970	kbps
KeyTree		1.6	ms
Challenge-Response	PUF = OFF	23	ms
	PUF = ON	6.6	ms
ECC Point Multiplication		590	ms
ECC Point Addition		8	ms

1. Using Cypher Block Chaining (CBC) mode.

30. CAN Controller Characteristics

Table 170 • CAN Controller Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units	Notes
FCANREFCLK	Internally Sourced CAN Reference Clock Frequency	–	–	128	MHz	*
BAUDCAN	CAN Performance Baud Rate	0.05	–	1	Mbps	–

Note: PCLK to CAN controller must be a multiple of 8 MHz.

31. USB Characteristics

Table 171 • USB Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
FUSBREFCLK	Internally Sourced USB Reference Clock Frequency	–	–	133	MHz
TUSBCLK	USB Clock Period	–	–	16.66	ns
TUSBPD	Clock to USB Data Propagation Delay	–	–	9.0	ns
TUSBSU	Setup Time for USB Data	–	–	6.0	ns
TUSBHD	Hold Time for USB Data	0	–	–	ns

32. SerDes Protocol Compliance

Table 172 • SerDes Protocol Compliance

Protocol	Maximum Data Rate (Gbps)	Speed Grade -1
PCIe Gen 1	2.5 Gbps	Yes
XAUI	3.125 Gbps	Yes
Generic EPCS	2.5 Gbps	Yes

33. MMUART Characteristics

This section describes the characteristics of MMUART in worst-Case automotive grade 2 conditions, $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$.

Table 173 • MMUART Characteristics

Parameter	Descriptions	Speed Grade - 1	Units
FMMUART_REF_CLK	Internally Sourced MMUART Reference Clock Frequency	133	MHz
BAUDMMUARTTx	Maximum Transmit Baud Rate	8.3125	Mbps
BAUDMMUARTRx	Maximum Receive Baud Rate	8.3125	Mbps

34. IGLOO2 Specifications

34.1 HPMS Clock Frequency

Table 174 • Maximum Frequency for HPMS Main Clock

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Speed Grade -1	Units
HPMS_CLK	Maximum Frequency for the HPMS Main Clock (FCLK)	133	MHz

34.2 IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to [Figure 23 on page 114](#).

Table 175 • SPI Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp1	SPI_[0]1_CLK minimum period					
	SPI_[0]1_CLK = PCLK/2	12	–	–	ns	–
	SPI_[0]1_CLK = PCLK/4	24.1	–	–	ns	–
	SPI_[0]1_CLK = PCLK/8	48.2	–	–	ns	–
	SPI_[0]1_CLK = PCLK/16	0.1	–	–	μs	–
	SPI_[0]1_CLK = PCLK/32	0.19	–	–	μs	–
	SPI_[0]1_CLK = PCLK/64	0.39	–	–	μs	–
	SPI_[0]1_CLK = PCLK/128	0.77	–	–	μs	–
sp2	SPI_[0]1_CLK minimum pulse width high					
	SPI_[0]1_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0]1_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0]1_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0]1_CLK = PCLK/16	0.05	–	–	μs	–
	SPI_[0]1_CLK = PCLK/32	0.095	–	–	μs	–
	SPI_[0]1_CLK = PCLK/64	0.195	–	–	μs	–
	SPI_[0]1_CLK = PCLK/128	0.385	–	–	μs	–

Table 175 • SPI Characteristics

 Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	0.05	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/32	0.095	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/64	0.195	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/128	0.385	–	–	μs	–
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	–	2.77	–	ns	1
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	–	2.906	–	ns	1
SPI Master Configuration						
sp6m	SPI_[0 1]_DO setup time	$(\text{SPI}_x_CLK_period/2) - 3.0$	–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	$(\text{SPI}_x_CLK_period/2) - 2.5$	–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	8	–	–	ns	2
sp9m	SPI_[0 1]_DI hold time	2.5	–	–	ns	2
SPI Slave Configuration						
sp6s	SPI_[0 1]_DO setup time	$(\text{SPI}_x_CLK_period/2) - 12.0$	–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	$(\text{SPI}_x_CLK_period/2) + 3.0$	–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	2	–	–	ns	2
sp9s	SPI_[0 1]_DI hold time	3	–	–	ns	2
Notes:						
1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models .						
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.						

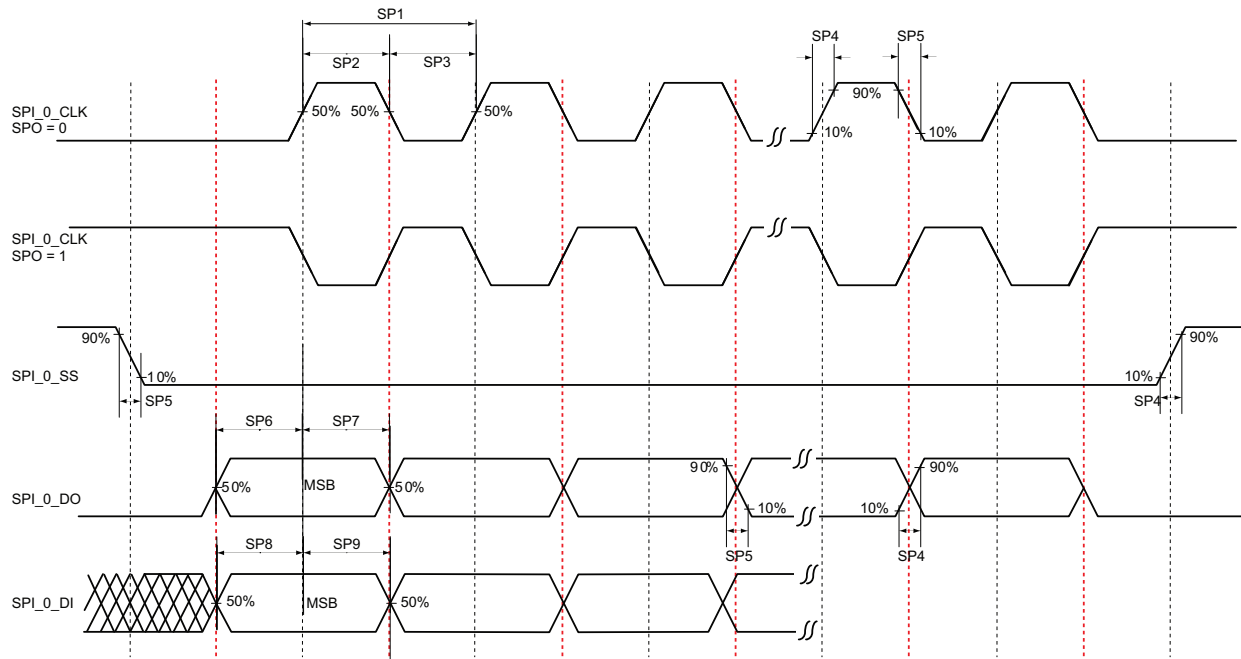


Figure 23 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes
Revision 4 (September 2018)	<p>The following information was updated in revision 4.0 of this document.</p> <ul style="list-style-type: none"> Information about VDDIx in recommended operational conditions table was updated. See Table 3. Information about VOH and VOL were updated. See Table 28. Information about DEVRSTN ramp time was updated. See Table 146. Information about RX-CID was updated. See Table 159. <p>The following information was added in revision 4.0 of this document.</p> <ul style="list-style-type: none"> A note about VID was added to LVDS differential voltage specification. See Table 84.
Revision 3 (May 2018)	<p>The following information was updated in revision 3.0 of this document.</p> <ul style="list-style-type: none"> 060 device status is changed to production. See Table 1. Currents during power cycle, verify cycle, and inrush current at power-up was updated. See Table 12, Table 13, and Table 14. Junction temperature. See Table 2. High temperature data retention. See Table 7 and Figure 1. Input capacitance and leakage current. See Table 19. DC input voltage. See Table 102. Speed grade -1. See Table 109, Table 110, Table 111, Table 112, Table 113, and Table 114. Acquisition time in CCC/PLL specification. See Table 139. SPI characteristics. See Table 149. F*F exit and entry timings. See Table 155. <p>The following information was added in revision 3.0 of this document.</p> <ul style="list-style-type: none"> 060 device was added to VPP. See Table 3. Digest temperature and digest cycle. See Table 4. Quiescent Supply Current characteristics of 060 device was added. See Table 10 and Table 11. Programming timing in typical and worse-case conditions. See Table 141 and Table 142. 060 device was added in JTAG. See Table 143. Power-up. See "Power-up to Functional Times". DEVRST_N. See "DEVRST_N to Functional Times". SRAM PUF. See Table 167. Non-deterministic Random Bit Generator (NRBG) Characteristics. See Table 168. Cryptographic block characteristics. See Table 169. SerDes protocol compliance. See Table 172. MMUART. See Table 173.

Revision	Changes
Revision 2 (September 2015)	Updated Table 10: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process" for typical process values.
	Updated Table 11: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process" for worst-case process values.
	Updated Table 140: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications" for FGG.
Revision 1 (June 2015)	Initial release.

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in [Table 1 on page 1](#) is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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