

#### 7 CIRCUIT DARLINGTON TRANSISTOR ARRAY

#### FEATURES

- Output Current : 500mA Max.
- High Sustaining Voltage Outputs : 50V Min.
- Output Clamp Diodes.
- Inputs Compatible With Various Types of Logic.
- PKG Type AP : DIP-16Pin AF : FLP-16Pin

TYPE	INPUT RESISTOR	DESIGNATION
KID65001AP/AF	No (External)	General Purpose
KID65002AP/AF	Zener Diode 7V+10.5k	14 25V P-MOS
KID65003AP/AF	2.7k	TTL, 5V C-MOS
KID65004AP/AF	10.5k	6 15V P-MOS, C-MOS

#### DESCRIPTION:

The KID65001AP/AF Series are high-voltage, high-current darlington transistor array comprised of seven NPN darlington pairs. All units feature internal clamp diodes for switching inductive loads.

#### MAXIMUM RATINGS (Ta=25 , unless otherwise noted)

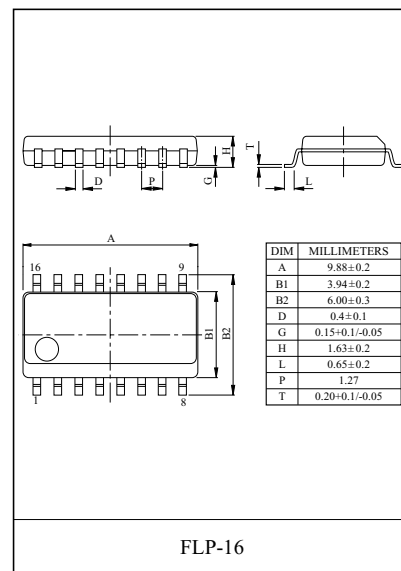
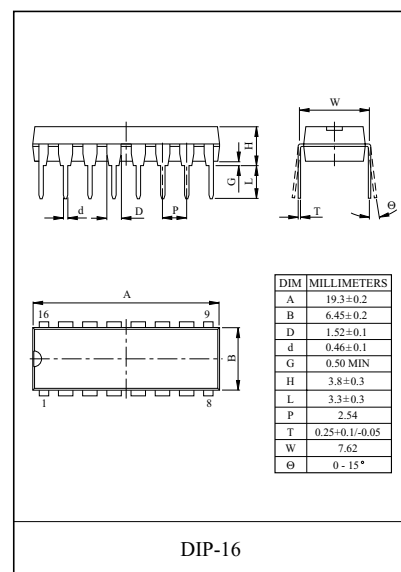
CHARACTERISTIC		SYMBOL	RATING	UNIT
Output Sustaining Voltage		$V_{CE(SUS)}$	50	V
Output Current		$I_{OUT}$	500	mA/ch
Input Voltage		$I_{IN}^{1)}$	-0.5 +30	V
Input Current		$I_{IN}^{2)}$	25	mA
Clamp Diode	Reverse Voltage	$V_R$	50	V
	Forward Current	$I_F$	500	mA
GND Terminal Current		$I_{GND}$	2.8	A
Power Dissipation	AP	$P_D$	1.47	W
	AF		0.54 /0.63 <sup>3)</sup> /1.25 <sup>4)</sup>	W
Operating Temperature		$T_{opr}$	-40 85	
Storage Temperature		$T_{stg}$	-55 150	

1) Except KID65001AP/AF

2) Only KID65001AP/AF

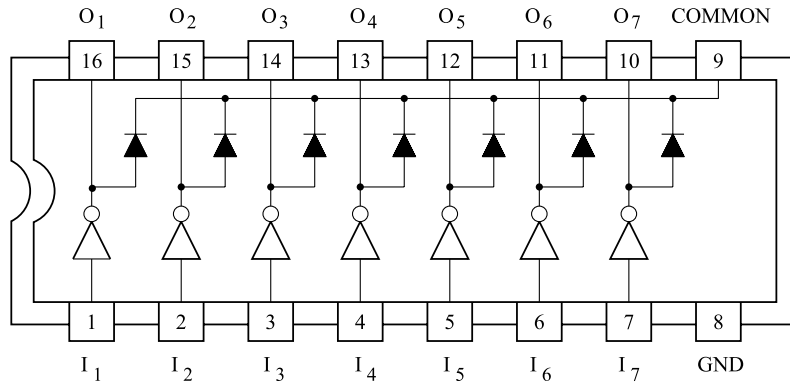
3) On PCB(30 × 30 × 1.6mm, Cu 50%)

4) On PCB (Test Board : JEDEC 2s2p)

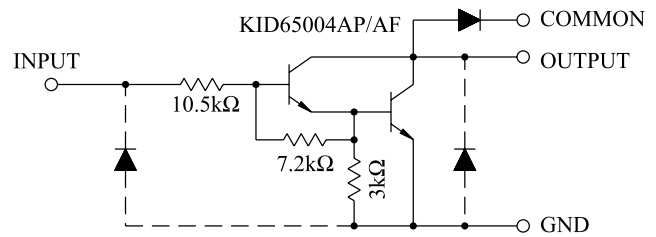
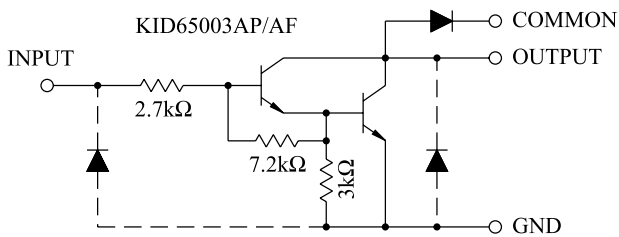
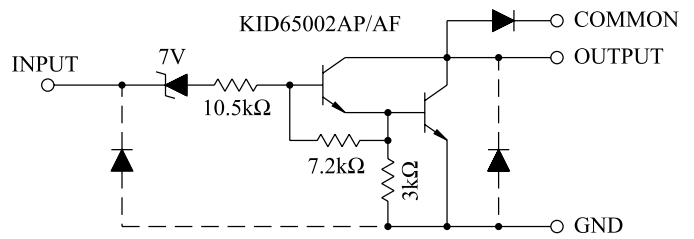
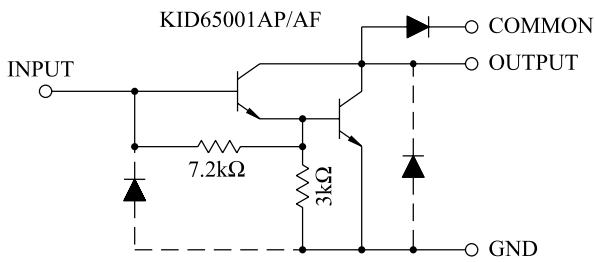


# KID65001AP/AF~KID65004AP/AF

## PIN CONNECTION (TOP VIEW)



## SCHEMATICS (EACH DRIVER)



# KID65001AP/AF~KID65004AP/AF

## RECOMMENDED OPERATING CONDITIONS (Ta=-40 ~ 85 °C)

CHARACTERISTIC		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Sustaining Voltage		V <sub>CE(SUS)</sub>	-	0	-	50	V
Output Current	I <sub>OUT</sub> (AP, Ta=85 °C)		T <sub>PW</sub> =25ms, Duty=10%, 7 Circuits	0	-	370	mA
			T <sub>PW</sub> =25ms, Duty=30%, 7 Circuits	0	-	200	
	I <sub>OUT</sub> (AF, Ta=85 °C)		T <sub>PW</sub> =25ms, Duty=10%, 7 Circuits	-	-	290	mA
			T <sub>PW</sub> =25ms, Duty=30%, 7 Circuits	-	-	150	
Input Voltage		V <sub>IN</sub>	Except KID65001AP/AF	0	-	30	V
Input Current		I <sub>IN</sub>	Only KID65001AP/AF	0	-	5	mA
Clamp Diode Reverse Voltage		V <sub>R</sub>	-	-	-	50	V
Clamp Diode Forward Current		I <sub>F</sub>	-	-	-	400	mA
Power Dissipation	AP	P <sub>D</sub>	Ta=85	-	-	0.76	W
	AF		Ta=85	0.28 / 0.32* / 0.65**			

\* On PCB (30 × 30 × 1.6mm, Cu 50%)

\*\* On PCB (Test Board : JEDEC 2s2p)

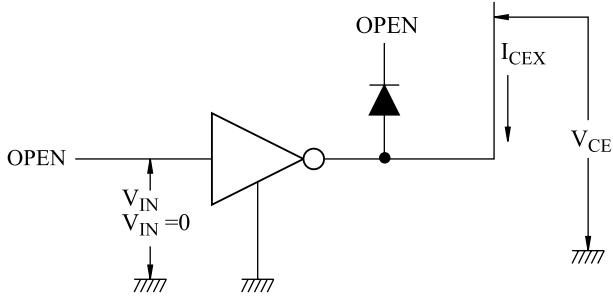
## ELECTRICAL CHARACTERISTICS (Ta=25 °C, unless otherwise noted)

CHARACTERISTICS		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leak Current	KID65002AP/AF KID65004AP/AF	I <sub>CEX</sub>	1	V <sub>CE</sub> =50V, Ta=25	-	-	50	μA
				V <sub>CE</sub> =50V, Ta=85	-	-	100	
				V <sub>CE</sub> =50V, V <sub>IN</sub> =6V	-	-	500	
				V <sub>CE</sub> =50V, V <sub>IN</sub> =1V	-	-	500	
Collector-Emitter Saturation Voltage		V <sub>CE(sat)</sub>	2	I <sub>OUT</sub> =350mA, I <sub>IN</sub> =500 μA	-	1.3	1.6	V
				I <sub>OUT</sub> =200mA, I <sub>IN</sub> =350 μA	-	1.1	1.3	
				I <sub>OUT</sub> =100mA, I <sub>IN</sub> =250 μA	-	0.9	1.1	
Input Current (Output On)	KID65002AP/AF KID65003AP/AF KID65004AP/AF	I <sub>IN(ON)</sub>	3	V <sub>IN</sub> =17V	-	0.82	1.25	mA
				V <sub>IN</sub> =3.85V	-	0.93	1.35	
				V <sub>IN</sub> =5V	-	0.35	0.5	
				V <sub>IN</sub> =12V	-	1.0	1.45	
Output Current (Output Open)		I <sub>IN(OFF)</sub>	4	I <sub>OUT</sub> =500 μA, Ta=85	50	65	-	μA
Input Voltage	KID65002AP/AF KID65003AP/AF KID65004AP/AF	V <sub>IN(ON)</sub>	5	V <sub>CE</sub> =2V, I <sub>OUT</sub> =300mA	-	-	13	V
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =200mA	-	-	2.4	
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =250mA	-	-	2.7	
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =300mA	-	-	3.0	
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =125mA	-	-	5.0	
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =200mA	-	-	6.0	
				V <sub>CE</sub> =2V, I <sub>OUT</sub> =275mA	-	-	7.0	
	V <sub>CE</sub> =2V, I <sub>OUT</sub> =350mA	-	-	8.0				
	KID65002AP/AF KID65003AP/AF KID65004AP/AF	V <sub>IN(OFF)</sub>			-	0	-	7.4
					-	0	-	0.7
-					0	-	1.0	
DC Current Transfer Ratio		h <sub>FE</sub>	2	V <sub>CE</sub> =2V, I <sub>OUT</sub> =350mA	1000	-	-	
Clamp Diode Reverse Current		I <sub>R</sub>	6	V <sub>R</sub> =50V, Ta=25	-	-	50	μA
				V <sub>R</sub> =50V, Ta=85	-	-	100	
Clamp Diode Forward Voltage		V <sub>F</sub>	7	I <sub>F</sub> =350mA	-	-	2.0	V
Input Capacitance		C <sub>IN</sub>	-	-	-	15	-	pF
Turn-ON Delay		t <sub>ON</sub>	8	V <sub>OUT</sub> =50V, R <sub>L</sub> =163 Ω, C <sub>L</sub> =15pF	-	0.1	-	μs
Turn-OFF Delay		t <sub>OFF</sub>			-	0.2	-	

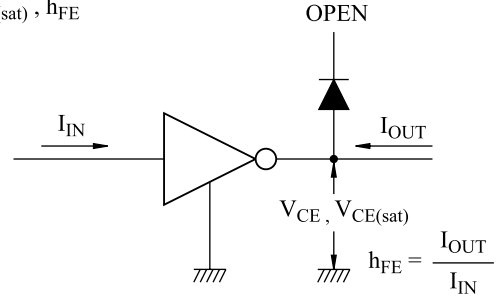
# KID65001AP/AF~KID65004AP/AF

## TEST CIRCUIT

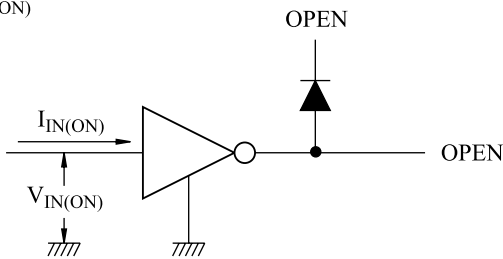
1.  $I_{CEX}$



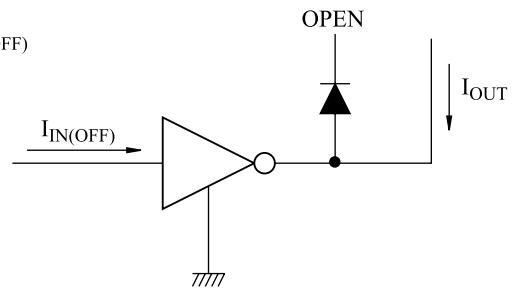
2.  $V_{CE(sat)}, h_{FE}$



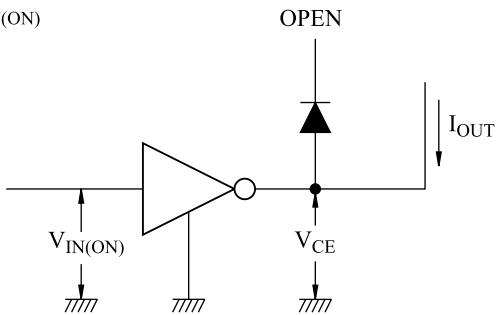
3.  $I_{IN(ON)}$



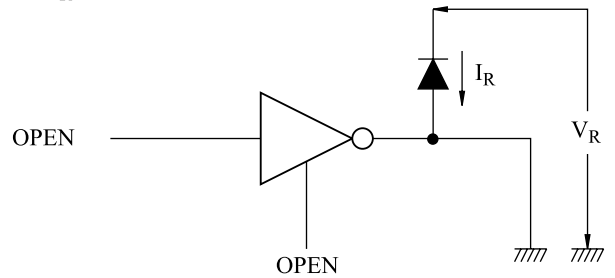
4.  $I_{IN(OFF)}$



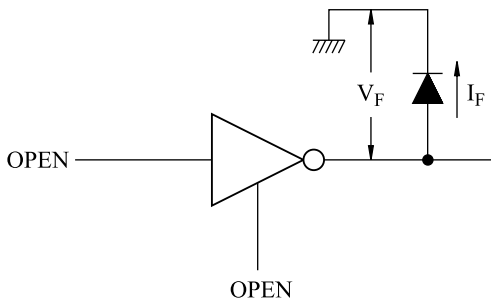
5.  $V_{IN(ON)}$



6.  $I_R$

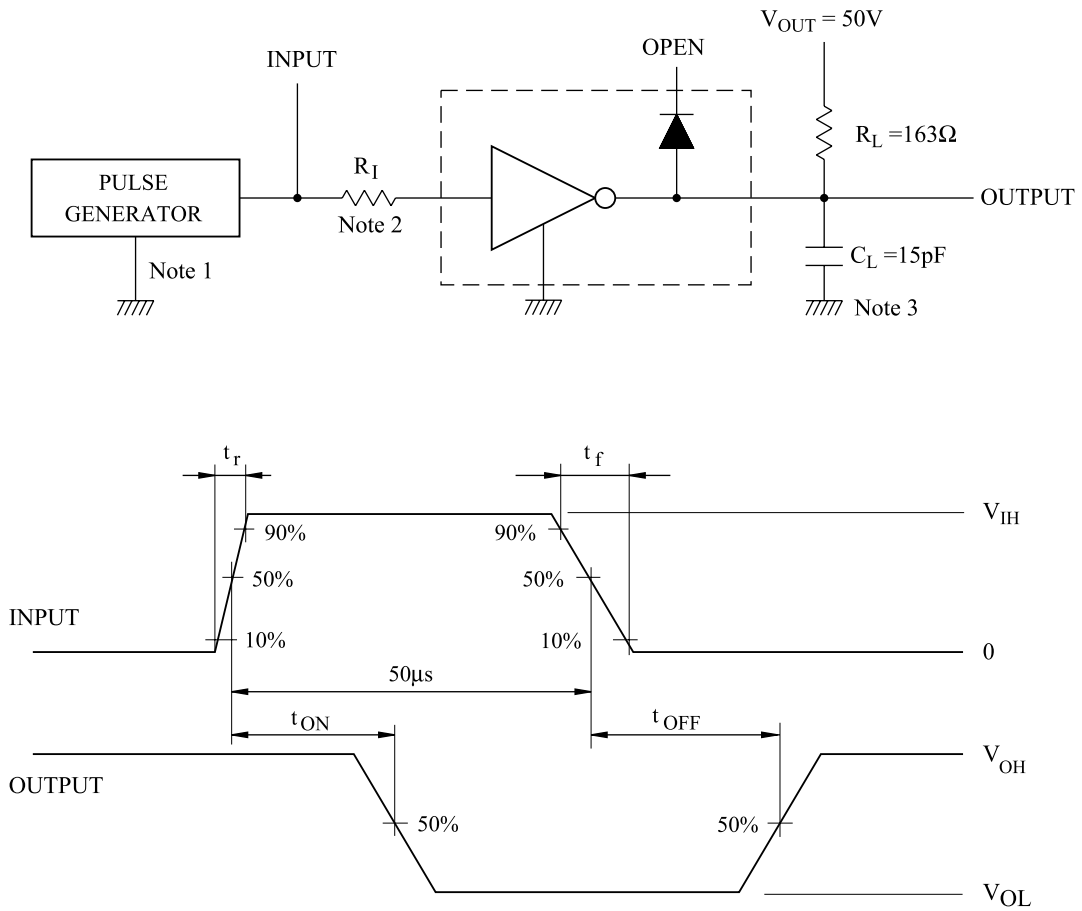


7.  $V_F$



# KID65001AP/AF~KID65004AP/AF

## 8. $t_{ON}$ , $t_{OFF}$



Notes : 1. Pulse Width 50  $\mu$ s, Duty Cycle 10%  
Output Impedance 50  $\Omega$ ,  $t_r$  5ns,  $t_f$  10ns

2. See below

### Input Conditions

Type Number	$R_I$	$V_{IH}$
KID65001AP/AF	2.7k	3V
KID65002AP/AF	0	13V
KID65003AP/AF	0	3V
KID65004AP/AF	0	8V

3.  $C_L$  includes probe and Jig capacitance.

# KID65001AP/AF~KID65004AP/AF

Fig. 1  $I_{OUT}$  - DUTY CYCLE

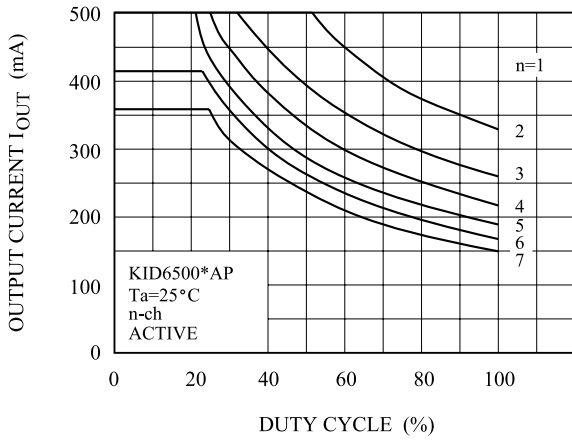


Fig. 2  $I_{OUT}$  - DUTY CYCLE

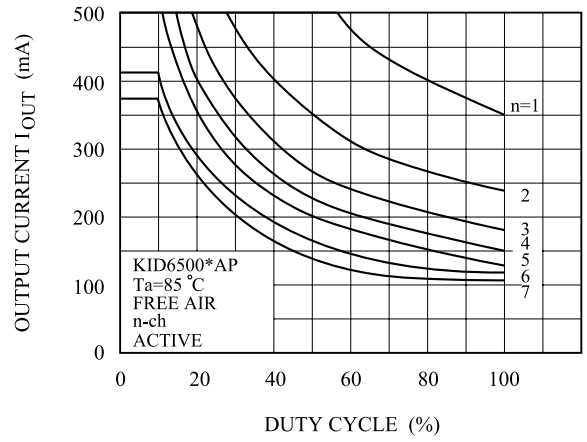


Fig. 3  $I_{OUT}$  - DUTY CYCLE

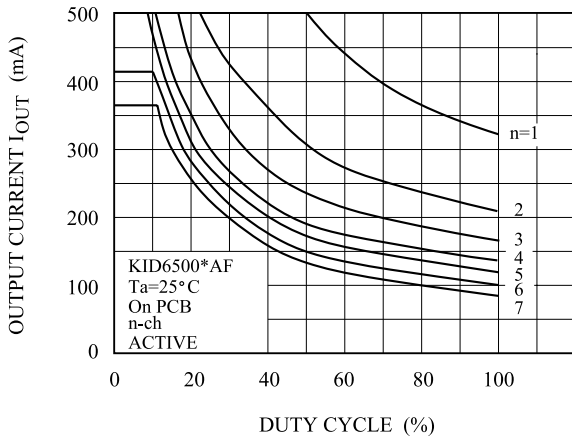


Fig. 4  $I_{OUT}$  - DUTY CYCLE

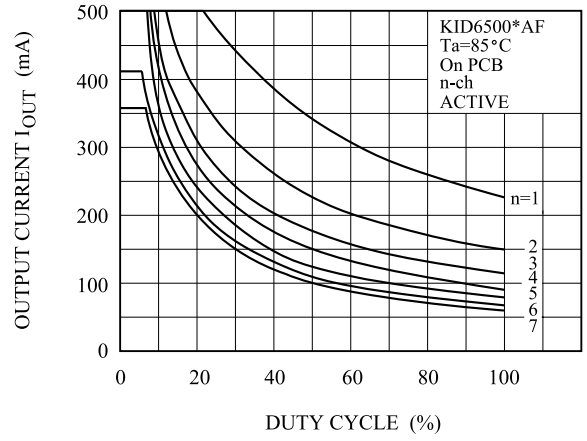


Fig. 5  $I_{IN}$  -  $V_{IN}$

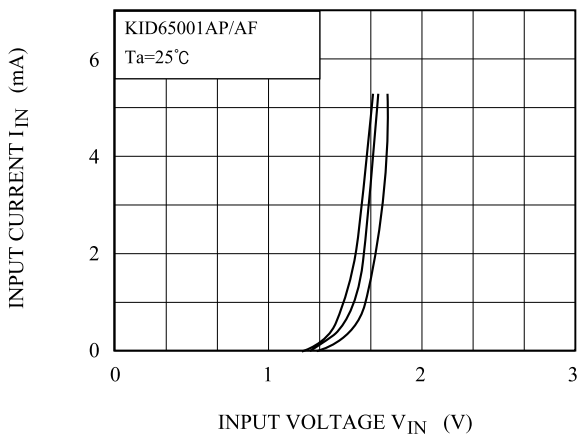
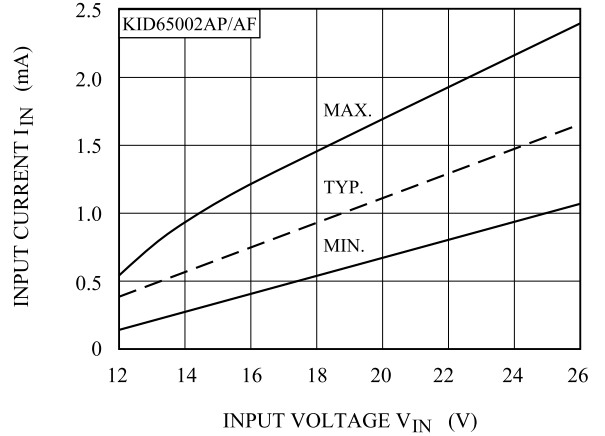


Fig. 6  $I_{IN}$  -  $V_{IN}$



# KID65001AP/AF~KID65004AP/AF

Fig. 7  $I_{IN} - V_{IN}$

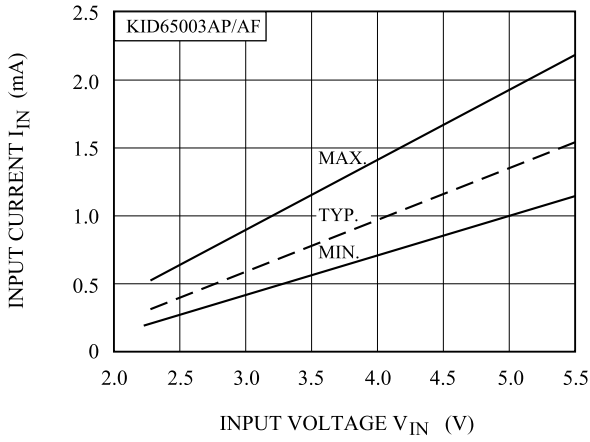


Fig. 8  $I_{IN} - V_{IN}$

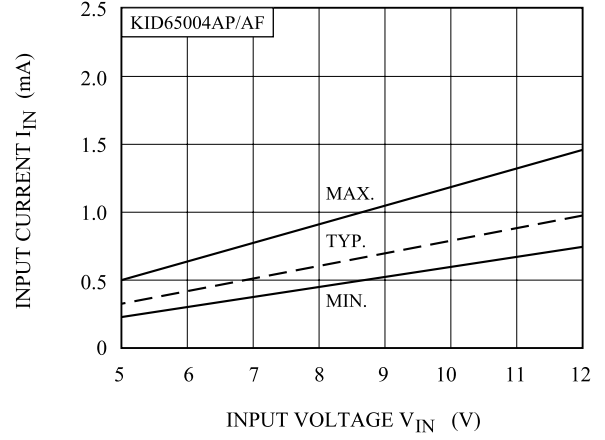


Fig. 9  $I_{OUT} - V_{CE(sat)}$

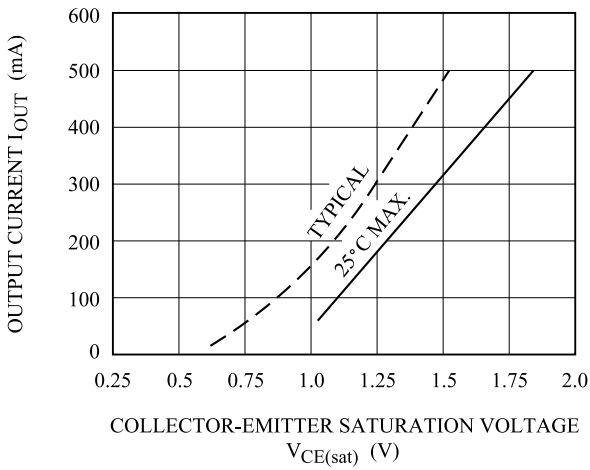


Fig. 10  $h_{FE} - I_{OUT}$

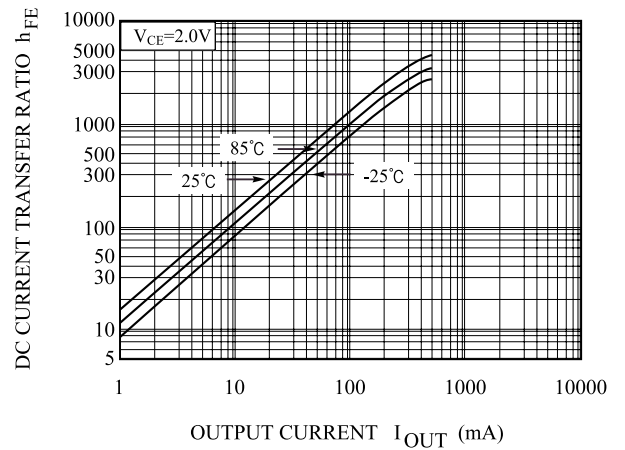


Fig. 11  $I_F - V_F$

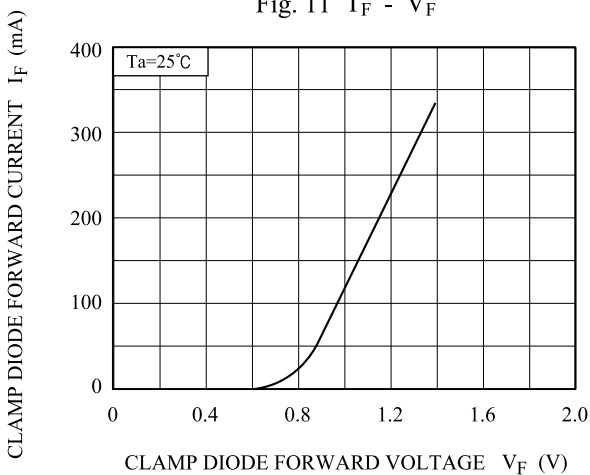


Fig. 12  $P_D - T_a$

