2ED2183 (4) S06F (J)

650 V half-bridge gate driver with integrated bootstrap diode

Features

- Unique Infineon Thin-Film-Silicon On Insulator (SOI)-Technology
- Negative VS transient immunity of 100 V
- Floating channel designed for bootstrap operation
- Operating voltages (VS node) upto + 650 V
- Maximum bootstrap voltage (VB node) of + 675 V
- Integrated ultra-fast, low resistance bootstrap diode
- Integrated shoot-through protection and built-in dead time
- Logic Operational up to –11 V on VS Pin
- Negative Voltage Tolerance On Inputs of –5 V
- Independent under voltage lockout for both channels
- Schmitt trigger inputs with hysteresis
- 3.3 V, 5 V and 15 V input logic compatible
- Maximum supply voltage of 25 V
- Dual package options of DSO-8 and DSO-14
- High and Low Voltage Pins Separated for Maximum Creepage and Clearance (2ED21834S06J version)
- Separate logic and power ground with the 2ED21834S06J version
- RoHS compliant

Product summary

V_{S_OFFSET} = 650 V max
I_{o+pk} / I_{o-pk} (typ.) =+ 2.5 A/ - 2.5 A
V_{CC} = 10 V to 20 V
Delay Matching = 35 ns max.
Propogation Delay = 200 ns
t_{ON} / t_{OFF} (typ.) = 200 ns/ 200 ns

Packages

DSO-8

DSO-14

Potential applications

Driving IGBTs, enhancement mode N-Channel MOSFETs in various power electronic applications.
Typical Infineon recommendations are as below:

- Motor drives, general purpose inverters having TRENCHSTOP™ IGBT6 or 600 V EasyPACK™ modules
- Refrigeration compressors, induction cookers, other major home appliances having RCD series IGBTs or TRENCHSTOP™ family IGBTs or their equivalent power stages
- Battery operated small home appliances such as power tools, vaccum cleaners using low voltage OptiMOS™ MOSFETs or their equivalent power stages
- Totem pole, half-bridge and full-bridge converters in offline AC-DC power supplies for industrial SMPS having high voltage CoolMOS™ super junction MOSFETs or TRENCHSTOP™ H3 and WR5 IGBT series
- High power LED and HID lighting having CoolMOS™ super junction MOSFETs
- Electric vehicle (EV) charging stations and battery management systems
- Driving 650 V SiC MOSFETs in above applications

Product validation

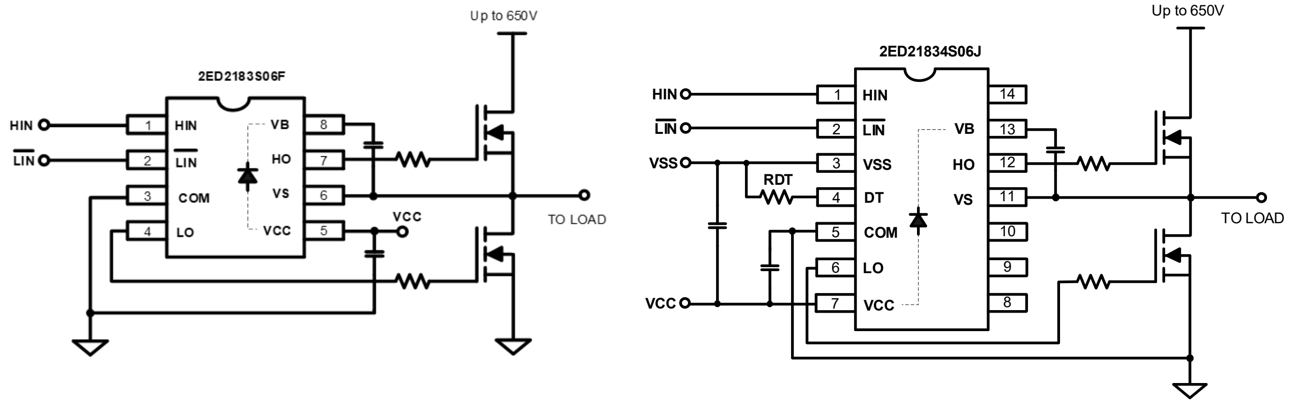
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
2ED2183S06F	DSO-8	Tape and Reel	2500	2ED2183S06FXUMA1
2ED21834S06J	DSO -14	Tape and Reel	2500	2ED21834S06JXUMA1

Description

The 2ED2183(4)S06F(J) is a half-bridge high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Based on Infineon's SOI-technology there is an excellent ruggedness and noise immunity with capability to maintain operational logic at negative voltages of up to - 11 V_{DC} on VS pin (V_{CC} = 15 V) on transient voltages. There are not any parasitic thyristor structures present in the device, hence no parasitic latch up may occur at all temperature and voltage conditions. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET, SiC MOSFET or IGBT in the high side configuration, which operate up to 650 V.



*Bootstrap diode is monolithically integrated

This diagram shows electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 **Typical application block diagram**

Summary of feature comparison of the 2ED218x family:

Table 1

Part No.	Package	Drive Current Source / Sink	Input logic	Cross conduction prevention logic	Deadtime	Ground pins	t_{ON} / t_{OFF}
2ED2181S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, LIN	No	None	COM	200 ns / 200 ns
2ED21814S06J	DSO – 14	+ 2.5 A / - 2.5 A				VSS / COM	
2ED2182S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, LIN	Yes	Internal 400 ns	COM	
2ED21824S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	
2ED2183S06F	DSO – 8	+ 2.5 A / - 2.5 A	HIN, $\overline{LIN}$	Yes	Internal 400 ns	COM	
2ED21834S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	
2ED2184S06F	DSO – 8	+ 2.5 A / - 2.5 A	IN, $\overline{SD}$	Yes	Internal 400 ns	COM	600 ns / 200 ns
2ED21844S06J	DSO – 14	+ 2.5 A / - 2.5 A			Programmable 400 ns - 5000 ns	VSS / COM	

1 Table of contents

2 Block diagram

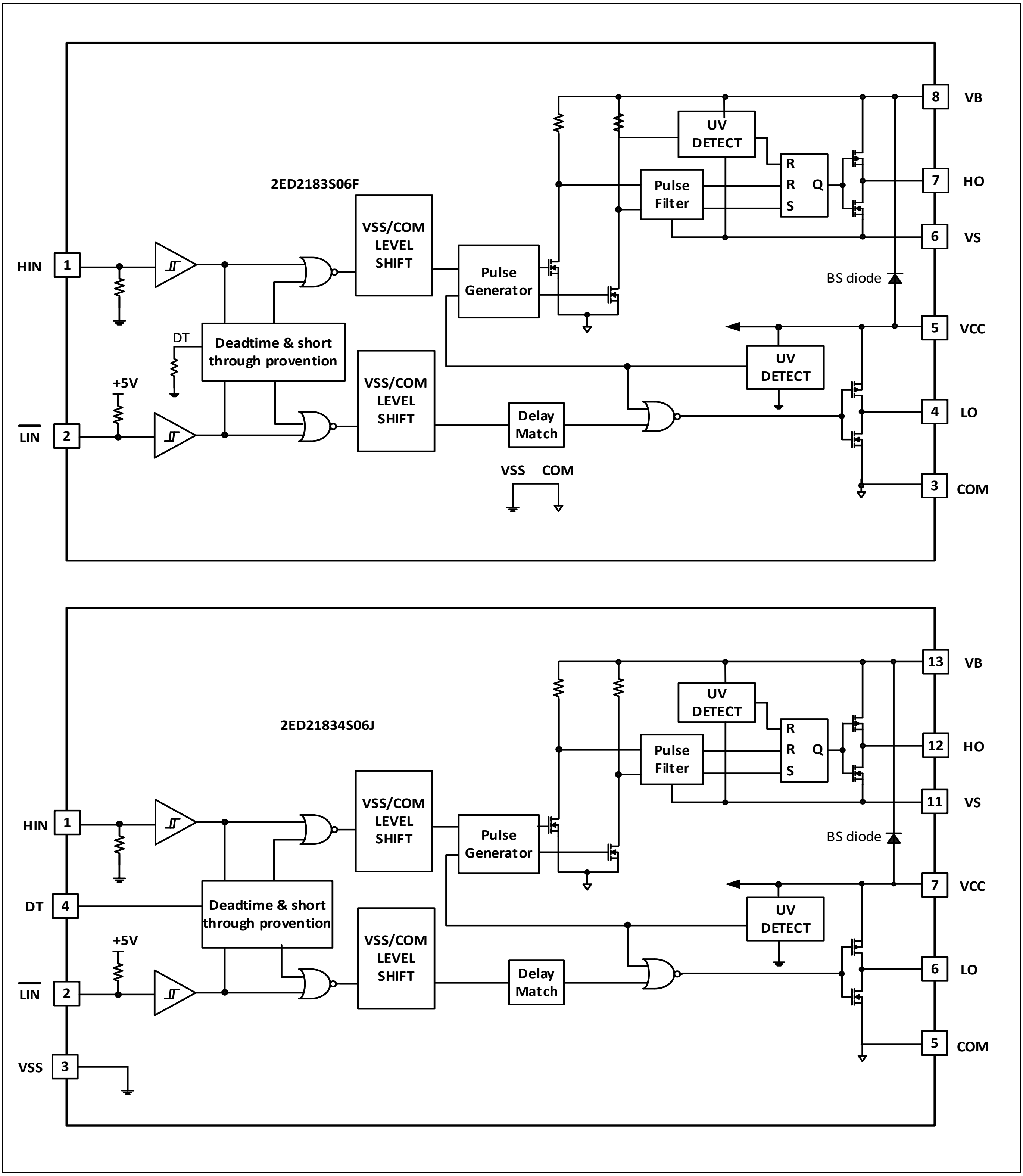


Figure 2 Block diagrams

3 Pin configuration and functionality

3.1 Pin configuration

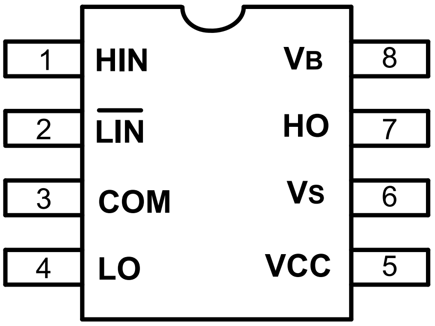
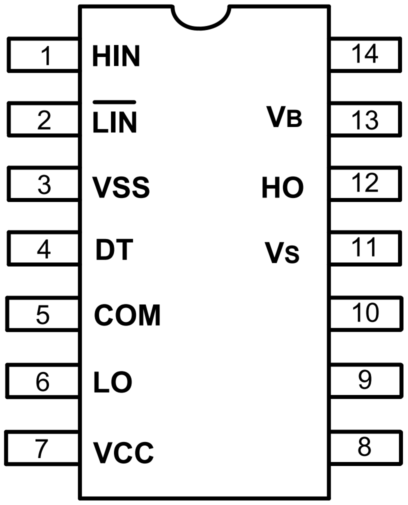
	
8-Lead DSO-8 (150 mil)	14-Lead DSO-14 (150 mil)
2ED2183S06F	2ED21834S06J

Figure 3 2ED2183(4)S06F(J) pin assignments (top view)

3.2 Pin functionality

Table 2

Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase with HO
$\overline{\text{LIN}}$	Logic inputs for low- side gate driver output (LO),out of phase with LO
VSS	Logic ground (2ED21834S06J only)
DT	Programmable dead-time, referenced to VSS.(2ED21834S06J only)
COM	Low-side gate drive return
LO	Low-side driver output
VCC	Low-side and logic supply voltage
VS	High voltage floating supply return
HO	High-side driver output
VB	High-side gate drive floating supply

4 Electrical parameters

4.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 3 Absolute maximum ratings

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating well supply voltage (Note 1)		$V_{CC} – 5$	675	V
V_S	High-side floating well supply return voltage		$V_{CC} – V_{BS} – 5$	650	
V_{HO}	Floating gate drive output voltage		$V_S – 0.5$	$V_B + 0.5$	
V_{CC}	Low side supply voltage		-1	25	
V_{LO}	Low-side output voltage		–0.5	$V_{CC} + 0.5$	
V_{IN}	Logic input voltage (HIN & LIN)		-5/ ($V_{SS} – 5$)	$V_{CC} + 0.5$	
Vss	Logic ground (2ED21834S06J only)		$V_{CC} – 25$	$V_{CC} + 0.5$	
DT	Programmable dead time pin voltage (2ED21834S06J only)		$V_{SS} – 5$	$V_{CC} + 0.5$	
dV_S/dt	Allowable V_S offset supply transient relative to COM		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$°C	8-Lead DSO-8	—	0.625	W
		14-Lead DSO-14	—	1	
Rth_{JA}	Thermal resistance, junction to ambient	8-Lead DSO-8	—	200	°C/W
		14-Lead DSO-14	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B in case of activated bootstrap diode.

4.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} – COM) = ($V_B – V_S$) = 15 V.

Table 4 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_B	Bootstrap voltage	$V_S + 10$	$V_S + 20$	V
V_{BS}	High-side floating well supply voltage	10	20	
V_S	High-side floating well supply offset voltage	Note 2	650	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{CC}	Low-side supply voltage	10	20	
V_{LO}	Low-side output voltage	COM	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	-4 / ($V_{SS} – 4$)	5 / ($V_{SS} + 5$)	
V_{SS}	Logic ground (2ED21834S06J only) with respect to COM	-5	+5	
DT	Programmable dead time pin voltage (2ED21834S06J only)	$V_{SS} – 4$	5	
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operation for V_S of – 10 V to +650 V. Logic state held for V_S of -10 to $–V_{BS}$.

4.3 Static electrical characteristics

(V_{CC}– COM) = (V_B – V_S) = 15 V, V_{SS} = COM and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to Vss / COM and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to V_S / COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 5 **Static electrical characteristics**

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.6	8.2	8.9	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	6.7	7.2	8.1		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis		1.0	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.4	9.1	9.8		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.5	8.2	8.9		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis		0.9	—		
I_{LK}	High-side floating well offset supply leakage	—	1	12.5	uA	V_B = V_S = 650 V
I_{QBS}	Quiescent V_{BS} supply current	—	170	—		All inputs are in the off state
I_{QCC}	Quiescent V_{CC} supply current	—	550	—		
V_{OH}	High level output voltage drop, V_{cc}- V_{LO}, V_B- V_{HO}	—	0.05	0.2	V	I_O = 20 mA
V_{OL}	Low level output voltage drop, V_O	—	0.02	0.1		
I_{o+mean}	Mean output current from 3 V to 6 V	1.65	2.2		A	C_L = 22 nF
I_{o+}	Peak output current turn-on[1]		2.5	—		V_O = 0 V PW ≤ 10 µs
I_{o-mean}	Mean output current from 12 V to 9 V	1.65	2.2			C_L = 22 nF
I_{o-}	Peak output current turn-off[1]		2.5			V_O = 15 V PW ≤ 10 µs
V_{IH}	Logic “1” input voltage	1.7	2.1	2.4	V	Vcc=10 V to 20 V
V_{IL}	Logic “0” input voltage	0.7	0.9	1.1		
I_{IN+}	Input bias current (Output = High)	—	25	50	µA	V_{IN} = 5 V
I_{IN-}	Input bias current (Output = Low)	—	—	10		V_{IN} = 0 V
V_{FBSD}	Bootstrap diode forward voltage between Vcc and VB	—	1	1.2	V	I_F=0.3 mA
I_{FBSD}	Bootstrap diode forward current between Vcc and VB	55	100	145	mA	V_{CC}-V_B=4 V
R_{BSD}	Bootstrap diode resistance	15	25	40	Ω	V_{F1}=4V,V_{F2}=5 V
V_S	Allowable Negative VS pin voltage for IN Signal propagation to HO	—	-11	-10	V	Vcc=15 V

[1] Not subjected to production test, verified by characterization.

4.4 Dynamic electrical characteristics

$V_{CC} = V_{BS} = 15$ V, V_{SS} = COM, $T_A = 25$ °C and $C_L = 1000$ pF unless otherwise specified.

Table 6 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	200	300	ns	$V_S = 0$ V or 650 V
t_{OFF}	Turn-off propagation delay	—	200	300		
t_R	Turn-on rise time	—	15	30		$V_S = 0$ V
t_F	Turn-off fall time	—	15	30		
MT	Delay matching time (HS & LS turn-on/off)	—	—	35		
DT	Deadtime: LO Turn-off to HO Turn-on & HO Turn-off to LO turn-on	260	400	540		RDT=0 Ω
		4	5	6	us	RDT=200 kΩ
MDT	Deadtime matching= I $DT_{LO\text{-}HO} - DT_{HO\text{-}LO}$ I			60	ns	RDT=0 Ω
				600		RDT=200 kΩ

5 Application information and additional details

5.1 IGBT / MOSFET gate drive

The 2ED2183 (4) S06F (J) HVIC is designed to drive MOSFET or IGBT power devices. Figures 4 and 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as IO. The voltage that drives the gate of the external power switch is defined as VHO for the high-side power switch and VLO for the low-side power switch; this parameter is sometimes generically called VOUT and in this case does not differentiate between the high-side or low-side output voltage.

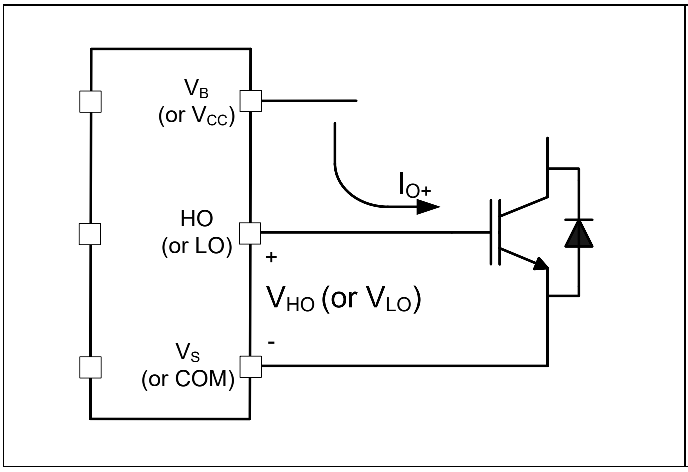


Figure 4 **HVIC Sourcing current**

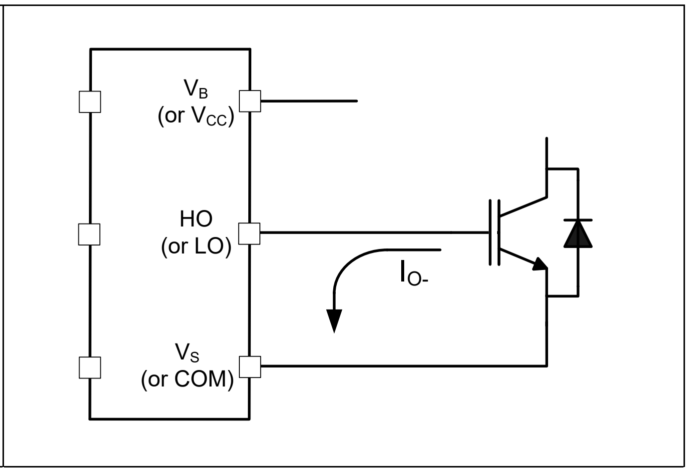


Figure 5 **HVIC Sinking current**

5.2 Switching and timing relationships

The relationships between the input and output signals of the 2ED2183 (4) S06F (J) are illustrated below in Figure 6 and Figure 7. From these figures, we can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

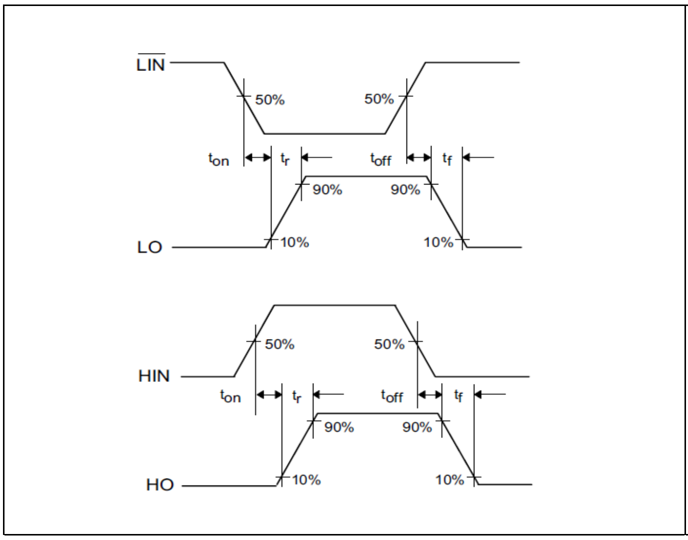


Figure 6 **Switching timing diagram**

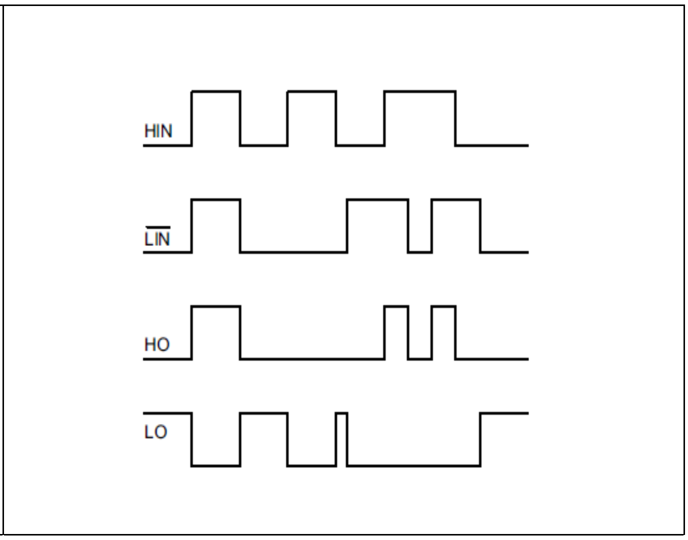


Figure 7 **Input/output logic diagram**

5.3 Deadtime and matched propagation delays

This 2ED2183 (4) S06F (J) features integrated deadtime protection circuitry. The deadtime is fixed for 2ED2183S06F; is programmable for 2ED2183S06J, it provides greater design flexibility. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 8 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of 2ED2183 (4) S06F (J) is matched with respect to the high- and low-side outputs. Figure 9 defines the two deadtime parameters (i.e., DTLO-HO and DTHO-LO); the deadtime matching parameter (MDT) associated with the 2ED2183S06F (J) specifies the maximum difference between DTLO-HO and DTHO-LO.

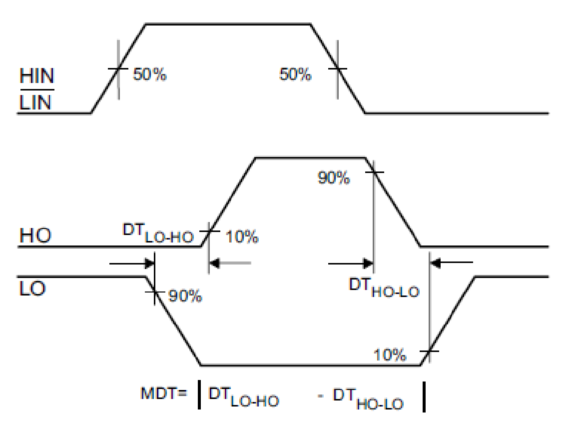


Figure 8 Dead Time Definitions

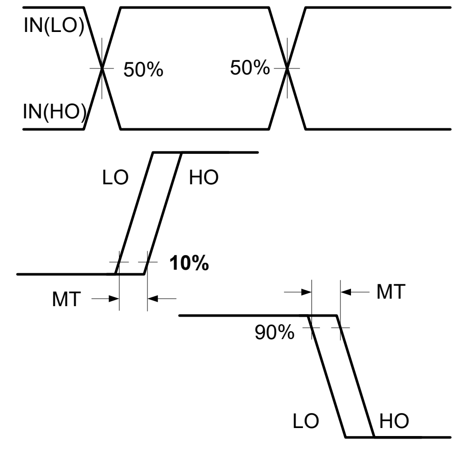


Figure 9 Delay Matching Waveform Definitions

The 2ED2183 (4) S06F (J) is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 2ED2183 (4) S06F (J) is matched to the propagation turn-on delay (t_{OFF}).

The 14-pin variant (2ED21834S06J) provides greater design flexibility with a programmable dead-time feature using an external resistor (RDT) connected between the DT pin and VSS pin as shown in figure 10.

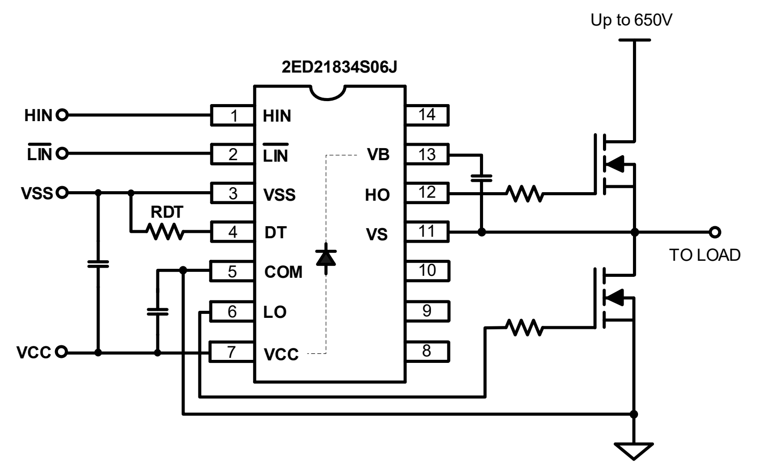


Figure 10 14-pin half-bridge variants having adjustable dead-time feature settable with a resistor

Figure 11 shows the linear relationship between the resistor (RDT) and dead time. Based on the end application, designers can choose to add the external resistor to increase the dead time. In case the DT pin is left open, the gate driver enters protection mode switching off the output stages. Hence this pin has to be connected to VSS pin with a 0 ohm to 200 k resistor based on application requirements. A 0 ohm (or shorted) provides a minimum deadtime of 400 ns and 200 k ohm provides a maximum deadtime of 5 us.

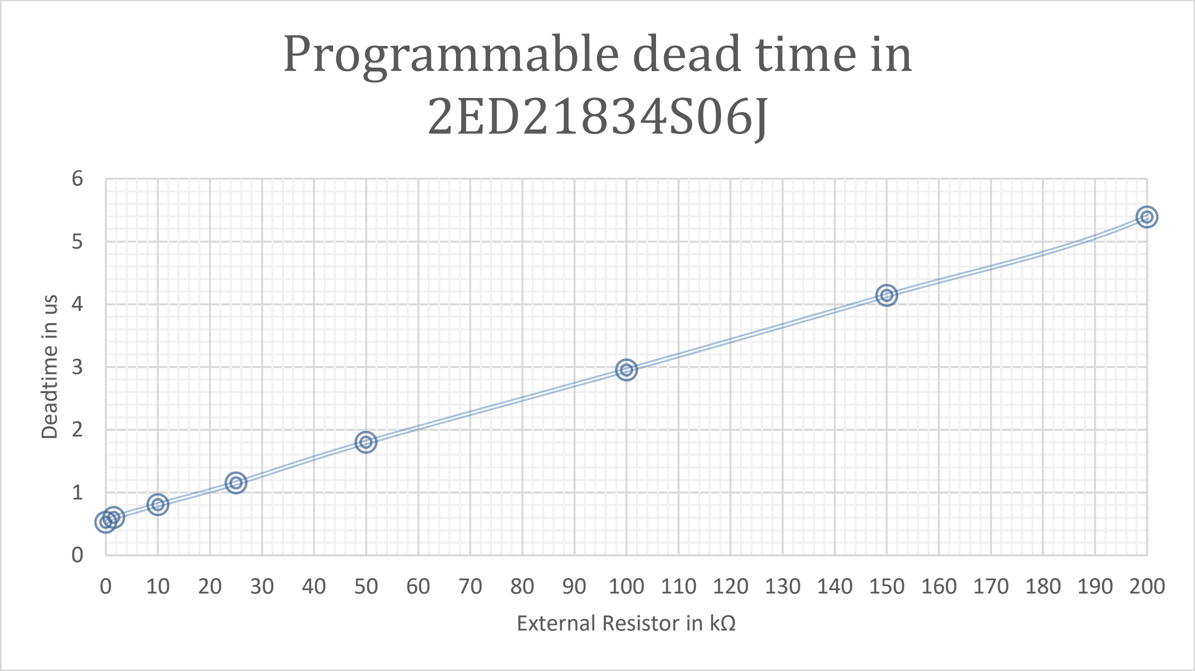


Figure 11 Variation of dead time vs. external resistor

5.4 Input logic compatibility

The input pins of are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. With typical high threshold (V_{IH}) of 2.1 V and typical low threshold (V_{IL}) of 0.9 V, along with very little temperature variation as summarized in Figure 12, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.9 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 2ED218x family also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 2ED218x features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 2ED218x family has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

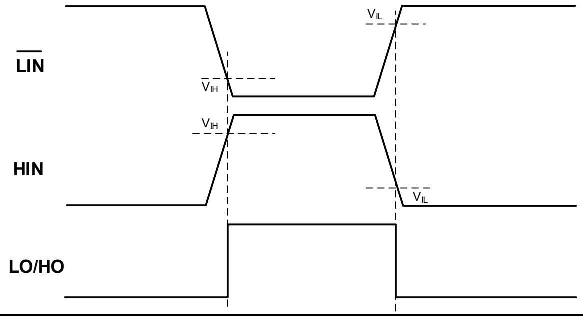


Figure 12 HIN & LIN input thresholds

5.5 Undervoltage lockout

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 13 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CCUV+/-}$ or $V_{BSUV+/-)}$ the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{CC} voltage fail to reach the V_{CCUV+} threshold, the IC won't turn-on. Additionally, if the V_{CC} voltage decreases below the V_{CCUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.

Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the V_{BSUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

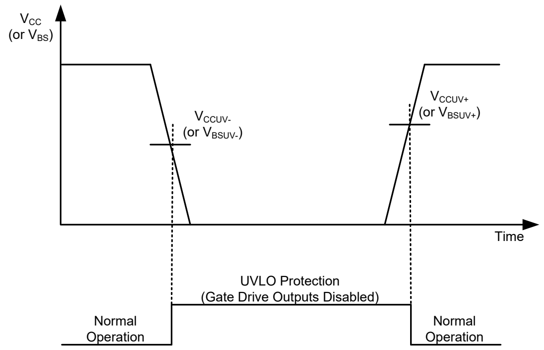


Figure 13 UVLO protection

5.6 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its resistance helps save cost and improve reliability by reducing external components as shown below figures 14 and 15.

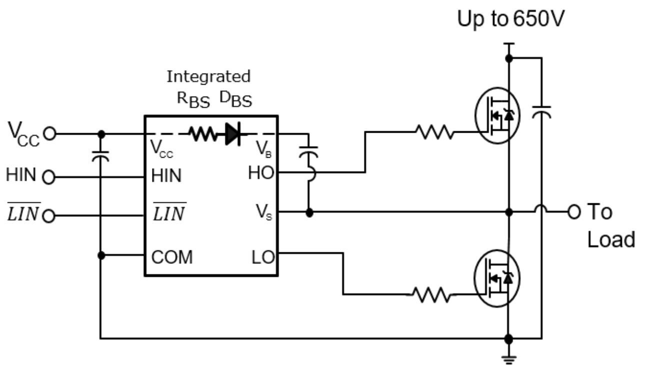


Figure 14 2ED218x with integrated components

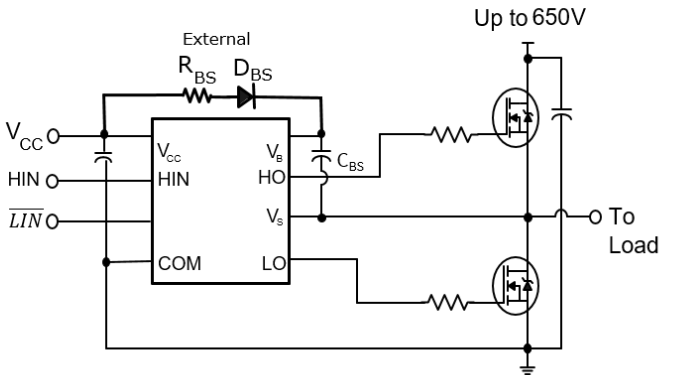


Figure 15 Standard bootstrap gate driver

The low ohmic current limiting resistor provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 2ED218x family allows faster recharching of the bootstrap capacitor during periods of small duty cycles on the low side transistor. Such points of operation occur e.g. during low speed operation of drives at high torque, which can be excellently controlled with field oriented control of induction, permanent magnet synchronous or BLDC motors. There is usually no complete recharging possible any more during small duty cycles, so that the bootstrap voltage at the bootstrap capacitor CBS sinks. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real pn-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 2ED218x family works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal drives control.

5.7 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 16.

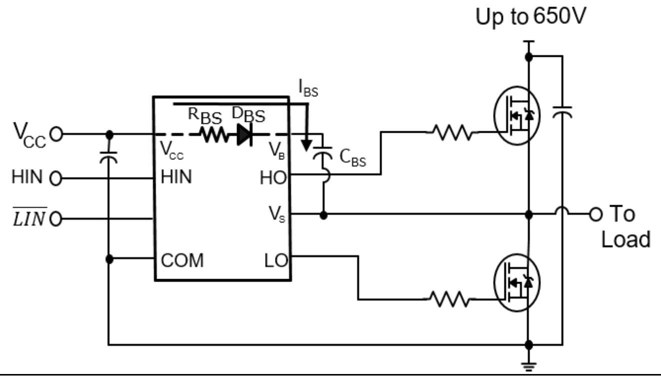


Figure 16 Half bridge bootstrap circuit in 2ED218x

When the low side MOSFET turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and V_{CC} results in a charging current I_{BS} into the capacitor C_{BS}. The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and V_{CC}. The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section.

The current limiting resistor R_{BS} according to Figure 16 reduces the peak of the pulse current during the low side MOSFET turn-on. The pulse current will occur at each turn-on of the low side MOSFET, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The high side quiescent current and the gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (V_{CC} - V_F - V_{GSmin} - V_{DSon})$$

$V_{GSmin} > V_{BSUV-}$, V_{GSmin} is the minimum gate source voltage we want to maintain and V_{BSUV-} is the high-side supply undervoltage negative threshold.

V_{CC} is the IC voltage supply, V_F is bootstrapdiode forward voltage and V_{DSon} is drain-source voltage of low side MOSFET.

Please note, that the value Q_{GTOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- MOSFET turn on required Gate charge (Q_G)
- MOSFET gate-source leakage current (I_{LK_GS})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Charge required by the internal level shifters (Q_{LS}): typical 1nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LK_{GS}} + I_{LK} + I_{LK_{DIODE}} + I_{LK_{CAP}}\right) * T_{HON}$$

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

5.8 Tolerant to negative tranisents on input pins

Typically the driver's ground pin is connected close to the source pin of the MOSFET or IGBT. The microcontroller which sends the HIN and LIN PWM signals refers to the same ground and in most cases there will be an offset voltage between the microcontroller ground pin and driver ground because of ground bounce. The 2ED218x family can handle negative voltage spikes up to 5 V. The recommended operating level is at negative 4 V with absolute maximum of negative 5 V. Standard half bridge or high-side/low-side drivers only allow negative voltage levels down to -0.3 V. The 2ED218x family has much better noise immunity capability on the input pins.

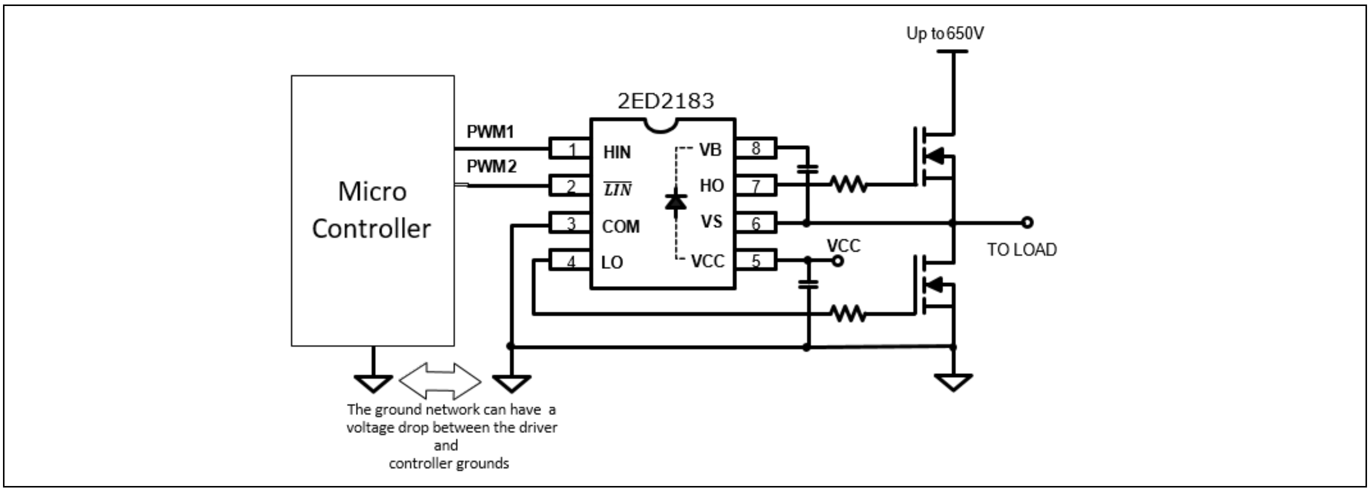


Figure 17 Negative voltage tolerance on inputs of upto –5 V

5.9 Negative voltage transient tolerance of VS pin

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 18, here we define the power switches and diodes of the inverter.
If the high-side switch (e.g., the IGBT Q1 in Figures 19 and 20) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

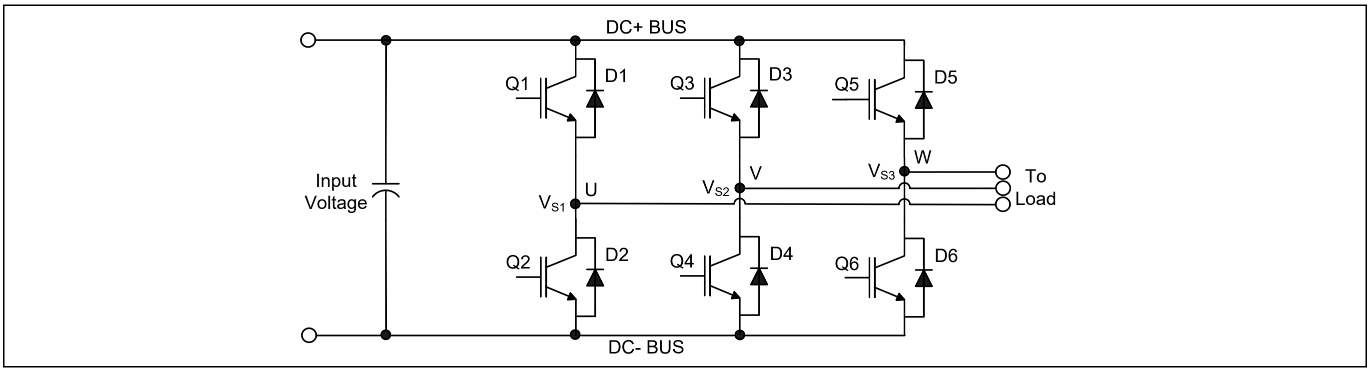


Figure 18 Three phase inverter

Also when the V phase current flows from the inductive load back to the inverter (see Figures 19 C) and D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called "negative V_S transient"

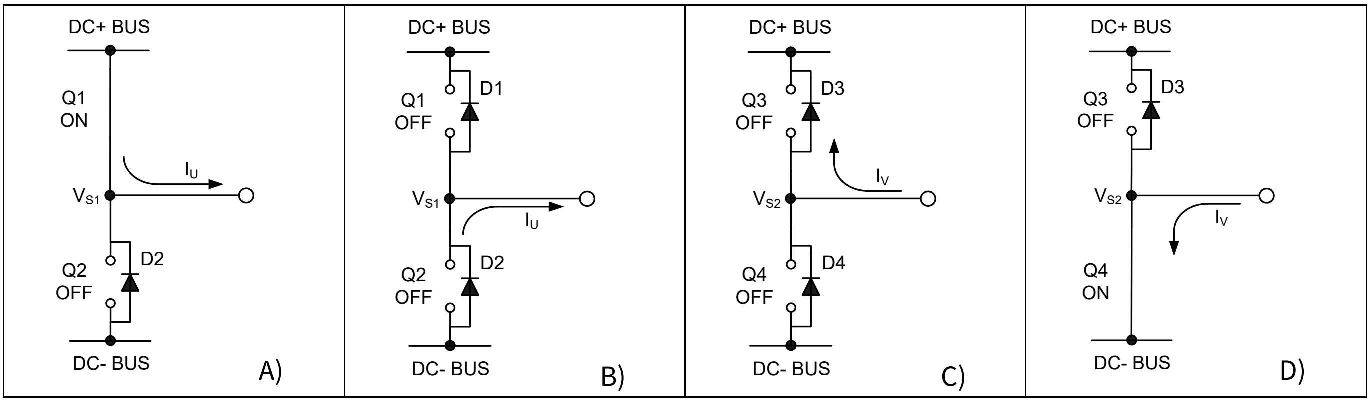


Figure 19 **A) Q1 conducting B) D2 conducting C) D3 conducting D) Q4 conducting**

The circuit shown in Figure 20-A depicts one leg of the three phase inverter; Figures 20-B and 20-C show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

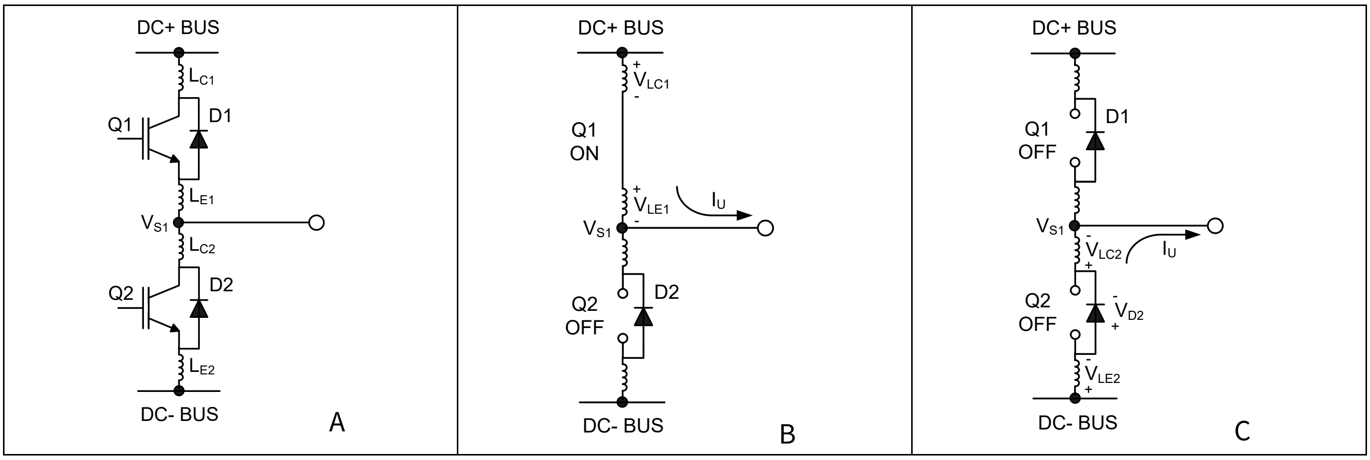


Figure 20 **Figure A shows the Parasitic Elements. Figure B shows the generation of V_S positive. Figure C shows the generation of V_S negative**

5.10 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3 – 5 V / ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 2ED2183's robustness can be seen in Figure 21, where the 2ED2183's Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative VS spikes. A negative VS transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

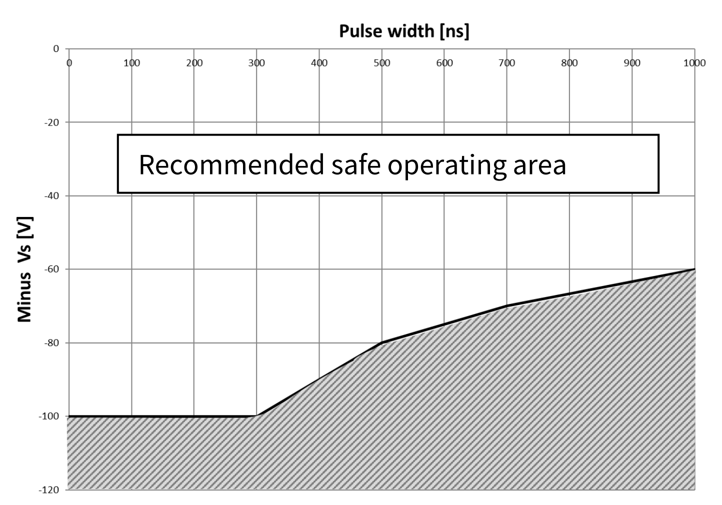


Figure 21 **Negative VS transient SOA for 2ED2183(4)S06F(J) @ VBS=15 V**

Even though the 2ED2183S06F(J) has been shown able to handle these large negative VS transient conditions, it is highly recommended that the circuit designer always limit the negative VS transients as much as possible by careful PCB layout and component use.

5.11 Higher headroom for input to output signal transmission with logic operation upto -11 V

If there is not enough voltage for the level shifter to transmit a valid signal to the high side.High side driver doesn't turn on. The level shifter circuit is with respect to COM (refer to Block Diagram on page 4), the voltage from V_B to COM is the supply voltage of level shifter. Under the condition of VS is negative voltage with respect to COM, the voltage of VS - COM is decreased, as shown in Figure 22. There is a minimum operational supply voltage of level shifter, if the supply voltage of level shifter is too low, the level shifter cannot pass through HIN signal to HO. The specification of VS is –11 V as the internal structure allows a maximum voltage difference of 20 V between VB and VS pins. If $V_B - V_S$ voltage is different, the minimum VS voltage changes accordingly.

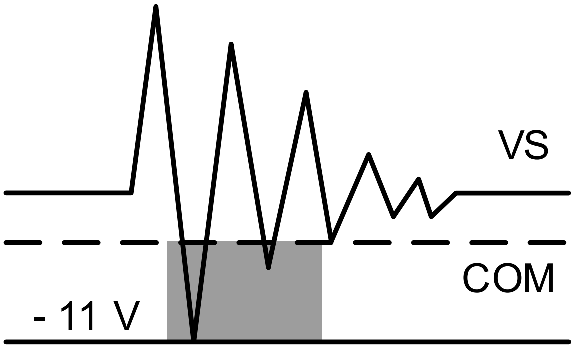


Figure 22 **Headroom for HV level shifter data transmission**

5.12 Maximum switching frequency

The 2ED218x family is capable of switching at higher frequencies as compared to standard half-bridge or high side / low side gate drivers. They are available in two packages, the PG-DSO-8 and the PG-DSO-14. It is essential to ensure that the component is not thermally overloaded when operating at higher frequencies. This can be checked by means of the thermal resistance junction to ambient and the calculation or measurement of the dissipated power. The thermal resistance is given in the datasheet (section 4) and refers to a specific layout.

Changes of this layout may lead to an increased thermal resistance, which will reduce the total dissipated power of the driver IC. One should therefore do temperature measurements in order to avoid thermal overload under application relevant conditions of ambient temperature and housing.

The maximum chip temperature T_J can be calculated with

$$T_J = \mathrm{Pd} \cdot Rth_{JA} + T_{A\_max}$$, where T_{A_max} is the maximum ambient temperature.

The dissipated power Pd by the driver IC is a combination of several sources. These are explained in detail in the application note “2ED2183 (4) S06F (J) (HVICs)”

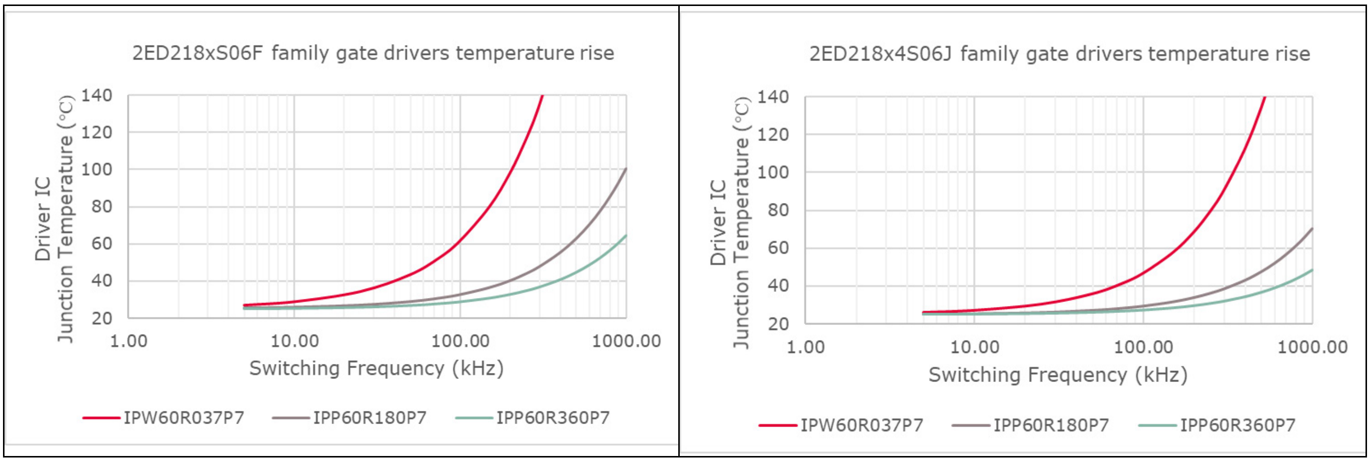
The output section is the major contributor for the power dissipation of the gate driver IC. The external gate resistors also contribute to the power disspation of the gate driver IC. The bigger the external gate resistor, the smaller the power dissipation in the gate driver.

The losses of the output section are calculated by means of the total gate charge of the power MOSFET or IGBT it is driving Q_{gtot}, the supply voltage V_{CC}, the switching frequency f_P, and the ext. gate resistor R_{gon} and R_{goff}. Different cases for turn-on and turn-off must be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses in respect to the external gate resistor R_{gxx}, ext and the internal resistances (R_{on_int} and R_{off_int}) of the output section.

Turn on losses: $Pdon = \frac{2}{2} \times Q_{gtot} \times V_{cc} \times f_p \times \frac{Ron\_int}{Ron\_int+Rgon\_ext}$

Turn off losses: $Pdoff = \frac{2}{2} \times Q_{gtot} \times V_{cc} \times f_p \times \frac{Roff\_int}{Roff\_int+Rgoff\_ext}$

The above two losses are then added to the remaining static losses within the gate driver IC and we arrive at the below figure which estimates the gate driver IC temperature rise when switching a given MOSFET or IGBT at different switching frequencies.



*Assumptions for above curves: T_a = 25 °C, V_{BUS} = 400 V, V_{CC} = 12 V, R_{gon} = 10 Ω, R_{goff} = 5Ω

Figure 23 Estimated temperature rise in the 2ED218x family gate drivers for different switching frequencies when switching CoolMOS^{TM} SJ MOSFETs

5.13 PCB layout tips

Distance between high and low voltage components: It’s strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.
Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 24). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

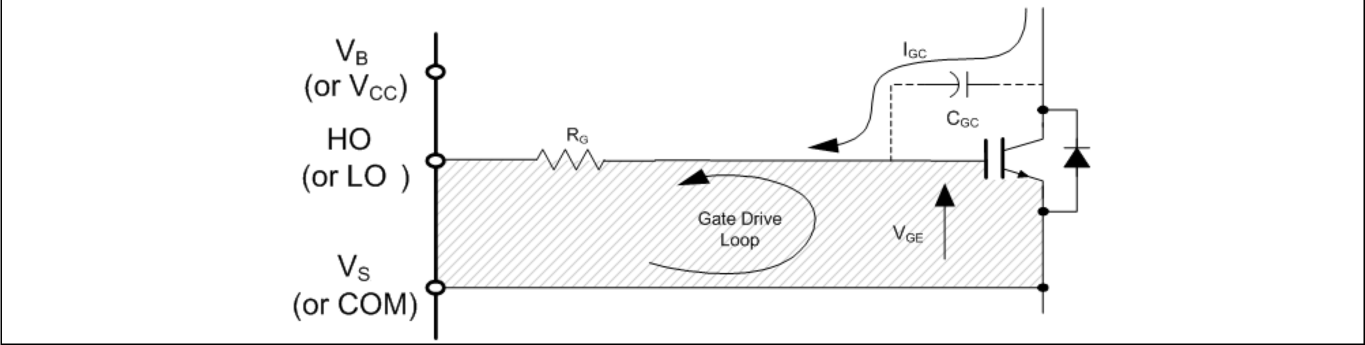


Figure 24 **Avoid antenna loops**

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the V_{CC} and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 25), and in some cases using a clamping diode between COM and V_S (see Figure 26). See DT04-4 at www.infineon.com for more detailed explanations.

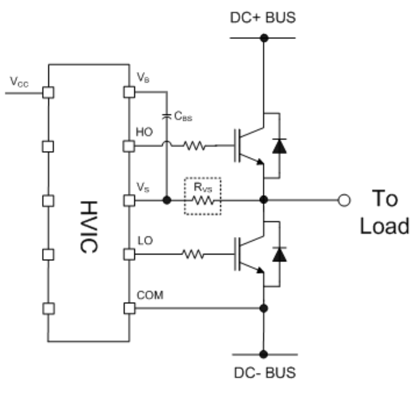


Figure 25 **Resistor between the VS pin and the switch node**

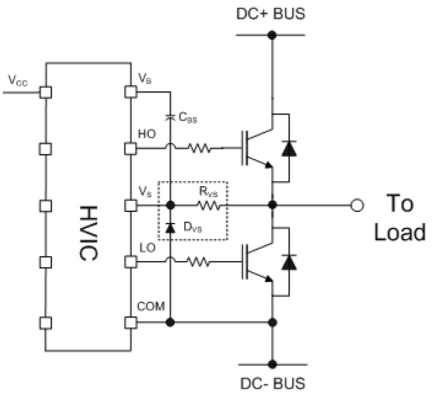


Figure 26 **Clamping diode between COM and V_S**

6 Qualification information[1]

Table 7 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		DSO-8	MSL2, 260°C (per IPC/JEDEC J-STD-020)
		DSO-14	MSL3[3], 260°C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (1.0 kV) (per JEDEC standard JS-002)	
	Human body model	Class 2 (2 kV) (per JEDEC standard JS-001)	
IC latch-up test		Class II Level A (per JESD85)	
RoHS compliant		Yes	

7 Related products

Table 8

Product	Description
Gate Driver ICs	
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, Fault reporting, and Enable for MOSFET or IGBT switches.
2EDL23I06 / 2EDL23N06	600 V, Half-bridge thin-film SOI level shift gate driver with integrated high speed, low *R*DSON bootstrap diode, with over-current protection (OCP), 2.3/2.8 A source/sink current driver, and one pin Enable/Fault function for MOSFET or IGBT switches.
Power Switches	
IKD04N60R / RF	600 V TRENCHSTOP™ IGBT with integrated diode in PG-TO252-3 package
IKD06N65ET6	650 V TRENCHSTOP™ IGBT with integrated diode in DPAK
IPD65R950CFD	650 V CoolMOS CFD2 with integrated fast body diode in DPAK
IPN50R950CE	500 V CoolMOS CE Superjunction MOSFET in PG-SOT223 package
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

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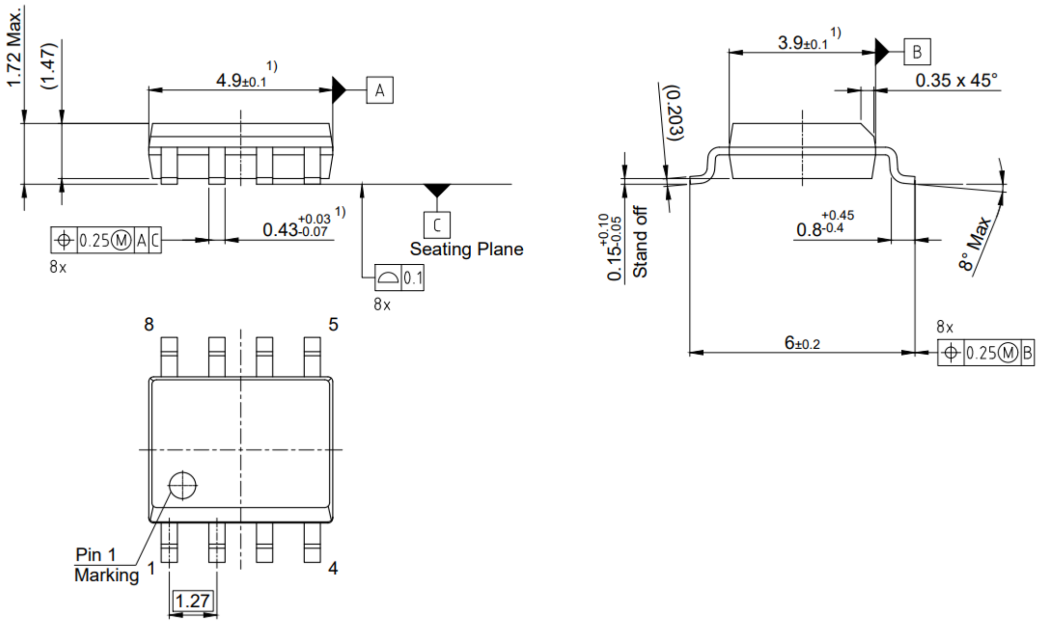
[1] Qualification standards can be found at Infineon's web site www.infineon.com

[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

[3] DSO-14 package with MSL2 rating is available if required. Please contact your Infineon sales representative for further information.

8 Package details

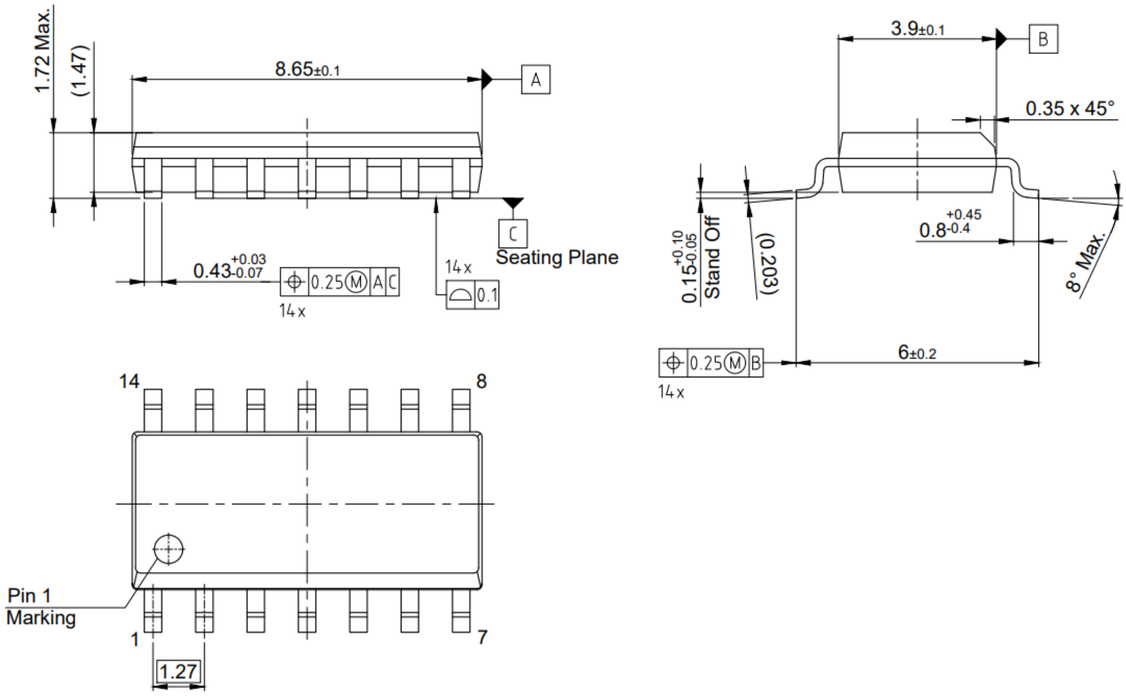


1) Does not include plastic or metal protrusion of 0.25 Max. per side

All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [◁⊕]

Figure 27 8 - Lead DSO (2ED2183S06F)



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [◁⊕]

Figure 28 14- Lead DSO (2ED21834S06J)

9 Part marking information

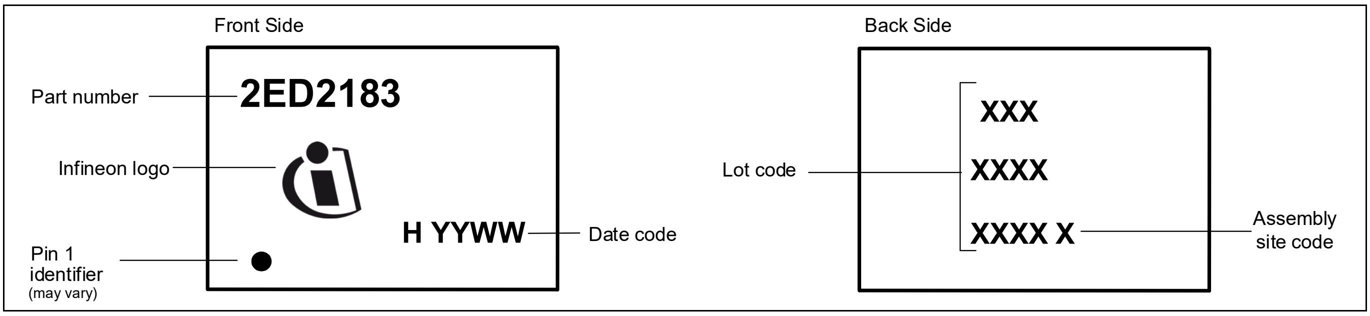


Figure 29 Marking information PG-DSO-8

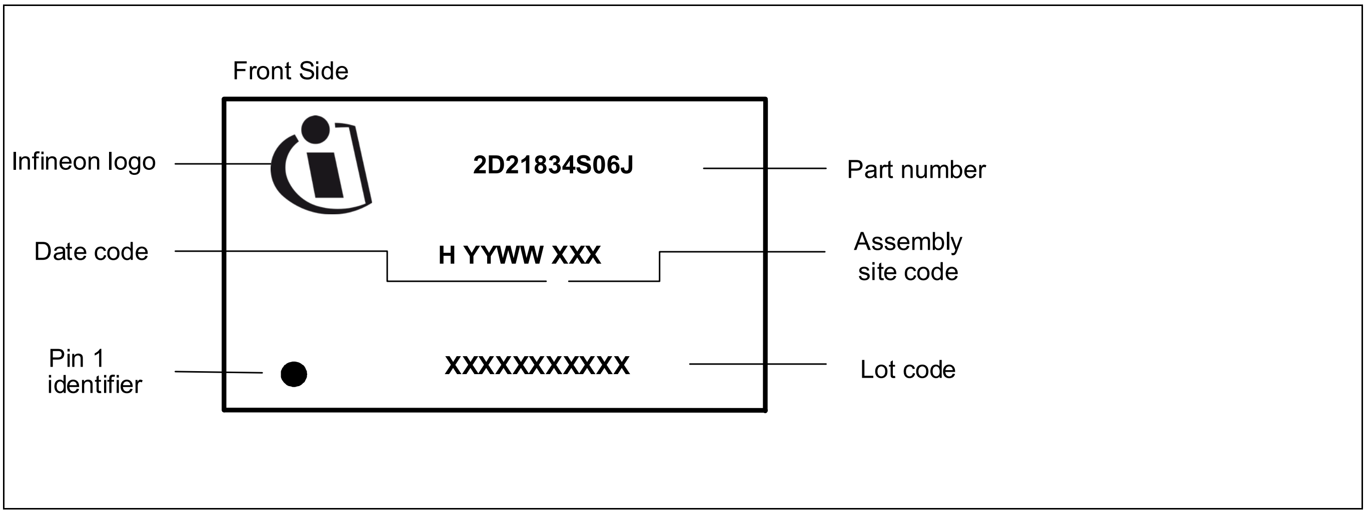


Figure 30 Marking information PG-DSO-14

10 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

10.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

11 Revision history

Document version	Date of release	Description of changes
2.00	July 29, 2019	Final Datasheet
2.10	September 12, 2019	Revised parameter values in Tables 5 & 7 to match the test conditions. Updated figure 1 to include 14 pin variant typical connection diagram.
2.20	January 14, 2020	Revised parameter values in Table 7 to match the test conditions. Added deadtime settings section in page 10-11, revised DSO 14-pin package marking information.

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