**MARCH 2016**

# 512Kx16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

## KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  – 36 mW (typical) operating
- TTL compatible interface levels
- Single power supply
  –1.65V—2.2V VDD (62/65WV51216EALL)
  – 2.2V--3.6V VDD (62/65WV51216EBLL)
- Data control for upper and lower bytes
- Automotive temperature (-40°C to +125°C)

## DESCRIPTION

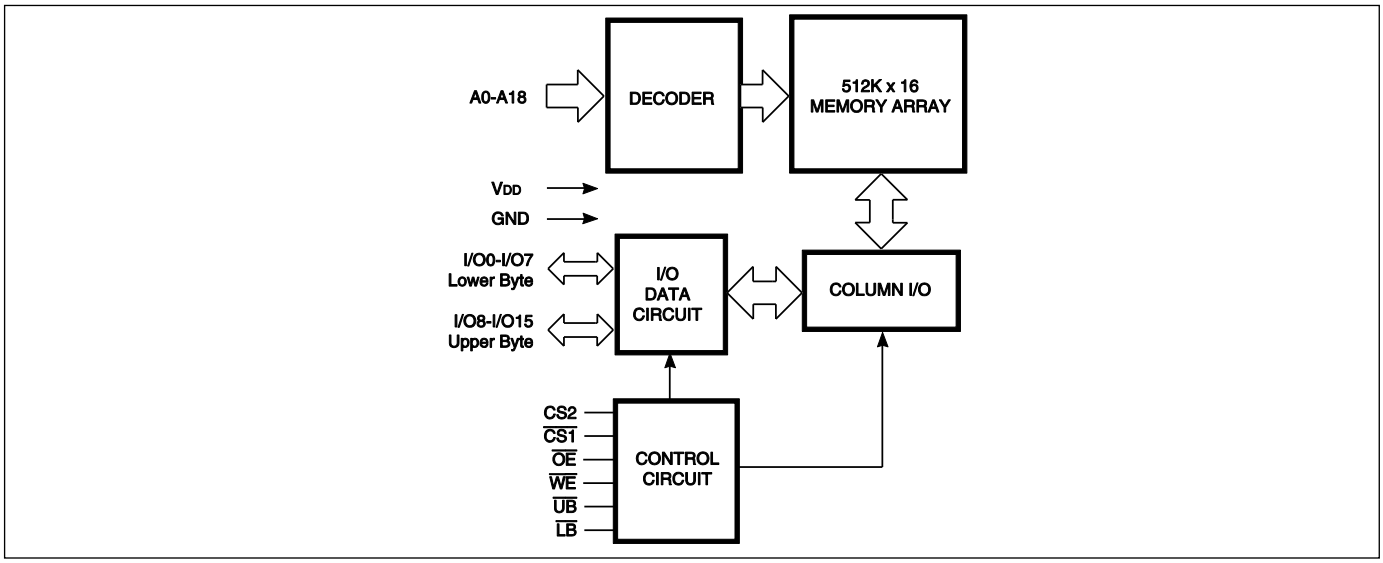
The *ISSI* IS62WV51216EALL/ IS62WV51216EBLL are high-speed, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is low (deselected) or when $\overline{CS1}$ is low , CS2 is high and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

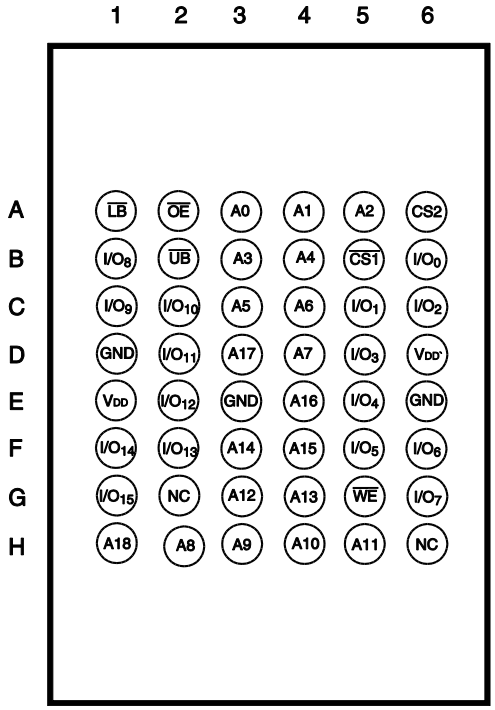
The IS62WV51216EALL and IS62WV51216EBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x8mm), 44-Pin TSOP (TYPE II) and 48-pin TSOP (TYPE I).

## BLOCK DIAGRAM

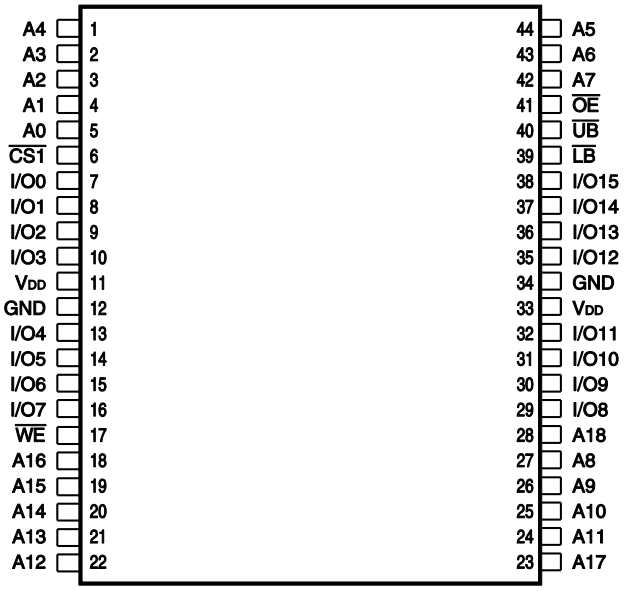


## PIN CONFIGURATIONS (512Kx16)

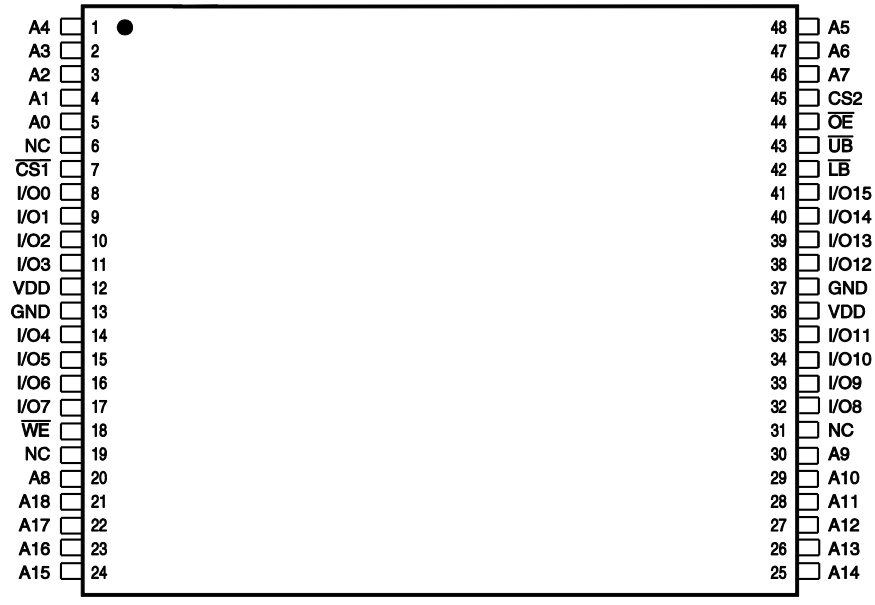
48-Pin mini BGA (6mm x 8mm)




44-Pin TSOP (Type II)




2 CS Option (Package Code T2)
48-pin TSOP-I (12mm x 20mm)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A18 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| CS1, CS2 | Chip Enable Input |
| OE | Output Enable Input |
| WE | Write Enable Input |
| LB | Lower-byte Control (I/O0-I/O7) |
| UB | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

## FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

## STANDBY MODE

Device enters standby mode when deselected ($\overline{CS1}$ HIGH or CS2 LOW or both $\overline{UB}$ and $\overline{LB}$ are HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be either ISB1 or ISB2 depending on the input level. CMOS input in this mode will maximize saving power.

## WRITE MODE

Write operation issues with Chip selected ($\overline{CS1}$ LOW and CS2 HIGH) and Write Enable ($\overline{WE}$) input LOW. The input and output pins(I/O0-15) are in data input mode. Output buffers are closed during this time even if $\overline{OE}$ is LOW. $\overline{UB}$ and $\overline{LB}$ enables a byte write feature. By enabling $\overline{LB}$ LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with $\overline{UB}$ being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

## READ MODE

Read operation issues with Chip selected ($\overline{CS1}$ LOW and CS2 HIGH) and Write Enable ($\overline{WE}$) input HIGH. When $\overline{OE}$ is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. $\overline{UB}$ and $\overline{LB}$ enables a byte read feature. By enabling $\overline{LB}$ LOW, data from memory appears on I/O0-7. And with $\overline{UB}$ being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling $\overline{OE}$ HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

## TRUTH TABLE

| Mode | $\overline{CS1}$ | CS2 | $\overline{WE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O0-I/O7 | I/O8-I/O15 | VDD Current |
|---|---|---|---|---|---|---|---|---|---|
| Not Selected | H | X | X | X | X | X | High-Z | High-Z | ISB1,ISB2 |
| | X | L | X | X | X | X | High-Z | High-Z | |
| | X | X | X | X | H | H | High-Z | High-Z | |
| Output Disabled | L | H | H | H | L | X | High-Z | High-Z | ICC |
| | L | H | H | H | X | L | High-Z | High-Z | |
| Read | L | H | H | L | L | H | DOUT | High-Z | ICC |
| | L | H | H | L | H | L | High-Z | DOUT | |
| | L | H | H | L | L | L | DOUT | DOUT | |
| Write | L | H | L | X | L | H | DIN | High-Z | ICC |
| | L | H | L | X | H | L | High-Z | DIN | |
| | L | H | L | X | L | L | DIN | DIN | |

## ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

### ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Vterm | Terminal Voltage with Respect to GND | –0.2 to +3.9($V_{DD}$+0.3V) | V |
| tBIAS | Temperature Under Bias | –55 to +125 | °C |
| $V_{DD}$ | $V_{DD}$ Related to GND | –0.2 to +3.9($V_{DD}$+0.3V) | V |
| tStg | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### OPERATING RANGE(1)

| Range | Device Marking | Ambient Temperature | VDD(min) | VDD(typ) | VDD(max) |
|---|---|---|---|---|---|
| Commercial | IS62WV51216EALL | 0°C to +70°C | 1.65V | 1.8V | 2.2V |
| Industrial | IS62WV51216EALL | -40°C to +85°C | 1.65V | 1.8V | 2.2V |
| Automotive | IS65WV51216EALL | -40°C to +125°C | 1.65V | 1.8V | 2.2V |
| Commercial | IS62WV51216EBLL | 0°C to +70°C | 2.2V | 3.3V | 3.6V |
| Industrial | IS62WV51216EBLL | -40°C to +85°C | 2.2V | 3.3V | 3.6V |
| Automotive | IS65WV51216EBLL | -40°C to +125°C | 2.2V | 3.3V | 3.6V |

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

### PIN CAPACITANCE (1)

| Parameter | Symbol | Test Condition | Max | Units |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = $V_{DD}$(typ) | 10 | pF |
| DQ capacitance (IO0–IO15) | $C_{I/O}$ | | 10 | pF |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

### THERMAL CHARACTERISTICS (1)

| Parameter | Package | Symbol | Rating | Units |
|---|---|---|---|---|
| Thermal resistance from junction to ambient (airflow = 0m/s) | 44-pin TSOP-II | $R_{\theta JA}$ | 51.8 | °C/W |
| | 48-ball VFBGA | | 48.05 | |
| Thermal resistance from junction to case (airflow = 0m/s) | 44-pin TSOP-II | $R_{\theta JC}$ | 9.6 | °C/W |
| | 48-ball VFBGA | | 13.35 | |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

## ELECTRICAL CHARACTERISTICS

### IS62(5)WV51216EALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -0.1 mA | 1.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | — | 0.2 | V |
| $V_{IH}$(1) | Input HIGH Voltage | | 1.4 | $V_{DD}$ + 0.2 | V |
| $V_{IL}$(1) | Input LOW Voltage | | –0.2 | 0.4 | V |
| $I_{LI}$ | Input Leakage | GND < $V_{IN}$ < $V_{DD}$ | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND < $V_{IN}$ < $V_{DD}$, Output Disabled | –1 | 1 | µA |

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

### IS62(5)WV51216EBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.2 ≤ $V_{DD}$ < 2.7, $I_{OH}$ = -0.1 mA | 2.0 | — | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6, $I_{OH}$ = -1.0 mA | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | 2.2 ≤ $V_{DD}$ < 2.7, $I_{OL}$ = 0.1 mA | — | 0.4 | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6, $I_{OL}$ = 2.1 mA | — | 0.4 | V |
| $V_{IH}$(1) | Input HIGH Voltage | 2.2 ≤ $V_{DD}$ < 2.7 | 1.8 | $V_{DD}$ + 0.3 | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6 | 2.2 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$(1) | Input LOW Voltage | 2.2 ≤ $V_{DD}$ < 2.7 | –0.3 | 0.6 | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6 | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND < $V_{IN}$ < $V_{DD}$ | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND < $V_{IN}$ < $V_{DD}$, Output Disabled | –1 | 1 | µA |

Notes:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

## IS62(5)WV51216EALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Grade | | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| ICC | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$=0mA, f=$f_{MAX}$ | Com. | | - | 12 | mA |
| | | | Ind. | | - | 15 | |
| | | | Auto. | | - | 15 | |
| ICC1 | $V_{DD}$ Static Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$ = 0mA, f=0Hz | Com. | | - | 6 | mA |
| | | | Ind. | | - | 6 | |
| | | | Auto. | | - | 6 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | $V_{DD}=V_{DD}(max)$,<br>(1) 0V ≤ CS2 ≤ 0.2V<br>or<br>(2) $\overline{CS1}$ ≥ $V_{DD}$ - 0.2V, CS2 ≥ $V_{DD}$ - 0.2V<br>or<br>(3) $\overline{LB}$ and $\overline{UB}$ ≥ $V_{DD}$- 0.2V<br>$\overline{CS1}$ ≤ 0.2V, CS2 ≥ $V_{DD}$ - 0.2V | Com. | 25°C | 11.1 | 15 | µA |
| | | | | 45°C | 11.4 | 17 | |
| | | | | 70°C | 13.6 | 20 | |
| | | | Ind./Auto A1 | | 15.1 | 25 | |
| | | | Auto. A3 | | 28.4 | 50 | |

Note:
1. Typical values are measured at VDD = 1.8V and not 100% tested.

## IS62(5)WV51216EBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Grade | | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| ICC | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$=0mA, f=$f_{MAX}$ | Com. | | - | 15 | mA |
| | | | Ind. | | - | 15 | |
| | | | Auto. | | - | 15 | |
| ICC1 | $V_{DD}$ Static Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$ = 0mA, f=0Hz | Com. | | - | 6 | mA |
| | | | Ind. | | - | 6 | |
| | | | Auto. | | - | 6 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | $V_{DD}=V_{DD}(max)$,<br>(1) 0V ≤ CS2 ≤ 0.2V<br>or<br>(2) $\overline{CS1}$ ≥ $V_{DD}$ - 0.2V, CS2 ≥ $V_{DD}$ - 0.2V<br>or<br>(3) $\overline{LB}$ and $\overline{UB}$ ≥ $V_{DD}$- 0.2V<br>$\overline{CS1}$ ≤ 0.2V, CS2 ≥ $V_{DD}$ - 0.2V | Com. | 25°C | 11.1 | 15 | µA |
| | | | | 45°C | 11.4 | 17 | |
| | | | | 70°C | 13.6 | 20 | |
| | | | Ind./Auto A1 | | 15.1 | 25 | |
| | | | Auto. A3 | | 28.4 | 50 | |

Note:
1. Typical values are measured at VDD = 3.0V, and not 100% tested.

## AC CHARACTERISTICS[6] (OVER OPERATING RANGE)

### READ CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Read Cycle Time | tRC | 45 | - | 55 | - | ns | 1,5 |
| Address Access Time | tAA | - | 45 | - | 55 | ns | 1 |
| Output Hold Time | tOHA | 8 | - | 8 | - | ns | 1 |
| $\overline{CS1}$, CS2 Access Time | tACS1/tACS2 | - | 45 | - | 55 | ns | 1 |
| $\overline{OE}$ Access Time | tDOE | - | 22 | - | 25 | ns | 1 |
| $\overline{OE}$ to High-Z Output | tHZOE | - | 18 | - | 18 | ns | 2 |
| $\overline{OE}$ to Low-Z Output | tLZOE | 5 | - | 5 | - | ns | 2 |
| $\overline{CS1}$, CS2 to High-Z Output | tHZCS//tHZCS2 | - | 18 | - | 18 | ns | 2 |
| $\overline{CS1}$, CS2 to Low-Z Output | tLZCS/tLZCS2 | 10 | - | 10 | - | ns | 2 |
| $\overline{LB}$, $\overline{UB}$ Access Time | tBA | - | 45 | - | 55 | ns | 1 |
| $\overline{LB}$, $\overline{UB}$ to High-Z Output | tHZB | - | 18 | - | 18 | ns | 2 |
| $\overline{LB}$, $\overline{UB}$ to Low-Z Output | tLZB | 10 | - | 10 | - | ns | 2 |

### WRITE CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Write Cycle Time | tWC | 45 | - | 55 | - | ns | 1,3,5 |
| $\overline{CS1}$,CS2 to Write End | tSCS1/tSCS2 | 35 | - | 40 | - | ns | 1,3 |
| Address Setup Time to Write End | tAW | 35 | - | 40 | - | ns | 1,3 |
| Address Hold from Write End | tHA | 0 | - | 0 | - | ns | 1,3 |
| Address Setup Time | tSA | 0 | - | 0 | - | ns | 1,3 |
| $\overline{LB}$, /$\overline{UB}$ Valid to End of Write | tPWB | 35 | - | 40 | - | ns | 1,3 |
| $\overline{WE}$ Pulse Width | tPWE | 35 | - | 40 | - | ns | 1,3,4 |
| Data Setup to Write End | tSD | 28 | - | 28 | - | ns | 1,3 |
| Data Hold from Write End | tHD | 0 | - | 0 | - | ns | 1,3 |
| $\overline{WE}$ LOW to High-Z Output | tHZWE | - | 18 | - | 18 | ns | 2,3 |
| $\overline{WE}$ HIGH to Low-Z Output | tLZWE | 10 | - | 10 | - | ns | 2,3 |

Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CS1}$=LOW, CS2=HIGH, ($\overline{UB}$ or $\overline{LB}$)=LOW, and $\overline{WE}$=LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE is LOW.
5. Address inputs must meet $V_{IH}$ and $V_{IL}$ SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

## AC TEST CONDITIONS (OVER THE OPERATING RANGE)

| Parameter | Symbol | Conditions | Units |
|---|---|---|---|
| Input Rise Time | $T_R$ | 1.0 | V/ns |
| Input Fall Time | $T_F$ | 1.0 | V/ns |
| Output Timing Reference Level | $V_{REF}$ | ½ $V_{TM}$ | V |
| Output Load Conditions | Refer to Figure 1 and 2 | | |

## OUTPUT LOAD CONDITIONS FIGURES

**Figure1**

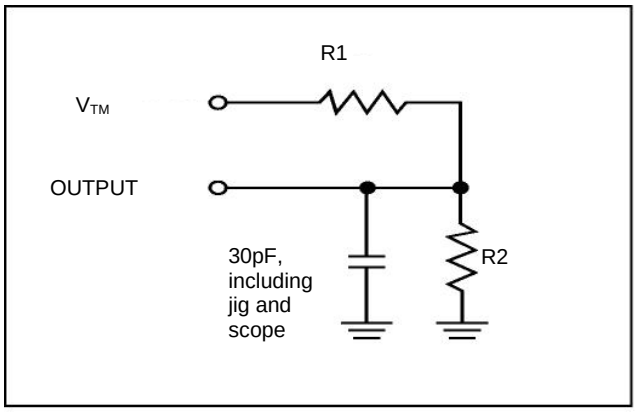
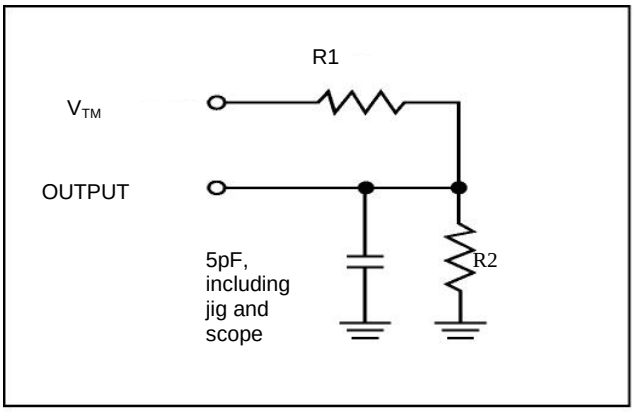


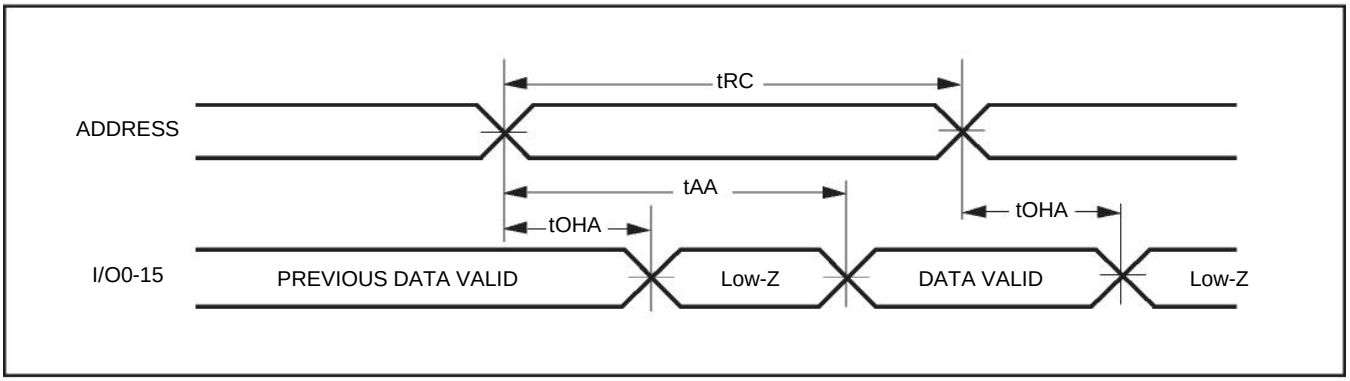

**Figure2**



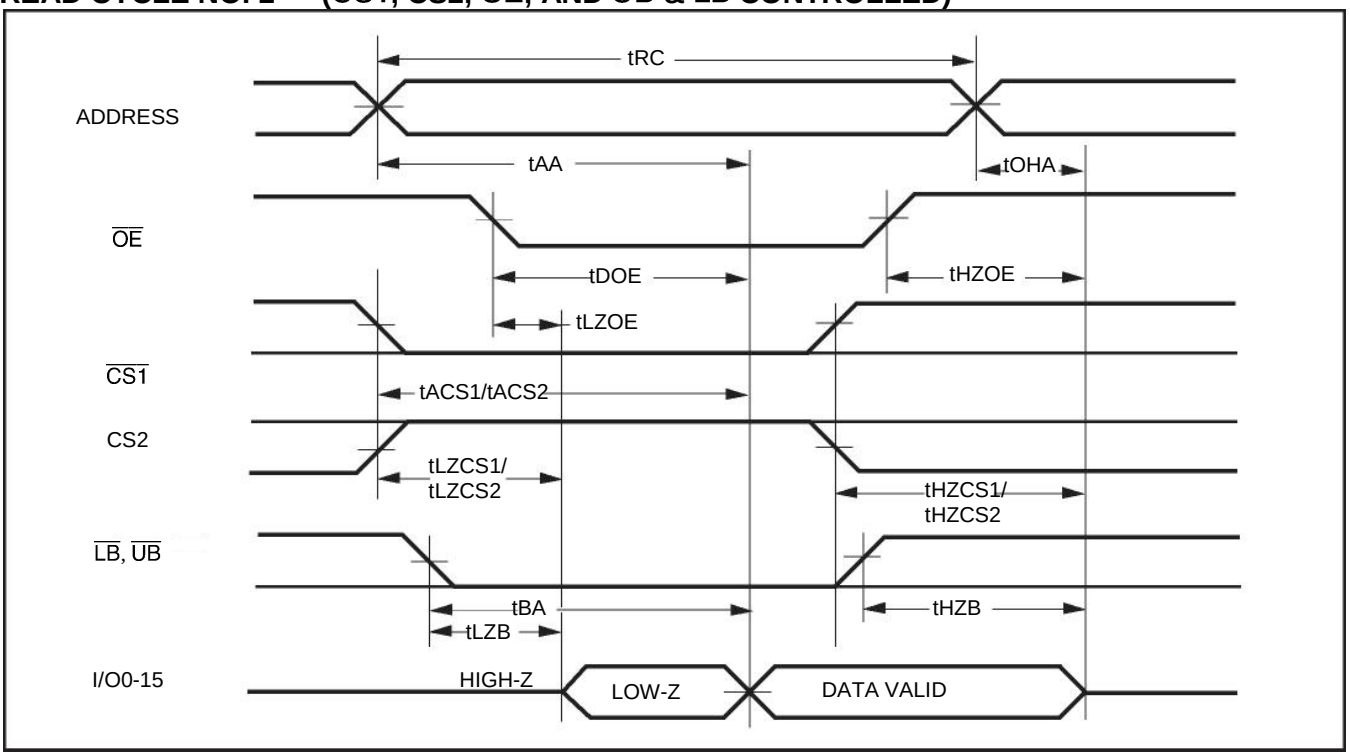

| Parameters | $V_{DD}$=1.65~2.2V | $V_{DD}$=2.2~2.7V | $V_{DD}$=2.7~3.6V |
|---|---|---|---|
| Input Pulse Level | 0.4V to VDD-0.2V | 0.4V to VDD-0.3V | |
| R1 | 13500Ω | 16667Ω | 1103Ω |
| R2 | 10800Ω | 15385Ω | 1554Ω |
| $V_{TM}$ | VDD | VDD | VDD |

## TIMING DIAGRAM

### READ CYCLE NO. 1[1,2] (ADDRESS CONTROLLED) ($\overline{CS1}$=$\overline{OE}$=VIL, CS2=$\overline{WE}$=VIH)

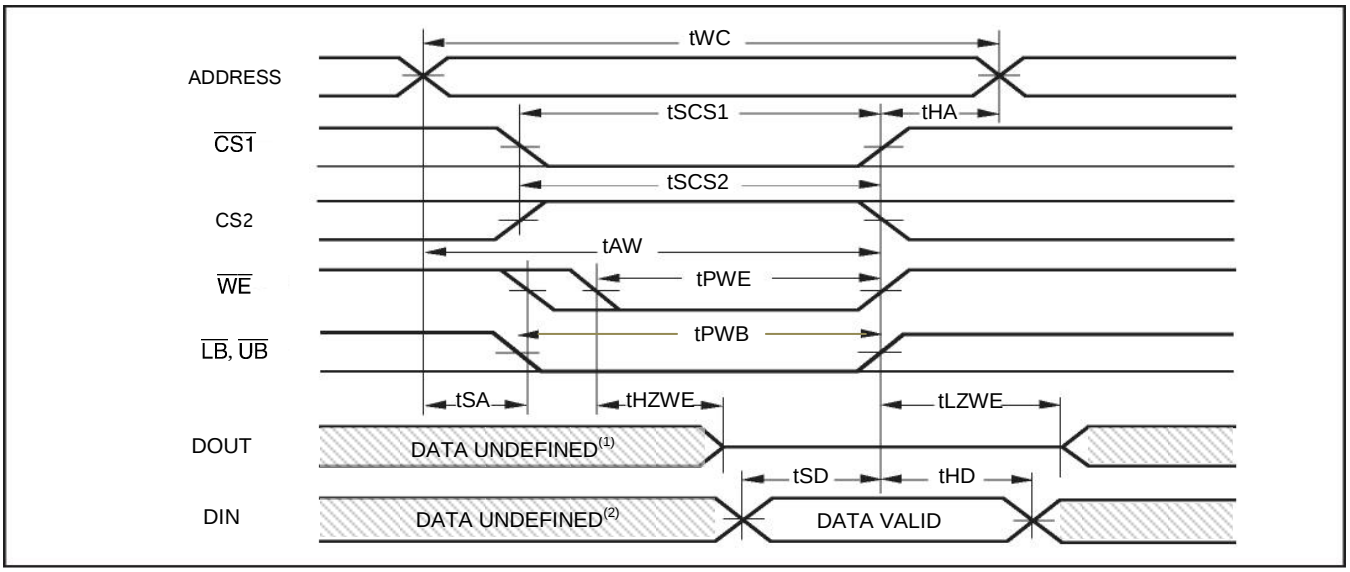



### READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$ & $\overline{LB}$ CONTROLLED)



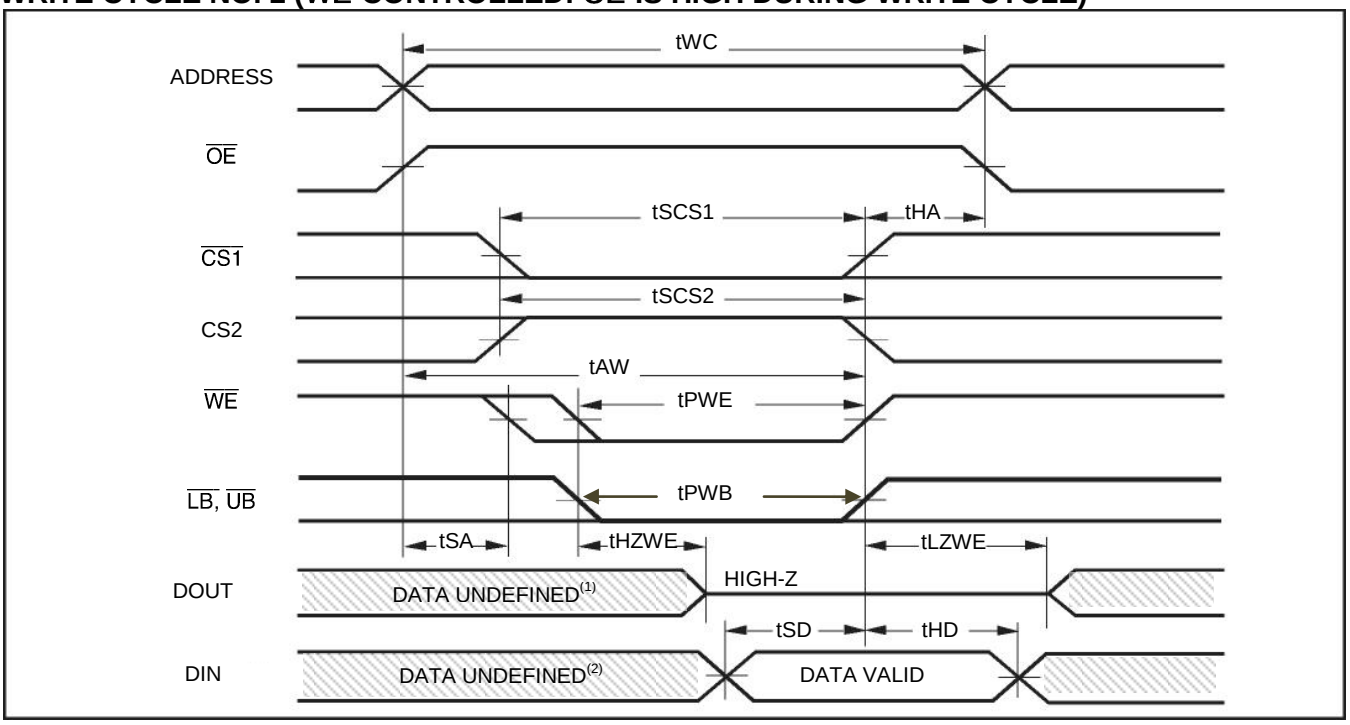

Notes:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$=VIL.CS2=$\overline{WE}$=VIH.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

## WRITE CYCLE NO. 1 ($\overline{CS1}$ CONTROLLED, $\overline{OE}$ = HIGH OR LOW)



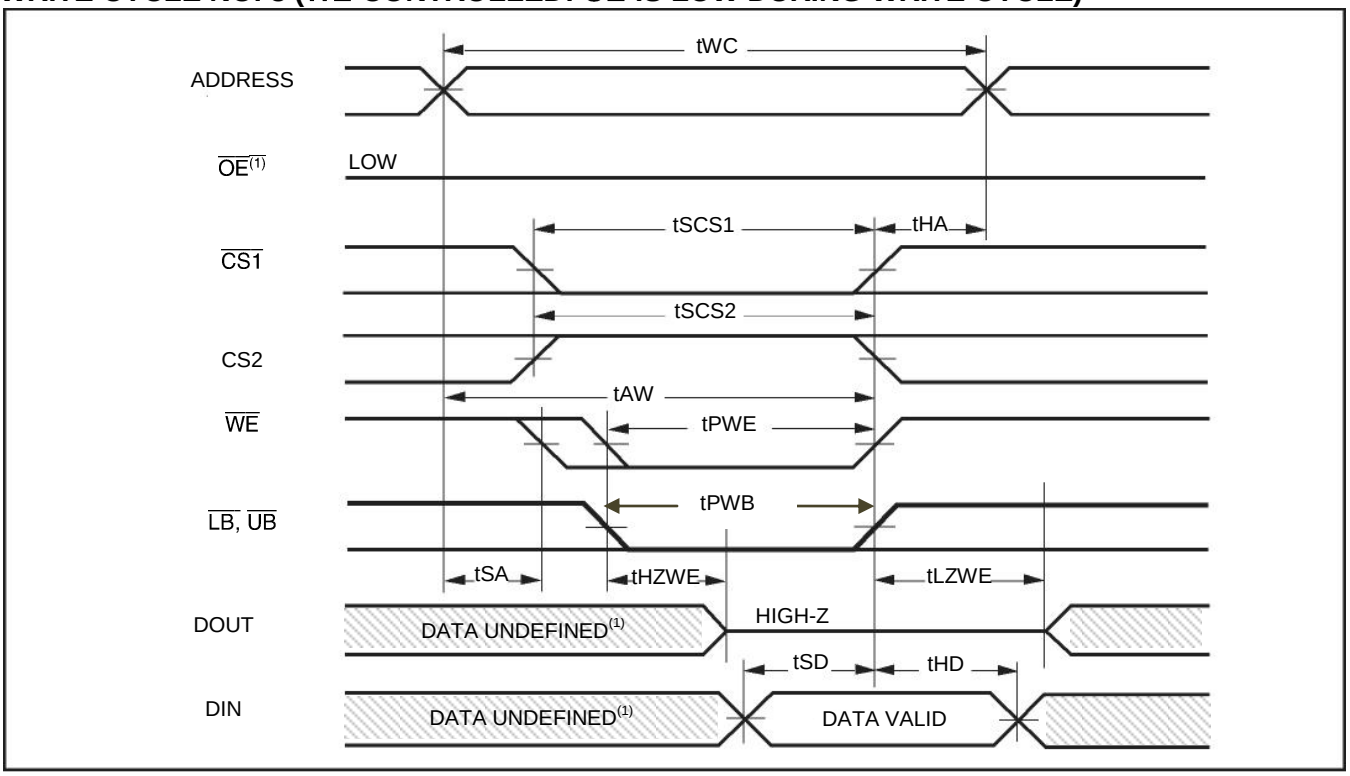

Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if $\overline{OE}$ goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after $\overline{OE}$ goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

## WRITE CYCLE NO. 2 ($\overline{WE}$ CONTROLLED: $\overline{OE}$ IS HIGH DURING WRITE CYCLE)



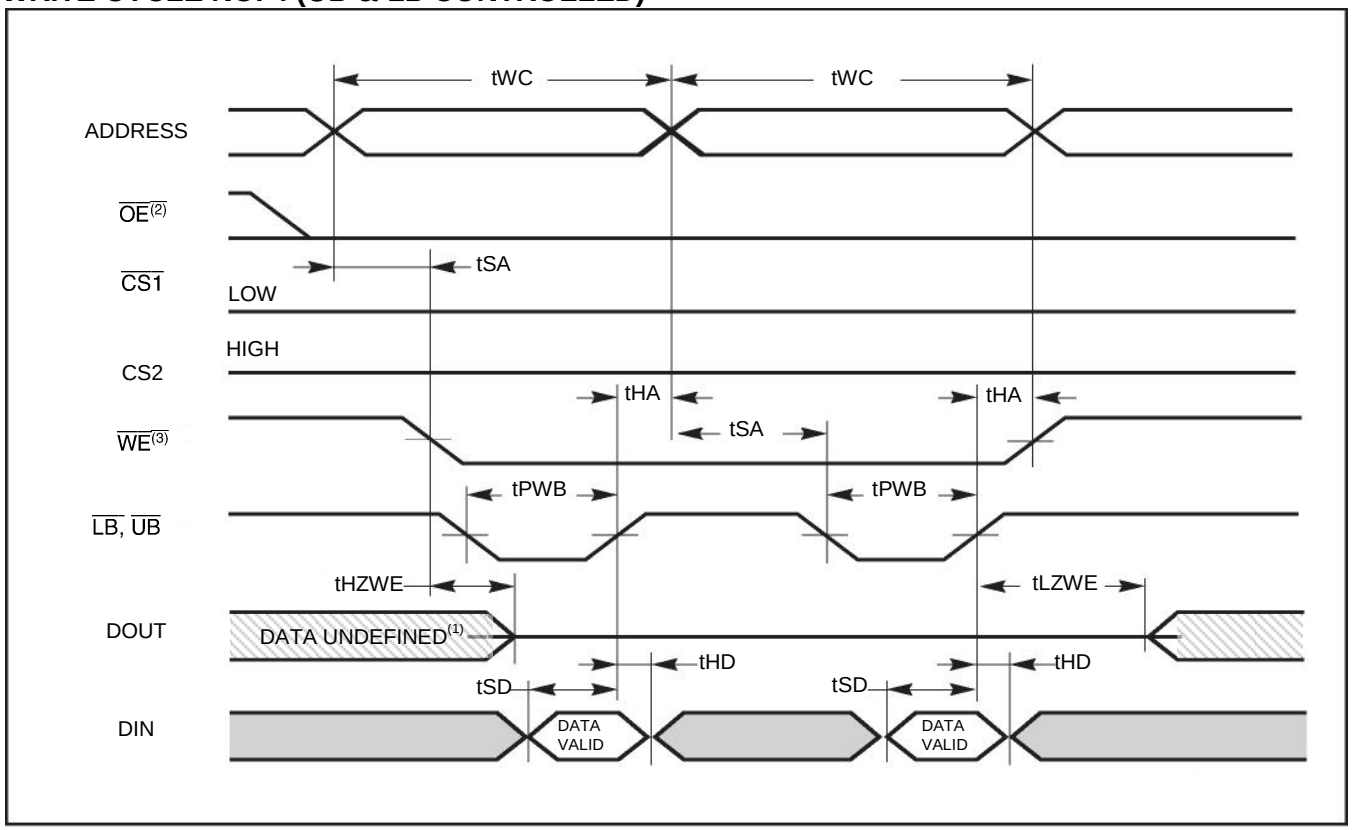

Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if $\overline{OE}$ goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after $\overline{OE}$ goes high.
2. During this period the I/Os are in output state. Do not apply input signals.

## WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED: $\overline{OE}$ IS LOW DURING WRITE CYCLE)




Notes:
1. If $\overline{OE}$ is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

## WRITE CYCLE NO. 4 ($\overline{UB}$ & $\overline{LB}$ CONTROLLED)



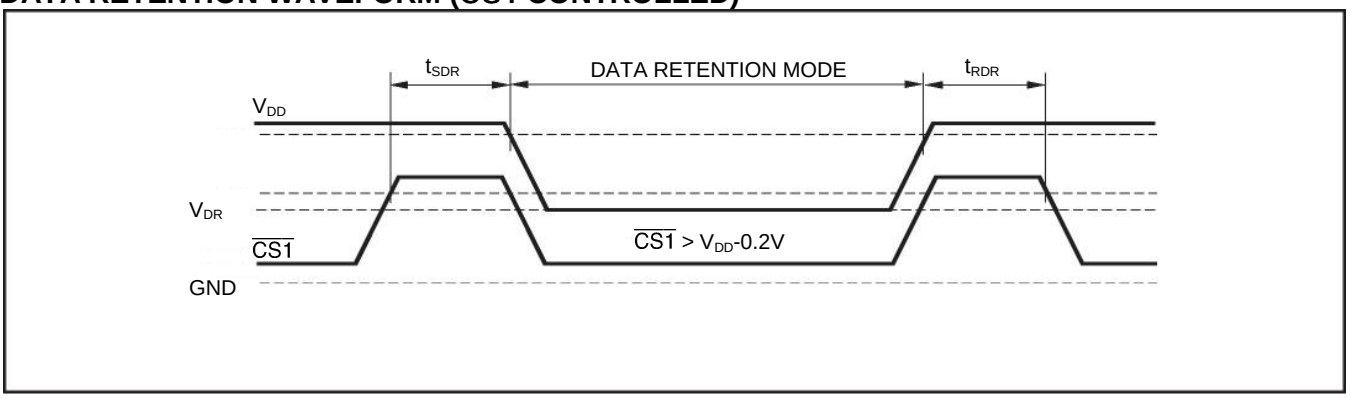

Notes:
1. If $\overline{OE}$ is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, $\overline{OE}$ is recommended to be HIGH during write period.
3. Note $\overline{WE}$ stays LOW in this example. If $\overline{WE}$ toggles, tPWE and tHZWE must be considered.

## DATA RETENTION CHARACTERISTICS

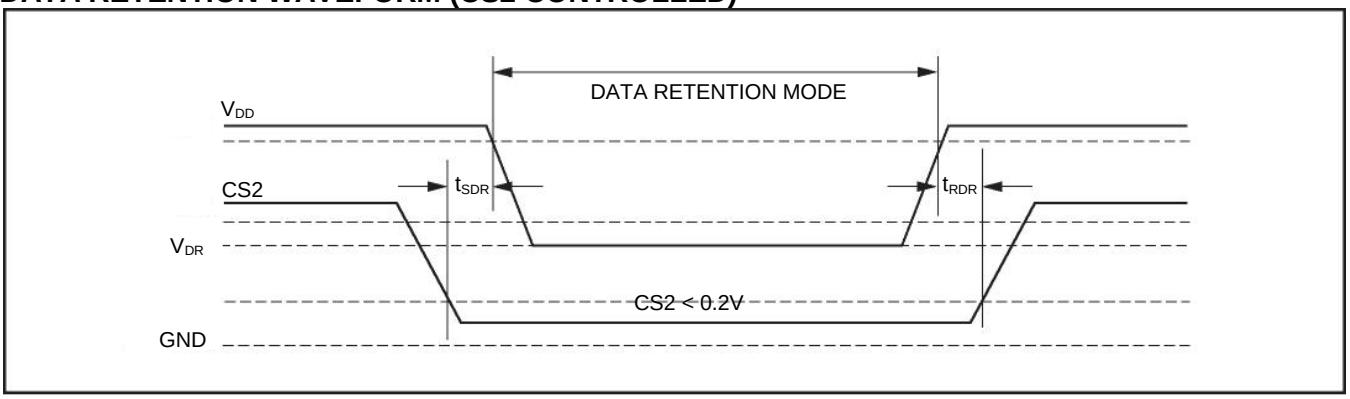
| Symbol | Parameter | Test Condition | OPTION | Min. | Typ.(2) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | IS62(5)WV51216EALL | 1.5 | | - | V |
| | | | IS62(5)WV51216EBLL | 1.5 | | - | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$= $V_{DR}$(min),<br>(1) 0V ≤ CS2 ≤ 0.2V, or<br>(2) $\overline{CS1}$ ≥ $V_{DD}$ – 0.2V,<br>CS2 ≥ $V_{DD}$ - 0.2V<br>(3) $\overline{LB}$ and $\overline{UB}$ ≥ $V_{DD}$ -0.2V,<br>$\overline{CS1}$ ≤ 0.2V, CS2 ≥ $V_{DD}$ - 0.2V | Com. | - | - | 20 | uA |
| | | | Ind. | - | - | 25 | |
| | | | Auto | - | - | 50 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | - | - | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | tRC | - | - | ns |

Note:
1. If $\overline{CS1}$>VDD–0.2V, all other inputs including CS2 and $\overline{UB}$ and $\overline{LB}$ must meet this condition.
2. Typical values are measured at VDD=VDR(min), TA = 25℃ and not 100% tested.

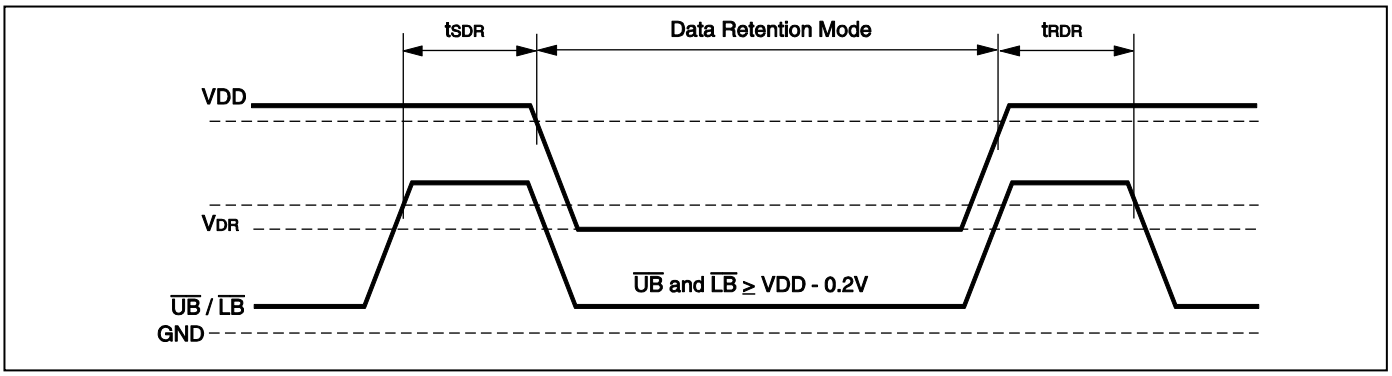
## DATA RETENTION WAVEFORM ($\overline{CS1}$ CONTROLLED)




## DATA RETENTION WAVEFORM (CS2 CONTROLLED)



## DATA RETENTION WAVEFORM ($\overline{UB}$ AND $\overline{LB}$ CONTROLLED)




**Note:**
1. CS2 must satisfy either CS2 ≥ Vcc -0.2V or CS2 ≤ 0.2V
2. $\overline{CS1}$ must satisfy either $\overline{CS1}$ ≥ Vcc -0.2V or $\overline{CS1}$ ≤ 0.2V

## ORDERING INFORMATION

### IS62/65WV51216EALL (1.65V - 2.2V)
### Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 55 | IS62WV51216EALL-55TI | TSOP-II |
| | IS62WV51216EALL-55TLI | TSOP-II, Lead-free |
| | IS62WV51216EALL-55BI | mini BGA |
| | IS62WV51216EALL-55BLI | mini BGA, Lead-free |

## ORDERING INFORMATION

### IS62/65WV51216EBLL (2.2V - 3.6V)

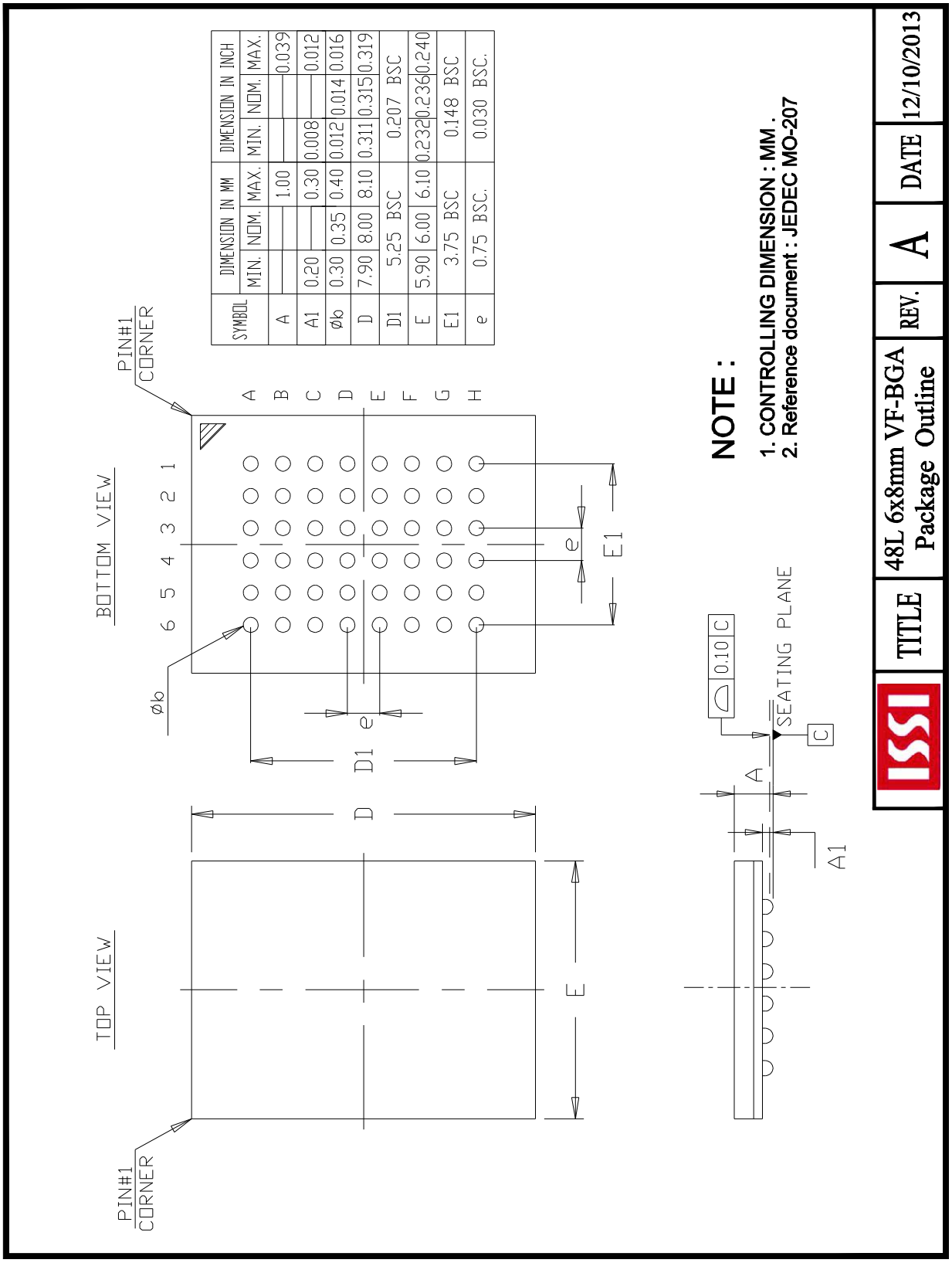
### Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 45 | IS62WV51216EBLL-45TI | TSOP-II |
| | IS62WV51216EBLL-45TLI | TSOP-II, Lead-free |
| | IS62WV51216EBLL-45T2LI | 2 CS option TSOP I, Lead-free |
| | IS62WV51216EBLL-45BI | mini BGA |
| | IS62WV51216EBLL-45BLI | mini BGA, Lead-free |
| 55 | IS62WV51216EBLL-55TI | TSOP-II |
| | IS62WV51216EBLL-55TLI | TSOP-II, Lead-free |
| | IS62WV51216EBLL-55BI | mini BGA |
| | IS62WV51216EBLL-55BLI | mini BGA, Lead-free |

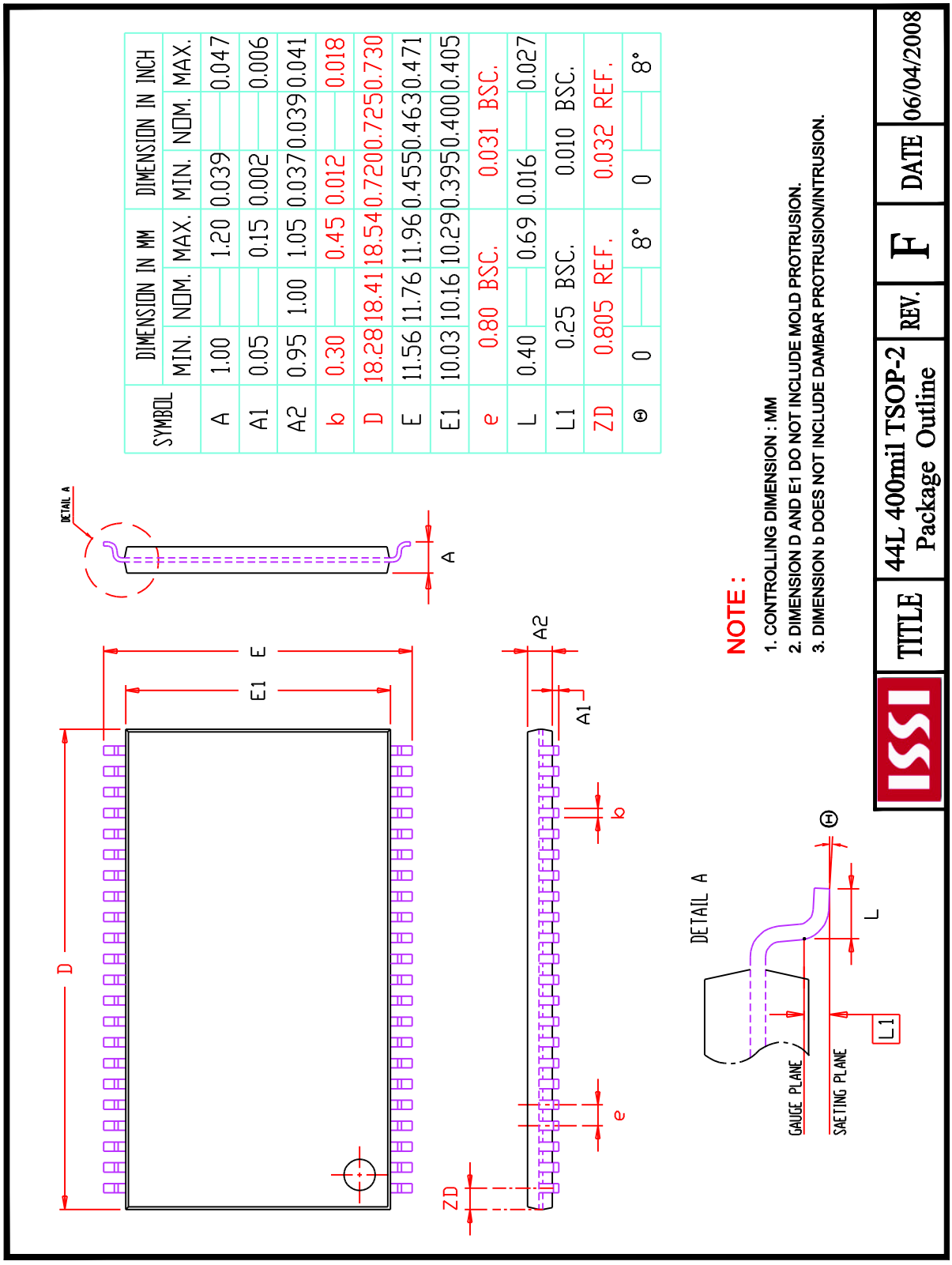
### Automotive Range A3: –40°C to +125°C

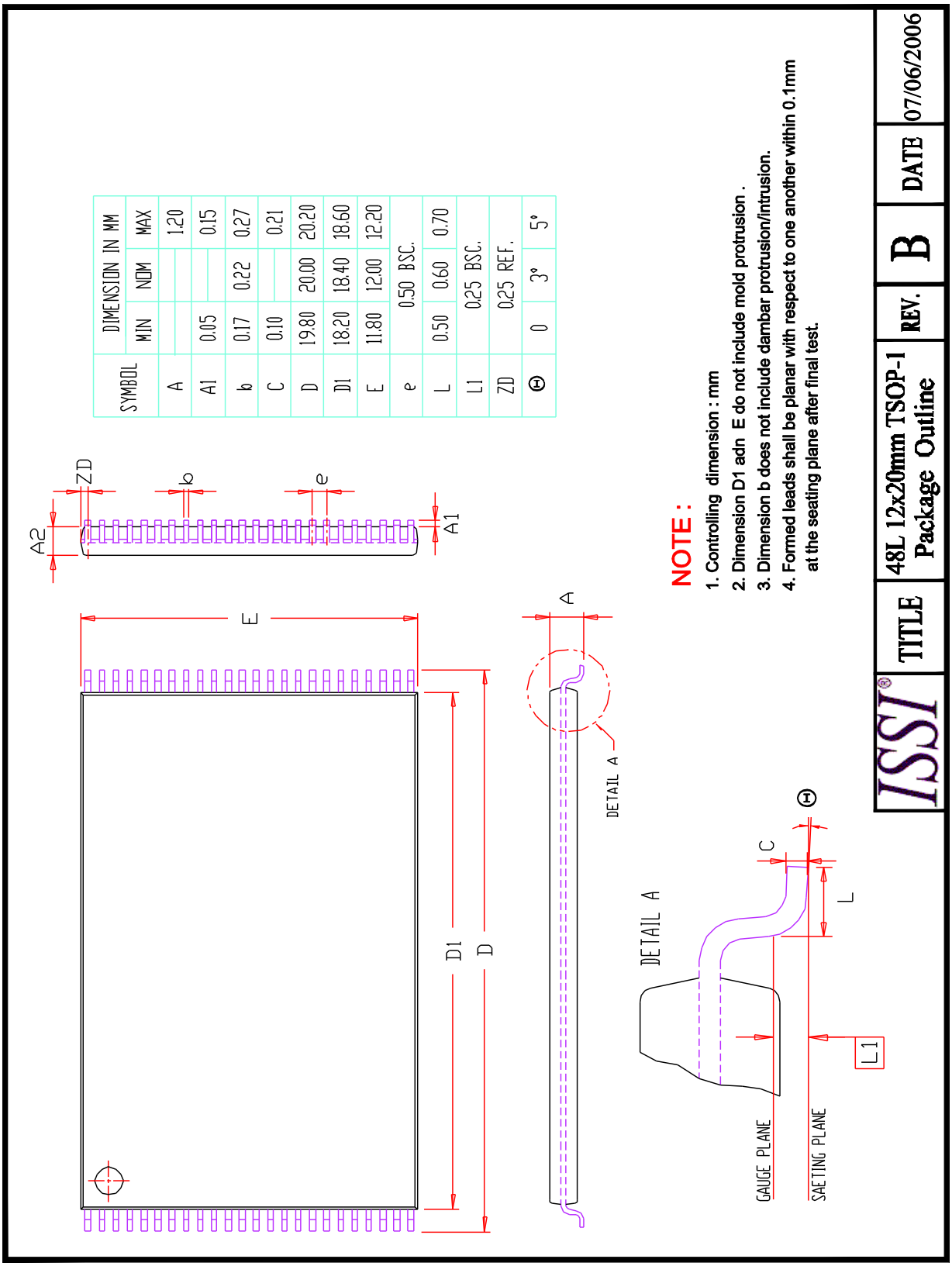
| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 45 | IS65WV51216EBLL-45BA3 | mini BGA |
| | IS65WV51216EBLL-45BLA3 | mini BGA, Lead-free |
| | IS65WV51216EBLL-45CTA3 | TSOP II, Copper Leadframe |
| | IS65WV51216EBLL-45CTLA3 | TSOP II, Lead-free, Copper Leadframe |

## PACKAGE INFORMATION




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.00 | | | 0.039 |
| A1 | 0.20 | | 0.30 | 0.008 | | 0.012 |
| øb | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | | 5.25 BSC | | | 0.207 BSC | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | | 3.75 BSC | | | 0.148 BSC | |
| e | | 0.75 BSC. | | | 0.030 BSC. | |


SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A 1.00 — 1.20 0.039 — 0.047
A1 0.05 — 0.15 0.002 — 0.006
A2 0.95 1.00 1.05 0.037 0.039 0.041
b 0.30 — 0.45 0.012 — 0.018
D 18.28 18.41 18.54 0.720 0.725 0.730
E 11.56 11.76 11.96 0.455 0.463 0.471
E1 10.03 10.16 10.29 0.395 0.400 0.405
e 0.80 BSC. 0.031 BSC.
L 0.40 — 0.69 0.016 — 0.027
L1 0.25 BSC. 0.010 BSC.
ZD 0.805 REF. 0.032 REF.
θ 0 — 8° 0 — 8°
NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
DETAIL A
A
E
E1
D
A2
A1
b
e
ZD
θ
L
L1
GAUGE PLANE
SEATING PLANE
ISSI
TITLE
44L 400mil TSOP-2 Package Outline
REV. F
DATE 06/04/2008


DIMENSION IN MM
SYMBOL
MIN
NOM
MAX
A 1.20
A1 0.05 0.15
b 0.17 0.22 0.27
C 0.10 0.21
D 19.80 20.00 20.20
D1 18.20 18.40 18.60
E 11.80 12.00 12.20
e 0.50 BSC.
L 0.50 0.60 0.70
L1 0.25 BSC.
ZD 0.25 REF.
θ 0 3° 5°
NOTE :
1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
ISSI
TITLE
48L 12x20mm TSOP-1 Package Outline
REV.
B
DATE
07/06/2006
A2
ZD
b
e
A1
E
D1
D
A
DETAIL A
C
L
L1
GAUGE PLANE
SEATING PLANE