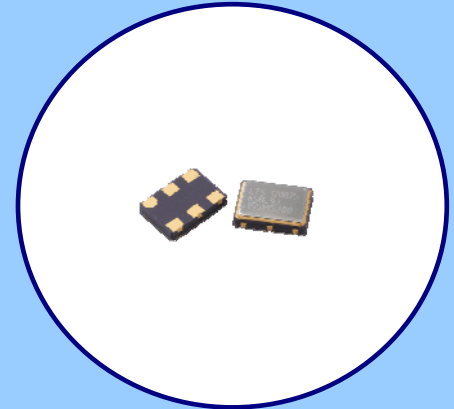


FEATURES

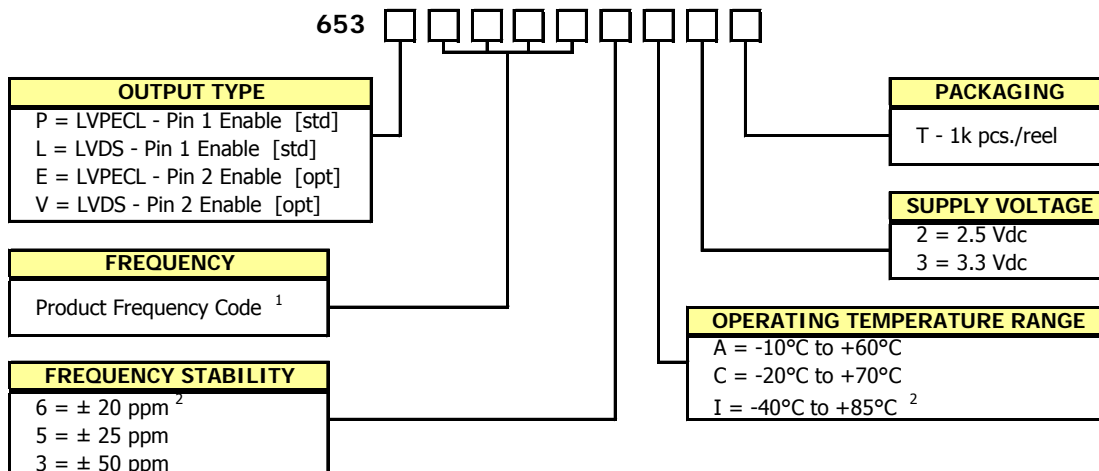
- Standard 5.0mm x 3.2mm 6-Pad Surface Mount Package
- Low Phase Jitter, 0.7ps RMS Maximum
- LVPECL or LVDS Output
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 25 – 320 MHz
- Frequency Stability ±50 ppm Standard
- Operating Voltages +2.5Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 653 is ideal for applications such as broadband access, Ethernet/Gigabit Ethernet, SONET/SDH and optical networking.

ORDERING INFORMATION

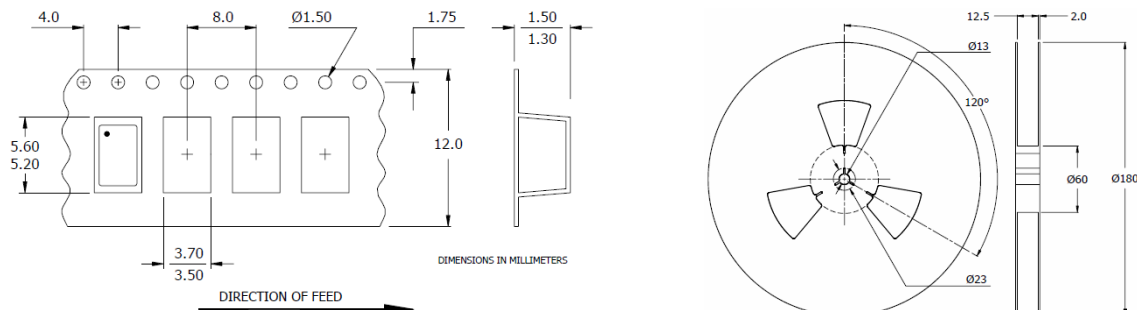


1] Refer to document 016-1454-0, Frequency Code Tables.
3-digits required for frequencies below 100MHz and 4-digits for frequencies 100MHz or greater.
2] Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.



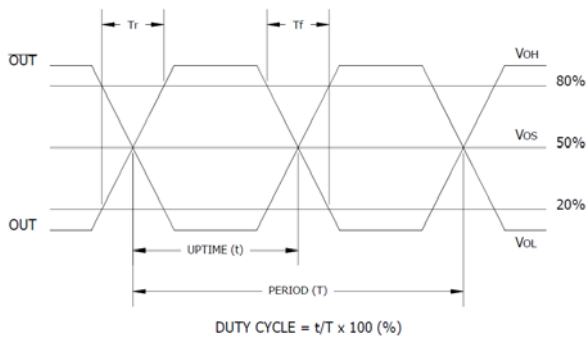
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V _{CC}	-	-0.5	-	5.0	V
Storage Temperature	T _{STG}	-	-40	-	+100	°C
Frequency Range	f ₀	-	25	-	320	MHz
LVPECL						
LVDS			80	-	320	
Frequency Stability	Δf/f ₀	All Inclusive, see Note 1.	-	-	20, 25, 50	± ppm
		1st year aging	-	-	3	
Operating Temperature	T _A	-	-20	25	+70	°C
Commercial						
Industrial			-40		+85	
Supply Voltage	V _{CC}	± 5 %	2.38	2.5	2.63	V
			3.14	3.3	3.47	
Supply Current	I _{CC}	Maximum Load	-	-	88	mA
LVPECL						
LVDS			-	-	65	
Start Up Time	T _S	Application of V _{CC}	-	2	5	ms
Phase Jitter	t _{jrms}	Bandwidth 12 kHz - 20 MHz	-	0.3	0.7	ps
Period Jitter RMS	p _{jrms}	-	-	2.6	-	
Period Jitter Pk-Pk	-	-	-	25	-	
Enable Function		Standby				V
Enable Input Voltage	V _{IH}	Pin 1 or 2 Logic '1', Output Enabled	0.7*V _{CC}	-	-	
Disable Input Voltage	V _{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	0.3*V _{CC}	
Disable Time	T _{PLZ}	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
Enable Time	T _{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
LVPECL WAVEFORM						
Output Load	R _L	Terminated to V _{CC} - 2.0V	-	50	-	Ohms
Output Duty Cycle	SYM	@ V _{CC} - 1.3V	45	-	55	%
Output Voltage Levels						V
Logic '1' Level	V _{OH}	PECL Load, -20°C to +70°C	V _{CC} - 1.025	-	V _{CC} - 0.880	
Logic '0' Level	V _{OL}	PECL Load, -20°C to +70°C	V _{CC} - 1.810	-	V _{CC} - 1.620	
Logic '1' Level	V _{OH}	PECL Load, -40°C to +85°C	V _{CC} - 1.085	-	V _{CC} - 0.880	V
Logic '0' Level	V _{OL}	PECL Load, -40°C to +85°C	V _{CC} - 1.830	-	V _{CC} - 1.555	
Rise and Fall Time	T _R , T _F	@ 20% - 80% Levels	-	0.6	1.0	ns
LVDS WAVEFORM						
Output Load	R _L	Between Outputs	-	100	-	Ohms
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V _{OD}	R _L = 100 Ohms	247	350	454	mV
Offset Voltage	V _{OS}	LVDS Load	1.125	1.25	1.375	V
Output Voltage Levels						V
Logic '1' Level	V _{OH}	LVDS Load	-	1.43	1.6	
Logic '0' Level	V _{OL}	LVDS Load	0.9	1.1	-	
Rise and Fall Time	T _R , T _F	@ 20% - 80% Levels	-	0.4	0.7	ns

Notes:

1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

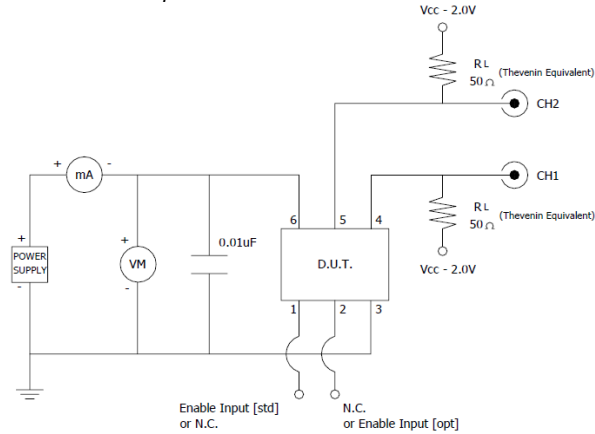
LVPECL/LVDS OUTPUT WAVEFORM



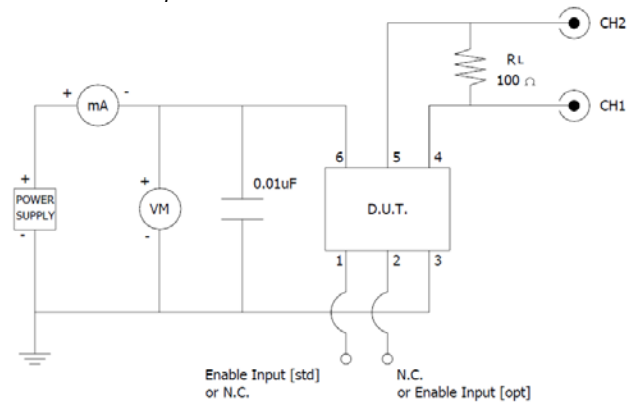
ENABLE TRUTH TABLE

PIN 1 or Pin 2	PIN 4 & 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

TEST CIRCUIT, LVPECL LOAD

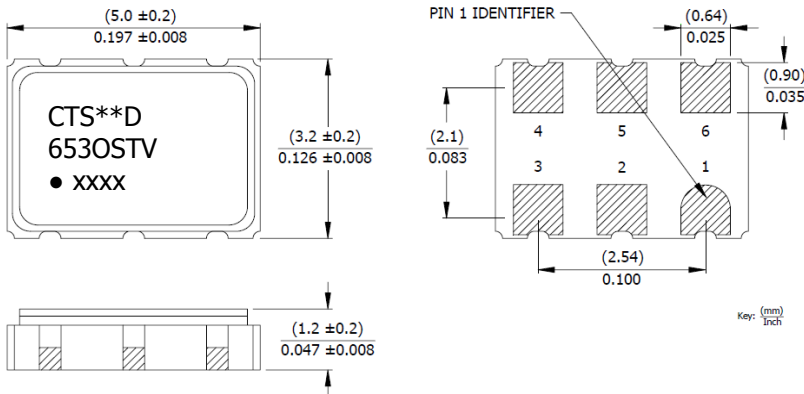


TEST CIRCUIT, LVDS LOAD



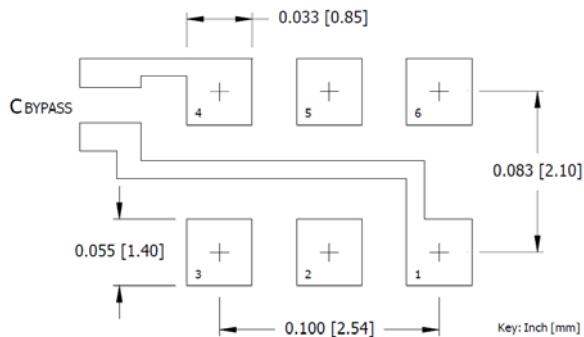
MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



MARKING INFORMATION

- ** - Manufacturing Site Code.
- D - Date Code. See Table I for codes.
- O - Output Type. P or E = LVPECL, L or V = LVDS. [Refer to Ordering Information.]
- ST - Frequency stability/temperature code. [Refer to Ordering Information.]
- V - Voltage code. 3 = 3.3V, 2 = 2.5V
- xxxx - Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater.
Refer to document 016-1454-0, Frequency Code Tables.

NOTES

- Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
- Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
- MSL = 1.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V _{CC}	Supply Voltage

TABLE I - DATE CODE

YEAR		MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
		2001	2005	2009	2013	2017												
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M		
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z		
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m		
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z		