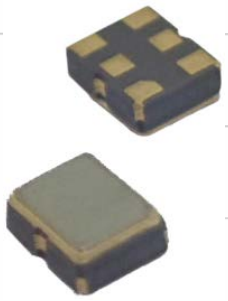
Model 626

Very Low Jitter LVPECL or LVDS Clock



Part Dimensions:
2.5 × 2.0 × 1.1mm • 14.25852mg

Features

- Ceramic Surface Mount Package
- Very Low Phase Jitter Performance, 500fs Maximum
- Fundamental or 3rd Overtone Crystal Design
- Frequency Range 6 – 220MHz *
- +2.5V or +3.3V Operation [+1.8V LVDS only]
- Output Enable Standard
- Tape and Reel Packaging, EIA-418

Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies

- 25.00MHz	- 100.00MHz
- 27.00MHz	- 125.00MHz
- 50.00MHz	- 155.52MHz
- 74.1758MHz	- 156.25MHz
- 74.25MHz	- 161.1328MHz

* See Page 9 for additional developed frequencies.
Check with factory for availability of frequencies not listed.

Description

CTS Model 626 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M626 has excellent stability and very low jitter/phase noise performance.

Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
626	P	XXX or XXXX	4	I	3	T

Code	Output
P	LVPECL - Pin 1 Enable
L	LVDS - Pin 1 Enable

Code	Stability
6	±20ppm [2]
5	±25ppm
4	±30ppm
3	±50ppm
2	±100ppm

Code	Voltage
M	+1.8Vdc [4]
2	+2.5Vdc
3	+3.3Vdc

Code	Frequency
Product Frequency Code [1]	

Code	Temp. Range
C	-20°C to +70°C
I	-40°C to +85°C
G	-40°C to +105°C [3]

Code	Packing
T	1k pcs./reel

Notes:

1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
2] Check factory for availability. Temperature code C only.
3] Check factory for availability. Stability codes 2 and 3 only.
4] LVDS output only. Consult factory for availability.

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.3	-	4.0	V
Supply Voltage [Note 1]	V_{CC}	±5%	1.710 2.375 3.135	1.8 2.5 3.3	1.890 2.625 3.465	V
Supply Current						
LVPECL	I_{CC}	V_{CC} = +3.3V or +2.5V @ maximum load	-	45	70	mA
LVDS			-	30	40	
LVDS		V_{CC} = +1.8V @ maximum load	-	7	20	
Operating Temperature	T_A	-	-20 -40 -40	 +25 	+70 +85 +105	°C
Storage Temperature	T_{STG}	-	-50	-	+125	°C

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	f_O	-		6 - 220		MHz
LVDS				6 - 220		
Frequency Stability [Note 2]	$\Delta f/f_O$	-		20, 25, 30, 50 or 100		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal V_{CC}	-5	-	5	ppm

1.] LVDS output only for +1.8V option.

2.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_L	Terminated to V_{CC} - 2.0V	-	50	-	Ohms
Output Voltage Levels	V_{OH}	PECL Load, -20°C to +70°C	V_{CC} - 1.025	-	V_{CC} - 0.880	V
	V_{OL}		V_{CC} - 1.810	-	V_{CC} - 1.620	
	V_{OH}	PECL Load, -40°C to +85°C	V_{CC} - 1.085	-	V_{CC} - 0.880	V
	V_{OL}		V_{CC} - 1.830	-	V_{CC} - 1.555	
Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 50 Ohms	-	0.3	0.7	ns
Output Type	-	-		LVDS		-
Output Load	R_L	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH}	LVDS Load	-	1.43	1.60	V
	V_{OL}		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V_{OD}	R_L = 100 Ohms	247	330	454	mV
Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, R_L = 100 Ohms	-	0.4	0.7	ns

Electrical Specifications

Output Parameters

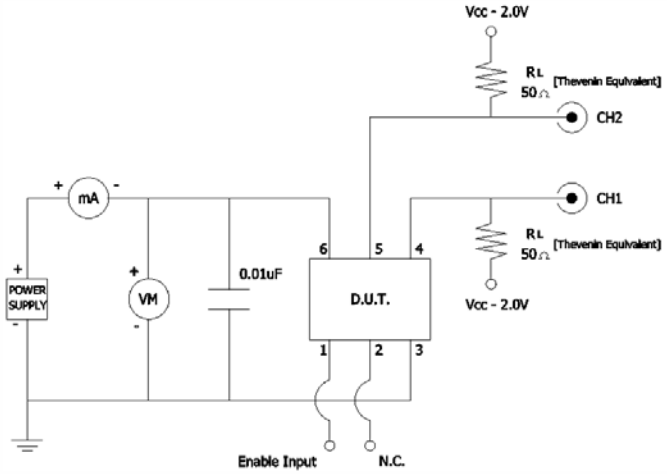
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	3	10	ms
Enable Function [Standby]						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Time	T_{PLZ}	Pin 1 Logic '0', Output Disabled	-	-	200	ns
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	15	µA
Enable Time	T_{PLZ}	Pin 1 Logic '1', Output Enabled	-	-	4	ms
Phase Jitter, RMS	tjrms	40MHz - 220MHz, Bandwidth 12kHz to 20MHz	-	300	500	fs
		6MHz - 39.999MHz, Bandwidth 12kHz to 5MHz	-	-	<1	ps

Enable Truth Table

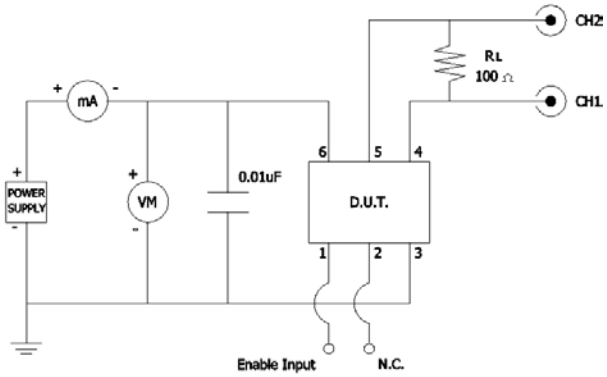
Pin 1	Pin 4 & Pin 5
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

Test Circuit

LVPECL

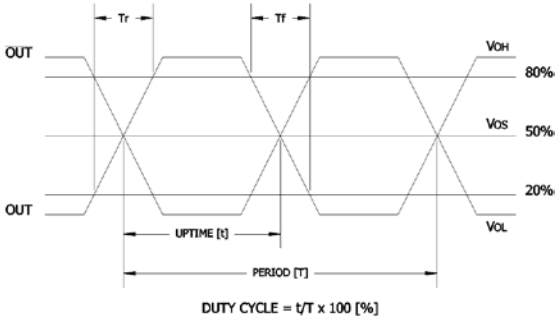


LVDS



Output Waveform

LVPECL or LVDS

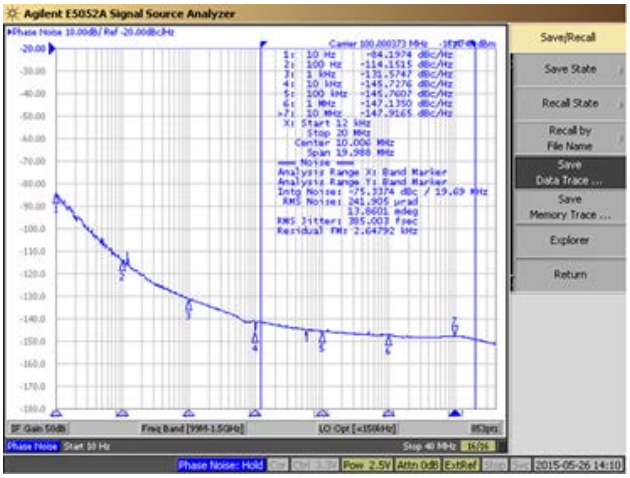


Electrical Specifications

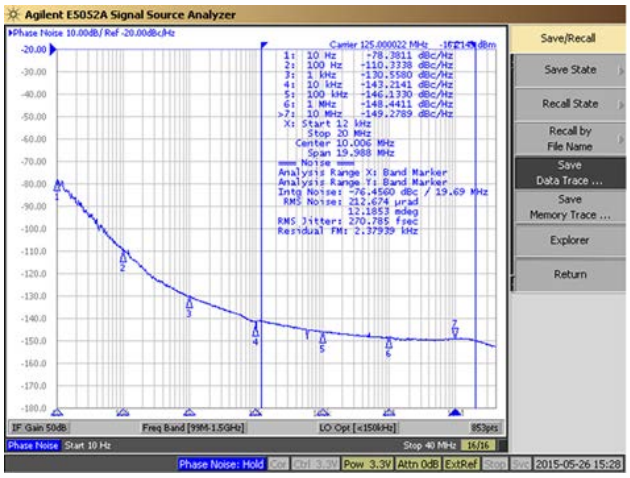
Performance Data

Phase Noise [typical]

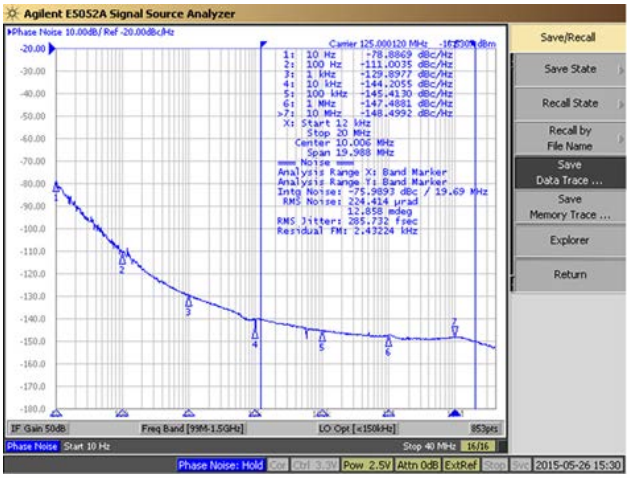
100MHz, LVDS, V_{CC} = +2.5V, T_A = +25°C



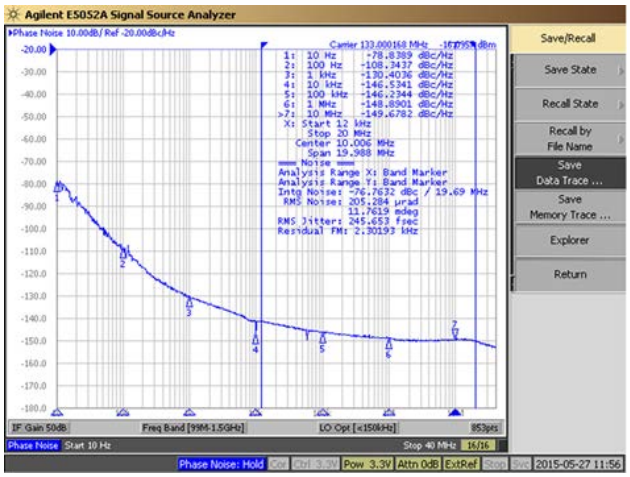
125MHz, LVDS, V_{CC} = +3.3V, T_A = +25°C



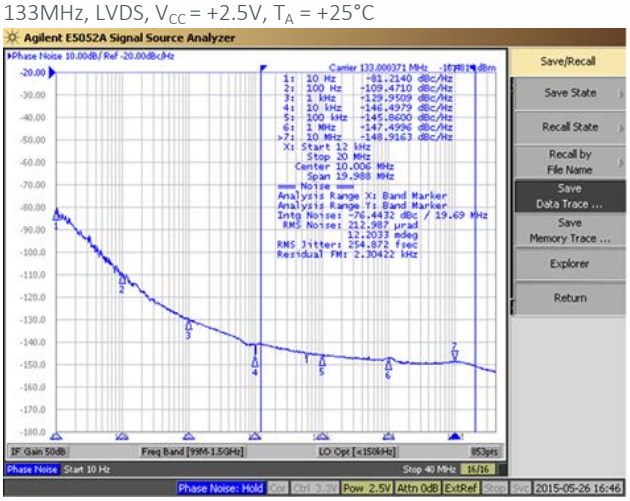
125MHz, LVDS, V_{CC} = +2.5V, T_A = +25°C



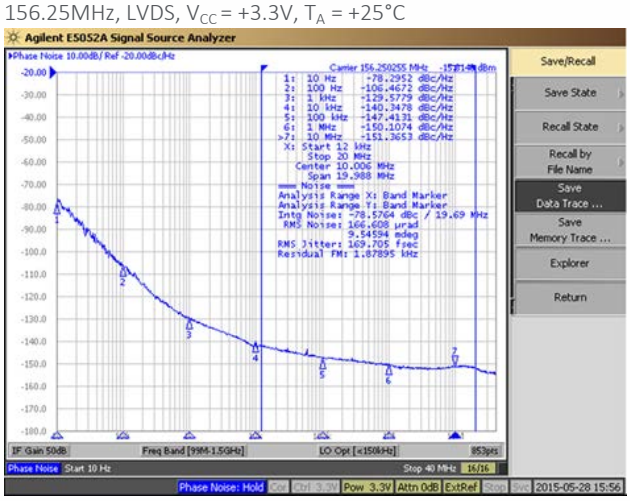
133MHz, LVDS, V_{CC} = +3.3V, T_A = +25°C



133MHz, LVDS, V_{CC} = +2.5V, T_A = +25°C



156.25MHz, LVDS, V_{CC} = +3.3V, T_A = +25°C

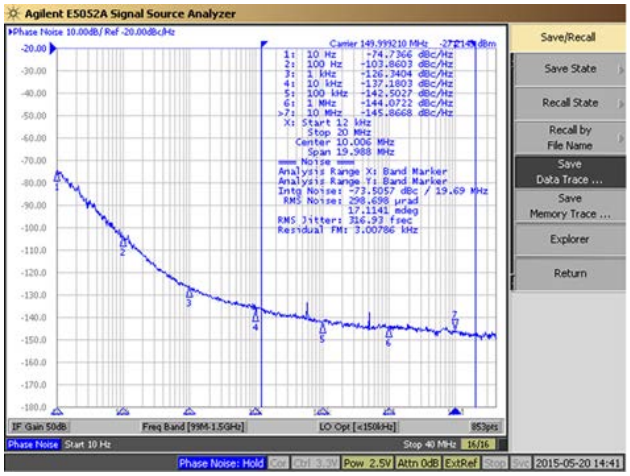


Electrical Specifications

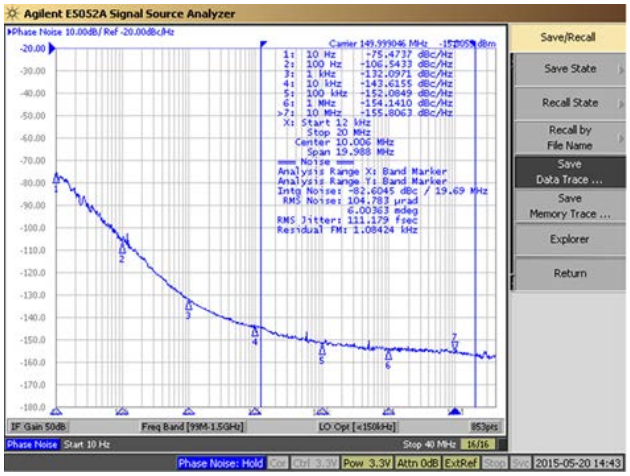
Performance Data

Phase Noise [typical]

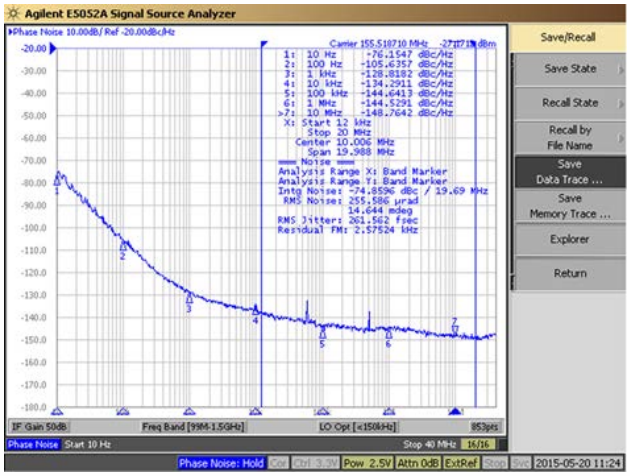
150MHz, LVPECL, V_{CC} = +2.5V, T_A = +25°C



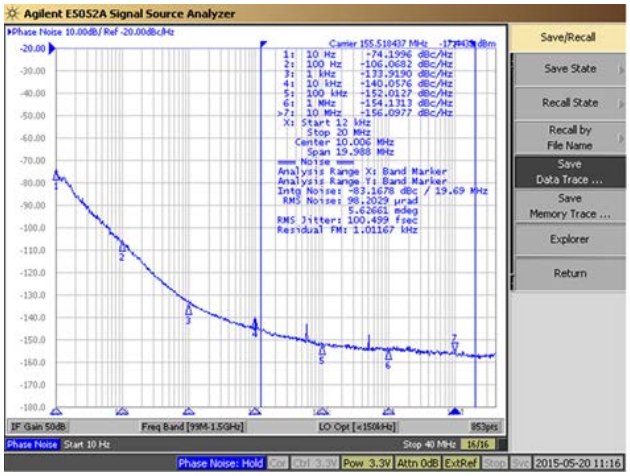
150MHz, LVPECL, V_{CC} = +3.3V, T_A = +25°C



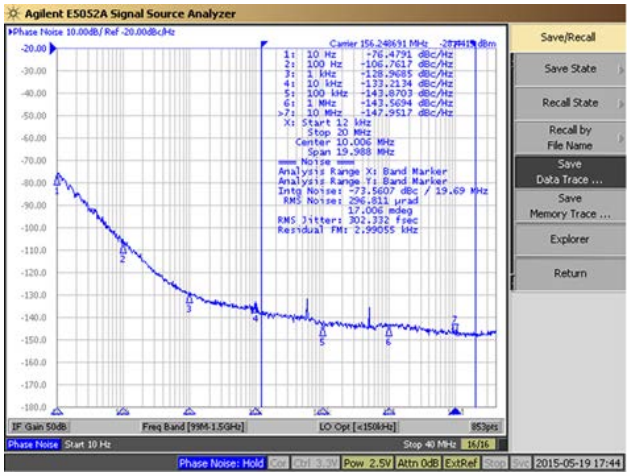
155.52MHz, LVPECL, V_{CC} = +2.5V, T_A = +25°C



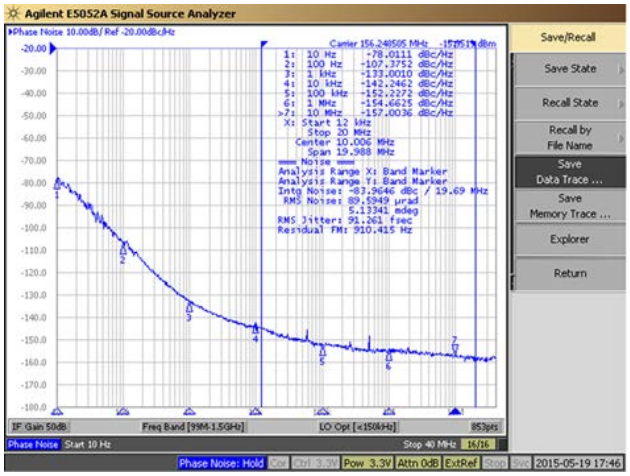
155.52MHz, LVPECL, V_{CC} = +3.3V, T_A = +25°C



156.25MHz, LVPECL, V_{CC} = +2.5V, T_A = +25°C



156.25MHz, LVPECL, V_{CC} = +3.3V, T_A = +25°C



Electrical Specifications

Phase Noise Tabulated - LVDS

Typical, V_{CC} = +2.5V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 100.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-84.20	
		@ 100Hz	-114.15	
		@ 1kHz	-131.57	
	-	@ 10kHz	-145.73	dBc/Hz
		@ 100kHz	-145.76	
		@ 1MHz	-147.14	
		@ 10MHz	-147.92	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	385.00	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 125.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-78.89	
		@ 100Hz	-111.00	
		@ 1kHz	-129.90	
	-	@ 10kHz	-144.21	dBc/Hz
		@ 100kHz	-145.41	
		@ 1MHz	-147.49	
		@ 10MHz	-148.50	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	285.73	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 133.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-81.21	
		@ 100Hz	-109.47	
		@ 1kHz	-129.95	
	-	@ 10kHz	-146.50	dBc/Hz
		@ 100kHz	-145.86	
		@ 1MHz	-147.50	
		@ 10MHz	-148.92	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	254.87	fs

Typical, V_{CC} = +3.3V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 125.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-78.38	
		@ 100Hz	-110.33	
		@ 1kHz	-130.56	
	-	@ 10kHz	-143.21	dBc/Hz
		@ 100kHz	-146.13	
		@ 1MHz	-148.44	
		@ 10MHz	-149.28	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	270.79	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 133.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-78.84	
		@ 100Hz	-108.34	
		@ 1kHz	-130.40	
	-	@ 10kHz	-146.53	dBc/Hz
		@ 100kHz	-146.23	
		@ 1MHz	-148.89	
		@ 10MHz	-149.68	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	245.65	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVDS @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-78.30	
		@ 100Hz	-106.47	
		@ 1kHz	-129.58	
	-	@ 10kHz	-140.35	dBc/Hz
		@ 100kHz	-147.41	
		@ 1MHz	-150.11	
		@ 10MHz	-151.37	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	169.71	fs

Electrical Specifications

Phase Noise Tabulated - LVPECL

Typical, V_{CC} = +2.5V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 150.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-74.74	
		@ 100Hz	-103.86	
		@ 1kHz	-126.34	
	-	@ 10kHz	-137.18	dBc/Hz
		@ 100kHz	-142.50	
		@ 1MHz	-144.07	
		@ 10MHz	-145.87	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	316.93	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 155.52MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-76.15	
		@ 100Hz	-105.64	
		@ 1kHz	-128.82	
	-	@ 10kHz	-134.29	dBc/Hz
		@ 100kHz	-144.64	
		@ 1MHz	-144.53	
		@ 10MHz	-148.76	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	261.56	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-76.48	
		@ 100Hz	-106.76	
		@ 1kHz	-128.97	
	-	@ 10kHz	-133.21	dBc/Hz
		@ 100kHz	-143.87	
		@ 1MHz	-143.57	
		@ 10MHz	-147.95	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	302.33	fs

Typical, V_{CC} = +3.3V, T_A = +25°C

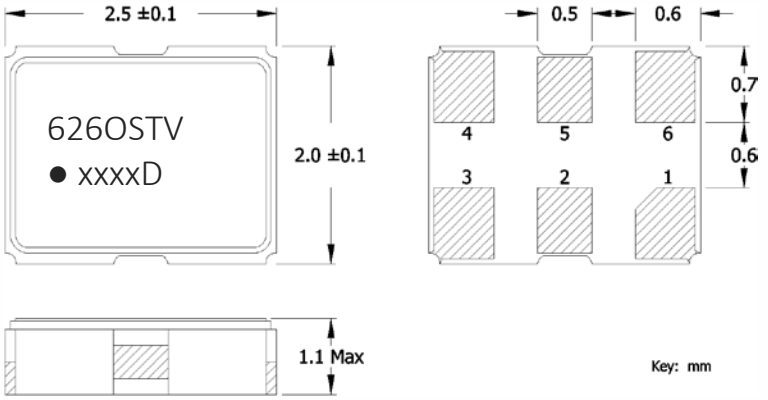
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 150.00MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-75.47	
		@ 100Hz	-106.54	
		@ 1kHz	-132.10	
	-	@ 10kHz	-143.62	dBc/Hz
		@ 100kHz	-152.08	
		@ 1MHz	-154.14	
		@ 10MHz	-155.81	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	383.70	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 155.52MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-74.20	
		@ 100Hz	-106.07	
		@ 1kHz	-133.92	
	-	@ 10kHz	-140.06	dBc/Hz
		@ 100kHz	-152.01	
		@ 1MHz	-154.13	
		@ 10MHz	-156.10	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	100.50	fs

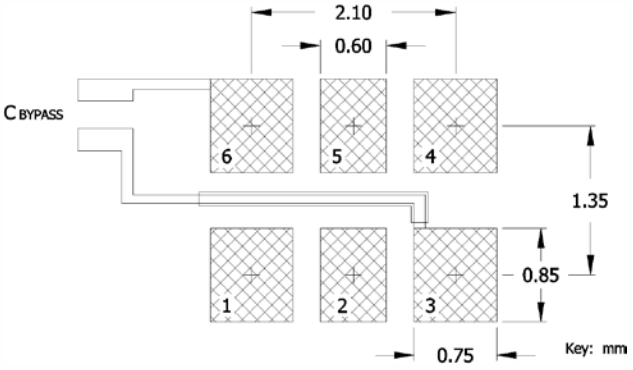
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
LVPECL @ 156.25MHz				
Phase Noise		Single Side Band		
		@ 10Hz	-78.01	
		@ 100Hz	-107.38	
		@ 1kHz	-133.00	
	-	@ 10kHz	-142.25	dBc/Hz
		@ 100kHz	-152.23	
		@ 1MHz	-154.66	
		@ 10MHz	-157.00	
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	91.26	fs

Mechanical Specifications

Package Drawing



Recommended Pad Layout



Marking Information

Preferred

1. O – Output Type; P = LVPECL, L = LVDS.
2. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
3. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
4. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater

[See document 016-1454-0, Frequency Code Tables.]

5. D – Date Code. See Table I for codes.

[Note: Manufacturing site code must appear on reel and carton labels.]

Optional

1. O – Output Type; P = LVPECL, L = LVDS.
2. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
3. xxxx – Frequency Code.
   3-digits, frequencies below 100MHz
   4-digits, frequencies 100MHz or greater

[See document 016-1454-0, Frequency Code Tables.]

4. D – Date Code. See Table I for codes.

[Note: Manufacturing site code must appear on reel and carton labels.]

626OST
● xxxxD

Pin Assignments

Pin	Symbol	Function
1	EOH	Enable
2	N.C.	No Connect
3	GND	Circuit & Package Ground
4	Output	RF Output
5	$\overline{\text{Output}}$	Complimentary RF Output
6	V_{CC}	Supply Voltage

Notes

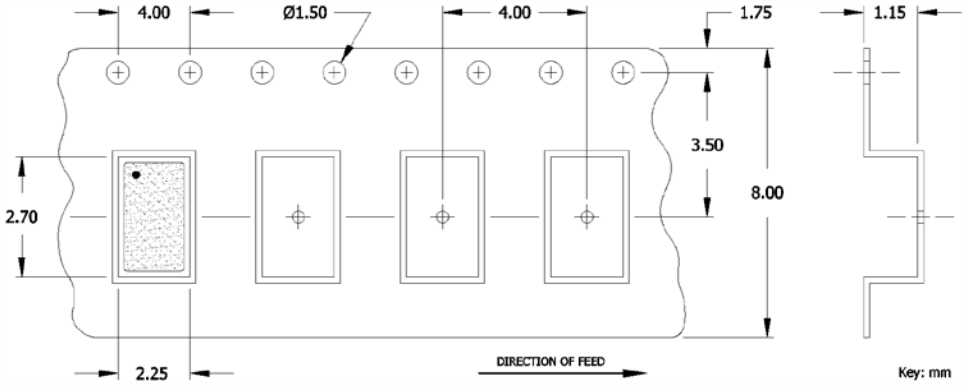
1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

Table I - Date Code

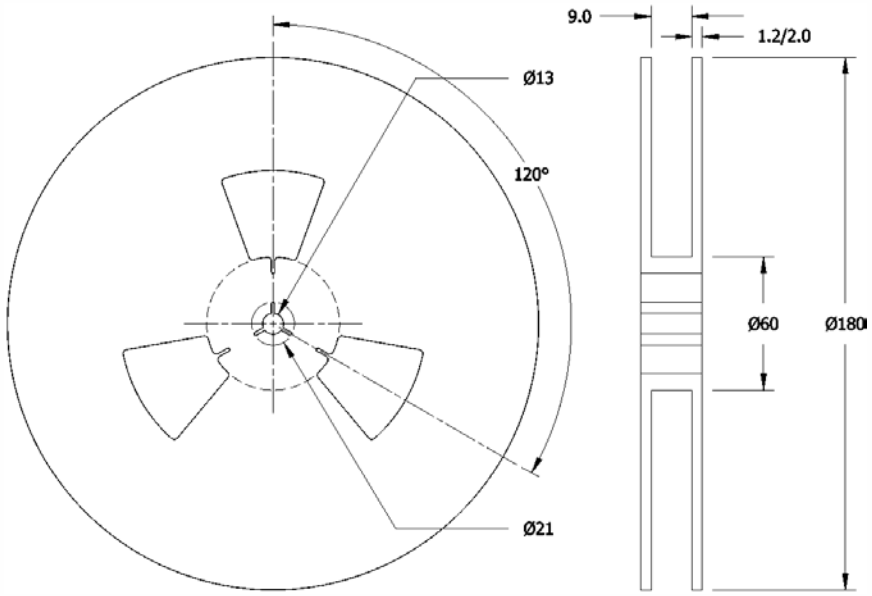
YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces minimum or 3k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

Addendum

Additional Developed Frequencies – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
10.000000	100	156.269530	156G				
19.440000	194						
40.000000	400						
44.736000	447						
77.760000	777						
133.000000	1330						
150.000000	1500						
156.253900	156E						
156.257812	156H						
156.258750	156J						

Frequency Codes for Cover Page Table – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	250	100.000000	1000				
27.000000	270	125.000000	1250				
50.000000	500	155.520000	1555				
74.175800	74A	156.250000	1562				
74.250000	742	161.132800	1611				