12-Cell Battery Stack Monitors

FEATURES

- **Pin-Compatible Upgrade from the LTC6804**
- **Measures Up to 12 Battery Cells in Series**
- **1.2mV Maximum Total Measurement Error**
- **Stackable Architecture for High Voltage Systems**
- **Built-in isoSPI™ Interface**
  - 1Mb Isolated Serial Communications
  - Uses a Single Twisted Pair, up to 100 Meters
  - Low EMI Susceptibility and Emissions
- 290µs to Measure All Cells in a System
- Synchronized Voltage and Current Measurement
- 16-Bit ADC with Programmable Noise Filter
- Engineered for ISO 26262-Compliant Systems
- Passive Cell Balancing with Programmable Timer
- 5 General Purpose Digital I/O or Analog Inputs
  - Temperature or other Sensor Inputs
  - Configurable as an I^2C or SPI master
- 4µA Sleep Mode Supply Current
- 48-Lead SSOP Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Electric and Hybrid Electric Vehicles
- Backup Battery Systems
- Grid Energy Storage
- High Power Portable Equipment

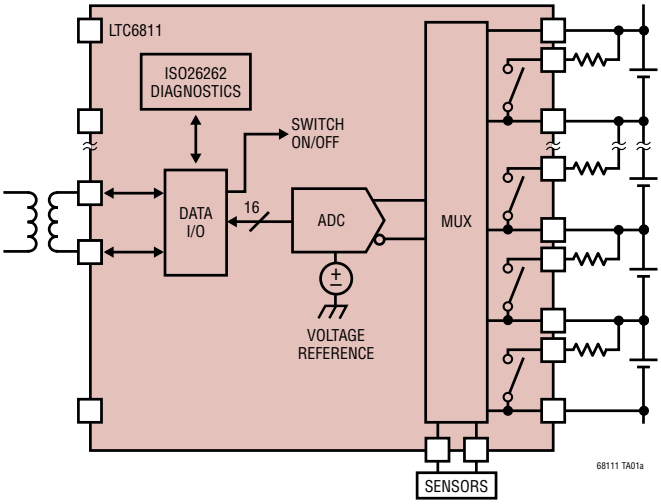
DESCRIPTION

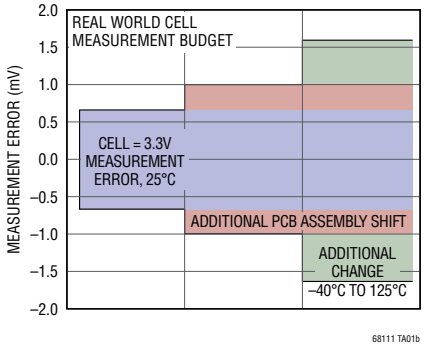
The LTC®6811 is a multicell battery stack monitor that measures up to 12 series connected battery cells with a total measurement error of less than 1.2mV. The cell measurement range of 0V to 5V makes the LTC6811 suitable for most battery chemistries. All 12 cells can be measured in 290µs, and lower data acquisition rates can be selected for high noise reduction.

Multiple LTC6811 devices can be connected in series, permitting simultaneous cell monitoring of long, high voltage battery strings. Each LTC6811 has an isoSPI interface for high speed, RF-immune, long distance communications. Using the LTC6811-1, multiple devices are connected in a daisy chain with one host processor connection for all devices. Using the LTC6811-2, multiple devices are connected in parallel to the host processor, with each device individually addressed.

The LTC6811 can be powered directly from the battery stack or from an isolated supply. The LTC6811 includes passive balancing for each cell, with individual PWM duty cycle control for each cell. Other features include an onboard 5V regulator, five general purpose I/O lines and a sleep mode, where current consumption is reduced to 4µA.

TYPICAL APPLICATION





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ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, V^+ to V^- 75V
Supply Voltage (Relative to C6), V^+ to C6 ..... 50V
Input Voltage (Relative to V^-),
- C0 ..... –0.3V to 0.3V
- C12 ..... –0.3V to MIN(V^+ + 5.5V, 75V)
- C(n) ..... –0.3V to MIN(8 • n, 75V)
- S(n) ..... –0.3V to MIN(8 • n, 75V)
- IPA, IMA, IPB, IMB ..... –0.3V to V_{REG} + 0.3V, ≤6V
- DRIVE ..... –0.3V to 7V
- All Other Pins ..... –0.3V to 6V

Voltage Between Inputs
- C(n) to C(n – 1) ..... –0.3V to 8V
- S(n) to C(n – 1) ..... –0.3V to 8V
- C12 to C9 ..... –0.3V to 21V
- C9 to C6 ..... –0.3V to 21V
- C6 to C3 ..... –0.3V to 21V
- C3 to C0 ..... –0.3V to 21V

Current In/Out of Pins
- All Pins Except V_{REG}, IPA, IMA, IPB, IMB, C(n), S(n) .. 10mA
- IPA, IMA, IPB, IMB 30mA

Operating Temperature Range
- LTC6811I ..... –40°C to 85°C
- LTC6811H ..... –40°C to 125°C

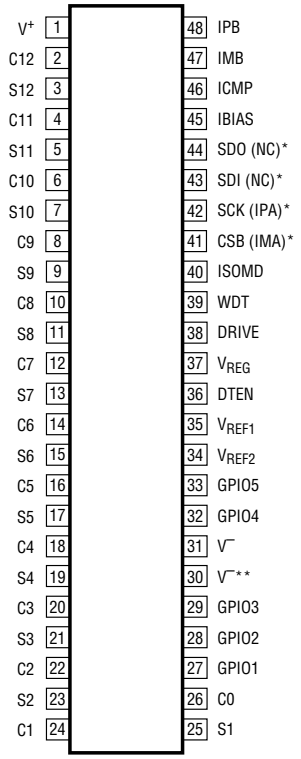
Specified Temperature Range
- LTC6811I ..... –40°C to 85°C
- LTC6811H ..... –40°C to 125°C

Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec) ..... 300°C
Device HBM ESD Classification Level 2
Device CDM ESD Classification Level C5

PIN CONFIGURATION

LTC6811-1

TOP VIEW

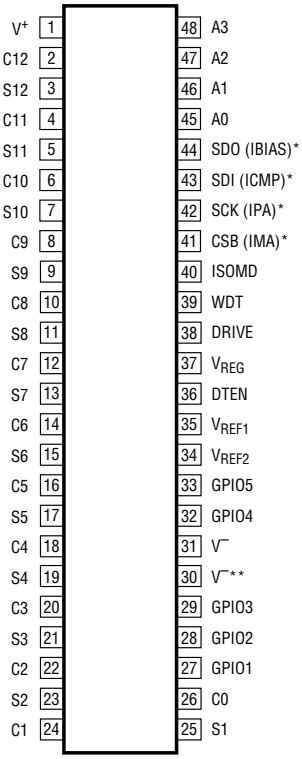


G PACKAGE
48-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 55°C/W
*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, NC, NC
**THIS PIN MUST BE CONNECTED TO V^-

LTC6811-2

TOP VIEW



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48-LEAD PLASTIC SSOP

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*THE FUNCTION OF THESE PINS DEPENDS ON THE CONNECTION OF ISOMD
ISOMD TIED TO V^-: CSB, SCK, SDI, SDO
ISOMD TIED TO V_{REG}: IMA, IPA, NC, NC
**THIS PIN MUST BE CONNECTED TO V^-

ORDER INFORMATION

TUBE (37PC)	TAPE AND REEL (2000PC)	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	SPECIFIED TEMPERATURE RANGE
LTC6811IG-1#PBF	LTC6811IG-1#TRPBF	LTC6811G-1	48-Lead Plastic SSOP	1	–40°C to 85°C
LTC6811HG-1#PBF	LTC6811HG-1#TRPBF	LTC6811G-1	48-Lead Plastic SSOP	1	–40°C to 125°C
LTC6811IG-2#PBF	LTC6811IG-2#TRPBF	LTC6811G-2	48-Lead Plastic SSOP	1	–40°C to 85°C
LTC6811HG-2#PBF	LTC6811HG-2#TRPBF	LTC6811G-2	48-Lead Plastic SSOP	1	–40°C to 125°C
AUTOMOTIVE PRODUCTS**					
LTC6811IG-1#3ZZPBF	LTC6811IG-1#3ZZTRPBF	LTC6811G-1	48-Lead Plastic SSOP	1	–40°C to 85°C
LTC6811HG-1#3ZZPBF	LTC6811HG-1#3ZZTRPBF	LTC6811G-1	48-Lead Plastic SSOP	1	–40°C to 125°C
LTC6811IG-2#3ZZPBF	LTC6811IG-2#3ZZTRPBF	LTC6811G-2	48-Lead Plastic SSOP	1	–40°C to 85°C
LTC6811HG-2#3ZZPBF	LTC6811HG-2#3ZZTRPBF	LTC6811G-2	48-Lead Plastic SSOP	1	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #3ZZ suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. The test conditions are V^+ = 39.6V, V_{REG} = 5.0V unless otherwise noted. The ISOMD pin is tied to the V^- pin, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC Specifications							
	Measurement Resolution				0.1		mV/bit
	ADC Offset Voltage	(Note 2)			0.1		mV
	ADC Gain Error	(Note 2)			0.01		%
	Total Measurement Error (TME) in Normal Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±0.2		mV
		C(n) to C(n – 1) = 2.0			±0.1	±0.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±1.4	mV
		C(n) to C(n – 1) = 3.3			±0.2	±1.2	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±2.2	mV
		C(n) to C(n – 1) = 4.2			±0.3	±1.6	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±2.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of All Cells	●		±0.05	±0.25	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.1	±0.25	%
		V_{REF2} Pin	●		±0.02	±0.1	%
		Digital Supply Voltage V_{REGD}	●		±0.1	±1	%

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Total Measurement Error (TME) in Filtered Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±0.1		mV
		C(n) to C(n – 1) = 2.0			±0.1	±0.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±1.4	mV
		C(n) to C(n – 1) = 3.3			±0.2	±1.2	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±2.2	mV
		C(n) to C(n – 1) = 4.2			±0.3	±1.6	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±2.8	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±1		mV
		Sum of All Cells	●		±0.05	±0.25	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.1	±0.25	%
		V_{REF2} Pin	●		±0.02	±0.1	%
		Digital Supply Voltage V_{REGD}	●		±0.1	±1	%
	Total Measurement Error (TME) in Fast Mode	C(n) to C(n – 1), GPIO(n) to V^- = 0			±2		mV
		C(n) to C(n – 1), GPIO(n) to V^- = 2.0	●			±4	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 3.3	●			±4.7	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 4.2	●			±8.3	mV
		C(n) to C(n – 1), GPIO(n) to V^- = 5.0			±10		mV
		Sum of All Cells	●		±0.15	±0.5	%
		Internal Temperature, T = Maximum Specified Temperature			±5		°C
		V_{REG} Pin	●		±0.3	±1	%
		V_{REF2} Pin	●		±0.1	±0.25	%
		Digital Supply Voltage V_{REGD}	●		±0.2	±2	%
	Input Range	C(n), n = 1 to 12	●	C(n – 1)		C(n – 1) + 5	V
		C0	●		0		
		GPIO(n), n = 1 to 5	●	0		5	V
I_L	Input Leakage Current When Inputs Are Not Being Measured (State: Core = STANDBY)	C(n), n = 0 to 12	●		10	±250	nA
		GPIO(n), n = 1 to 5	●		10	±250	nA
	Input Current When Inputs Are Being Measured (State: Core = MEASURE)	C(n), n = 0 to 12			±1		µA
		GPIO(n), n = 1 to 5			±1		µA
	Input Current During Open Wire Detection		●	70	100	130	µA
Voltage Reference Specifications							
V_{REF1}	1st Reference Voltage	V_{REF1} Pin, No Load	●	3.1	3.2	3.3	V
	1st Reference Voltage TC	V_{REF1} Pin, No Load			3		ppm/°C
	1st Reference Voltage Hysteresis	V_{REF1} Pin, No Load			20		ppm
	1st Reference V. Long Term Drift	V_{REF1} Pin, No Load			20		ppm/$\sqrt{khr}$

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{REF2}	2nd Reference Voltage	V_{REF2} Pin, No Load		●	2.995	3	3.005	V
		V_{REF2} Pin, 5k Load to V^-		●	2.995	3	3.005	V
	2nd Reference Voltage TC	V_{REF2} Pin, No Load				10		ppm/°C
	2nd Reference Voltage Hysteresis	V_{REF2} Pin, No Load				100		ppm
	2nd Reference V. Long Term Drift	V_{REF2} Pin, No Load				60		ppm/$\sqrt{khr}$
General DC Specifications								
I_{VP}	V^+ Supply Current (See Figure 1: LTC6811 Operation State Diagram)	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 0V			4.1	7	µA
			V_{REG} = 0V	●		4.1	10	µA
			V_{REG} = 5V			1.9	3	µA
			V_{REG} = 5V	●		1.9	5	µA
		State: Core = STANDBY			8	13	19	µA
				●	6	13	24	µA
		State: Core = REFUP or MEASURE			0.4	0.55	0.75	mA
				●	0.375	0.55	0.775	mA
$I_{REG(CORE)}$	V_{REG} Supply Current (See Figure 1: LTC6811 Operation State Diagram)	State: Core = SLEEP, isoSPI = IDLE	V_{REG} = 5V			2.2	4	µA
			V_{REG} = 5V	●		2.2	6	µA
		State: Core = STANDBY			17	40	67	µA
				●	14	40	70	µA
		State: Core = REFUP			0.2	0.45	0.7	mA
				●	0.15	0.45	0.75	mA
		State: Core = MEASURE			10.8	11.5	12.2	mA
				●	10.7	11.5	12.3	mA
$I_{REG(isoSPI)}$	Additional V_{REG} Supply Current if isoSPI in READY/ACTIVE States Note: ACTIVE State Current Assumes t_{CLK} = 1µs. (Note 3)	LTC6811-2, ISOMD = 1 $R_{B1} + R_{B2}$ = 2K	READY	●	3.6	4.5	5.4	mA
			ACTIVE	●	4.6	5.8	7.0	mA
		LTC6811-1, ISOMD = 0 $R_{B1} + R_{B2}$ = 2K	READY	●	3.6	4.5	5.2	mA
			ACTIVE	●	5.6	6.8	8.1	mA
		LTC6811-1, ISOMD = 1 $R_{B1} + R_{B2}$ = 2K	READY	●	4.0	5.2	6.5	mA
			ACTIVE	●	7.0	8.5	10.5	mA
		LTC6811-2, ISOMD = 1 $R_{B1} + R_{B2}$ = 20K	READY	●	1.0	1.8	2.6	mA
			ACTIVE	●	1.2	2.2	3.2	mA
		LTC6811-1, ISOMD = 0 $R_{B1} + R_{B2}$ = 20K	READY	●	1.0	1.8	2.4	mA
			ACTIVE	●	1.3	2.3	3.3	mA
		LTC6811-1, ISOMD = 1 $R_{B1} + R_{B2}$ = 20K	READY	●	1.6	2.5	3.5	mA
			ACTIVE	●	1.8	3.1	4.8	mA
	V^+ Supply Voltage	TME Specifications Met		●	11	40	55	V
	V^+ to C12 Voltage	TME Specifications Met		●	–0.3			V
	V^+ to C6 Voltage	TME Specifications Met		●			40	V
V_{REG}	V_{REG} Supply Voltage	TME Supply Rejection < 1mV/V		●	4.5	5	5.5	V

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	DRIVE Output Voltage	Sourcing 1µA	 ●	5.4 5.2	5.7 5.7	5.9 6.1	V V
		Sourcing 500µA	●	5.1	5.7	6.1	V
V_{REGD}	Digital Supply Voltage		●	2.7	3	3.6	V
	Discharge Switch ON Resistance	V_{CELL} = 3.6V	●		10	25	Ω
	Thermal Shutdown Temperature				150		°C
$V_{OL(WDT)}$	Watch Dog Timer Pin Low	WDT Pin Sinking 4mA	●			0.4	V
$V_{OL(GPIO)}$	General Purpose I/O Pin Low	GPIO Pin Sinking 4mA (Used as Digital Output)	●			0.4	V
ADC Timing Specifications							
t_{CYCLE} (Figure 3, Figure 4, Figure 6)	Measurement + Calibration Cycle Time When Starting from the REFUP State in Normal Mode	Measure 12 Cells	●	2120	2335	2480	µs
		Measure 2 Cells	●	365	405	430	µs
		Measure 12 Cells and 2 GPIO Inputs	●	2845	3133	3325	µs
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Filtered Mode	Measure 12 Cells	●	183	201.3	213.5	ms
		Measure 2 Cells	●	30.54	33.6	35.64	ms
		Measure 12 Cells and 2 GPIO Inputs	●	244	268.4	284.7	ms
	Measurement + Calibration Cycle Time When Starting from the REFUP State in Fast Mode	Measure 12 Cells	●	1010	1113	1185	µs
		Measure 2 Cells	●	180	201	215	µs
		Measure 12 Cells and 2 GPIO Inputs	●	1420	1564	1660	µs
t_{SKEW1} (Figure 6)	Skew Time. The Time Difference between Cell 12 and GPIO1 Measurements, Command = ADCVAX	Fast Mode	●	176	194	206	µs
		Normal Mode	●	493	543	576	µs
t_{SKEW2} (Figure 3)	Skew Time. The Time Difference between Cell 12 and Cell 1 Measurements, Command = ADCV	Fast Mode	●	211	233	248	µs
		Normal Mode	●	609	670	711	µs
t_{WAKE}	Regulator Startup Time	V_{REG} Generated from DRIVE Pin (Figure 32)	●		200	400	µs
t_{SLEEP} (Figure 1)	Watchdog or Discharge Timer	DTEN Pin = 0 or DCTO[3:0] = 0000	●	1.8	2	2.2	sec
		DTEN Pin = 1 and DCTO[3:0] ≠ 0000		0.5		120	min
t_{REFUP} (Figure 3 for example)	Reference Wake-Up Time. Added to t_{CYCLE} Time when Starting from the STANDBY State. t_{REFUP} = 0 When Starting from Other States.	t_{REFUP} Is Independent of the Number of Channels Measured and the ADC Mode.	●	2.7	3.5	4.4	ms
f_S	ADC Clock Frequency				3.3		MHz
SPI interface DC Specifications							
$V_{IH(SPI)}$	SPI Pin Digital Input Voltage High	Pins CSB, SCK, SDI	●	2.3			V
$V_{IL(SPI)}$	SPI Pin Digital Input Voltage Low	Pins CSB, SCK, SDI	●			0.8	V
$V_{IH(CFG)}$	Configuration Pin Digital Input Voltage High	Pins ISOMD, DTEN, GPIO1 to GPIO5, A0 to A3	●	2.7			V
$V_{IL(CFG)}$	Configuration Pin Digital Input Voltage Low	Pins ISOMD, DTEN, GPIO1 to GPIO5, A0 to A3	●			1.2	V
$I_{LEAK(DIG)}$	Digital Input Current	Pins CSB, SCK, SDI, ISOMD, DTEN, A0 to A3	●			±1	µA
$V_{OL(SDO)}$	Digital Output Low	Pin SDO Sinking 1mA	●			0.3	V

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
isoSPI DC Specifications (see Figure 17)							
V_{BIAS}	Voltage on IBIAS Pin	READY/ACTIVE State IDLE State	● ●	1.9	2.0 0	2.1	V V
I_B	Isolated Interface Bias Current	R_{BIAS} = 2k to 20k	●	0.1		1.0	mA
A_{IB}	Isolated Interface Current Gain	$V_A \le 1.6V$ I_B = 1mA I_B = 0.1mA	● ●	18 18	20 20	22 24.5	mA/mA mA/mA
V_A	Transmitter Pulse Amplitude	$V_A = \lvert V_{IP} - V_{IM} \rvert$	●			1.6	V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
$I_{LEAK(ICMP)}$	Input Leakage Current on ICMP Pin	V_{ICMP} = 0V to V_{REG}	●			±1	µA
$I_{LEAK(IP/IM)}$	Leakage Current on IP and IM Pins	IDLE State, V_{IP} or V_{IM}, 0V to V_{REG}	●			±1	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	$V_{CM} = V_{REG}$ /2 to V_{REG} – 0.2V, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP/IM Not Driving		(V_{REG} – V_{ICMP}/3 – 167mV)			V
R_{IN}	Receiver Input Resistance	Single-Ended to IPA, IMA, IPB, IMB	●	26	35	45	kΩ
isoSPI Idle/Wake-Up Specifications (see Figure 26)							
V_{WAKE}	Differential Wake-Up Voltage	t_{DWELL} = 240ns	●	200			mV
t_{DWELL}	Dwell Time at V_{WAKE} Before Wake Detection	V_{WAKE} = 200mV	●	240			ns
t_{READY}	Startup Time After Wake Detection		●			10	µs
t_{IDLE}	Idle Timeout Duration		●	4.3	5.5	6.7	ms
isoSPI Pulse Timing Specifications (see Figure 24)							
$t_{½PW(CS)}$	Chip-Select Half-Pulse Width	Transmitter	●	120	150	180	ns
$t_{FILT(CS)}$	Chip-Select Signal Filter	Receiver	●	70	90	110	ns
$t_{INV(CS)}$	Chip-Select Pulse Inversion Delay	Transmitter	●	120	155	190	ns
$t_{WNDW(CS)}$	Chip-Select Valid Pulse Window	Receiver	●	220	270	330	ns
$t_{½PW(D)}$	Data Half-Pulse Width	Transmitter	●	40	50	60	ns
$t_{FILT(D)}$	Data Signal Filter	Receiver	●	10	25	35	ns
$t_{INV(D)}$	Data Pulse Inversion Delay	Transmitter	●	40	55	65	ns
$t_{WNDW(D)}$	Data Valid Pulse Window	Receiver	●	70	90	110	ns
SPI Timing Requirements (see Figure 16 and Figure 25)							
t_{CLK}	SCK Period	(Note 4)	●	1			µs
t_1	SDI Setup Time before SCK Rising Edge		●	25			ns
t_2	SDI Hold Time after SCK Rising Edge		●	25			ns
t_3	SCK Low	$t_{CLK} = t_3 + t_4 \ge 1µs$	●	200			ns
t_4	SCK High	$t_{CLK} = t_3 + t_4 \ge 1µs$	●	200			ns
t_5	CSB Rising Edge to CSB Falling Edge		●	0.65			µs
t_6	SCK Rising Edge to CSB Rising Edge	(Note 4)	●	0.8			µs
t_7	CSB Falling Edge to SCK Rising Edge	(Note 4)	●	1			µs

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
isoSPI Timing Specifications (See Figure 25)							
t_8	SCK Falling Edge to SDO Valid	(Note 5)	●			60	ns
t_9	SCK Rising Edge to Short ±1 Transmit		●			50	ns
t_{10}	CSB Transition to Long ±1 Transmit		●			60	ns
t_{11}	CSB Rising Edge to SDO Rising	(Note 5)	●			200	ns
t_{RTN}	Data Return Delay		●	325	375	425	ns
$t_{DSY(CS)}$	Chip-Select Daisy-Chain Delay		●		120	180	ns
$t_{DSY(D)}$	Data Daisy-Chain Delay		●	200	250	300	ns
t_{LAG}	Data Daisy-Chain Lag (vs. Chip-Select)	= $[t_{DSY(D)} + t_{½PW(D)}] - [t_{DSY(CS)} + t_{½PW(CS)}]$	●	0	35	70	ns
$t_{5(GOV)}$	Chip-Select High-to-Low Pulse Governor		●	0.6		0.82	µs
$t_{6(GOV)}$	Data to Chip-Select Pulse Governor		●	0.8		1.05	µs

Note 1: Stresses beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The ADC specifications are guaranteed by the Total Measurement Error specification.

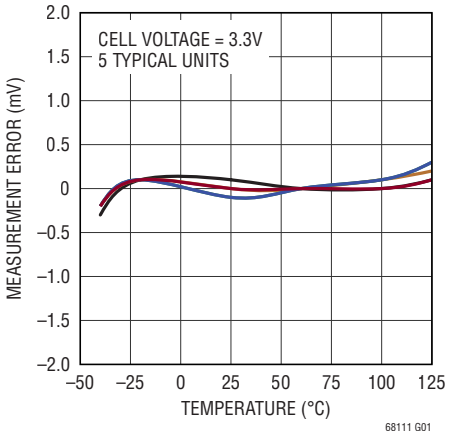
Note 3: The ACTIVE state current is calculated from DC measurements. The ACTIVE state current is the additional average supply current into V_{REG} when there is continuous 1MHz communications on the isoSPI ports with 50% data 1's and 50% data 0's. Slower clock rates reduce the supply current. See Applications Information section for additional details.

Note 4: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

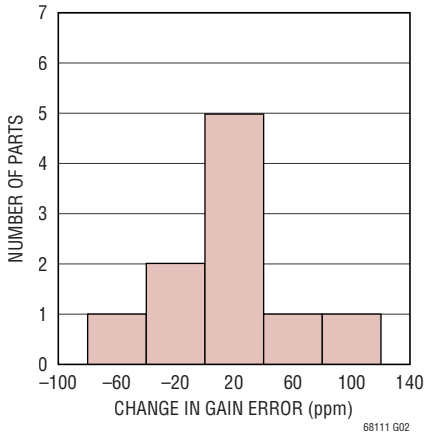
Note 5: These specifications do not include rise or fall time of SDO. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance on the SDO pin. The time constant must be chosen such that SDO meets the setup time requirements of the MCU.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

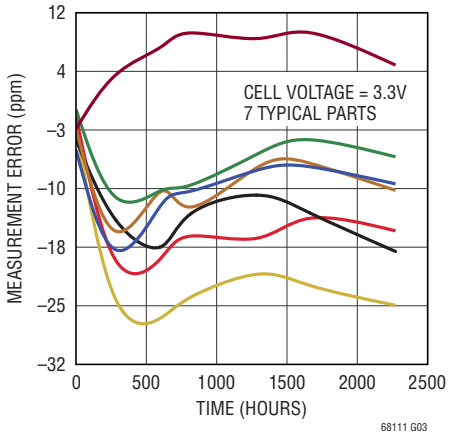
Measurement Error vs Temperature



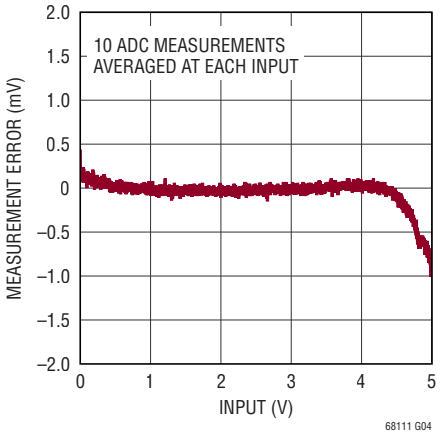
Measurement Error Due to IR Reflow



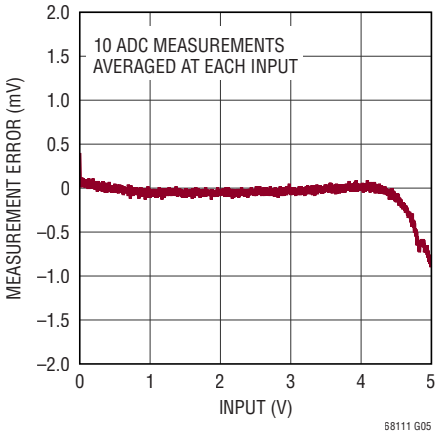
Measurement Error Long-Term Drift



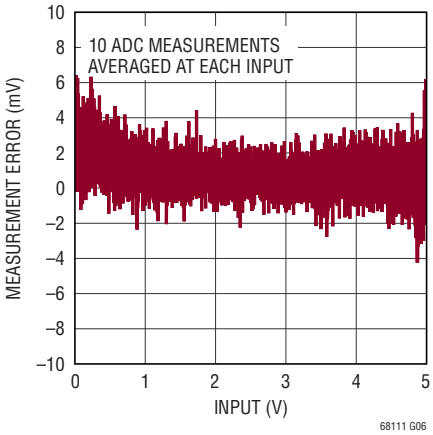
Measurement Error vs Input, Normal Mode



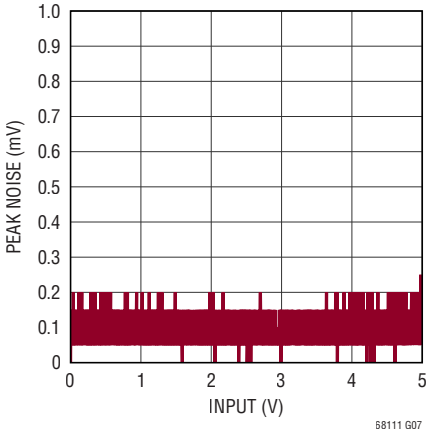
Measurement Error vs Input, Filtered Mode



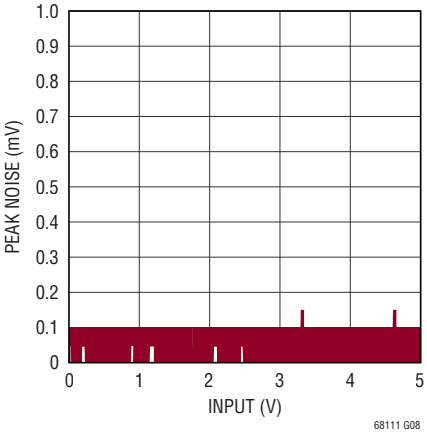
Measurement Error vs Input, Fast Mode



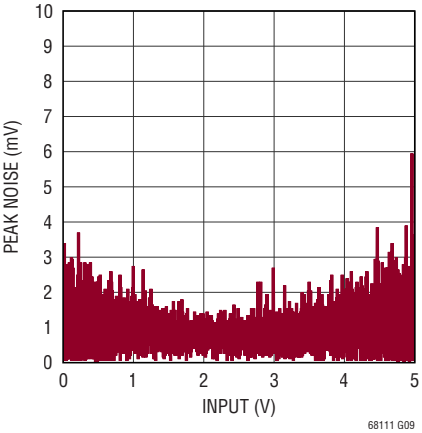
Measurement Noise vs Input, Normal Mode



Measurement Noise vs Input, Filtered Mode

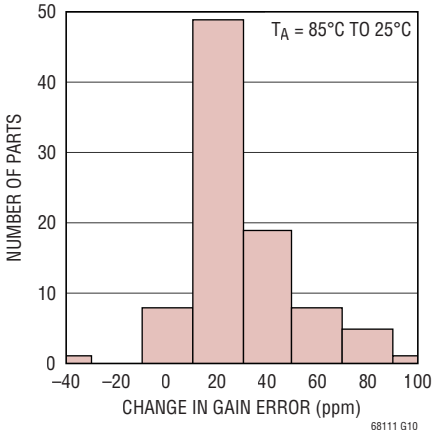


Measurement Noise vs Input, Fast Mode

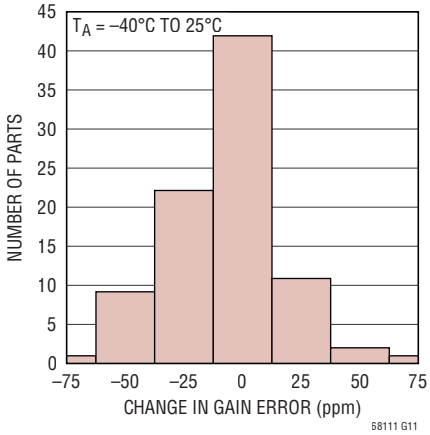


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

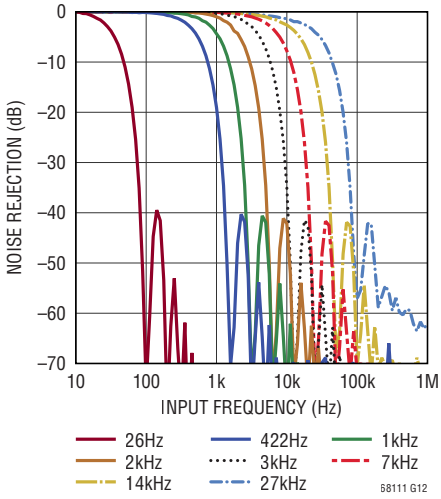
Measurement Gain Error Hysteresis, Hot



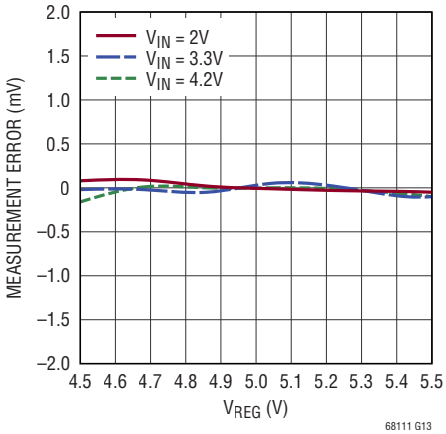
Measurement Gain Error Hysteresis, Cold



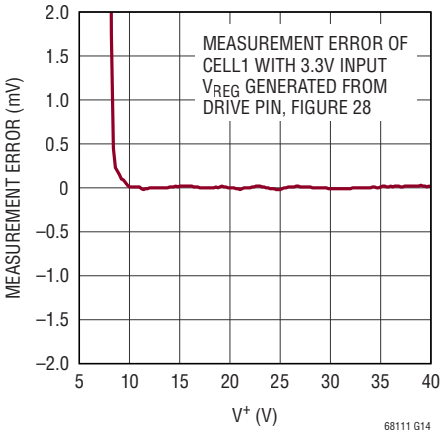
Noise Filter Response



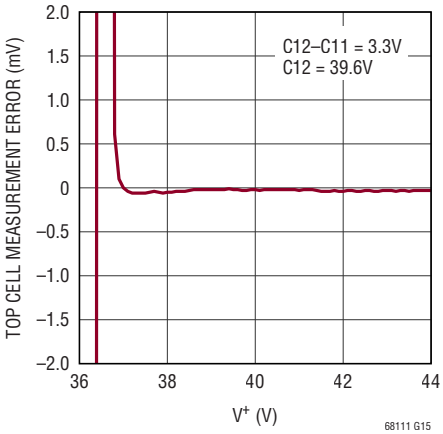
Measurement Error vs V_{REG}



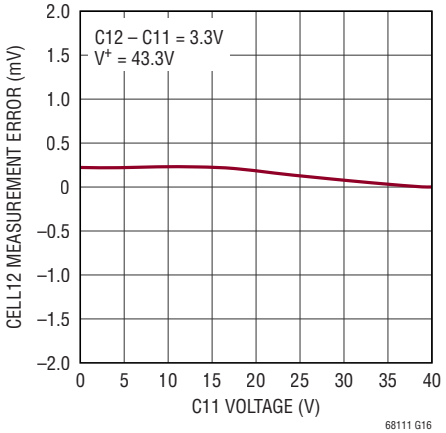
Measurement Error vs V+



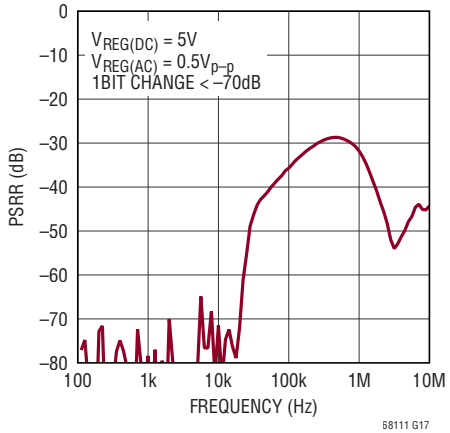
Top Cell Measurement Error vs V+



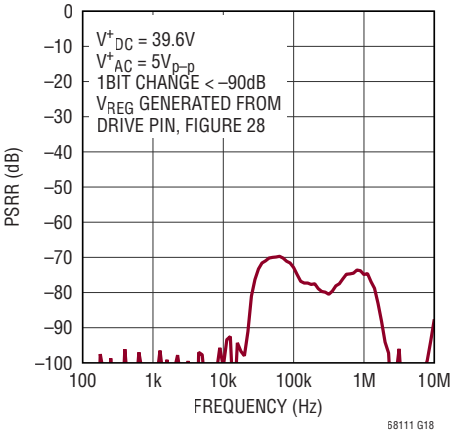
Measurement Error vs Common Mode Voltage



Measurement Error Due to a V_{REG} AC Disturbance



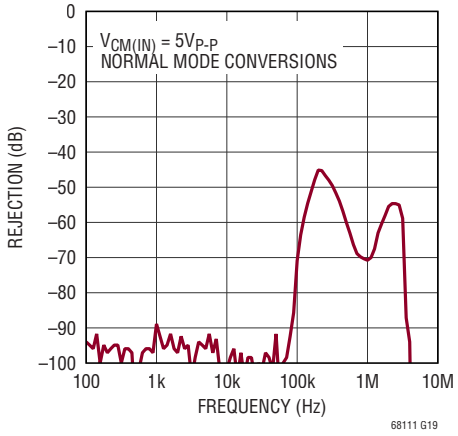
Measurement Error Due to a V+ AC Disturbance



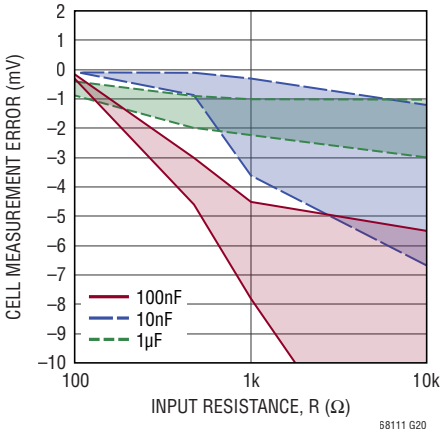
Rev. C

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

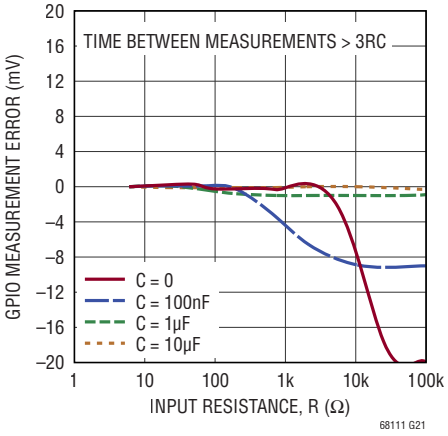
Measurement Error CMRR vs Frequency



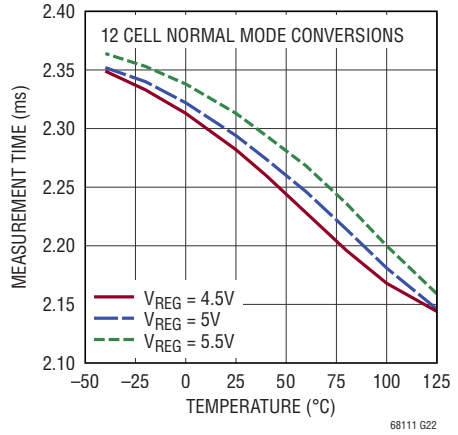
Cell Measurement Error Range vs Input RC Values



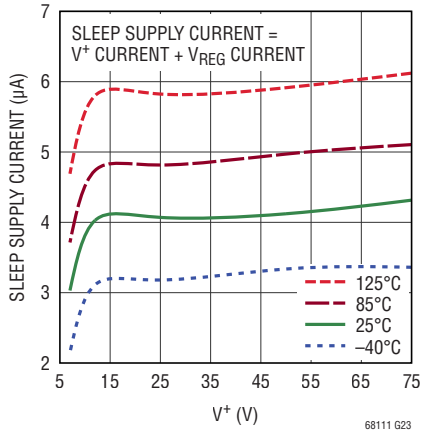
GPIO Measurement Error vs Input RC Values



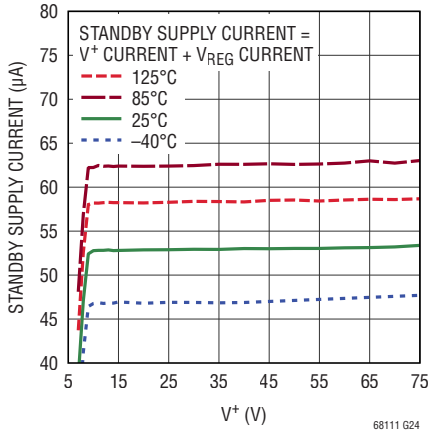
Measurement Time vs Temperature



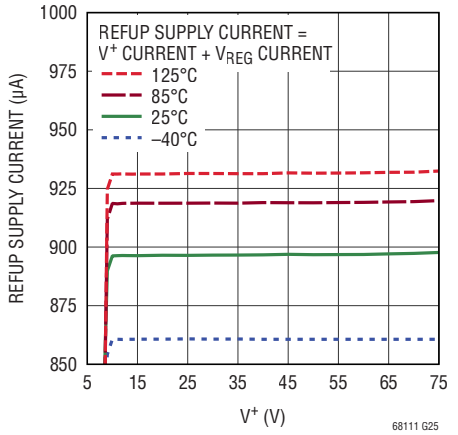
Sleep Supply Current vs V⁺



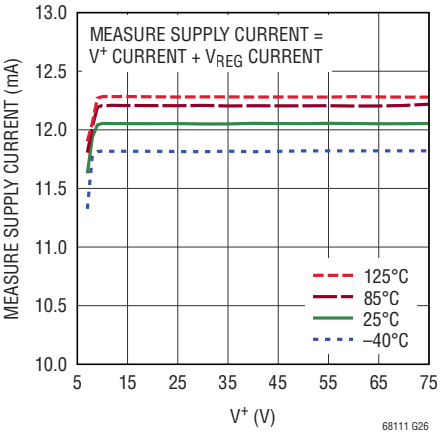
Standby Supply Current vs V⁺



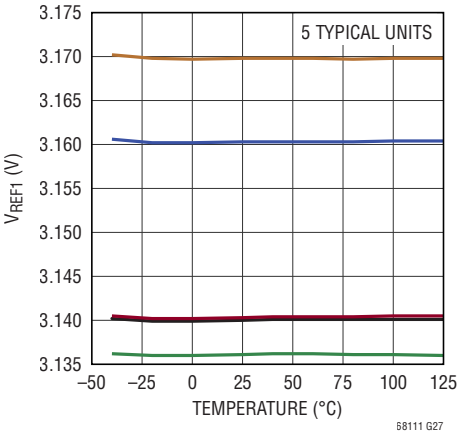
REFUP Supply Current vs V⁺



Measure Supply Current vs V⁺

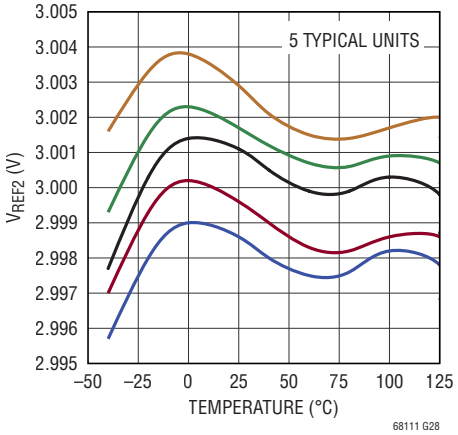


V_{REF1} vs Temperature

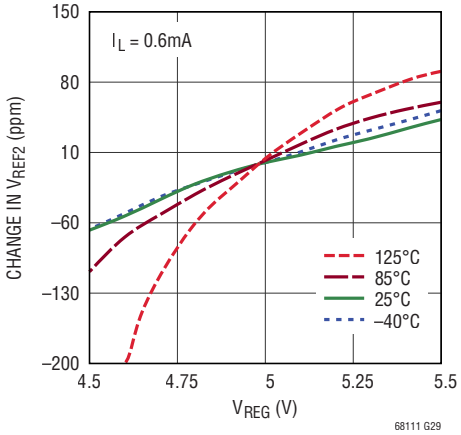


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

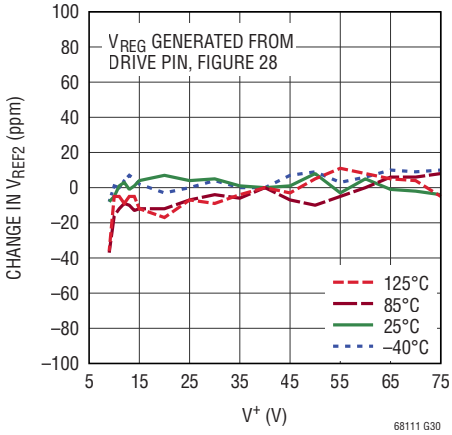
V_{REF2} vs Temperature



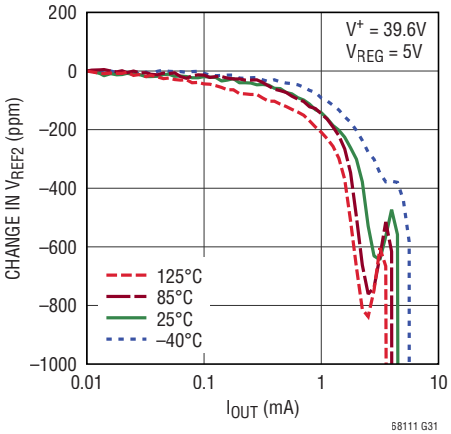
V_{REF2} V_{REG} Line Regulation



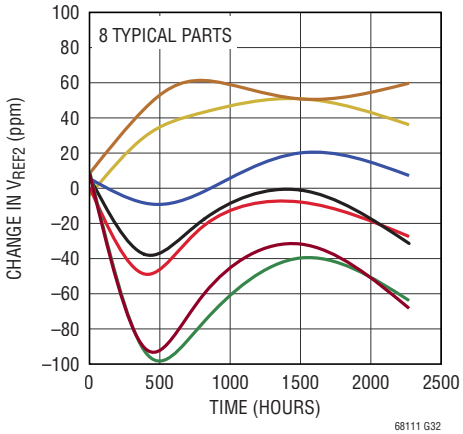
V_{REF2} V^+ Line Regulation



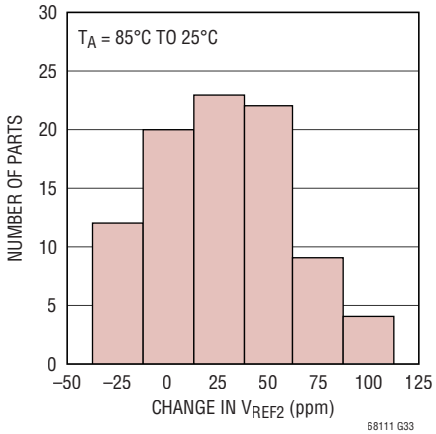
V_{REF2} Load Regulation



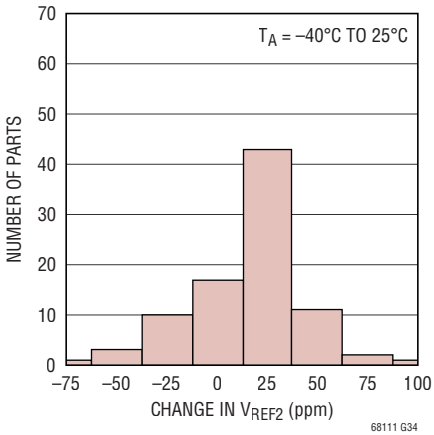
V_{REF2} Long-Term Drift



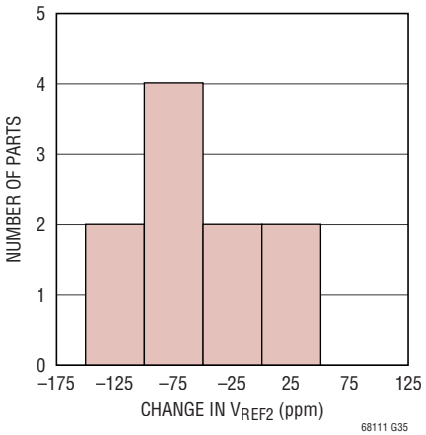
V_{REF2} Hysteresis, Hot



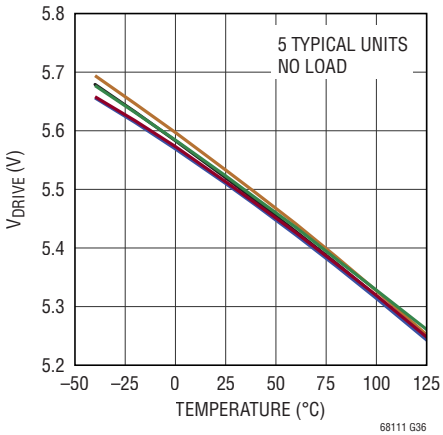
V_{REF2} Hysteresis, Cold



V_{REF2} Change Due to IR Reflow

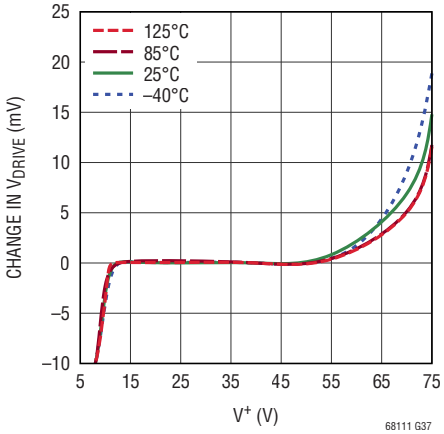


V_{DRIVE} vs Temperature

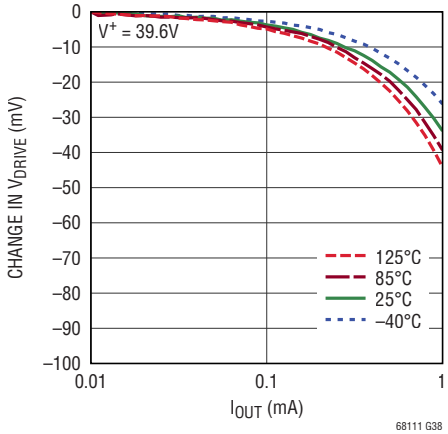


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

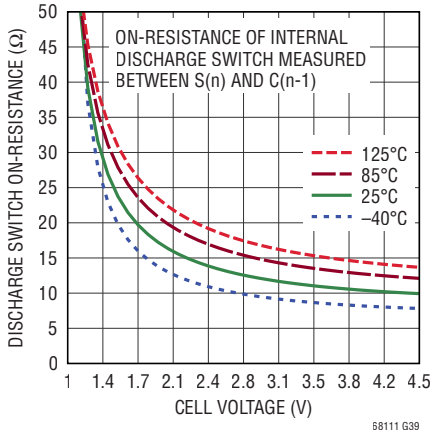
V_{DRIVE} V^+ Line Regulation



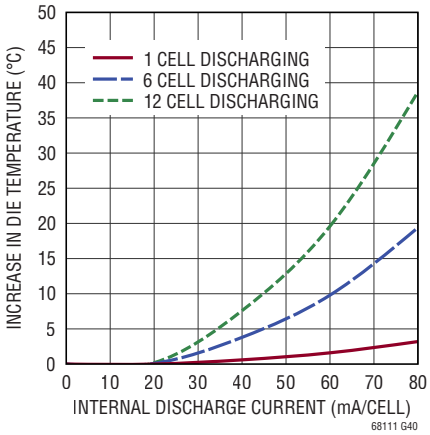
V_{DRIVE} Load Regulation



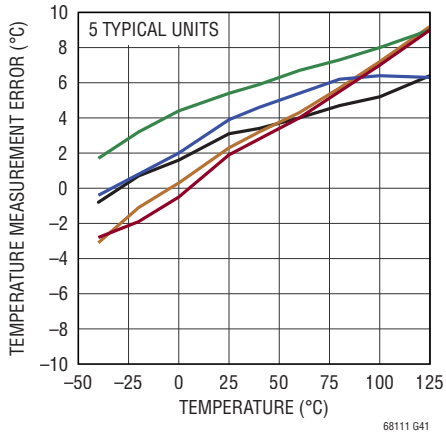
Discharge Switch On-Resistance vs Cell Voltage



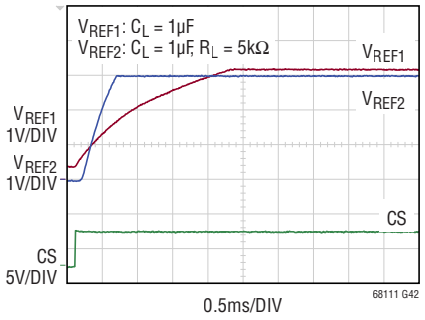
Internal Die Temperature Increase vs Discharge Current



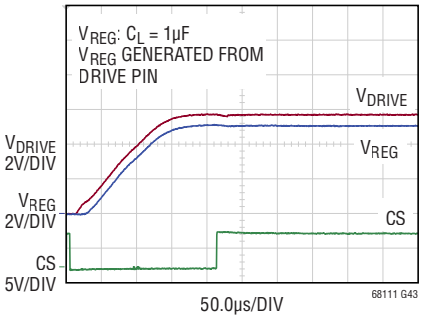
Internal Die Temperature Measurement Error vs Temperature



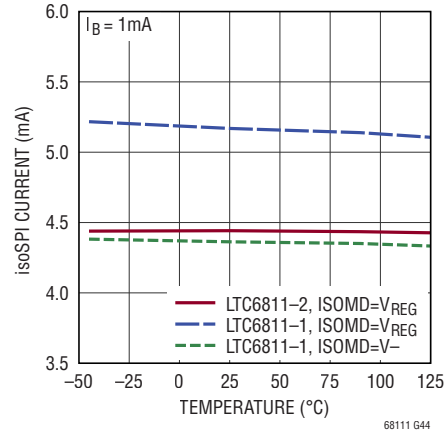
V_{REF1} and V_{REF2} Power-Up



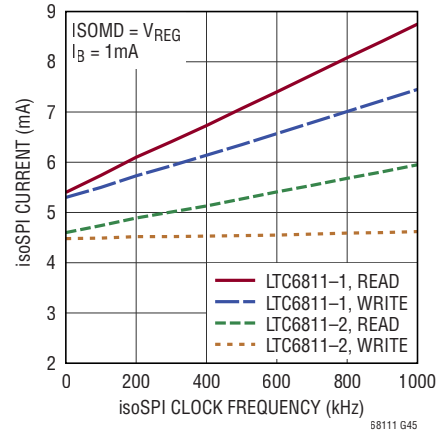
V_{REG} and V_{DRIVE} Power-Up



isoSPI Current (READY) vs Temperature

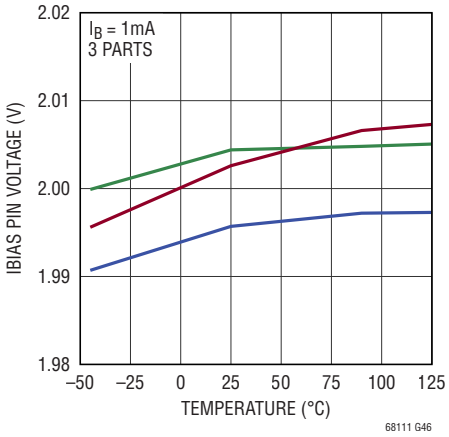


isoSPI Current (ACTIVE) vs isoSPI Clock Frequency

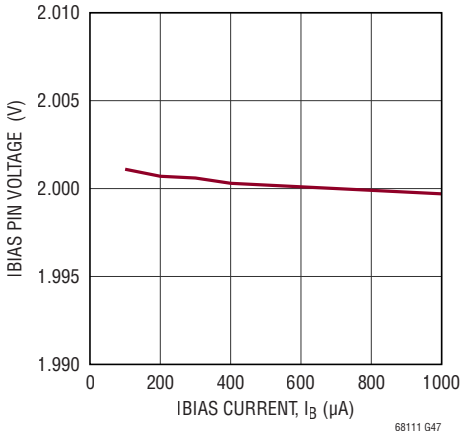


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

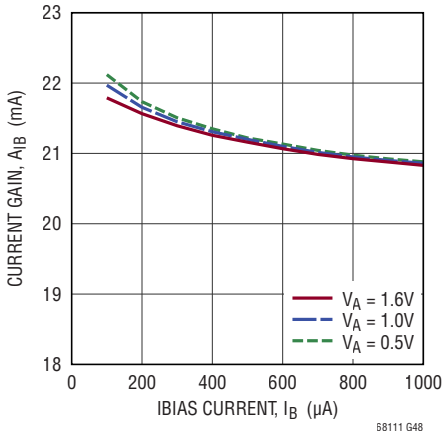
IBIAS Voltage vs Temperature



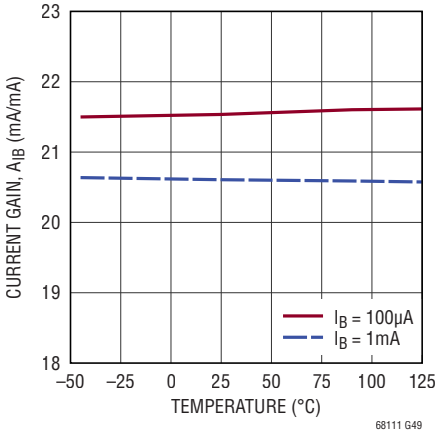
IBIAS Voltage Load Regulation



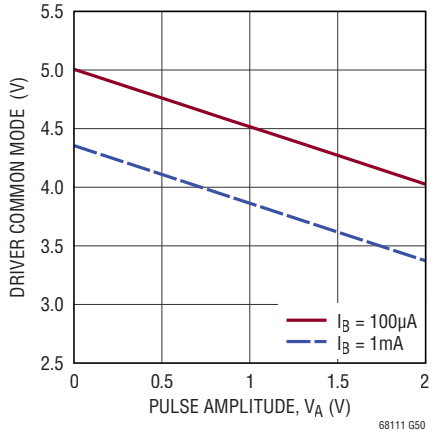
isoSPI Driver Current Gain (Port A/Port B) vs IBIAS Current



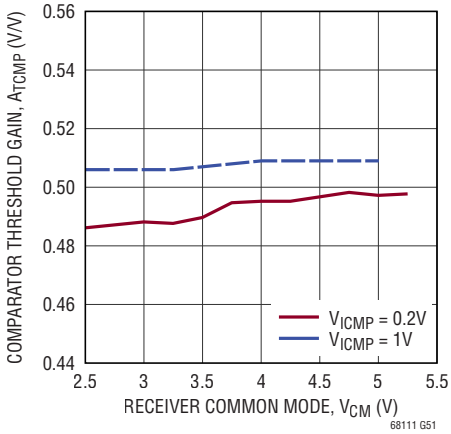
isoSPI Driver Current Gain (Port A/Port B) vs Temperature



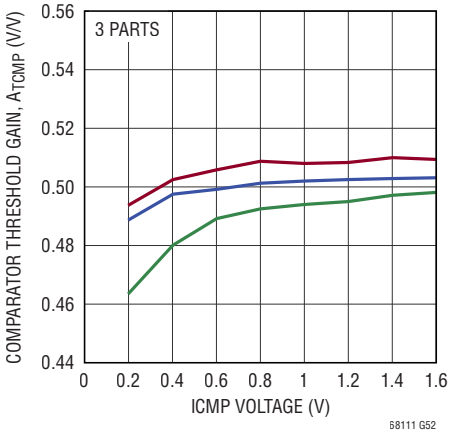
isoSPI Driver Common Mode Voltage (Port A/Port B) vs Pulse Amplitude



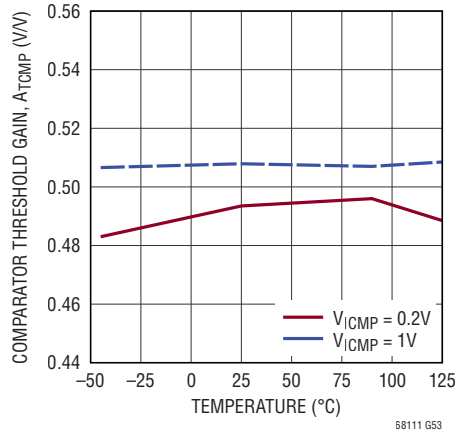
isoSPI Comparator Threshold Gain (Port A/Port B) vs Receiver Common Mode



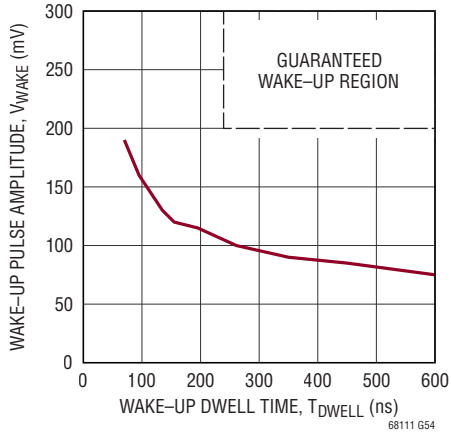
isoSPI Comparator Threshold Gain (Port A/Port B) vs ICMP Voltage



isoSPI Comparator Threshold Gain (Port A/Port B) vs Temperature



Typical Wake-Up Pulse Amplitude (Port A) vs Dwell Time



PIN FUNCTIONS

C0 to C12: Cell Inputs.

S1 to S12: Balance Inputs/Outputs. 12 internal N-MOSFETs are connected between S(n) and C(n – 1) for discharging cells.

V^+: Positive Supply Pin.

V^-: Negative Supply Pins. The V^- pins must be shorted together, external to the IC.

V_{REF2}: Buffered 2nd Reference Voltage for Driving Multiple 10k Thermistors. Bypass with an external 1µF capacitor.

V_{REF1}: ADC Reference Voltage. Bypass with an external 1µF capacitor. No DC loads allowed.

GPIO[1:5]: General Purpose I/O. Can be used as digital inputs or digital outputs, or as analog inputs with a measurement range from V^- to 5V. GPIO[3:5] can be used as an I^2C or SPI port.

DTEN: Discharge Timer Enable. Connect this pin to V_{REG} to enable the discharge timer.

DRIVE: Connect the base of an NPN to this pin. Connect the collector to V^+ and the emitter to V_{REG}.

V_{REG}: 5V Regulator Input. Bypass with an external 1µF capacitor.

ISOMD: Serial Interface Mode. Connecting ISOMD to V_{REG} configures pins 41 to 44 of the LTC6811 for 2-wire isolated interface (isoSPI) mode. Connecting ISOMD to V^- configures the LTC6811 for 4-wire SPI mode.

WDT: Watchdog Timer Output Pin. This is an open drain NMOS digital output. It can be left unconnected or connected with a 1M resistor to V_{REG}. If the LTC6811 does not receive a valid command within 2 seconds, the watchdog timer circuit will reset the LTC6811 and the WDT pin will go high impedance.

Serial Port Pins

	LTC6811-1 (DAISY-CHAINABLE)		LTC6811-2 (ADDRESSABLE)	
	ISOMD = V_{REG}	**ISOMD = V^-**	**ISOMD = V_{REG}**	**ISOMD = V^-**
PORT B (Pins 45 to 48)	IPB	IPB	A3	A3
	IMB	IMB	A2	A2
	ICMP	ICMP	A1	A1
	IBIAS	IBIAS	A0	A0
PORT A (Pins 41 to 44)	(NC)	SDO	IBIAS	SDO
	(NC)	SDI	ICMP	SDI
	IPA	SCK	IPA	SCK
	IMA	CSB	IMA	CSB

CSB, SCK, SDI, SDO: 4-Wire Serial Peripheral Interface (SPI). Active low chip select (CSB), serial clock (SCK) and serial data in (SDI) are digital inputs. Serial data out (SDO) is an open drain NMOS output pin. SDO requires a 5k pull-up resistor.

A0 to A3: Address Pins. These digital inputs are connected to V_{REG} or V^- to set the chip address for addressable serial commands.

IPA, IMA: Isolated 2-Wire Serial Interface Port A. IPA (plus) and IMA (minus) are a differential input/output pair.

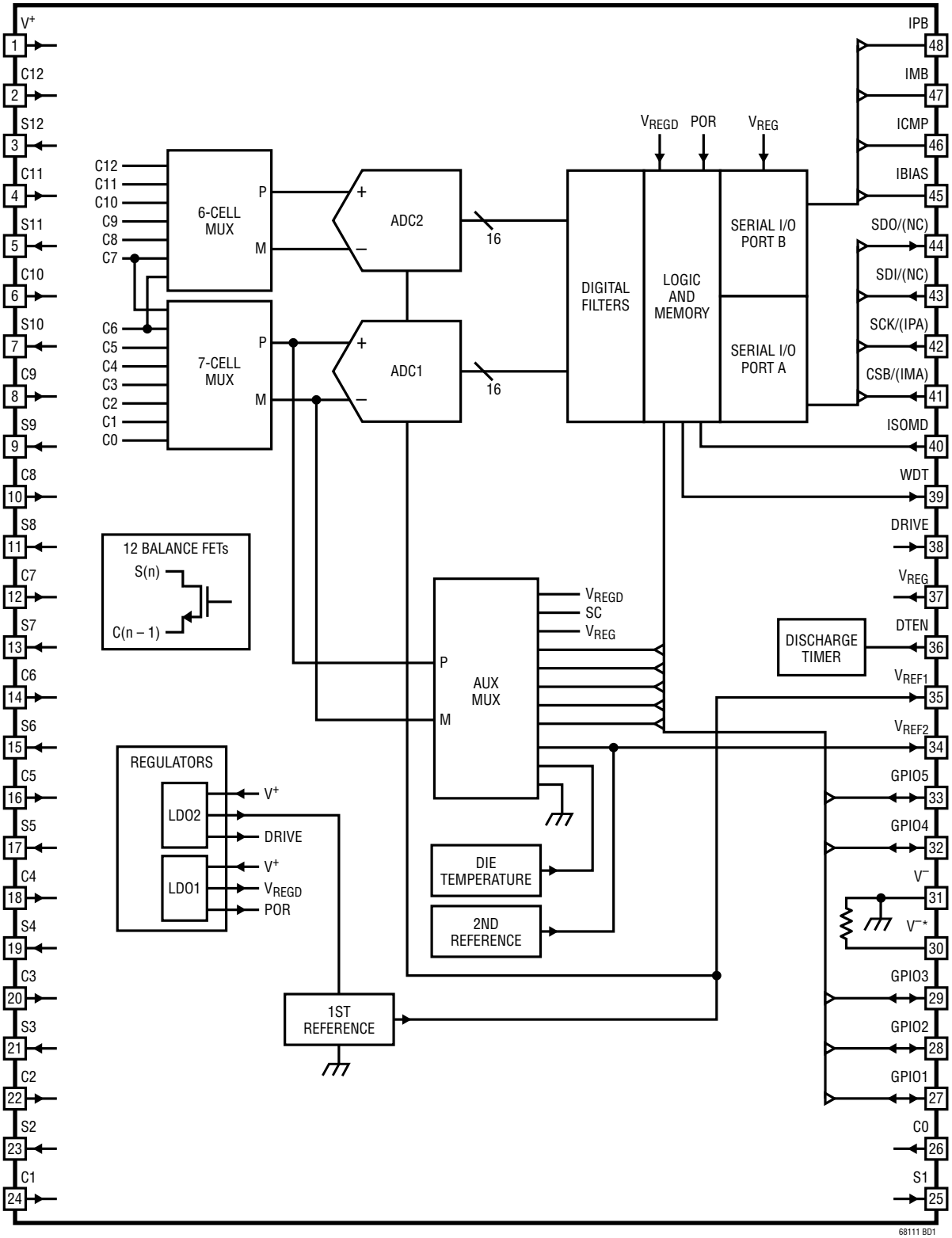
IPB, IMB: Isolated 2-Wire Serial Interface Port B. IPB (plus) and IMB (minus) are a differential input/output pair.

IBIAS: Isolated Interface Current Bias. Tie IBIAS to V^- through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is 2V. The IPA/IMA or IPB/IMB output current drive is set to 20 times the current, I_B, sourced from the IBIAS pin.

ICMP: Isolated Interface Comparator Voltage Threshold Set. Tie this pin to the resistor divider between IBIAS and V^- to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to half the voltage on the ICMP pin.

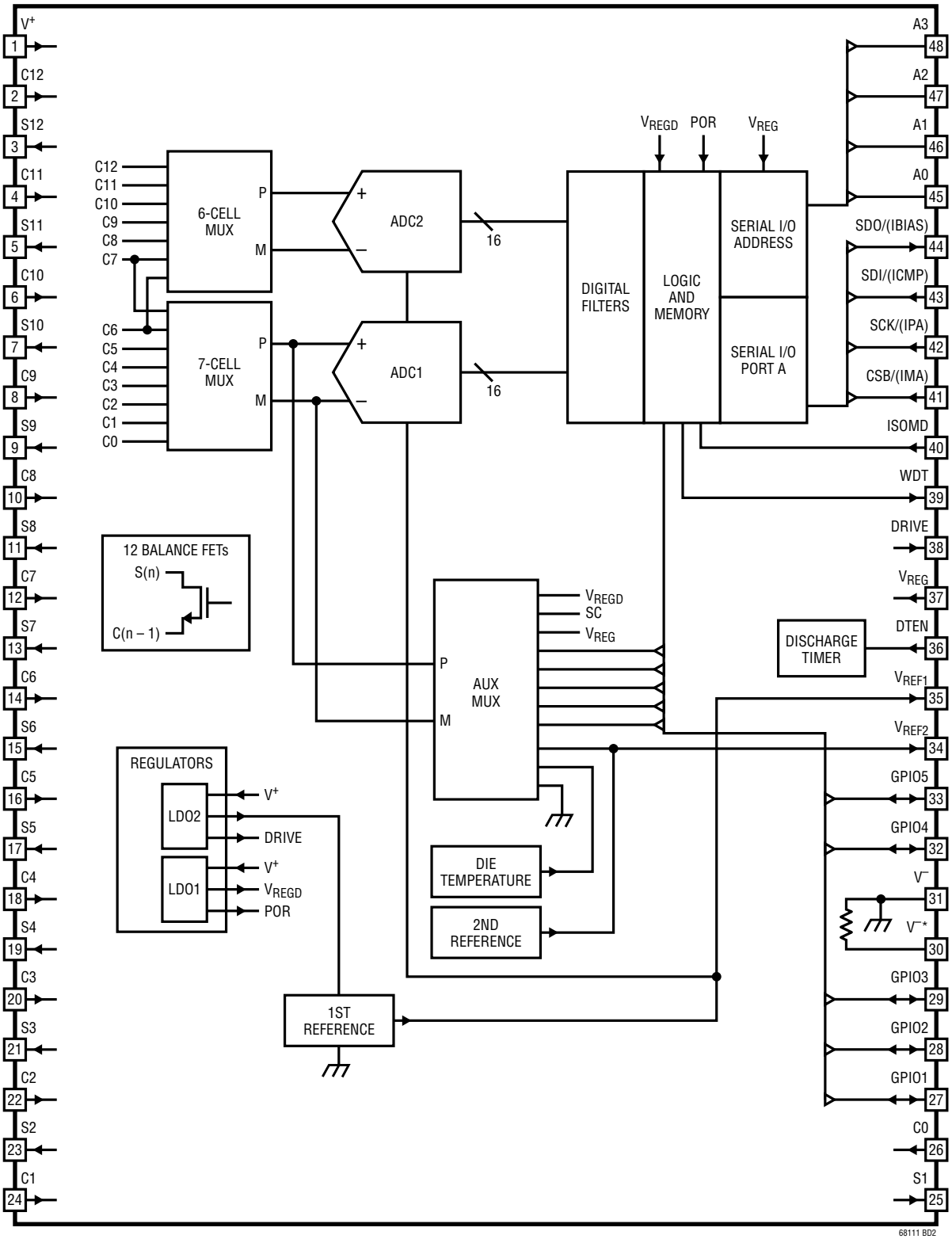
BLOCK DIAGRAM

LTC6811-1



BLOCK DIAGRAM

LTC6811-2



DIFFERENCES BETWEEN THE LTC6804 AND THE LTC6811

The newer LTC6811 is pin compatible and backwards software compatible with the older LTC6804. Users of the LTC6804 should review the following tables of product differences before upgrading existing designs.

Additional LTC6811 Feature	Benefit	Relevant Data Sheet Section(s)
Eight choices of ADC speed vs resolution. The LTC6804 has six choices.	Flexibility for noise filtering.	"ADC Modes" for a description and MD[1,0] Bits in Table 39.
Each discharge control pin (S pin) can have a unique duty cycle.	Improved cell balancing.	"S Pin Pulse Width Modulation for Cell Balancing" for a description and PWMx[x] bits in Table 51.
Measure Cell 7 with both ADCs simultaneously using the ADOL command.	Improved way to check that ADC2 is as accurate as ADC1.	"Overlap Cell Measurement (ADOL Command)"
Sum of All Cells measurement has higher accuracy.	Improved way to check that the individual cell measurements are correct.	"Measuring Internal Device Parameters (ADSTAT Command)"
The new ADCVSC command measures the Sum of All Cells and the individual cells at the same time.	Reduces the influence of noise on the accuracy of the Sum of All Cells measurement.	"Measuring Cell Voltages and Sum of All Cells (ADCVSC Command)"
Auxiliary measurements are processed with 2 digital filters simultaneously.	Checks that the digital filters are free of faults.	"Auxiliary (GPIO) Measurements with Digital Redundancy (ADAXD Command)" and "Measuring Internal Device Parameters with Digital Redundancy (ADSTATD Command)"
The S pin has a stronger PMOS pull-up transistor.	Reduces the possibility that board leakage can turn on discharge circuits.	"Cell Balancing with External Transistors"
The 2nd voltage reference has improved specifications.	Improved V_{REF2} specifications mean improved diagnostics for safety.	"Accuracy Check"
The LTC6811 supports daisy-chain polling.	Easier ADC communications.	"Polling Methods"
Commands to control the LT8584 active balance IC.	Easier to program the LT8584.	"S Pin Pulsing Using the S Control Register Group" for a description and SCTLx[x] bits in Table 50.

LTC6811 Restriction vs. LTC6804	Impact	Relevant Data Sheet Section(s)
The ABS MAX specifications for the C pins have changed.	The ABS MAX voltage between input pins, C(n) to C(n – 1), is 8V for both the LTC6804 and LTC6811. In addition, for the LTC6804, the AVERAGE cell voltage between C(n) and C(n – 1) from pins C12 to C8, C8 to C4 and C4 to C0 must be less than 6.25V. For the LTC6811, the AVERAGE cell voltage between C(n) and C(n – 1) from pins C12 to C9, C9 to C6, C6 to C3 and C3 to C0, must be less than 7.0V.	C12 to C9, C9 to C6, C6 to C3 and C3 to C0 in "Absolute Maximum Ratings"
The ABS MAX specifications for the C pins have changed.	If V^+ is powered from a separate supply (not directly powered from the battery stack), the V^+ supply voltage must be less than (50V + C6). If V^+ is powered from the battery stack (ie. V^+ = C12), this restriction has no impact since the maximum voltage between C6–C12 is already restricted to 42V as noted above.	C12 to C9, C9 to C6, C6 to C3 and C3 to C0 in "Absolute Maximum Ratings"
There is now an Operating Max voltage specification for V^+ to C6.	If V^+ is powered from a separate supply (not directly powered from the battery stack), the V^+ supply voltage must be less than (40V + C6) to achieve the TME specifications listed in the "Electrical Characteristics" table.	V^+ to C6 Voltage in "Electrical Characteristics"

OPERATION

STATE DIAGRAM

The operation of the LTC6811 is divided into two separate sections: the Core circuit and the isoSPI circuit. Both sections have an independent set of operating states, as well as a shutdown timeout.

CORE LTC6811 STATE DESCRIPTIONS

SLEEP State

The references and ADCs are powered down. The watchdog timer (see Watchdog and Discharge Timer) has timed out. The discharge timer is either disabled or timed out. The supply currents are reduced to minimum levels. The isoSPI ports will be in the IDLE state. The Drive pin is 0V. All state machines are reset to their default states.

If a WAKEUP signal is received (see Waking Up the Serial Interface), the LTC6811 will enter the STANDBY state.

STANDBY State

The references and the ADCs are off. The watchdog timer and/or the discharge timer is running. The DRIVE pin powers the V_{REG} pin to 5V through an external transistor. (Alternatively, V_{REG} can be powered by an external supply).

When a valid ADC command is received or the REFON bit is set to 1 in the Configuration Register Group, the IC pauses for t_{REFUP} to allow for the references to power up and then enters either the REFUP or MEASURE state. Otherwise, if no valid commands are received for t_{SLEEP}, the IC returns to the SLEEP state if DTEN = 0 or enters the EXTENDED BALANCING state if DTEN = 1.

REFUP State

To reach this state the REFON bit in the Configuration Register Group must be set to 1 (using the WRCFGA command, see Table 38). The ADCs are off. The references are powered up so that the LTC6811 can initiate ADC conversions more quickly than from the STANDBY state.

When a valid ADC command is received, the IC goes to the MEASURE state to begin the conversion. Otherwise, the LTC6811 will return to the STANDBY state when the REFON bit is set to 0 (using WRCFGA command). If no valid commands are received for t_{SLEEP}, the IC returns to the SLEEP state if DTEN = 0 or enters the EXTENDED BALANCING state if DTEN = 1.

MEASURE State

The LTC6811 performs ADC conversions in this state. The references and ADCs are powered up.

After ADC conversions are complete, the LTC6811 will transition to either the REFUP or STANDBY state, depending on the REFON bit. Additional ADC conversions can be initiated more quickly by setting REFON = 1 to take advantage of the REFUP state.

Note: Non-ADC commands do not cause a Core state transition. Only an ADC conversion or diagnostic commands will place the Core in the MEASURE state.

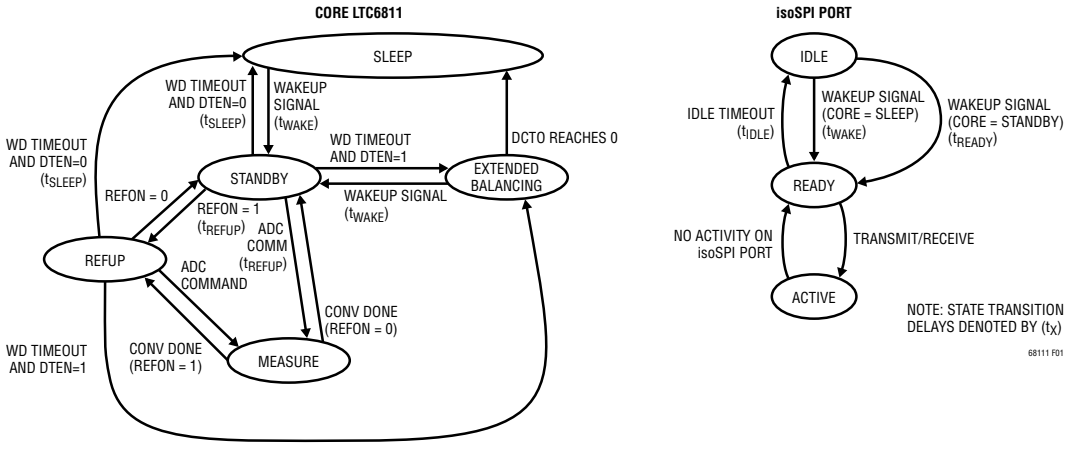


Figure 1. LTC6811 Operation State Diagram

OPERATION

EXTENDED BALANCING State

The watchdog timer has timed out, but the discharge timer has not yet timed out (DTEN = 1). Discharge by PWM may be in progress. If a WAKEUP signal is received, the LTC6811 will transition from EXTENDED BALANCING state to STANDBY state.

isoSPI STATE DESCRIPTIONS

Note: The LTC6811-1 has two isoSPI ports (A and B), for daisy-chain communication. The LTC6811-2 has only one isoSPI port (A), for parallel-addressable communication.

IDLE State

The isoSPI ports are powered down.

When isoSPI Port A receives a WAKEUP signal (see Waking Up the Serial Interface), the isoSPI enters the READY state. This transition happens quickly (within t_{READY}) if the Core is in the STANDBY state because the DRIVE and V_{REG} pins are already biased up. If the Core is in the SLEEP state when the isoSPI receives a WAKEUP signal, the part transitions to the READY state within t_{WAKE}.

READY State

The isoSPI port(s) are ready for communication. Port B is enabled only for LTC6811-1, and is not present on the LTC6811-2. The serial interface current in this state depends on if the part is LTC6811-1 or LTC6811-2, the status of the ISOMD pin and $R_{BIAS} = R_{B1} + R_{B2}$ (the external resistors tied to the IBIAS pin).

If there is no activity (i.e. no WAKEUP signal) on Port A for greater than t_{IDLE} = 5.5ms, the LTC6811 goes to the IDLE state. When the serial interface is transmitting or receiving data the LTC6811 goes to the ACTIVE state.

ACTIVE State

The LTC6811 is transmitting/receiving data using one or both of the isoSPI ports. The serial interface consumes maximum power in this state. The supply current increases with clock frequency as the density of isoSPI pulses increases.

POWER CONSUMPTION

The LTC6811 is powered via two pins: V^+ and V_{REG}. The V^+ input requires voltage greater than or equal to the top cell voltage minus 0.3V, and it provides power to the high voltage elements of the core circuitry. The V_{REG} input requires 5V and provides power to the remaining core circuitry and the isoSPI circuitry. The V_{REG} input can be powered through an external transistor, driven by the regulated DRIVE output pin. Alternatively, V_{REG} can be powered by an external supply.

The power consumption varies according to the operational states. Table 1 and Table 2 provide equations to approximate the supply pin currents in each state. The V^+ pin current depends only on the Core state. However, the V_{REG} pin current depends on both the Core state and isoSPI state, and can therefore be divided into two components. The isoSPI interface draws current only from the V_{REG} pin.

$$I_{REG} = I_{REG(Core)} + I_{REG(isoSPI)}$$

Table 1. Core Supply Current

STATE		I_{VP}	$I_{REG(CORE)}$
SLEEP	V_{REG} = 0V	4.1µA	0µA
	V_{REG} = 5V	1.9µA	2.2µA
STANDBY		13µA	40µA
REFUP		550µA	450µA
MEASURE		550µA	11.5mA

In the SLEEP state the V_{REG} pin will draw approximately 2.2µA if powered by an external supply. Otherwise, the V^+ pin will supply the necessary current.

ADC OPERATION

There are two ADCs inside the LTC6811. The two ADCs operate simultaneously when measuring twelve cells. Only one ADC is used to measure the general purpose inputs. The following discussion uses the term ADC to refer to one or both ADCs, depending on the operation being performed. The following discussion will refer to ADC1 and ADC2 when it is necessary to distinguish between the two circuits, in timing diagrams, for example.

ADC Modes

The ADCOPT bit (CFGR0[0]) in the Configuration Register Group and the mode selection bits MD[1:0] in the conversion command together provide eight modes of operation for the ADC, which correspond to different oversampling ratios (OSR). The accuracy and timing of these modes are summarized in Table 3. In each mode, the ADC first measures the inputs, and then performs a calibration of each channel. The names of the modes are based on the –3dB bandwidth of the ADC measurement.

Table 2. isoSPI Supply Current Equations

isoSPI STATE	DEVICE	ISOMD CONNECTION	$I_{REG(isoSPI)}$
IDLE	LTC6811-1/LTC6811-2	N/A	0mA
READY	LTC6811-1	V_{REG}	$2.2mA + 3 \bullet I_B$
		V^-	$1.5mA + 3 \bullet I_B$
	LTC6811-2	V_{REG}	$1.5mA + 3 \bullet I_B$
		V^-	0mA
ACTIVE	LTC6811-1	V_{REG}	Write: $2.5mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$ Read: $2.5mA + \left(3 + 20 \bullet \frac{100ns \bullet 1.5}{t_{CLK}}\right) \bullet I_B$
		V^-	$1.8mA + \left(3 + 20 \bullet \frac{100ns}{t_{CLK}}\right) \bullet I_B$
	LTC6811-2	V_{REG}	Write: $1.8mA + 3 \bullet I_B$ Read: $1.8mA + \left(3 + 20 \bullet \frac{100ns \bullet 0.5}{t_{CLK}}\right) \bullet I_B$
		V^-	0mA

Note: $I_B = V_{BIAS}/(R_{B1} + R_{B2})$

OPERATION

Table 3. ADC Filter Bandwidth and Accuracy

MODE	–3dB FILTER BW	–40dB FILTER BW	TME SPEC AT 3.3V, 25°C	TME SPEC AT 3.3V,–40°C, 125°C
27kHz (Fast Mode)	27kHz	84kHz	±4.7mV	±4.7mV
14kHz	13.5kHz	42kHz	±4.7mV	±4.7mV
7kHz (Normal Mode)	6.8kHz	21kHz	±1.2mV	±2.2mV
3kHz	3.4kHz	10.5kHz	±1.2mV	±2.2mV
2kHz	1.7kHz	5.3kHz	±1.2mV	±2.2mV
1kHz	845Hz	2.6kHz	±1.2mV	±2.2mV
422Hz	422Hz	1.3kHz	±1.2mV	±2.2mV
26Hz (Filtered Mode)	26Hz	82Hz	±1.2mV	±2.2mV

Note: TME is the total measurement error.

Mode 7kHz (Normal):

In this mode, the ADC has high resolution and low TME (total measurement error). This is considered the normal operating mode because of the optimum combination of speed and accuracy.

Mode 27kHz (Fast):

In this mode, the ADC has maximum throughput but has some increase in TME (total measurement error). So this mode is also referred to as the fast mode. The increase in speed comes from a reduction in the oversampling ratio. This results in an increase in noise and average measurement error.

Mode 26Hz (Filtered):

In this mode, the ADC digital filter –3dB frequency is lowered to 26Hz by increasing the OSR. This mode is also referred to as the filtered mode due to its low –3dB frequency. The accuracy is similar to the 7kHz (Normal) mode with lower noise.

Modes 14kHz, 3kHz, 2kHz, 1kHz and 422Hz:

Modes 14kHz, 3kHz, 2kHz, 1kHz and 422Hz provide additional options to set the ADC digital filter –3dB frequency at 13.5kHz, 3.4kHz, 1.7kHz, 845Hz and 422Hz respectively. The accuracy of the 14kHz mode is similar to the 27kHz (fast) mode. The accuracy of 3kHz, 2kHz, 1kHz and 422Hz modes is similar to the 7kHz (normal) mode.

The filter bandwidths and the conversion times for these modes are provided in Table 3 and Table 5. If the Core is in STANDBY state, an additional t_{REFUP} time is required to power up the reference before beginning the ADC conversions. The reference can remain powered up between ADC conversions if the REFON bit in the Configuration Register Group is set to 1 so the Core is in REFUP state after a delay t_{REFUP}. Then, the subsequent ADC commands will not have the t_{REFUP} delay before beginning ADC conversions.

OPERATION

ADC Range and Resolution

The C inputs and GPIO inputs have the same range and resolution. The ADC inside the LTC6811 has an approximate range from –0.82V to +5.73V. Negative readings are rounded to 0V. The format of the data is a 16-bit unsigned integer where the LSB represents 100µV. Therefore, a reading of 0x80E8 (33,000 decimal) indicates a measurement of 3.3V.

Delta-Sigma ADCs have quantization noise which depends on the input voltage, especially at low oversampling ratios (OSR), such as in FAST mode. In some of the ADC modes, the quantization noise increases as the input voltage approaches the upper and lower limits of the ADC range. For example, the total measurement noise versus input voltage in normal and filtered modes is shown in Figure 2.

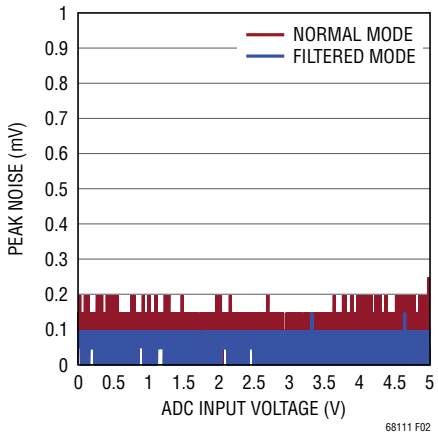


Figure 2. Measurement Noise vs Input Voltage

The specified range of the ADC is 0V to 5V. In Table 4, the precision range of the ADC is arbitrarily defined as 0.5V to 4.5V. This is the range where the quantization noise is relatively constant even in the lower OSR modes (see Figure 2). Table 4 summarizes the total noise in this range for all eight ADC operating modes. Also shown is the noise free resolution. For example, 14-bit noise free resolution in normal mode implies that the top 14 bits will be noise free with a DC input, but that the 15th and 16th least significant bits (LSB) will flicker.

Table 4. ADC Range and Resolution

MODE	FULL RANGE[1]	SPECIFIED RANGE	PRECISION RANGE[2]	LSB	FORMAT	MAX NOISE	NOISE FREE RESOLUTION[3]
27kHz (fast)	–0.8192V to 5.7344V	0V to 5V	0.5V to 4.5V	100µV	Unsigned 16 Bits	$\pm 4mV_{P-P}$	10 Bits
14kHz						$\pm 1mV_{P-P}$	12 Bits
7kHz (normal)						$\pm 250\mu V_{P-P}$	14 Bits
3kHz						$\pm 150\mu V_{P-P}$	14 Bits
2kHz						$\pm 100\mu V_{P-P}$	15 Bits
1kHz						$\pm 100\mu V_{P-P}$	15 Bits
422Hz						$\pm 100\mu V_{P-P}$	15 Bits
26Hz (filtered)						$\pm 50\mu V_{P-P}$	16 Bits

1. Negative readings are rounded to 0V.

2. PRECISION RANGE is the range over which the noise is less than MAX NOISE.

3. NOISE FREE RESOLUTION is a measure of the noise level within the PRECISION RANGE.

OPERATION

ADC Range vs Voltage Reference Value

Typical ADCs have a range which is exactly twice the value of the voltage reference, and the ADC measurement error is directly proportional to the error in the voltage reference. The LTC6811 ADC is not typical. The absolute value of V_{REF1} is trimmed up or down to compensate for gain errors in the ADC. Therefore, the ADC total measurement error (TME) specifications are superior to the V_{REF1} specifications. For example, the 25°C specification of the total measurement error when measuring 3.300V in 7kHz (normal) mode is ±1.2mV and the 25°C specification for V_{REF1} is 3.200V±100mV.

Measuring Cell Voltages (ADCV Command)

The ADCV command initiates the measurement of the battery cell inputs, pins C0 through C12. This command has options to select the number of channels to measure and the ADC mode. See the section on Commands for the ADCV command format.

Figure 3 illustrates the timing of the ADCV command which measures all twelve cells. After the receipt of the ADCV command to measure all 12 cells, ADC1 sequentially measures the bottom 6 cells. ADC2 sequentially measures the top 6 cells. After the cell measurements are complete, each channel is calibrated to remove any offset errors.

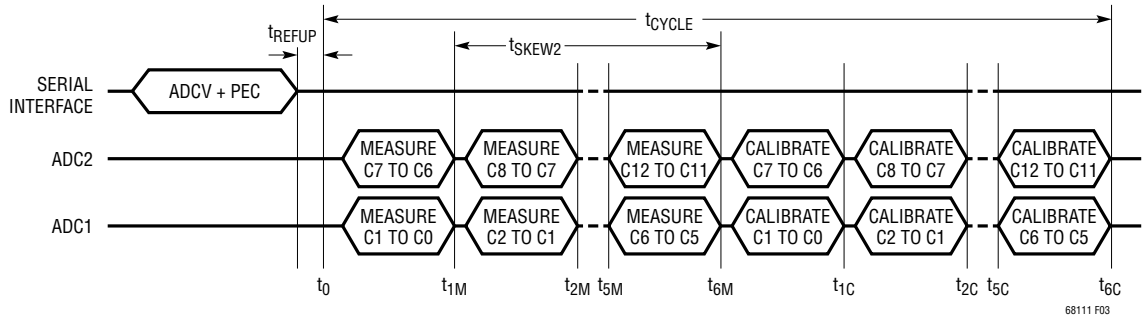


Figure 3. Timing for ADCV Command Measuring All 12 Cells

Table 5. Conversion Times for ADCV Command Measuring All 12 Cells in Different Modes

	CONVERSION TIMES (in µs)								
MODE	t_0	t_{1M}	t_{2M}	t_{5M}	t_{6M}	t_{1C}	t_{2C}	t_{5C}	t_{6C}
27kHz	0	57	103	243	290	432	568	975	1,113
14kHz	0	86	162	389	465	606	742	1,149	1,288
7kHz	0	144	278	680	814	1,072	1,324	2,080	2,335
3kHz	0	260	511	1,262	1,512	1,770	2,022	2,778	3,033
2kHz	0	493	976	2,425	2,908	3,166	3,418	4,175	4,430
1kHz	0	959	1,907	4,753	5,701	5,961	6,213	6,970	7,222
422Hz	0	1,890	3,769	9,407	11,287	11,547	11,799	12,555	12,807
26Hz	0	29,817	59,623	149,043	178,850	182,599	186,342	197,571	201,317

OPERATION

Table 5 shows the conversion times for the ADCV command measuring all 12 cells. The total conversion time is given by t_{6C} which indicates the end of the calibration step.

Figure 4 illustrates the timing of the ADCV command that measures only two cells.

Table 6 shows the conversion time for the ADCV command measuring only 2 cells. t_{1C} indicates the total conversion time for this command.

Table 6. Conversion Times for ADCV Command Measuring Only 2 Cells in Different Modes

	CONVERSION TIMES (in µs)		
MODE	**t_0**	**t_{1M}**	**t_{1C}**
27kHz	0	57	201
14kHz	0	86	230
7kHz	0	144	405
3kHz	0	240	501
2kHz	0	493	754
1kHz	0	959	1,219
422Hz	0	1,890	2,150
26Hz	0	29,817	33,568

Under/Over Voltage Monitoring

Whenever the C inputs are measured, the results are compared to undervoltage and overvoltage thresholds stored in memory. If the reading of a cell is above the overvoltage limit, a bit in memory is set as a flag. Similarly, measurement results below the undervoltage limit cause a flag to be set. The overvoltage and undervoltage thresholds are stored in the Configuration Register Group. The flags are stored in the Status Register Group B.

Auxiliary (GPIO) Measurements (ADAX Command)

The ADAX command initiates the measurement of the GPIO inputs. This command has options to select which GPIO input to measure (GPIO1-5) and which ADC mode to use. The ADAX command also measures the 2nd reference. There are options in the ADAX command to measure each GPIO and the 2nd reference separately or to measure all five GPIOs and the 2nd reference in a single command. See the section on Commands for the ADAX command format. All auxiliary measurements are relative to the V^- pin voltage. This command can be used to read external temperatures

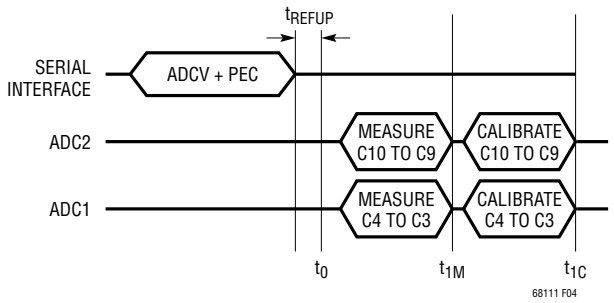


Figure 4. Timing for ADCV Command Measuring 2 Cells

OPERATION

by connecting temperature sensors to the GPIOs. These sensors can be powered from the 2nd reference which is also measured by the ADAX command, resulting in precise ratiometric measurements.

Figure 5 illustrates the timing of the ADAX command measuring all GPIOs and the 2nd reference. Since all six measurements are carried out on ADC1 alone, the conversion time for the ADAX command is similar to the ADCV command.

Auxiliary (GPIO) Measurements with Digital Redundancy (ADAXD Command)

The ADAXD command operates similarly to the ADAX command except that an additional diagnostic is performed using digital redundancy.

The analog modulator from ADC1 is used to measure GPIO1-5 and the 2nd reference. This bit stream is input to the digital integration and differentiation machines for both ADC1 and ADC2. Thus the measurement result is calculated with redundancy. At the end of each measurement, the two results are compared and if any result bit mismatch is detected then a digital redundancy fault code is stored in place of the ADC result. The digital redundancy fault code is a value of 0xFF0X. This is detectable because it falls outside the normal result range of 0x0000 to 0xDFFF. The last four bits are used to indicate which nibble(s) of the result values did not match.

Indication of Digital Redundancy Fault Codes

DIGITAL REDUNDANCY FAULT CODE 4 LSBs	INDICATION
0b0XXX	No fault detected in bits 15-12
0b1XXX	Fault detected in bits 15-12
0bX0XX	No fault detected in bits 11-8
0bX1XX	Fault detected in bits 11-8
0bXX0X	No fault detected in bits 7-4
0bXX1X	Fault detected in bits 7-4
0bXXX0	No fault detected in bits 3-0
0bXXX1	Fault detected in bits 3-0
0b000	The digital redundancy feature will not write this value of all zeros in the last 4 bits

The execution time of ADAX and ADAXD is the same.

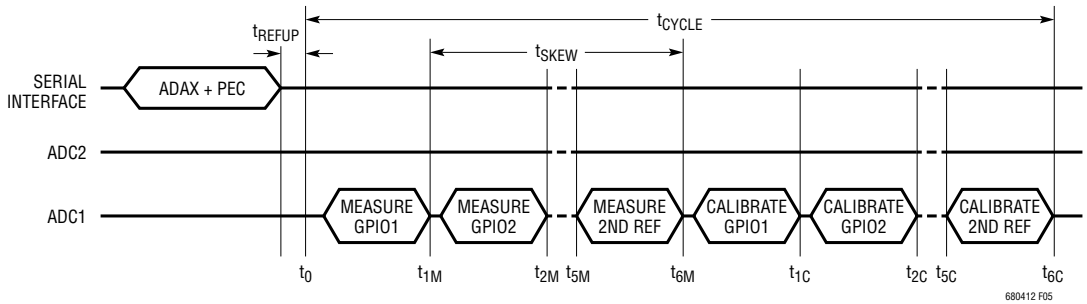


Figure 5. Timing for ADAX Command Measuring All GPIOs and 2nd Reference

Table 7. Conversion Times for ADAX Command Measuring All GPIOs and 2nd Reference in Different Modes

	CONVERSION TIMES (in µs)								
MODE	t_0	t_{1M}	t_{2M}	t_{5M}	t_{6M}	t_{1C}	t_{2C}	t_{5C}	t_{6C}
27kHz	0	57	103	243	290	432	568	975	1,113
14kHz	0	86	162	389	465	606	742	1,149	1,288
7kHz	0	144	278	680	814	1,072	1,324	2,080	2,335
3kHz	0	260	511	1,262	1,512	1,770	2,022	2,778	3,033
2kHz	0	493	976	2,425	2,908	3,166	3,418	4,175	4,430
1kHz	0	959	1,907	4,753	5,701	5,961	6,213	6,970	7,222
422Hz	0	1,890	3,769	9,407	11,287	11,547	11,799	12,555	12,807
26Hz	0	29,817	59,623	149,043	178,850	182,599	186,342	197,571	201,317

OPERATION

Measuring Cell Voltages and GPIOs (ADCVAX Command)

The ADCVAX command combines twelve cell measurements with two GPIO measurements (GPIO1 and GPIO2). This command simplifies the synchronization of battery cell voltage and current measurements when current sensors are connected to GPIO1 or GPIO2 inputs. Figure 6 illustrates the timing of the ADCVAX command. See the section on Commands for the ADCVAX command format. The synchronization of the current and voltage measurements, t_{SKEW1}, in FAST MODE is within 194µs.

Table 8 shows the conversion and synchronization time for the ADCVAX command in different modes. The total conversion time for the command is given by t_{8C}.

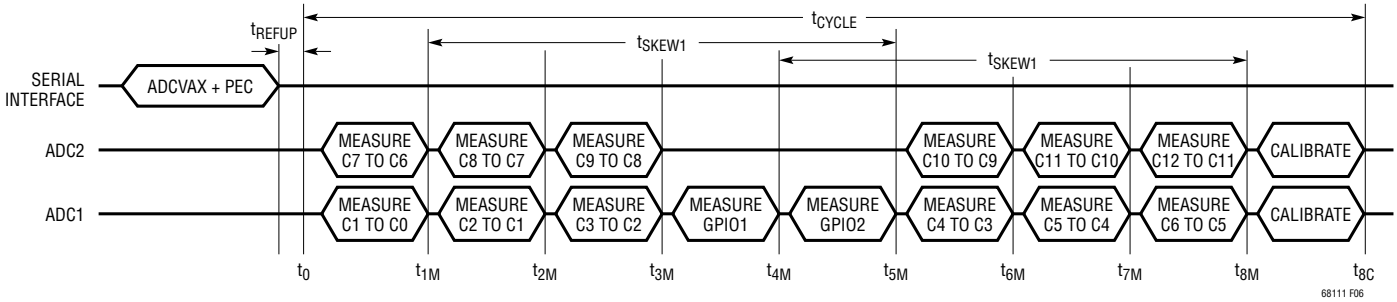


Figure 6. Timing of ADCVAX Command

Table 8. Conversion and Synchronization Times for ADCVAX Command in Different Modes

	CONVERSION TIMES (in µs)										SYNCHRONIZATION TIME (in µs)
MODE	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{5M}	t_{6M}	t_{7M}	t_{8M}	t_{8C}	t_{SKEW1}
27kHz	0	57	104	150	204	251	305	352	398	1,503	194
14kHz	0	86	161	237	320	396	479	555	630	1,736	310
7kHz	0	144	278	412	553	687	828	962	1,096	3,133	543
3kHz	0	260	511	761	1,018	1,269	1,526	1,777	2,027	4,064	1009
2kHz	0	493	976	1,459	1,949	2,432	2,923	3,406	3,888	5,925	1939
1kHz	0	959	1,907	2,856	3,812	4,760	5,716	6,664	7,613	9,648	3801
422Hz	0	1,890	3,769	5,648	7,535	9,415	11,301	13,181	15,060	17,096	7,525
26Hz	0	29,817	59,623	89,430	119,244	149,051	178,864	208,671	238,478	268,442	119,234

OPERATION

DATA ACQUISITION SYSTEM DIAGNOSTICS

The battery monitoring data acquisition system is comprised of the multiplexers, ADCs, 1st reference, digital filters and memory. To ensure long term reliable performance there are several diagnostic commands which can be used to verify the proper operation of these circuits.

Measuring Internal Device Parameters (ADSTAT Command)

The ADSTAT command is a diagnostic command that measures the following internal device parameters: Sum of All Cells (SC), Internal Die Temperature (ITMP), Analog Power Supply (VA) and the Digital Power Supply (VD). These parameters are described in the section below. All the 8 ADC modes described earlier are available for these conversions. See the section on Commands for the ADSTAT command format. Figure 7 illustrates the timing of the ADSTAT command measuring all 4 internal device parameters.

Table 9 shows the conversion time of the ADSTAT command measuring all 4 internal parameters. t_{4C} indicates the total conversion time for the ADSTAT command.

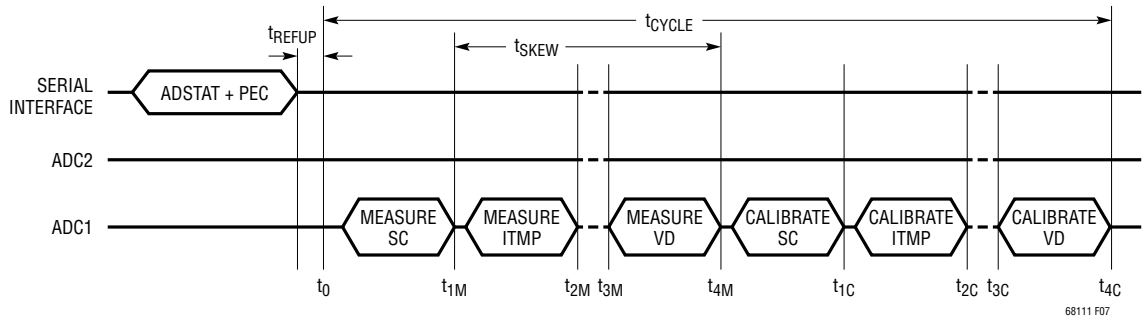


Figure 7. Timing for ADSTAT Command Measuring SC, ITMP, VA, VD

Table 9. Conversion Times for ADSTAT Command Measuring SC, ITMP, VA, VD

	CONVERSION TIMES (in µs)								
MODE	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{1C}	t_{2C}	t_{3C}	t_{4C}
27kHz	0	57	103	150	197	338	474	610	748
14kHz	0	86	162	237	313	455	591	726	865
7kHz	0	144	278	412	546	804	1,056	1,308	1,563
3kHz	0	260	511	761	1,011	1,269	1,522	1,774	2,028
2kHz	0	493	976	1,459	1,942	2,200	2,452	2,705	2,959
1kHz	0	959	1,907	2,856	3,804	4,062	4,313	4,563	4,813
422Hz	0	1,890	3,769	5,648	7,528	7,786	8,036	8,287	8,537
26Hz	0	29,817	59,623	89,430	119,237	122,986	126,729	130,472	134,218

OPERATION

Sum of All Cells Measurement: The Sum of All Cells measurement is the voltage between C12 and C0 with a 20:1 attenuation. The 16-bit ADC value of Sum of All Cells measurement (SC) is stored in Status Register Group A. Any potential difference between the C0 and V^- pins results in an error in the SC measurement equal to this difference. From the SC value, the sum of all cell voltage measurements is given by:

Sum of All Cells = SC • 20 • 100µV

Internal Die Temperature: The ADSTAT command can measure the internal die temperature. The 16-bit ADC value of the die temperature measurement (ITMP) is stored in Status Register Group A. From ITMP, the actual die temperature is calculated using the expression:

$$\text{Internal Die Temperature (°C)} = \text{ITMP} \bullet \frac{100\mu V}{7.5mV}\,°C - 273°C$$

Power Supply Measurements: The ADSTAT command is also used to measure the Analog Power Supply (V_{REG}) and Digital Power Supply (V_{REGD}). The 16-bit ADC value of the analog power supply measurement (VA) is stored in Status Register Group A. The 16-bit ADC value of the digital power supply measurement (VD) is stored in Status Register Group B. From VA and VD, the power supply measurements are given by:

Analog power supply measurement (V_{REG}) = VA • 100µV

Digital power supply measurement (V_{REGD}) = VD • 100µV

The value of V_{REG} is determined by external components. V_{REG} should be between 4.5V and 5.5V to maintain accuracy. The value of V_{REGD} is determined by internal components. The normal range of V_{REGD} is 2.7V to 3.6V.

Measuring Internal Device Parameters with Digital Redundancy (ADSTATD Command)

The ADSTATD command operates similarly to the ADSTAT command except that an additional diagnostic is performed using digital redundancy.

The analog modulator from ADC1 is used to measure Sum of All Cells, Internal Die Temperature, Analog Power Supply and Digital Power Supply. This bit stream is input to the digital integration and differentiation machines for both ADC1 and ADC2. Thus the measurement result is calculated with redundancy. At the end of the measurement, the two results are compared and if any result bit mismatch is detected, then a digital redundancy fault code is stored in place of the ADC result. The digital redundancy fault code is a value of 0xFF0X. This is detectable because it falls outside the normal result range of 0x0000 to 0xDFFF. The last four bits are used to indicate which nibble(s) of the result values did not match.

Indication of Digital Redundancy Fault Codes

DIGITAL REDUNDANCY FAULT CODE 4 LSBs	INDICATION
0b0XXX	No fault detected in bits 15-12
0b1XXX	Fault detected in bits 15-12
0bX0XX	No fault detected in bits 11-8
0bX1XX	Fault detected in bits 11-8
0bXX0X	No fault detected in bits 7-4
0bXX1X	Fault detected in bits 7-4
0bXXX0	No fault detected in bits 3-0
0bXXX1	Fault detected in bits 3-0
0b000	The digital redundancy feature will not write this value of all zeros in the last 4 bits

The execution time of ADSTAT and ADSTATD is the same.

OPERATION

Measuring Cell Voltages and Sum of All Cells (ADCVSC Command)

The ADCVSC command combines twelve cell measurements and the measurement of Sum of All Cells. This command simplifies the synchronization of the individual battery cell voltage and the total Sum of All Cells measurements. Figure 8 illustrates the timing of the ADCVSC command. See the section on Commands for the ADCVSC command format. The synchronization of the cell voltage and Sum of All Cells measurements, t_{SKEW}, in FAST MODE is within 159µs.

Table 10 shows the conversion and synchronization time for the ADCVSC command in different modes. The total conversion time for the command is given by t_{7C}.

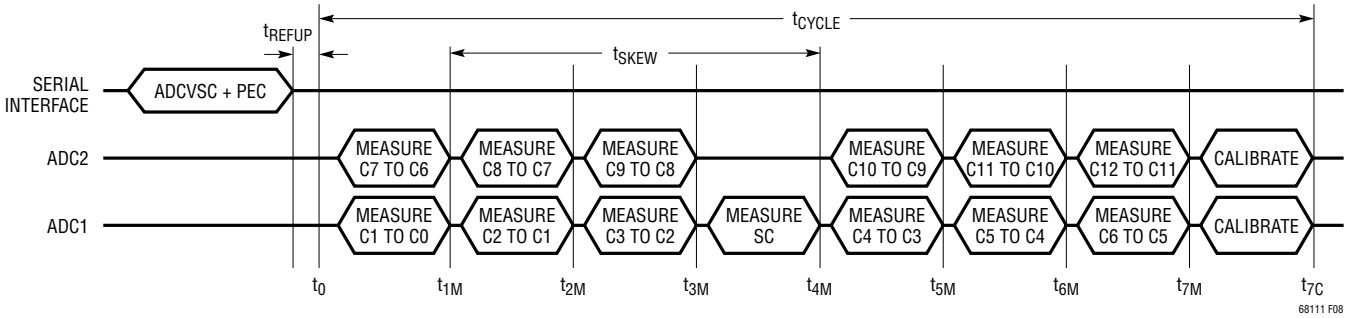


Figure 8. Timing for ADCVSC Command Measuring All 12 Cells, SC

Table 10. Conversion and Synchronization Times for ADCVSC Command in Different Modes

	CONVERSION TIMES (in µs)									SYNCHRONIZATION TIME (in µs)
MODE	t_0	t_{1M}	t_{2M}	t_{3M}	t_{4M}	t_{5M}	t_{6M}	t_{7M}	t_{7C}	t_{SKEW}
27kHz	0	57	106	155	216	265	326	375	1,322	159
14kHz	0	86	161	237	320	396	479	555	1,526	234
7kHz	0	144	278	412	553	695	829	962	2,748	409
3kHz	0	260	511	761	1,018	1,269	1,526	1,777	3,562	758
2kHz	0	493	976	1,459	1,949	2,432	2,923	3,406	5,192	1,456
1kHz	0	959	1,907	2,856	3,812	4,767	5,716	6,664	8,450	2,853
422Hz	0	1,890	3,769	5,648	7,535	9,422	11,301	13,181	14,966	5,645
26Hz	0	29,817	59,623	89,430	119,244	149,058	178,864	208,672	234,893	89,427

OPERATION

Overlap Cell Measurement (ADOL Command)

The ADOL command simultaneously measures Cell 7 with ADC1 and ADC2. The host can compare the results from the two ADCs against each other to look for inconsistencies which may indicate a fault. The result from ADC2 is placed in Cell Voltage Register Group C where the Cell 7 result normally resides. The result from ADC1 is placed in Cell Voltage Register Group C where the Cell 8 result normally resides. Figure 9 illustrates the timing of the ADOL command. See the section on Commands for the ADOL command format.

Table 11 shows the conversion time for the ADOL command. t_{1C} indicates the total conversion time for this command.

Table 11. Conversion Times for ADOL Command

	CONVERSION TIMES (in µs)		
MODE	**t_0**	**t_{1M}**	**t_{1C}**
27kHz	0	57	201
14kHz	0	86	230
7kHz	0	144	405
3kHz	0	240	501
2kHz	0	493	754
1kHz	0	959	1,219
422Hz	0	1,890	2,150
26Hz	0	29,817	33,568

Accuracy Check

Measuring an independent voltage reference is the best means to verify the accuracy of a data acquisition system. The LTC6811 contains a 2nd reference for this purpose. The ADAX command will initiate the measurement of the 2nd reference. The results are placed in Auxiliary Register Group B. The range of the result depends on the ADC1 measurement accuracy and the accuracy of the 2nd reference, including thermal hysteresis and long term drift. Readings outside the range 2.99V to 3.01V indicate the system is out of its specified tolerance. ADC2 is verified by comparing it to ADC1 using the ADOL command.

MUX Decoder Check

The diagnostic command DIAGN ensures the proper operation of each multiplexer channel. The command cycles through all channels and sets the MUXFAIL bit to 1 in Status Register Group B if any channel decoder fails. The MUXFAIL bit is set to 0 if the channel decoder passes the test. The MUXFAIL bit is also set to 1 on power-up (POR) or after a CLRSTAT command.

The DIAGN command takes about 400µs to complete if the Core is in REFUP state and about 4.5ms to complete if the Core is in STANDBY state. The polling methods described in the section Polling Methods can be used to determine the completion of the DIAGN command.

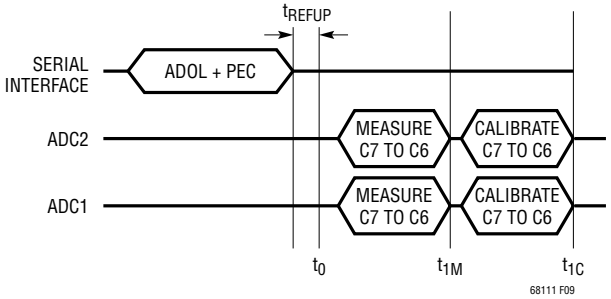


Figure 9. Timing for ADOL Command Measuring Cell 7 with both ADC1 and ADC2

OPERATION

Digital Filter Check

The delta-sigma ADC is composed of a 1-bit pulse density modulator followed by a digital filter. A pulse density modulated bit stream has a higher percentage of 1s for higher analog input voltages. The digital filter converts this high frequency 1-bit stream into a single 16-bit word. This is why a delta-sigma ADC is often referred to as an oversampling converter.

The self test commands verify the operation of the digital filters and memory. Figure 10 illustrates the operation of the ADC during self test. The output of the 1-bit pulse density modulator is replaced by a 1-bit test signal. The test signal passes through the digital filter and is converted to a 16-bit value. The 1-bit test signal undergoes the same digital conversion as the regular 1-bit signal from the modulator, so the conversion time for any self test command is exactly the same as the regular ADC conversion command. The 16-bit ADC value is stored in the same register groups as the corresponding regular ADC conversion command. The test signals are designed to place alternating one-zero patterns in the registers. Table 12 provides a list of the self test commands. If the digital filters and memory are working properly, then the registers will contain the values shown in Table 12. For more details see the Commands section.

ADC Clear Commands

LTC6811 has three clear commands: CLRCELL, CLRAUX and CLRSTAT. These commands clear the registers that store all ADC conversion results.

The CLRCELL command clears Cell Voltage Register Groups A, B, C and D. All bytes in these registers are set to 0xFF by CLRCELL command.

The CLRAUX command clears Auxiliary Register Groups A and B. All bytes in these registers are set to 0xFF by CLRAUX command.

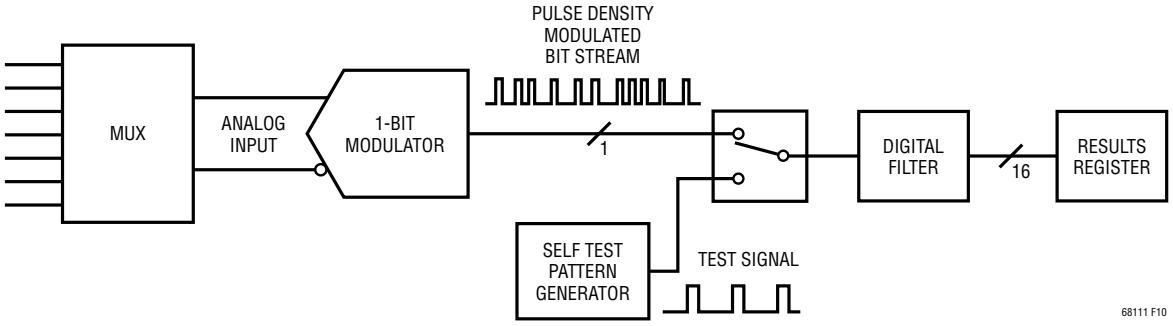


Figure 10. Operation of LTC6811 ADC Self Test

Table 12. Self Test Command Summary

COMMAND	SELF TEST OPTION	OUTPUT PATTERN IN DIFFERENT ADC MODES			RESULTS REGISTER GROUPS
		27kHz	14kHz	7kHz, 3kHz, 2kHz, 1kHz, 422Hz, 26Hz	
CVST	ST[1:0]=01	0x9565	0x9553	0x9555	C1V to C12V
	ST[1:0]=10	0x6A9A	0x6AAC	0x6AAA	(CVA, CVB, CVC, CVD)
AXST	ST[1:0]=01	0x9565	0x9553	0x9555	G1V to G5V, REF
	ST[1:0]=10	0x6A9A	0x6AAC	0x6AAA	(AUXA, AUXB)
STATST	ST[1:0]=01	0x9565	0x9553	0x9555	SC, ITMP, VA, VD
	ST[1:0]=10	0x6A9A	0x6AAC	0x6AAA	(STATA, STATB)

OPERATION

The CLRSTAT command clears Status Register Groups A and B except the REV and RSVD bits in Status Register Group B. A read back of REV will return the revision code of the part. RSVD bits always read back 0s. All OV and UV flags, MUXFAIL bit and the THSD bit in Status Register Group B are set to 1 by CLRSTAT command. The THSD bit is set to 0 after RDSTATB command. The registers storing SC, ITMP, VA and VD are all set to 0xFF by CLRSTAT command.

Open Wire Check (ADOW Command)

The ADOW command is used to check for any open wires between the ADCs of the LTC6811 and the external cells. This command performs ADC conversions on the C pin inputs identically to the ADCV command, except two internal current sources sink or source current into the two C pins while they are being measured. The pull-up (PUP) bit of the ADOW command determines whether the current sources are sinking or sourcing 100µA.

The following simple algorithm can be used to check for an open wire on any of the 13 C pins:

1. Run the 12-cell command ADOW with PUP = 1 at least twice. Read the cell voltages for cells 1 through 12 once at the end and store them in array $CELL_{PU}(n)$.
2. Run the 12-cell command ADOW with PUP = 0 at least twice. Read the cell voltages for cells 1 through 12 once at the end and store them in array $CELL_{PD}(n)$.
3. Take the difference between the pull-up and pull-down measurements made in above steps for cells 2 to 12: $CELL_{\Delta}(n) = CELL_{PU}(n) – CELL_{PD}(n)$.
4. For all values of n from 1 to 11: If $CELL_{\Delta}(n+1) < –400mV$, then C(n) is open. If $CELL_{PU}(1) = 0.0000$, then C(0) is open. If $CELL_{PD}(12) = 0.0000$, then C(12) is open.

The above algorithm detects open wires using normal mode conversions with as much as 10nF of capacitance remaining on the LTC6811 side of the open wire. However, if more external capacitance is on the open C pin, then the length of time that the open wire conversions are ran in steps 1 and 2 must be increased to give the 100µA current sources time to create a large enough difference for the algorithm to detect an open connection. This can be accomplished by running more than two ADOW commands in steps 1 and 2, or by using filtered mode conversions instead of normal mode conversions. Use Table 13 to determine how many conversions are necessary:

Table 13

EXTERNAL C PIN CAPACITANCE	NUMBER OF ADOW COMMANDS REQUIRED IN STEPS 1 AND 2	
	NORMAL MODE	FILTERED MODE
≤10nF	2	2
100nF	10	2
1µF	100	2
C	1 + ROUNDUP(C/10nF)	2

Thermal Shutdown

To protect the LTC6811 from overheating, there is a thermal shutdown circuit included inside the IC. If the temperature detected on the die goes above approximately 150°C, the thermal shutdown circuit trips and resets the Configuration Register Group and turns off all discharge switches. When a thermal shutdown event has occurred, the THSD bit in Status Register Group B will go high. The CLRSTAT command can also set the THSD bit high for diagnostic purposes. This bit is cleared when a read operation is performed on Status Register Group B (RDSTATB command). The CLRSTAT command sets the THSD bit high for diagnostic purposes but does not reset the Configuration Register Group.

Revision Code and Reserved Bits

The Status Register Group B contains a 4-bit revision code (REV) and 2 reserved (RSVD) bits. If software detection of device revision is necessary, then contact the factory for details. Otherwise the code can be ignored. In all cases, however, the values of all bits must be used when calculating the Packet Error Code (PEC) on data reads.

OPERATION

WATCHDOG AND DISCHARGE TIMER

When there is no valid command for more than 2 seconds, the watchdog timer expires. This resets Configuration Register bytes CFGR0-3 in all cases. CFGR4 and CFGR5 and the S Control Register Group are reset by the watchdog timer when the discharge timer is disabled. The WDT pin is pulled high by the external pull-up when the watchdog time elapses. The watchdog timer is always enabled and it resets after every valid command with matching command PEC.

The discharge timer is used to keep the discharge switches turned ON for programmable time duration. If the discharge timer is being used, the discharge switches are not turned OFF when the watchdog timer is activated.

To enable the discharge timer, connect the DTEN pin to V_{REG} (Figure 11). In this configuration, the discharge switches will remain ON for the programmed time duration as determined by the DCTO value in the Configuration Register Group. Table 14 shows the various time settings and the corresponding DCTO value. Table 15 summarizes the status of the Configuration Register Group after a watchdog timer or discharge timer event.

Table 15

	WATCHDOG TIMER	DISCHARGE TIMER
DTEN = 0, DCTO = XXXX	Resets CFGR0-5 and SCTRL when it fires	Disabled
DTEN = 1, DCTO = 0000	Resets CFGR0-5 and SCTRL when it fires	Disabled
DTEN = 1, DCTO ! = 0000	Resets CFGR0-3 when it fires	Resets CFGR4-5 and SCTRL when it fires

The status of the discharge timer can be determined by reading the Configuration Register Group using the RDCFGA command. The DCTO value indicates the time left before the discharge timer expires as shown in Table 16.

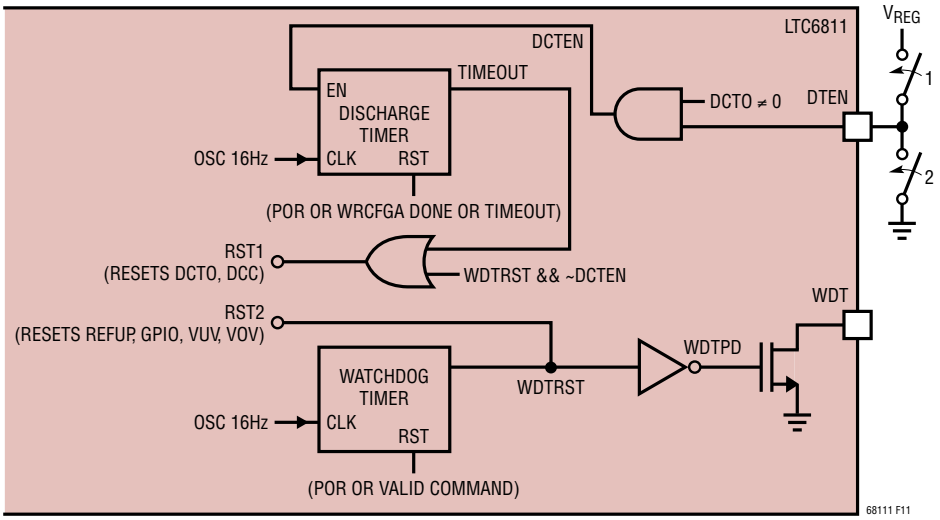


Figure 11. Watchdog and Discharge Timer

Table 14. DCTO Settings

DCTO	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Time (min)	Disabled	0.5	1	2	3	4	5	10	15	20	30	40	60	75	90	120

OPERATION

Unlike the watchdog timer, the discharge timer does not reset when there is a valid command. The discharge timer can only be reset after a valid WRCFGA (Write Configuration Register Group) command. There is a possibility that the discharge timer will expire in the middle of some commands.

If the discharge timer activates in the middle of a WRCFGA command, the Configuration Register Group and S Control Register Group will reset as per Table 15. However, at the end of the valid WRCFGA command, the new data is copied to the Configuration Register Group. The new configuration data is not lost when the discharge timer is activated.

If the discharge timer activates in the middle of a RDCFGA command, the Configuration Register Group resets as per Table 15. As a result, the read back data from bytes CFRG4 and CFRG5 could be corrupted. If the discharge timer activates in the middle of a RDSCTRL command, the S Control Register Group resets as per Table 15. As a result, the read back data could be corrupted.

Table 16

DCTO (READ VALUE)	DISCHARGE TIME LEFT (MIN)
0	Disabled (or) Timer has timed out
1	0 < Timer ≤ 0.5
2	0.5 < Timer ≤ 1
3	1 < Timer ≤ 2
4	2 < Timer ≤ 3
5	3 < Timer ≤ 4
6	4 < Timer ≤ 5
7	5 < Timer ≤ 10
8	10 < Timer ≤ 15
9	15 < Timer ≤ 20
A	20 < Timer ≤ 30
B	30 < Timer ≤ 40
C	40 < Timer ≤ 60
D	60 < Timer ≤ 75
E	75 < Timer ≤ 90
F	90 < Timer ≤ 120

OPERATION

RESET BEHAVIORS

Power cycling, thermal shutdown, watchdog timeout and discharge timeout can cause various registers and circuitry to reset when they occur. The following summarizes the behaviors when these events occur:

RESET EVENT	DEVICE BEHAVIOR
Power Cycle (V^+ and V_{REG} both power cycled)	Transition to STANDBY state. All registers and state machines are reset to default values. Cell discharge is disabled.
Thermal Shutdown	Cell discharge is disabled, but S Control Register Group is not reset. All of the Configuration Register Group is reset. The COMM Register Group is reset.
Watchdog Timeout (while Discharge Timer is Running)	Transition to EXTENDED BALANCING state. CFGR0, CFGR1, CFGR2 and CFGR3 of the Configuration Register Group are reset. The COMM Register Group is reset.
Watchdog Timeout (no Discharge Timer Running)	Transition to SLEEP state. Cell discharge is disabled. All state machines are reset. All of the Configuration Register Group is reset. The PWM Register Group is reset. The S Control Register Group is reset. The COMM Register Group is reset.
Discharge Timeout (while Watchdog Timeout has Elapsed)	Transition to SLEEP state. Same behavior as the previous case above.
Discharge Timeout (while Watchdog Timeout is not Elapsed)	Cell discharge is disabled. The PWM Register Group is reset. The S Control Register Group is reset. CFGR4 and CFGR5 of the Configuration Register Group are reset.

OPERATION

S PIN PULSE WIDTH MODULATION FOR CELL BALANCING

For additional control of cell discharging, the host may configure the S pins to operate using pulse width modulation. While the watchdog timer is not expired, the DCC bits in the Configuration Register Group control the S pins directly. After the watchdog timer expires, PWM operation begins and continues for the remainder of the selected discharge time or until a wake-up event occurs (and the watchdog timer is reset). During PWM operation, the DCC bits must be set to 1 for the PWM feature to operate.

Once PWM operation begins, the configurations in the PWM register may cause some or all S pins to be periodically de-asserted to achieve the desired duty cycle as shown in Table 17. Each PWM signal operates on a 30 second period. For each cycle, the duty cycle can be programmed from 0% to 100% in increments of 1/15 = 6.67% (2 seconds).

Table 17. S Pin Pulse Width Modulation Settings

DCC BIT (CONFIG REGISTER GROUP)	PWMC SETTING	ON TIME (SECONDS)	OFF TIME (SECONDS)	DUTY CYCLE (%)
0	4'bXXXX	0	Continuously Off	0.0
1	4'b1111	Continuously On	0	100.0
1	4'b1110	28	2	93.3
1	4'b1101	26	4	86.7
1	4'b1100	24	6	80.0
1	4'b1011	22	8	73.3
1	4'b1010	20	10	66.7
1	4'b1001	18	12	60.0
1	4'b1000	16	14	53.3
1	4'b0111	14	16	46.7
1	4'b0110	12	18	40.0
1	4'b0101	10	20	33.3
1	4'b0100	8	22	26.7
1	4'b0011	6	24	20.0
1	4'b0010	4	26	13.3
1	4'b0001	2	28	6.7
1	4'b0000	0	Continuously Off	0.0

Table 18. COMM Register Memory Map

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

OPERATION

Each S pin PWM signal is sequenced at different intervals to ensure that no two pins switch on or off at the same time. The switching interval between channels is 62.5ms, and 0.75 seconds is required for all twelve pins to switch (12 • 62.5ms).

The default value of the PWM register is all 1s so that the LTC6811 will maintain backwards compatibility with the LTC6804. Upon entering sleep mode, the PWM register will be initialized to its default value.

I^2C/SPI MASTER ON LTC6811 USING GPIOS

The I/O ports GPIO3, GPIO4 and GPIO5 on LTC6811-1 and LTC6811-2 can be used as an I^2C or SPI master port to communicate to an I^2C or SPI slave. In the case of an I^2C master, GPIO4 and GPIO5 form the SDA and SCL ports of the I^2C interface respectively. In the case of a SPI master, GPIO3, GPIO4 and GPIO5 become the CSBM, SDIOM and SCKM ports of the SPI interface respectively. The SPI master on LTC6811 supports SPI mode 3 (CHPA = 1, CPOL = 1).

The GPIOs are open drain outputs, so an external pull-up is required on these ports to operate as an I^2C or SPI master. It is also important to write the GPIO bits to 1 in the Configuration Register Group so these ports are not pulled low internally by the device.

COMM Register

LTC6811 has a 6-byte COMM register as shown in Table 18. This register stores all data and control bits required for I^2C or SPI communication to a slave. The COMM register contains three bytes of data Dn[7:0] to be transmitted to or received from the slave device. ICOMn[3:0] specify control actions before transmitting/receiving each data byte. FCOMn[3:0] specify control actions after transmitting/receiving each data byte.

If the bit ICOMn[3] in the COMM register is set to 1 the part becomes a SPI master and if the bit is set to 0 the part becomes an I^2C master.

Table 19 describes the valid write codes for ICOMn[3:0] and FCOMn[3:0] and their behavior when using the part as an I^2C master.

Table 19. Write Codes for ICOMn[3:0] and FCOMn[3:0] on I^2C Master

CONTROL BITS	CODE	ACTION	DESCRIPTION
ICOMn[3:0]	0110	START	Generate a START signal on I^2C port followed by data transmission
	0001	STOP	Generate a STOP signal on I^2C port
	0000	BLANK	Proceed directly to data transmission on I^2C port
	0111	No Transmit	Release SDA and SCL and ignore the rest of the data
FCOMn[3:0]	0000	Master ACK	Master generates an ACK signal on ninth clock cycle
	1000	Master NACK	Master generates a NACK signal on ninth clock cycle
	1001	Master NACK + STOP	Master generates a NACK signal followed by STOP signal

OPERATION

Table 20. Write Codes for ICOMn[3:0] and FCOMn[3:0] on SPI Master

CONTROL BITS	CODE	ACTION	DESCRIPTION
ICOMn[3:0]	1000	CSBM low	Generates a CSBM low signal on SPI port (GPIO3)
	1010	CSBM falling edge	Drives CSBM (GPIO3) high, then low
	1001	CSBM high	Generates a CSBM high signal on SPI port (GPIO3)
	1111	No Transmit	Releases the SPI port and ignores the rest of the data
FCOMn[3:0]	X000	CSBM low	Holds CSBM low at the end of byte transmission
	1001	CSBM high	Transitions CSBM high at the end of byte transmission

Table 20 describes the valid write codes for ICOMn[3:0] and FCOMn[3:0] and their behavior when using the part as a SPI master.

Note that only the codes listed in Tables 19 and 20 are valid for ICOMn[3:0] and FCOMn[3:0]. Writing any other code that is not listed in Tables 19 and 20 to ICOMn[3:0] and FCOMn[3:0] may result in unexpected behavior on the I^2C or SPI port.

COMM Commands

Three commands help accomplish I^2C or SPI communication to the slave device: WRCOMM, STCOMM and RDCOMM.

WRCOMM Command: This command is used to write data to the COMM register. This command writes 6 bytes of data to the COMM register. The PEC needs to be written at the end of the data. If the PEC does not match, all data in the COMM register is cleared to 1s when CSB goes high. See the section Bus Protocols for more details on a write command format.

STCOMM Command: This command initiates I^2C/SPI communication on the GPIO ports. The COMM register contains 3 bytes of data to be transmitted to the slave. During this command, the data bytes stored in the COMM register are transmitted to the slave I^2C or SPI device and the data received from the I^2C or SPI device is stored in the COMM register. This command uses GPIO4 (SDA) and GPIO5 (SCL) for I^2C communication or GPIO3 (CSBM), GPIO4 (SDIOM) and GPIO5 (SCKM) for SPI communication.

The STCOMM command is to be followed by 24 clock cycles for each byte of data to be transmitted to the slave device while holding CSB low. For example, to transmit three bytes of data to the slave, send STCOMM command and its PEC followed by 72 clock cycles. Pull CSB high at the end of the 72 clock cycles of STCOMM command.

During I^2C or SPI communication, the data received from the slave device is updated in the COMM register.

RDCOMM Command: The data received from the slave device can be read back from the COMM register using the RDCOMM command. The command reads back six bytes of data followed by the PEC. See the section Bus Protocols for more details on a read command format.

Table 21 describes the possible read back codes for ICOMn[3:0] and FCOMn[3:0] when using the part as an I^2C master. Dn[7:0] contains the data byte transmitted by the I^2C slave.

Table 21. Read Codes for ICOMn[3:0] and FCOMn[3:0] on I^2C Master

CONTROL BITS	CODE	DESCRIPTION
ICOMn[3:0]	0110	Master generated a START signal
	0001	Master generated a STOP signal
	0000	Blank, SDA was held low between bytes
	0111	Blank, SDA was held high between bytes
FCOMn[3:0]	0000	Master generated an ACK signal
	0111	Slave generated an ACK signal
	1111	Slave generated a NACK signal
	0001	Slave generated an ACK signal, master generated a STOP signal
	1001	Slave generated a NACK signal, master generated a STOP signal

In case of the SPI master, the read back codes for ICOMn[3:0] and FCOMn[3:0] are always 0111 and 1111 respectively. Dn[7:0] contains the data byte transmitted by the SPI slave.

OPERATION

Figure 12 illustrates the operation of LTC6811 as an I²C or SPI master using the GPIOs.

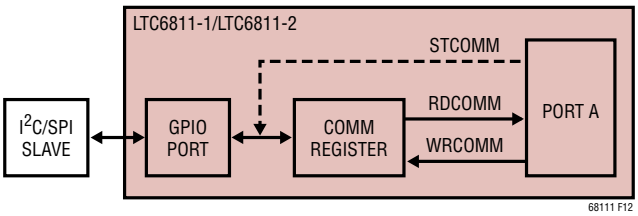


Figure 12. LTC6811 I²C/SPI Master Using GPIOs

Any number of bytes can be transmitted to the slave in groups of 3 bytes using these commands. The GPIO ports will not get reset between different STCOMM commands. However, if the wait time between the commands is greater than 2s, the watchdog will time out and reset the ports to their default values.

To transmit several bytes of data using an I²C master, a START signal is only required at the beginning of the entire data stream. A STOP signal is only required at the end of the data stream. All intermediate data groups can use a BLANK code before the data byte and an ACK/NACK signal as appropriate after the data byte. SDA and SCL will not get reset between different STCOMM commands.

To transmit several bytes of data using SPI master, a CSBM low signal is sent at the beginning of the 1st data byte. CSBM can be held low or taken high for intermediate data groups using the appropriate code on FCOMn[3:0]. A CSBM high signal is sent at the end of the last byte of data. CSBM, SDIOM and SCKM will not get reset between different STCOMM commands.

Figure 13 shows the 24 clock cycles following STCOMM command for an I²C master in different cases. Note that if ICOMn[3:0] specified a STOP condition, after the STOP signal is sent, the SDA and SCL lines are held high and all data in the rest of the word is ignored. If ICOMn[3:0] is a NO TRANSMIT, both SDA and SCL lines are released, and the rest of the data in the word is ignored. This is used when a particular device in the stack does not have to communicate to a slave.

Figure 14 shows the 24 clock cycles following STCOMM command for a SPI master. Similar to the I²C master, if ICOMn[3:0] specified a CSBM HIGH or a NO TRANSMIT condition, the CSBM, SCKM and SDIOM lines of the SPI master are released and the rest of the data in the word is ignored.

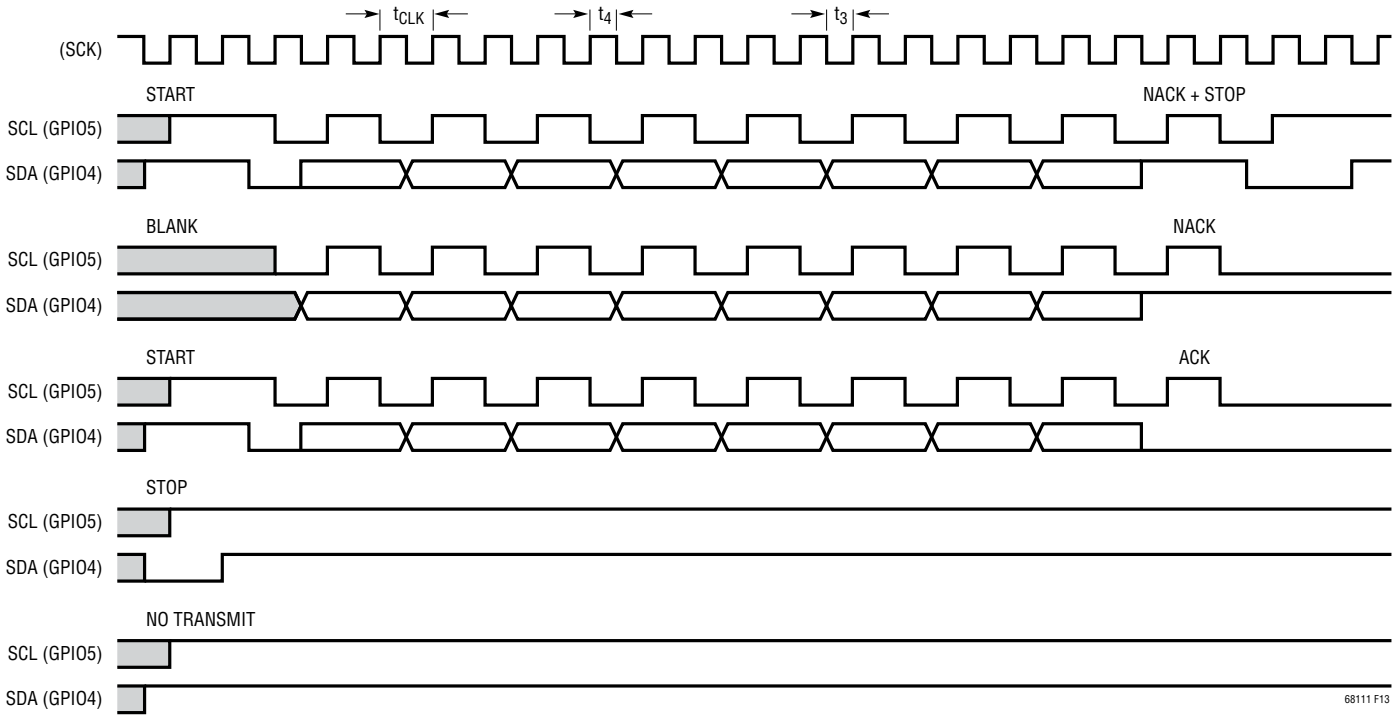


Figure 13. STCOMM Timing Diagram for an I²C Master

OPERATION

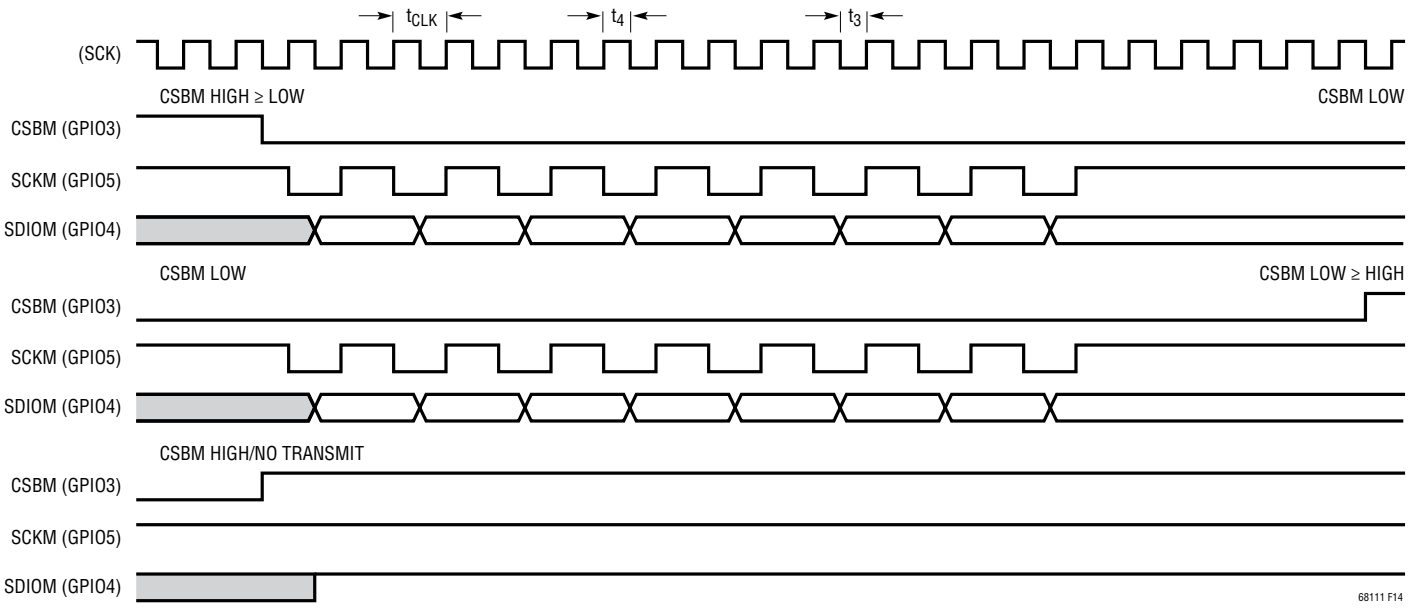


Figure 14. STCOMM Timing Diagram for a SPI Master

Timing Specifications of I²C and SPI Master

The timing of the LTC6811 I²C or SPI master will be controlled by the timing of the communication at the LTC6811's primary SPI interface. Table 22 shows the I²C master timing relationship to the primary SPI clock. Table 23 shows the SPI master timing specifications.

Table 22. I²C Master Timing

I²C MASTER PARAMETER	TIMING RELATIONSHIP TO PRIMARY SPI INTERFACE	TIMING SPECIFICATIONS AT t_{CLK} = 1µs
SCL Clock Frequency	$1/(2 \cdot t_{CLK})$	Max 500kHz
t_{HD};STA	t_3	Min 200ns
t_{LOW}	t_{CLK}	Min 1µs
t_{HIGH}	t_{CLK}	Min 1µs
t_{SU};STA	$t_{CLK} + t_4$*	Min 1.03µs
t_{HD};DAT	t_4*	Min 30ns
t_{SU};DAT	t_3	Min 200ns
t_{SU};STO	$t_{CLK} + t_4$*	Min 1.03µs
t_{BUF}	$3 \cdot t_{CLK}$	Min 3µs

* Note: When using isoSPI, t_4 is generated internally and is a minimum of 30ns. Also, $t_3 = t_{CLK} - t_4$. When using SPI, t_3 and t_4 are the low and high times of the SCK input, each with a specified minimum of 200ns.

Table 23. SPI Master Timing

SPI MASTER PARAMETER	TIMING RELATIONSHIP TO PRIMARY SPI INTERFACE	TIMING SPECIFICATIONS AT t_{CLK} = 1µs
SDIOM Valid to SCKM Rising Setup	t_3	Min 200ns
SDIOM Valid from SCKM Rising Hold	$t_{CLK} + t_4$*	Min 1.03µs
SCKM Low	t_{CLK}	Min 1µs
SCKM High	t_{CLK}	Min 1µs
SCKM Period (SCKM_Low + SCKM_High)	$2 \cdot t_{CLK}$	Min 2µs
CSBM Pulse Width	$3 \cdot t_{CLK}$	Min 3µs
SCKM Rising to CSBM Rising	$5 \cdot t_{CLK} + t_4$*	Min 5.03µs
CSBM Falling to SCKM Falling	t_3	Min 200ns
CSBM Falling to SCKM Rising	$t_{CLK} + t_3$	Min 1.2µs
SCKM Falling to SDIOM Valid	Master requires < t_{CLK}	

* Note: When using isoSPI, t_4 is generated internally and is a minimum of 30ns. Also, $t_3 = t_{CLK} - t_4$. When using SPI, t_3 and t_4 are the low and high times of the SCK input, each with a specified minimum of 200ns.

OPERATION

S PIN PULSING USING THE S CONTROL REGISTER GROUP

The S pins of the LTC6811 can be used as a simple serial interface. This is particularly useful for controlling Linear Technology's LT8584, a monolithic flyback DC/DC converter designed to actively balance large battery stacks. The LT8584 has several operating modes which are controlled through a serial interface. The LTC6811 can communicate to an LT8584 by sending a sequence of pulses on each S pin to select a specific LT8584 mode. The S Control Register Group is used to specify the behavior for each of the 12 S pins, where each nibble specifies whether the S pin should drive high, drive low, or send a pulse sequence of between 1 and 7 pulses. Table 24 shows the possible S pin behaviors that can be sent to the LT8584.

The S pin pulses occur at a pulse rate of 6.44kHz (155µs period). The pulse width will be 77.6µs. The S pin pulsing begins when the STSCTRL command is sent, after the last command PEC clock, provided that the command PEC matches. The host may then continue to clock SCK in order to poll the status of the pulsing. This polling works similarly to the ADC polling feature. The data out will remain logic low until the S pin pulsing sequence has completed.

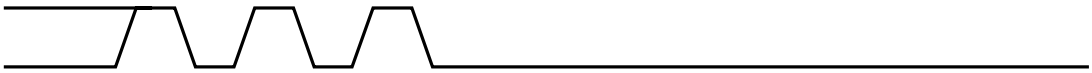
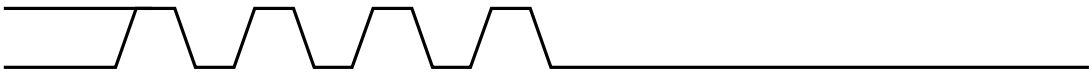
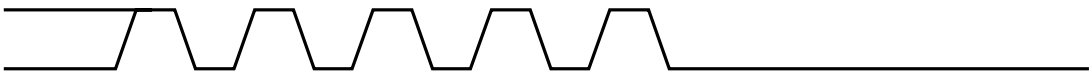
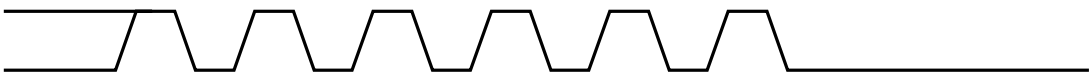
While the S pin pulsing is in progress, new STSCTRL or WRSCTRL commands are ignored. The PLADC command may be used to determine when the S pin pulsing has completed.

If the WRSCTRL command and command PEC are received correctly but the data PEC does not match, then the S Control Register Group will be cleared.

If a DCC bit in the Configuration Register Group is asserted, the LTC6811 will drive the selected S pin low, regardless of the S Control Register Group. The host should leave the DCC bits set to 0 when using the S Control Register Group.

The CLRSCTRL command can be used to quickly reset the S Control Register Group to all 0s and force the pulsing machine to release control of the S pins. This command may be helpful in reducing the diagnostic control loop time in an automotive application.

Table 24

NIBBLE VALUE	S PIN BEHAVIOR
0000	
0001	
0010	
0011	
0100	
0101	
0110	
0111	
1XXX	

OPERATION

SERIAL INTERFACE OVERVIEW

There are two types of serial ports on the LTC6811: a standard 4-wire serial peripheral interface (SPI) and a 2-wire isolated interface (isoSPI). The state of the ISOMD pin determines whether pins 41 through 44 are a 2-wire or 4-wire serial port.

There are two versions of the IC: the LTC6811-1 and the LTC6811-2. The LTC6811-1 is used in a daisy-chain configuration and the LTC6811-2 is used in an addressable bus configuration. The LTC6811-1 provides a second isoSPI interface using pins 45 through 48. The LTC6811-2 uses pins 45 through 48 to set the address of the device, by tying these pins to V^- or V_{REG}.

4-WIRE SERIAL PERIPHERAL INTERFACE (SPI) PHYSICAL LAYER

External Connections

Connecting ISOMD to V^- configures serial Port A for 4-wire SPI. The SDO pin is an open drain output which requires a pull-up resistor tied to the appropriate supply voltage (Figure 15).

Timing

The 4-wire serial port is configured to operate in a SPI system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCK. The timing is depicted in Figure 16. The maximum data rate is 1Mbps.

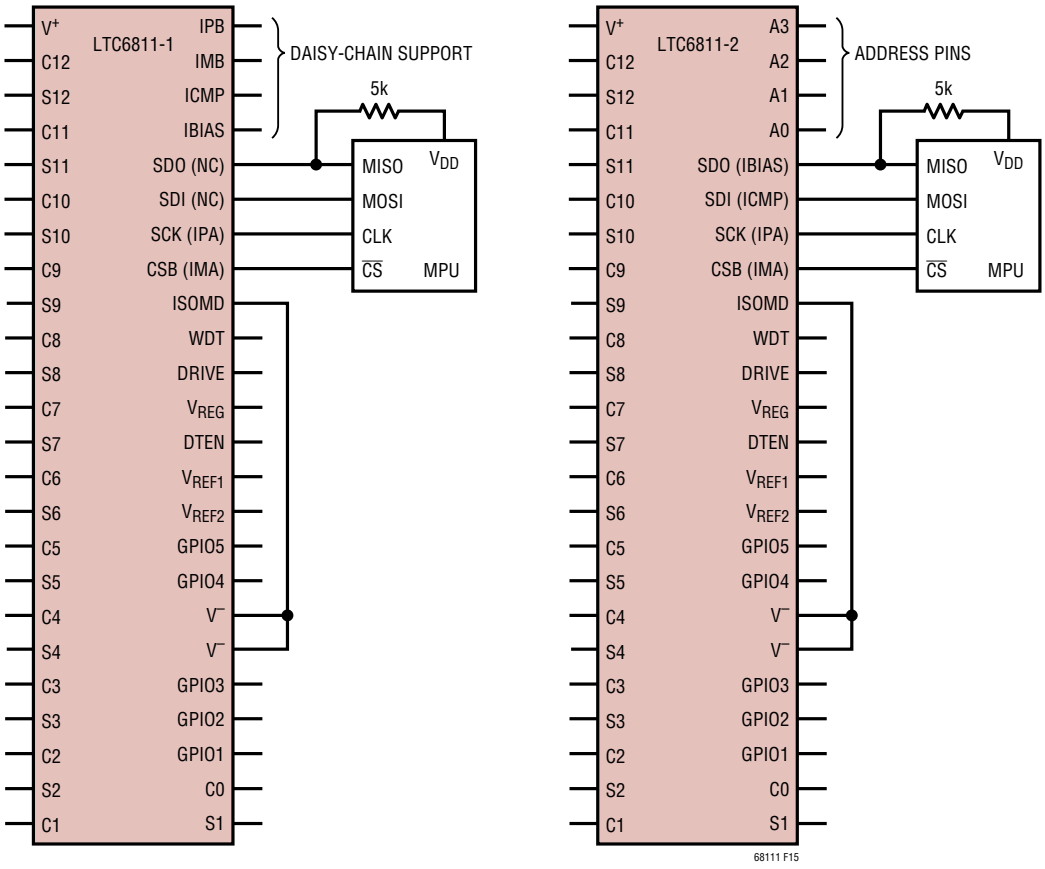


Figure 15. 4-Wire SPI Configuration

OPERATION

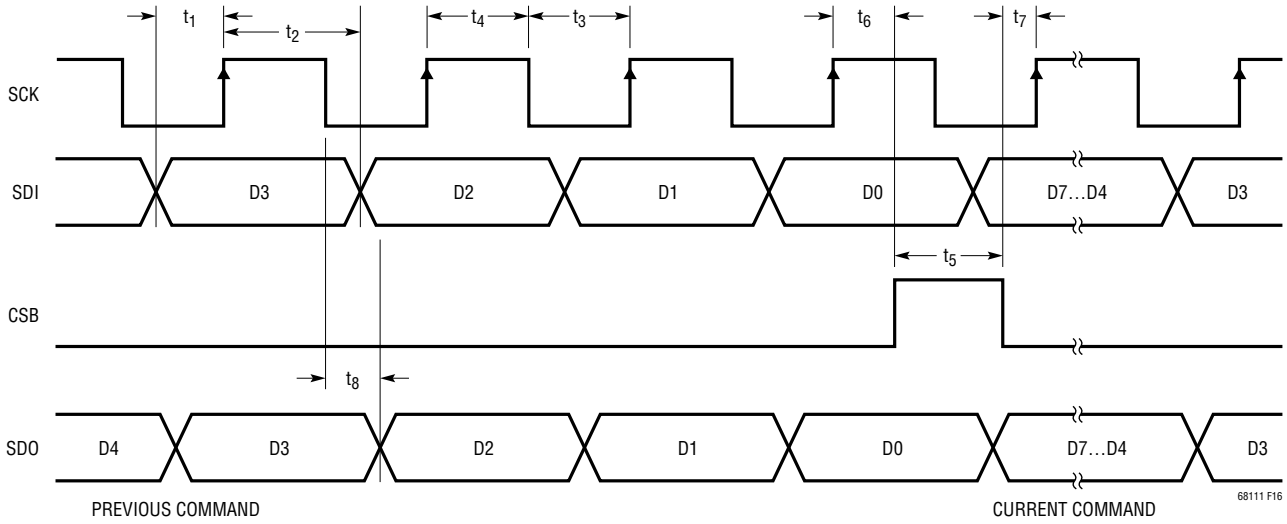


Figure 16. Timing Diagram of 4-Wire Serial Peripheral Interface

2-WIRE ISOLATED INTERFACE (isoSPI) PHYSICAL LAYER

The 2-wire interface provides a means to interconnect LTC6811 devices using simple twisted pair cabling. The interface is designed for low packet error rates when the cabling is subjected to high RF fields. Isolation is achieved through an external transformer.

Standard SPI signals are encoded into differential pulses. The strength of the transmission pulse and the threshold level of the receiver are set by two external resistors. The values of the resistors allow the user to trade off power dissipation for noise immunity.

Figure 17 illustrates how the isoSPI circuit operates. A 2V reference drives the IBIAS pin. External resistors R_{B1} and R_{B2} create the reference current I_B. This current sets the drive strength of the transmitter. R_{B1} and R_{B2} also form a voltage divider to supply a fraction of the 2V reference for the ICMP pin, which sets the threshold voltage of the receiver circuit.

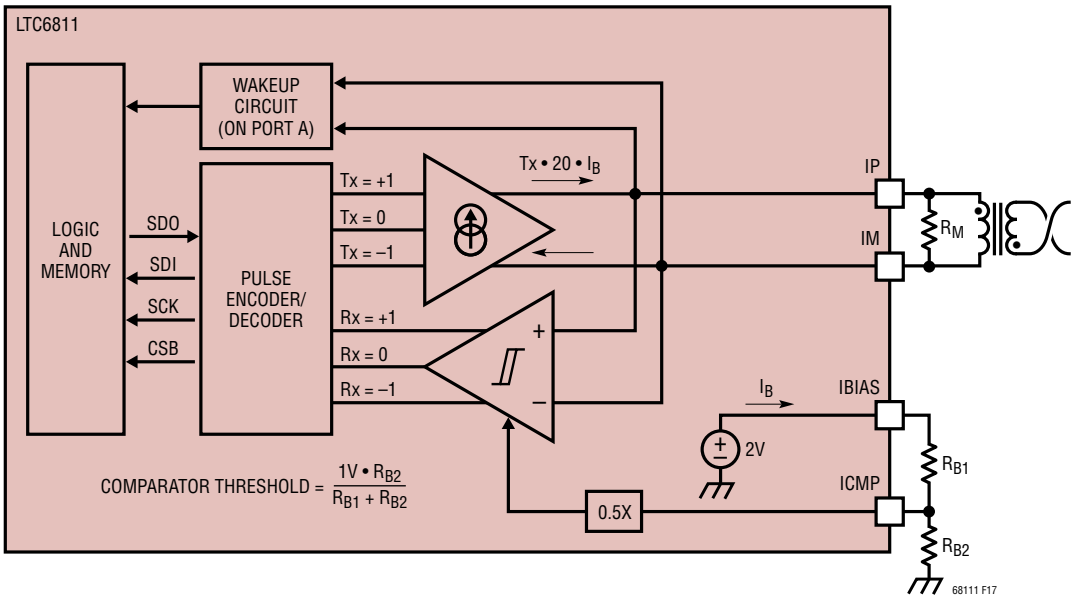


Figure 17. isoSPI Interface

OPERATION

External Connections

The LTC6811-1 has two serial ports which are called Port B and Port A. Port B is always configured as a 2-wire interface (master). Port A is either a 2-wire or 4-wire interface (slave), depending on the connection of the ISOMD pin.

Figure 18 is an example of a robust interconnection of multiple identical PCBs, each containing one LTC6811-1. The microprocessor is located on a separate PCB. To achieve 2-wire isolation between the microprocessor PCB and the 1st LTC6811-1 PCB, use the LTC6820 support IC. The LTC6820 is functionally equivalent to the diagram in Figure 17. The final LTC6811-1 in the daisy chain does not use Port B; however, the R_M should still be present.

The LTC6811-2 has a single serial port (Port A) which can be 2-wire or 4-wire, depending on the state of the ISOMD pin. When configured for 2-wire communications, several devices can be connected in a multi-drop configuration as shown in Figure 19. The LTC6820 IC is used to interface the MPU (master) to the LTC6811-2s (slaves).

Using a Single LTC6811

When only one LTC6811 is needed, the LTC6811-2 is recommended. It does not have isoSPI Port B, so it requires fewer external components and consumes less power, especially when Port A is configured as a 4-wire interface.

However, the LTC6811-1 can be used as a single (non daisy-chained) device if the second isoSPI port (Port B) is properly biased and terminated, as shown in Figures 20 and 22. ICMP should *not* be tied to GND, but can be tied directly to IBIAS. A bias resistance (2k to 20k) is required for IBIAS. Do *not* tie IBIAS directly to V_{REG} or V^-. Finally, IPB and IMB should be terminated into a 100Ω resistor (*not* tied to V_{REG} or V^-).

Selecting Bias Resistors

The adjustable signal amplitude allows the system to trade power consumption for communication robustness, and the adjustable comparator threshold allows the system to account for signal losses.

The isoSPI transmitter drive current and comparator voltage threshold are set by a resistor divider ($R_{BIAS} = R_{B1} + R_{B2}$) between IBIAS and V^-. The divided voltage is connected to the ICMP pin, which sets the comparator threshold to ½ of this voltage (V_{ICMP}). When either isoSPI interface is enabled (not IDLE) IBIAS is held at 2V, causing a current I_B to flow out of the IBIAS pin. The IP and IM pin drive currents are $20 \bullet I_B$.

As an example, if divider resistor R_{B1} is 2.8k and resistor R_{B2} is 1.21k (so that R_{BIAS} = 4k), then:

$$I_B = \frac{2V}{R_{B1} + R_{B2}} = 0.5mA$$

$$I_{DRV} = I_{IP} = I_{IM} = 20 \bullet I_B = 10mA$$

$$V_{ICMP} = 2V \bullet \frac{R_{B2}}{R_{B1} + R_{B2}} = I_B \bullet R_{B2} = 603mV$$

$$V_{TCMP} = 0.5 \bullet V_{ICMP} = 302mV$$

In this example, the pulse drive current I_{DRV} will be 10mA and the receiver comparators will detect pulses with IP-IM amplitudes greater than ±302mV.

If the isolation barrier uses 1:1 transformers connected by a twisted pair and terminated with 120Ω resistors on each end, then the transmitted differential signal amplitude (±) will be:

$$V_A = I_{DRV} \bullet \frac{R_M}{2} = 0.6V$$

(This result ignores transformer and cable losses, which may reduce the amplitude).

OPERATION

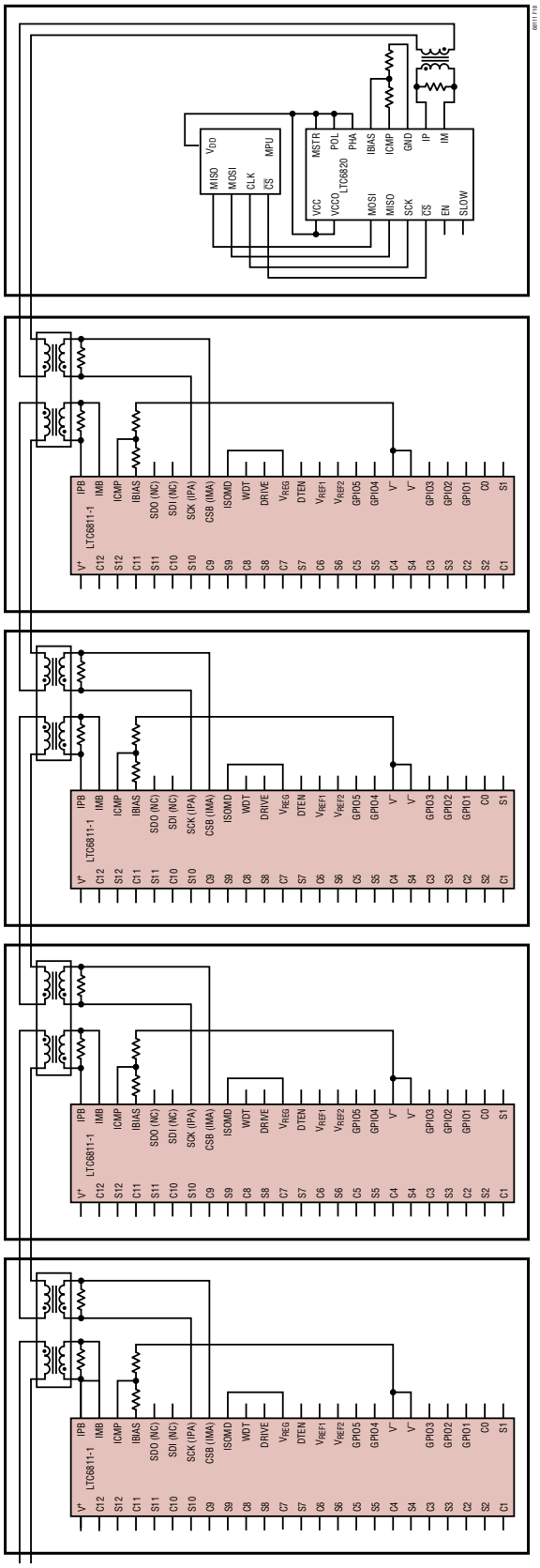


Figure 18. Transformer-Isolated Daisy-Chain Configuration Using LTC6811-1

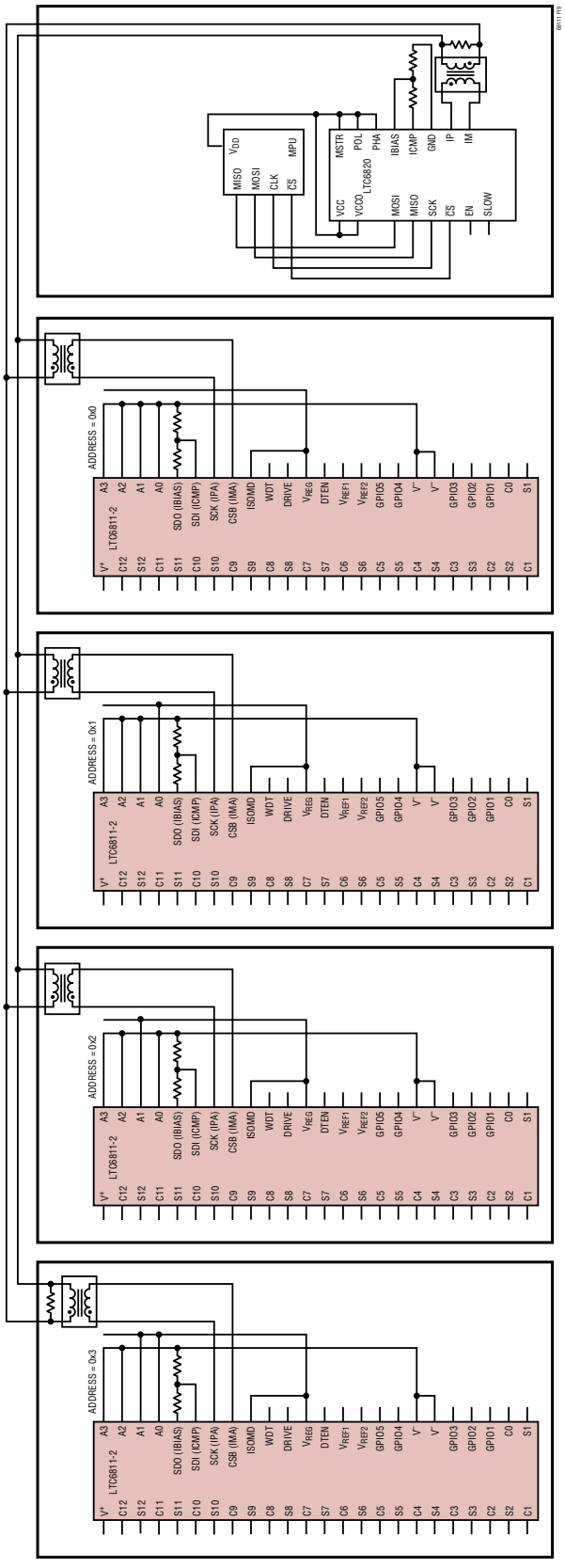


Figure 19. Multi-Drop Configuration Using LTC6811-2

OPERATION

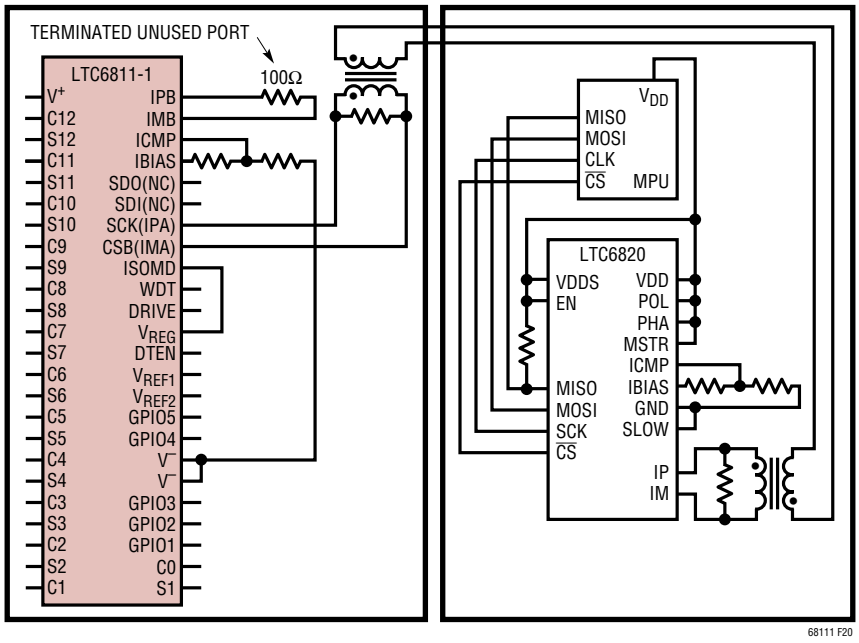


Figure 20. Single Device LTC6811-1 Using 2-Wire Port A

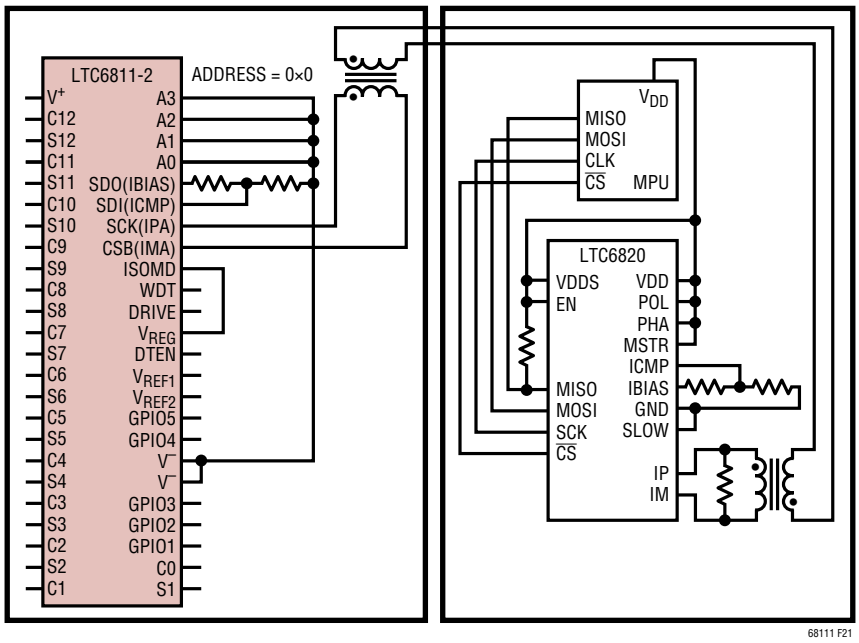


Figure 21. Single Device LTC6811-2 Using 2-Wire Port A

OPERATION

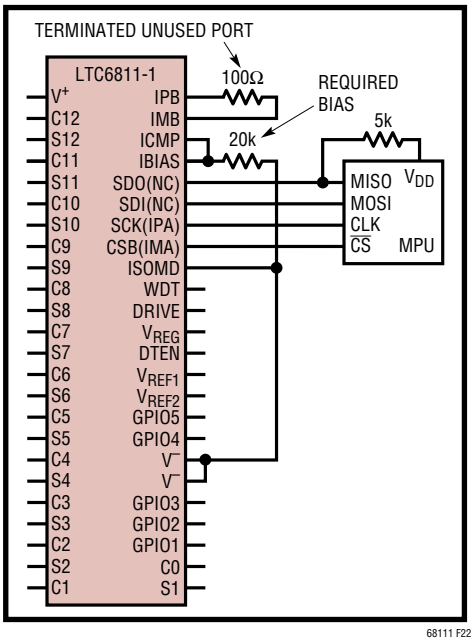


Figure 22. Single Device LTC6811-1 Using 4-Wire Port A

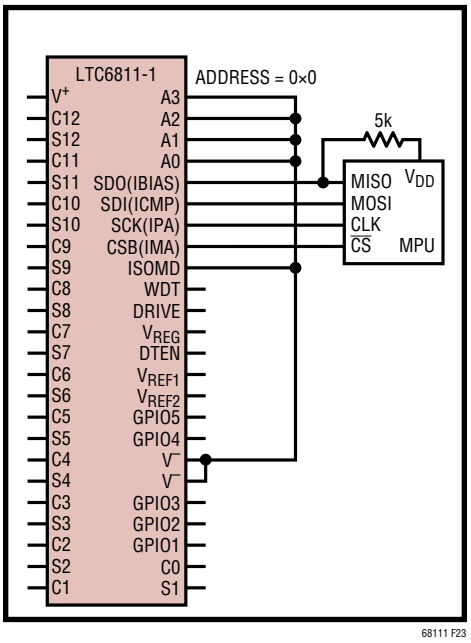


Figure 23. Single Device LTC6811-2 Using 4-Wire Port A

isoSPI Pulse Detail

Two LTC6811 devices can communicate by transmitting and receiving differential pulses back and forth through an isolation barrier. The transmitter can output three voltage levels: $+V_A$, 0V and $-V_A$. A positive output results from IP sourcing current and IM sinking current across load resistor R_M. A negative voltage is developed by IP sinking and IM sourcing. When both outputs are off, the load resistance forces the differential output to 0V.

To eliminate the DC signal component and enhance reliability, the isoSPI uses two different pulse lengths. This allows four types of pulses to be transmitted, as shown in Table 25. A +1 pulse will be transmitted as a positive pulse followed by a negative pulse. A –1 pulse will be transmitted as a negative pulse followed by a positive pulse. The duration of each pulse is defined as $t_{½PW}$, since each is half of the required symmetric pair (the total isoSPI pulse duration is $2 \cdot t_{½PW}$).

Table 25. isoSPI Pulse Types

PULSE TYPE	FIRST LEVEL ($t_{½PW}$)	SECOND LEVEL ($t_{½PW}$)	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$–V_A$ (150ns)	0V
Long –1	$–V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$–V_A$ (50ns)	0V
Short –1	$–V_A$ (50ns)	$+V_A$ (50ns)	0V

A host microcontroller does not have to generate isoSPI pulses to use this 2-wire interface. The first LTC6811 in the system can communicate to the microcontroller using the 4-wire SPI interface on its Port A, then daisy-chain to other LTC6811s using the 2-wire isoSPI interface on its Port B. Alternatively, the LTC6820 can be used to translate the SPI signals into isoSPI pulses.

OPERATION

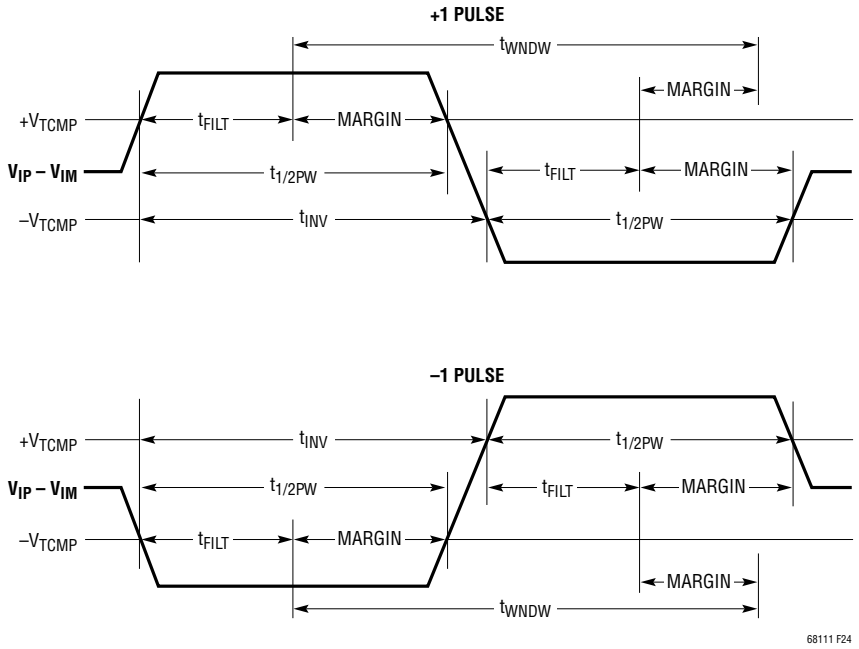


Figure 24. isoSPI Pulse Detail

LTC6811-1 Operation with Port A Configured for SPI

When the LTC6811-1 is operating with Port A as a SPI (ISOMD = V⁻), the SPI detects one of four communication events: CSB falling, CSB rising, SCK rising with SDI = 0 and SCK rising with SDI = 1. Each event is converted into one of the four pulse types for transmission through the daisy chain. Long pulses are used to transmit CSB changes and short pulses are used to transmit data, as explained in Table 26.

Table 26. Port B (Master) isoSPI Port Function

COMMUNICATION EVENT (Port A SPI)	TRANSMITTED PULSE (Port B isoSPI)
CSB Rising	Long +1
CSB Falling	Long –1
SCK Rising Edge, SDI = 1	Short +1
SCK Rising Edge, SDI = 0	Short –1

On the other side of the isolation barrier (i.e. at the other end of the cable), the 2nd LTC6811 will have ISOMD = V_{REG}. Its Port A operates as a slave isoSPI interface. It receives each transmitted pulse and reconstructs the SPI signals internally, as shown in Table 27. In addition, during a READ command this port may transmit return data pulses.

Table 27. Port A (Slave) isoSPI Port Function

RECEIVED PULSE (Port A isoSPI)	INTERNAL SPI PORT ACTION	RETURN PULSE
Long +1	Drive CSB High	None
Long –1	Drive CSB Low	
Short +1	1. Set SDI = 1 2. Pulse SCK	Short –1 pulse if reading a 0 bit
Short –1	1. Set SDI = 0 2. Pulse SCK	(No return pulse if not in READ mode or if reading a 1 bit)

The lower isoSPI port (Port A) never transmits long (CSB) pulses. Furthermore, a slave isoSPI port will only transmit short –1 pulses, never a +1 pulse. The master port recognizes a null response as a logic 1. This allows for multiple slave devices on a single cable without risk of collisions (Multi-drop).

OPERATION

Figure 25 shows the isoSPI timing diagram for a READ command to daisy-chained LTC6811-1 parts. The ISOMD pin is tied to V^- on the bottom part so its Port A is configured as a SPI port (CSB, SCK, SDI and SDO). The isoSPI signals of three stacked devices are shown labeled with the port (A or B) and part number. Note that ISO B1 and ISO A2 is actually the same signal, but shown on each end of the transmission cable that connects Parts 1 and 2. Likewise, ISO B2 and ISO A3 is the same signal, but with the cable delay shown between Parts 2 and 3.

Bits W_N-W_0 refer to the 16-bit command code and the 16-bit PEC of a READ command. At the end of Bit W_0, the three parts decode the READ command and begin shifting out data, which is valid on the next rising edge of clock SCK. Bits X_N-X_0 refer to the data shifted out by Part 1. Bits Y_N-Y_0 refer to the data shifted out by Part 2 and bits Z_N-Z_0 refer to the data shifted out by Part 3. All this data is read back from the SDO port on Part 1 in a daisy-chained fashion.

Waking Up the Serial Interface

The serial ports (SPI or isoSPI) will enter the low power IDLE state if there is no activity on Port A for a time of t_{IDLE}. The WAKEUP circuit monitors activity on pins 41 and 42.

If ISOMD = V^-, Port A is in SPI mode. Activity on the CSB or SCK pin will wake up the SPI interface. If ISOMD = V_{REG}, Port A is in isoSPI mode. Differential activity on IPA-IMA wakes up the isoSPI interface. The LTC6811 will be ready to communicate when the isoSPI state changes to READY within t_{WAKE} or t_{READY}, depending on the Core state (see Figure 1 and state descriptions for details).

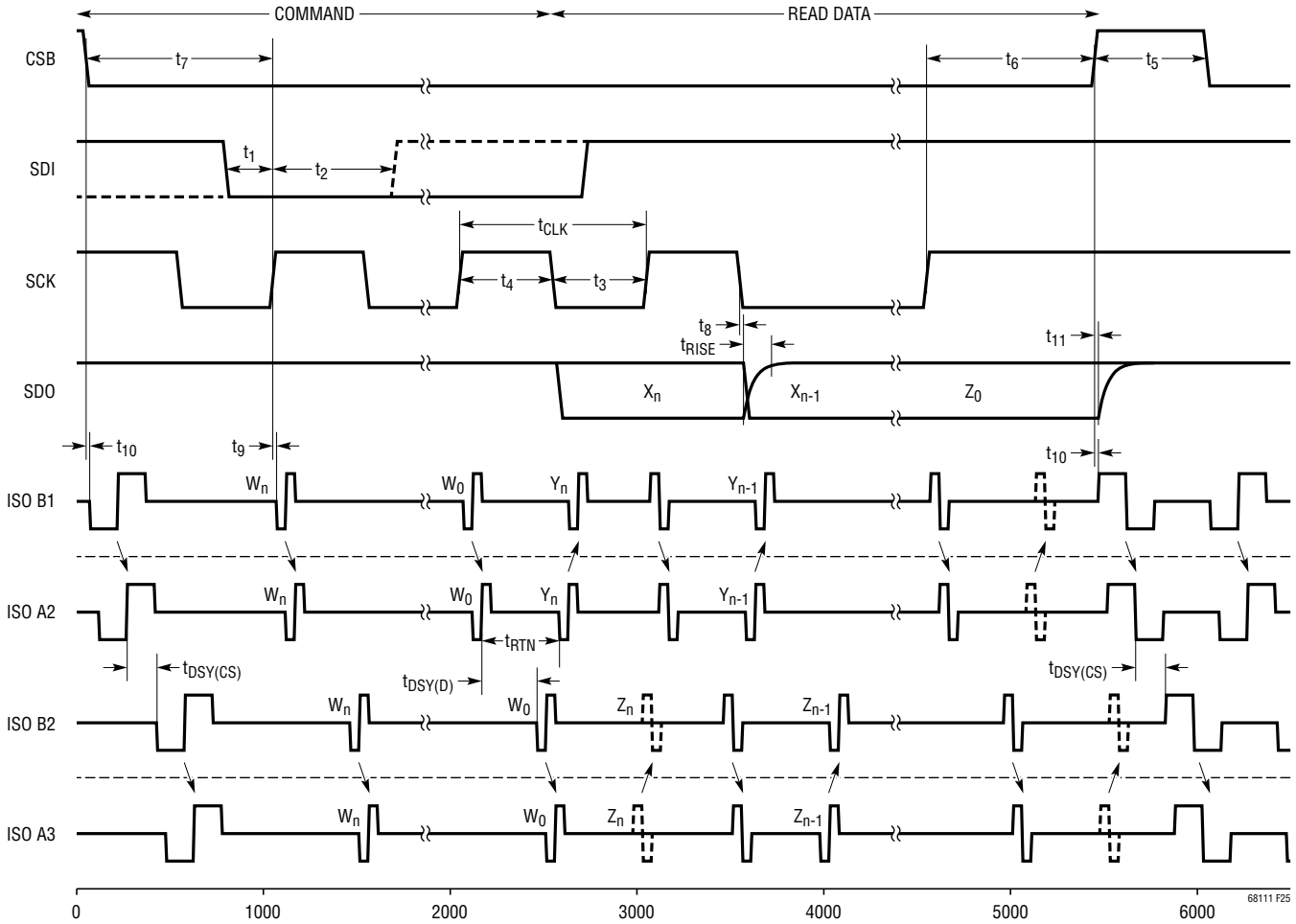


Figure 25. isoSPI Timing Diagram

OPERATION

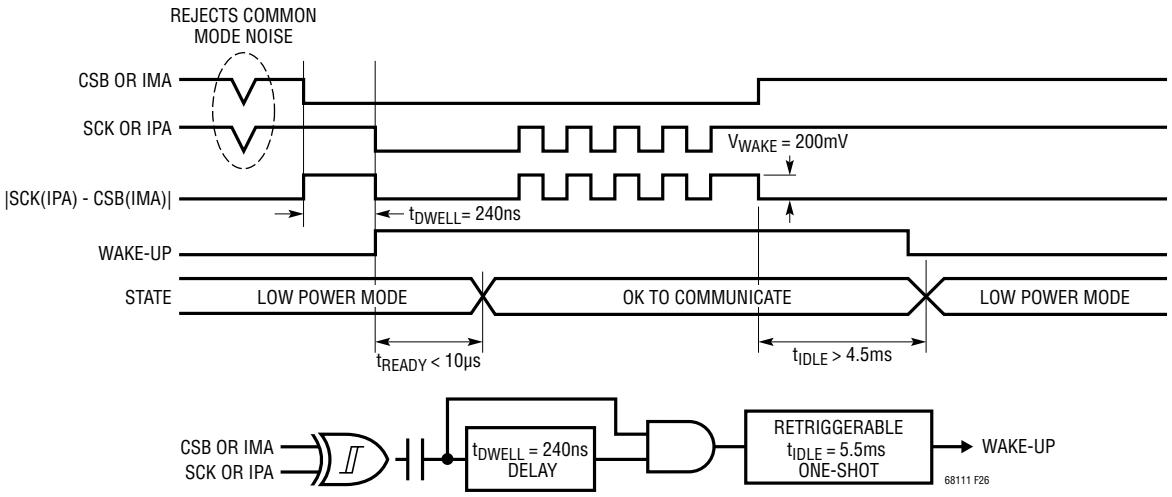


Figure 26. Wake-Up Detection and IDLE Timer

Figure 26 illustrates the timing and the functionally equivalent circuit. Common mode signals will not wake up the serial interface. The interface is designed to wake up after receiving a large signal single-ended pulse, or a low-amplitude symmetric pulse. The differential signal | SCK(IPA) – CSB(IMA)|, must be at least V_{WAKE} = 200mV for a minimum duration of t_{DWELL} = 240ns to qualify as a wake-up signal that powers up the serial interface.

Waking a Daisy Chain—Method 1

The LTC6811-1 sends a long +1 pulse on Port B after it is ready to communicate. In a daisy-chained configuration, this pulse wakes up the next device in the stack which will, in turn, wake up the next device. If there are 'N' devices in the stack, all the devices are powered up within the time N • t_{WAKE} or N • t_{READY}, depending on the Core state. For large stacks, the time N • t_{WAKE} may be equal to or larger than t_{IDLE}. In this case, after waiting longer than the time of N • t_{WAKE}, the host may send another dummy byte and wait for the time N • t_{READY}, in order to ensure that all devices are in the READY state.

Method 1 can be used when all devices on the daisy chain are in the IDLE state. This guarantees that they propagate the wake-up signal up the daisy chain. However, this method will fail to wake up all devices when a device in the middle of the chain is in the READY state instead of IDLE. When this happens, the device in READY state will not propagate the wake-up pulse, so the devices above it will remain IDLE. This situation can occur when attempting to wake up the daisy chain after only t_{IDLE} of idle time (some devices may be IDLE, some may not).

Waking a Daisy Chain—Method 2

A more robust wake-up method does not rely on the built-in wake-up pulse, but manually sends isoSPI traffic for enough time to wake the entire daisy chain. At minimum, a pair of long isoSPI pulses (–1 and +1) is needed for each device, separated by more than t_{READY} or t_{WAKE} (if the Core state is STANDBY or SLEEP, respectively), but less than t_{IDLE}. This allows each device to wake up and propagate the next pulse to the following device. This method works even if some devices in the chain are not in the IDLE state. In practice, implementing method 2 requires toggling the CSB pin (of the LTC6820, or bottom LTC6811-1 with ISOMD = 0) to generate the long isoSPI pulses. Alternatively, dummy commands (such as RDCFGA) can be executed to generate the long isoSPI pulses.

DATA LINK LAYER

All data transfers on LTC6811 occur in byte groups. Every byte consists of 8 bits. Bytes are transferred with the most significant bit (MSB) first. CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. On a write command, data is latched in on the rising edge of CSB.

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NETWORK LAYER

Packet Error Code

The Packet Error Code (PEC) is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC value of 000000000010000 and the following characteristic polynomial: $x^{15} + x^{14} + x^{10} + x^8 + x^7 + x^4 + x^3 + 1$. To calculate the 15-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group).
2. For each bit DIN coming into the PEC register group, set
   IN0 = DIN XOR PEC [14]
   IN3 = IN0 XOR PEC [2]
   IN4 = IN0 XOR PEC [3]
   IN7 = IN0 XOR PEC [6]
   IN8 = IN0 XOR PEC [7]
   IN10 = IN0 XOR PEC [9]
   IN14 = IN0 XOR PEC [13].
3. Update the 15-bit PEC as follows
   PEC [14] = IN14,
   PEC [13] = PEC [12],
   PEC [12] = PEC [11],
   PEC [11] = PEC [10],
   PEC [10] = IN10,
   PEC [9] = PEC [8],
   PEC [8] = IN8,
   PEC [7] = IN7,
   PEC [6] = PEC [5],
   PEC [5] = PEC [4],
   PEC [4] = IN4,
   PEC [3] = IN3,
   PEC [2] = PEC [1],
   PEC [1] = PEC [0],
   PEC [0] = IN0.
4. Go back to step 2 until all the data is shifted. The final PEC (16 bits) is the 15-bit value in the PEC register with a 0 bit appended to its LSB.

Figure 27 illustrates the algorithm described above. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 28. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0 bit at the LSB. For longer data streams, the PEC is valid at the end of the last bit of data sent to the PEC register.

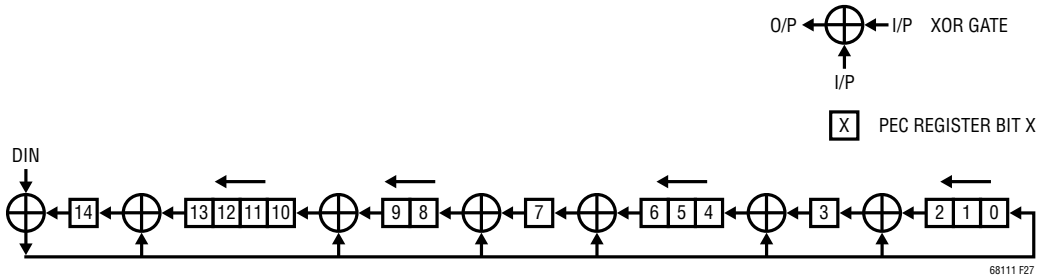

Figure 27. 15-Bit PEC Computation Circuit

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Table 28. PEC Calculation for 0x0001

PEC[14]	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	**0**
PEC[13]	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	**0**
PEC[12]	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	**1**
PEC[11]	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	**1**
PEC[10]	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	**1**
PEC[9]	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[8]	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	**0**
PEC[7]	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	**1**
PEC[6]	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0**
PEC[5]	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[4]	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	**1**
PEC[3]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	**0**
PEC[2]	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	**1**
PEC[1]	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	**1**
PEC[0]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	**1**
IN14	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		**0**
IN10	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1		**PEC Word**
IN8	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0		
IN7	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1		
IN4	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1		
IN3	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0		
IN0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
Clock Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

OPERATION

Table 29. Write/Read PEC Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PEC0	RD/WR	PEC[14]	PEC[13]	PEC[12]	PEC[11]	PEC[10]	PEC[9]	PEC[8]	PEC[7]
PEC1	RD/WR	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	0

LTC6811 calculates PEC for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. LTC6811 also attaches the calculated PEC at the end of the data it shifts out. Table 29 shows the format of PEC while writing to or reading from LTC6811.

While writing any command to LTC6811, the command bytes CMD0 and CMD1 (see Table 36 and Table 37) and the PEC bytes PEC0 and PEC1 are sent on Port A in the following order:

CMD0, CMD1, PEC0, PEC1

After a broadcast write command to daisy-chained LTC6811-1 devices, data is sent to each device followed by the PEC. For example, when writing the Configuration Register Group to two daisy-chained devices (primary device P, stacked device S), the data will be sent to the primary device on Port A in the following order:

CFGR0(S), … , CFGR5(S), PEC0(S), PEC1(S), CFGR0(P), …, CFGR5(P), PEC0(P), PEC1(P)

After a read command for daisy-chained devices, each device shifts out its data and the PEC that it computed for its data on Port A followed by the data received on Port B. For example, when reading Status Register Group B from two daisy-chained devices (primary device P, stacked device S), the primary device sends out data on port A in the following order:

STBR0(P), …, STBR5(P), PEC0(P), PEC1(P), STBR0(S), … , STBR5(S), PEC0(S), PEC1(S)

Address Commands (LTC6811-2 Only)

An address command is one in which only the addressed device on the bus responds. Address commands are used only with LTC6811-2 parts. All commands are compatible with addressing. See Bus Protocols for Address command format.

Broadcast Commands (LTC6811-1 or LTC6811-2)

A broadcast command is one to which all devices on the bus will respond, regardless of device address. This command format can be used with LTC6811-1 and LTC6811-2 parts. See Bus Protocols for Broadcast command format. With broadcast commands all devices can be sent commands simultaneously.

In parallel (LTC6811-2) configurations, broadcast commands are useful for initiating ADC conversions or for sending write commands when all parts are being written with the same data. The polling function (automatic at the end of ADC commands, or manual using the PLADC command) can also be used with broadcast commands, but not with parallel isoSPI devices. Likewise, broadcast read commands should not be used in the parallel configuration (either SPI or isoSPI).

Daisy-chained (LTC6811-1) configurations support broadcast commands only, because they have no addressing. All devices in the chain receive the command bytes simultaneously. For example, to initiate ADC conversions in a stack of devices, a single ADCV command is sent, and all devices will start conversions at the same time. For read and write commands, a single command is sent, and then the stacked devices effectively turn into a cascaded shift register, in which data is shifted through each device to the next higher (on a write) or the next lower (on a read) device in the stack. See the Serial Interface section.

Polling Methods

The simplest method to determine ADC completion is for the controller to start an ADC conversion and wait for the specified conversion time to pass before reading the results. Both LTC6811-1 and LTC6811-2 also allow polling to determine ADC completion.

In parallel configurations that communicate in SPI mode (ISOMD pin tied low), there are two methods of polling.

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The first method is to hold CSB low after an ADC conversion command is sent. After entering a conversion command, the SDO line is driven low when the device is busy performing conversions. SDO is pulled high when the device completes conversions. However, SDO will also go back high when CSB goes high even if the device has not completed the conversion (Figure 28). An addressed device drives the SDO line based on its status alone. A problem with this method is that the controller is not free to do other serial communication while waiting for ADC conversions to complete.

The next method overcomes this limitation. The controller can send an ADC start command, perform other tasks, and then send a poll ADC converter status (PLADC) command to determine the status of the ADC conversions (Figure 29). After entering the PLADC command, SDO will go low if the device is busy performing conversions. SDO is pulled high at the end of conversions. However, SDO will also go high when CSB goes high even if the device has not completed the conversion.

In parallel configurations that communicate in isoSPI mode, the low side port transmits a data pulse only in response to a master isoSPI pulse received by it. So, after entering the command in either method of polling described above, isoSPI data pulses are sent to the part to update the conversion status. These pulses can be sent using LTC6820 by simply clocking its SCK pin. In response to this pulse, the LTC6811-2 sends back a low isoSPI pulse if it is still busy performing conversions or a high data pulse if it has completed the conversions. If a CSB high isoSPI pulse is sent to the device, it exits the polling command.

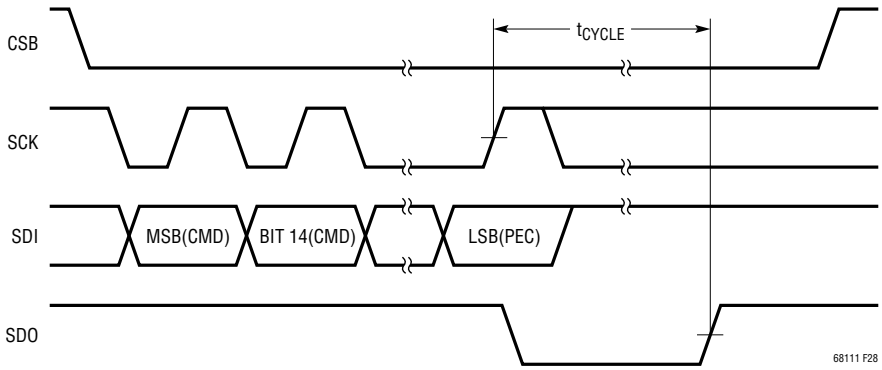

Figure 28. SDO Polling After an ADC Conversion Command (Parallel Configuration)

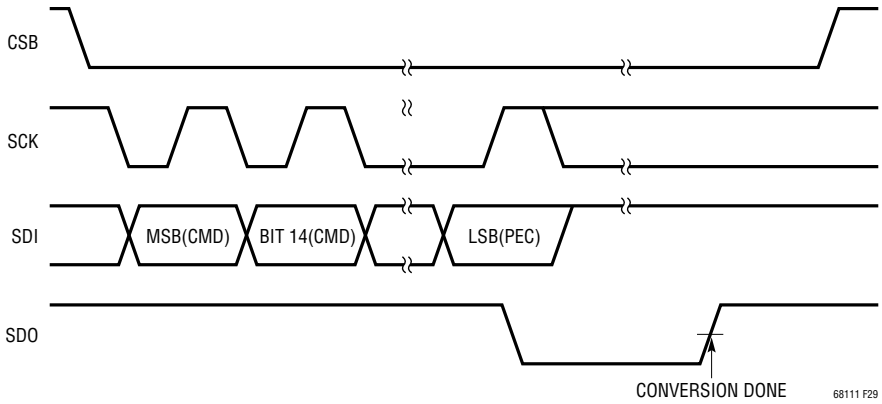

Figure 29. SDO Polling Using PLADC Command (Parallel Configuration)

OPERATION

In a daisy-chained configuration of N stacked devices, the same two polling methods can be used. If the bottom device communicates in SPI mode, the SDO of the bottom device indicates the conversion status of the entire stack i.e. SDO will remain low until all the devices in the stack have completed the conversions. In the first method of polling, after an ADC conversion command is sent, clock pulses are sent on SCK while keeping CSB low. The SDO status becomes valid only at the end of N clock pulses on SCK. During the first N clock pulses, the bottom LTC6811-1 in the daisy chain will output 0 or a low data pulse. After N clock pulses, the output data from the bottom LTC6811-1 gets updated for every clock pulse that follows (Figure 30). In the second method, the PLADC command is sent followed by clock pulses on SCK while keeping CSB low. Similar to the first method, the SDO status is valid only after N clock cycles on SCK and gets updated after every clock cycle that follows (Figure 31).

If the bottom device communicates in isoSPI mode, isoSPI data pulses are sent to the device to update the conversion status. Using LTC6820, this can be achieved by just clocking its SCK pin. The conversion status is valid only after the bottom LTC6811 device receives N isoSPI data pulses and the status gets updated for every isoSPI data pulse that follows. The device returns a low data pulse if any of the devices in the stack is busy performing conversions and returns a high data pulse if all the devices are free.

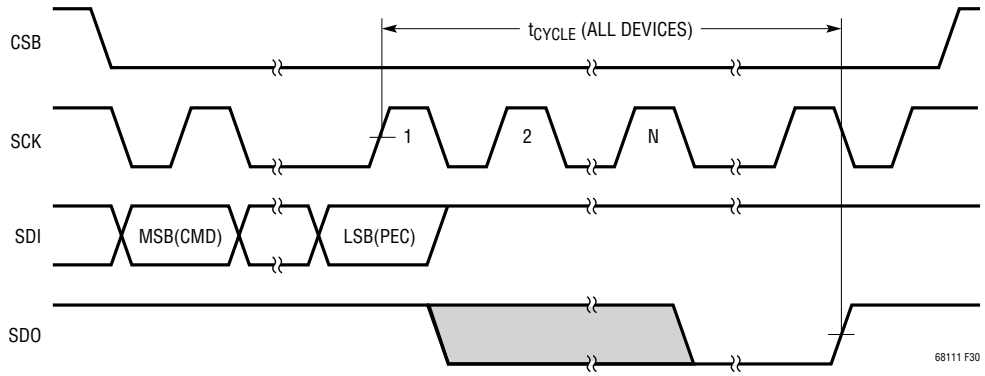

Figure 30. SDO Polling After an ADC Conversion Command (Daisy-Chain Configuration)

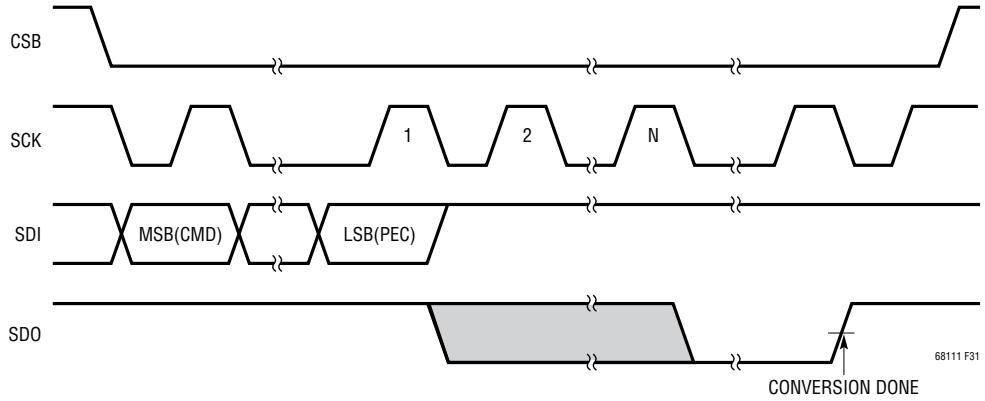

Figure 31. SDO Polling Using PLADC Command (Daisy-Chain Configuration)

OPERATION

Bus Protocols

Protocol Format: The protocol formats for both broadcast and address commands are depicted in Table 31 through Table 35. Table 30 is the key for reading the protocol diagrams.

Table 30. Protocol Key

CMD0	Command Byte 0 (See Table 36 and Table 37)
CMD1	Command Byte 1 (See Table 36 and Table 37)
PEC0	Packet Error Code Byte 0 (See Table 29)
PEC1	Packet Error Code Byte 1 (See Table 29)
n	Number of Bytes
…	Continuation of Protocol
	Master to Slave
	Slave to Master

Command Format: The formats for the broadcast and address commands are shown in Table 36 and Table 37 respectively. The 11-bit command code CC[10:0] is the same for a broadcast or an address command. A list of all the command codes is shown in Table 38. A broadcast command has a value 0 for CMD0[7] through CMD0[3]. An address command has a value 1 for CMD0[7] followed by the 4-bit address of the device (a3, a2, a1, a0) in bits CMD0[6:3]. An addressed device will respond to an address command only if the physical address of the device on pins A3 to A0 match the address specified in the address command. The PEC for broadcast and address commands must be computed on the entire 16-bit command (CMD0 and CMD1).

Table 31. Broadcast/Address Poll Command

8	8	8	8	
CMD0	CMD1	PEC0	PEC1	Poll Data

Table 32. Broadcast Write Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	Shift Byte 1	…	Shift Byte *n*

Table 33. Address Write Command

8	8	8	8	8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 34. Broadcast Read Command

8	8	8	8	8		8	8	8	8		8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1	Shift Byte 1	…	Shift Byte *n*

Table 35. Address Read Command

8	8	8	8	8		8	8	8
CMD0	CMD1	PEC0	PEC1	Data Byte Low	…	Data Byte High	PEC0	PEC1

Table 36. Broadcast Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	0	0	0	0	0	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

Table 37. Address Command Format

NAME	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	WR	1	a3*	a2*	a1*	a0*	CC[10]	CC[9]	CC[8]
CMD1	WR	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

*ax is Address Bit x

OPERATION

Commands

Table 38 lists all the commands and their options for both LTC6811-1 and LTC6811-2. The command set is backwards compatible with LTC6804.

Table 38. Command Codes

COMMAND DESCRIPTION	NAME	CC[10:0] - COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Write Configuration Register Group A	WRCFGA	0	0	0	0	0	0	0	0	0	0	1
Write Configuration Register Group B*	WRCFGB*	0	0	0	0	0	1	0	0	1	0	0
Read Configuration Register Group A	RDCFGA	0	0	0	0	0	0	0	0	0	1	0
Read Configuration Register Group B*	RDCFGB*	0	0	0	0	0	1	0	0	1	1	0
Read Cell Voltage Register Group A	RDCVA	0	0	0	0	0	0	0	0	1	0	0
Read Cell Voltage Register Group B	RDCVB	0	0	0	0	0	0	0	0	1	1	0
Read Cell Voltage Register Group C	RDCVC	0	0	0	0	0	0	0	1	0	0	0
Read Cell Voltage Register Group D	RDCVD	0	0	0	0	0	0	0	1	0	1	0
Read Cell Voltage Register Group E*	RDCVE*	0	0	0	0	0	0	0	1	0	0	1
Read Cell Voltage Register Group F*	RDCVF*	0	0	0	0	0	0	0	1	0	1	1
Read Auxiliary Register Group A	RDAUXA	0	0	0	0	0	0	0	1	1	0	0
Read Auxiliary Register Group B	RDAUXB	0	0	0	0	0	0	0	1	1	1	0
Read Auxiliary Register Group C*	RDAUXC*	0	0	0	0	0	0	0	1	1	0	1
Read Auxiliary Register Group D*	RDAUXD*	0	0	0	0	0	0	0	1	1	1	1
Read Status Register Group A	RDSTATA	0	0	0	0	0	0	1	0	0	0	0
Read Status Register Group B	RDSTATB	0	0	0	0	0	0	1	0	0	1	0
Write S Control Register Group	WRSCTRL	0	0	0	0	0	0	1	0	1	0	0
Write PWM Register Group	WRPWM	0	0	0	0	0	1	0	0	0	0	0
Write PWM/S Control Register Group B*	WRPSB*	0	0	0	0	0	0	1	1	1	0	0
Read S Control Register Group	RDSCTRL	0	0	0	0	0	0	1	0	1	1	0
Read PWM Register Group	RDPWM	0	0	0	0	0	1	0	0	0	1	0

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COMMAND DESCRIPTION	NAME	CC[10:0] - COMMAND CODE										
		10	9	8	7	6	5	4	3	2	1	0
Read PWM/S Control Register Group B*	RDPSB*	0	0	0	0	0	0	1	1	1	1	0
Start S Control Pulsing and Poll Status	STSCTRL	0	0	0	0	0	0	1	1	0	0	1
Clear S Control Register Group	CLRSCTRL	0	0	0	0	0	0	1	1	0	0	0
Start Cell Voltage ADC Conversion and Poll Status	ADCV	0	1	MD[1]	MD[0]	1	1	DCP	0	CH[2]	CH[1]	CH[0]
Start Open Wire ADC Conversion and Poll Status	ADOW	0	1	MD[1]	MD[0]	PUP	1	DCP	1	CH[2]	CH[1]	CH[0]
Start Self Test Cell Voltage Conversion and Poll Status	CVST	0	1	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Overlap Measurement of Cell 7 Voltage	ADOL	0	1	MD[1]	MD[0]	0	0	DCP	0	0	0	1
Start GPIOs ADC Conversion and Poll Status	ADAX	1	0	MD[1]	MD[0]	1	1	0	0	CHG [2]	CHG [1]	CHG [0]
Start GPIOs ADC Conversion With Digital Redundancy and Poll Status	ADAXD	1	0	MD[1]	MD[0]	0	0	0	0	CHG [2]	CHG [1]	CHG [0]
Start Self Test GPIOs Conversion and Poll Status	AXST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	0	1	1	1
Start Status Group ADC Conversion and Poll Status	ADSTAT	1	0	MD[1]	MD[0]	1	1	0	1	CHST [2]	CHST [1]	CHST [0]
Start Status Group ADC Conversion With Digital Redundancy and Poll Status	ADSTATD	1	0	MD[1]	MD[0]	0	0	0	1	CHST [2]	CHST [1]	CHST [0]
Start Self Test Status Group Conversion and Poll Status	STATST	1	0	MD[1]	MD[0]	ST[1]	ST[0]	0	1	1	1	1
Start Combined Cell Voltage and GPIO1, GPIO2 Conversion and Poll Status	ADCVAX	1	0	MD[1]	MD[0]	1	1	DCP	1	1	1	1
Start Combined Cell Voltage and SC Conversion and Poll Status	ADCVSC	1	0	MD[1]	MD[0]	1	1	DCP	0	1	1	1
Clear Cell Voltage Register Groups	CLRCELL	1	1	1	0	0	0	1	0	0	0	1
Clear Auxiliary Register Groups	CLRAUX	1	1	1	0	0	0	1	0	0	1	0
Clear Status Register Groups	CLRSTAT	1	1	1	0	0	0	1	0	0	1	1
Poll ADC Conversion Status	PLADC	1	1	1	0	0	0	1	0	1	0	0
Diagnose MUX and Poll Status	DIAGN	1	1	1	0	0	0	1	0	1	0	1
Write COMM Register Group	WRCOMM	1	1	1	0	0	1	0	0	0	0	1
Read COMM Register Group	RDCOMM	1	1	1	0	0	1	0	0	0	1	0
Start I^2C /SPI Communication	STCOMM	1	1	1	0	0	1	0	0	0	1	1

*These commands provided for forward-compatibility with LTC6813/6812.

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Table 39. Command Bit Descriptions

NAME	DESCRIPTION	VALUES								
MD[1:0]	ADC Mode	MD	ADCOPT(CFGR0[0]) = 0				ADCOPT(CFGR0[0]) = 1			
		00	422Hz Mode				1kHz Mode			
		01	27kHz Mode (Fast)				14kHz Mode			
		10	7kHz Mode (Normal)				3kHz Mode			
		11	26Hz Mode (Filtered)				2kHz Mode			
DCP	Discharge Permitted	DCP								
		0	Discharge Not Permitted							
		1	Discharge Permitted							
CH[2:0]	Cell Selection for ADC Conversion			Total Conversion Time in the 8 ADC Modes						
		CH		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		000	All Cells	1.1ms	1.3ms	2.3ms	3.0ms	4.4ms	7.2ms	12.8ms	201ms
		001	Cell 1 and Cell 7	201µs	230µs	405µs	501µs	754µs	1.2ms	2.2ms	34ms
		010	Cell 2 and Cell 8								
		011	Cell 3 and Cell 9								
		100	Cell 4 and Cell 10								
		101	Cell 5 and Cell 11								
		110	Cell 6 and Cell 12								
PUP	Pull-Up/Pull-Down Current for Open Wire Conversions	PUP								
		0	Pull-Down Current							
		1	Pull-Up Current							
ST[1:0]	Self Test Mode Selection			Self Test Conversion Result						
		ST		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		01	Self Test 1	0x9565	0x9553	0x9555	0x9555	0x9555	0x9555	0x9555	0x9555
		10	Self Test 2	0x6A9A	0x6AAC	0x6AAA	0x6AAA	0x6AAA	0x6AAA	0x6AAA	0x6AAA
CHG[2:0]	GPIO Selection for ADC Conversion			Total Conversion Time in the 8 ADC Modes						
		CHG		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		000	GPIO 1-5, 2nd Ref	1.1ms	1.3ms	2.3ms	3.0ms	4.4ms	7.2ms	12.8ms	201ms
		001	GPIO 1	201µs	230µs	405µs	501µs	754µs	1.2ms	2.2ms	34ms
		010	GPIO 2								
		011	GPIO 3								
		100	GPIO 4								
		101	GPIO 5								
		110	2nd Reference								
CHST[2:0]*	Status Group Selection			Total Conversion Time in the 8 ADC Modes						
		CHST		27kHz	14kHz	7kHz	3kHz	2kHz	1kHz	422Hz	26Hz
		000	SC, ITMP, VA, VD	748µs	865µs	1.6ms	2.0ms	3.0ms	4.8ms	8.5ms	134ms
		001	SC	201µs	230µs	405µs	501µs	754µs	1.2ms	2.2ms	34ms
		010	ITMP								
		011	VA								
		100	VD								

*Note: Valid options for CHST in ADSTAT command are 0-4. If CHST is set to 5/6 in ADSTAT command, the LTC6811 treats it like ADAX command with CHG = 5/6.

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Memory Map

Table 40. Configuration Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CFGR0	RD/WR	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	REFON	DTEN	ADCOPT
CFGR1	RD/WR	VUV[7]	VUV[6]	VUV[5]	VUV[4]	VUV[3]	VUV[2]	VUV[1]	VUV[0]
CFGR2	RD/WR	VOV[3]	VOV[2]	VOV[1]	VOV[0]	VUV[11]	VUV[10]	VUV[9]	VUV[8]
CFGR3	RD/WR	VOV[11]	VOV[10]	VOV[9]	VOV[8]	VOV[7]	VOV[6]	VOV[5]	VOV[4]
CFGR4	RD/WR	DCC8	DCC7	DCC6	DCC5	DCC4	DCC3	DCC2	DCC1
CFGR5	RD/WR	DCTO[3]	DCTO[2]	DCTO[1]	DCTO[0]	DCC12	DCC11	DCC10	DCC9

Table 41. Cell Voltage Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVAR0	RD	C1V[7]	C1V[6]	C1V[5]	C1V[4]	C1V[3]	C1V[2]	C1V[1]	C1V[0]
CVAR1	RD	C1V[15]	C1V[14]	C1V[13]	C1V[12]	C1V[11]	C1V[10]	C1V[9]	C1V[8]
CVAR2	RD	C2V[7]	C2V[6]	C2V[5]	C2V[4]	C2V[3]	C2V[2]	C2V[1]	C2V[0]
CVAR3	RD	C2V[15]	C2V[14]	C2V[13]	C2V[12]	C2V[11]	C2V[10]	C2V[9]	C2V[8]
CVAR4	RD	C3V[7]	C3V[6]	C3V[5]	C3V[4]	C3V[3]	C3V[2]	C3V[1]	C3V[0]
CVAR5	RD	C3V[15]	C3V[14]	C3V[13]	C3V[12]	C3V[11]	C3V[10]	C3V[9]	C3V[8]

Table 42. Cell Voltage Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVBR0	RD	C4V[7]	C4V[6]	C4V[5]	C4V[4]	C4V[3]	C4V[2]	C4V[1]	C4V[0]
CVBR1	RD	C4V[15]	C4V[14]	C4V[13]	C4V[12]	C4V[11]	C4V[10]	C4V[9]	C4V[8]
CVBR2	RD	C5V[7]	C5V[6]	C5V[5]	C5V[4]	C5V[3]	C5V[2]	C5V[1]	C5V[0]
CVBR3	RD	C5V[15]	C5V[14]	C5V[13]	C5V[12]	C5V[11]	C5V[10]	C5V[9]	C5V[8]
CVBR4	RD	C6V[7]	C6V[6]	C6V[5]	C6V[4]	C6V[3]	C6V[2]	C6V[1]	C6V[0]
CVBR5	RD	C6V[15]	C6V[14]	C6V[13]	C6V[12]	C6V[11]	C6V[10]	C6V[9]	C6V[8]

Table 43. Cell Voltage Register Group C

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVCR0	RD	C7V[7]	C7V[6]	C7V[5]	C7V[4]	C7V[3]	C7V[2]	C7V[1]	C7V[0]
CVCR1	RD	C7V[15]	C7V[14]	C7V[13]	C7V[12]	C7V[11]	C7V[10]	C7V[9]	C7V[8]
CVCR2*	RD	C8V[7]*	C8V[6]*	C8V[5]*	C8V[4]*	C8V[3]*	C8V[2]*	C8V[1]*	C8V[0]*
CVCR3*	RD	C8V[15]*	C8V[14]*	C8V[13]*	C8V[12]*	C8V[11]*	C8V[10]*	C8V[9]*	C8V[8]*
CVCR4	RD	C9V[7]	C9V[6]	C9V[5]	C9V[4]	C9V[3]	C9V[2]	C9V[1]	C9V[0]
CVCR5	RD	C9V[15]	C9V[14]	C9V[13]	C9V[12]	C9V[11]	C9V[10]	C9V[9]	C9V[8]

*After performing the ADOL command, CVCR2 and CVCR3 of Cell Voltage Register Group C will contain the result of measuring Cell 7 from ADC1.

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Table 44. Cell Voltage Register Group D

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CVDR0	RD	C10V[7]	C10V[6]	C10V[5]	C10V[4]	C10V[3]	C10V[2]	C10V[1]	C10V[0]
CVDR1	RD	C10V[15]	C10V[14]	C10V[13]	C10V[12]	C10V[11]	C10V[10]	C10V[9]	C10V[8]
CVDR2	RD	C11V[7]	C11V[6]	C11V[5]	C11V[4]	C11V[3]	C11V[2]	C11V[1]	C11V[0]
CVDR3	RD	C11V[15]	C11V[14]	C11V[13]	C11V[12]	C11V[11]	C11V[10]	C11V[9]	C11V[8]
CVDR4	RD	C12V[7]	C12V[6]	C12V[5]	C12V[4]	C12V[3]	C12V[2]	C12V[1]	C12V[0]
CVDR5	RD	C12V[15]	C12V[14]	C12V[13]	C12V[12]	C12V[11]	C12V[10]	C12V[9]	C12V[8]

Table 45. Auxiliary Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVAR0	RD	G1V[7]	G1V[6]	G1V[5]	G1V[4]	G1V[3]	G1V[2]	G1V[1]	G1V[0]
AVAR1	RD	G1V[15]	G1V[14]	G1V[13]	G1V[12]	G1V[11]	G1V[10]	G1V[9]	G1V[8]
AVAR2	RD	G2V[7]	G2V[6]	G2V[5]	G2V[4]	G2V[3]	G2V[2]	G2V[1]	G2V[0]
AVAR3	RD	G2V[15]	G2V[14]	G2V[13]	G2V[12]	G2V[11]	G2V[10]	G2V[9]	G2V[8]
AVAR4	RD	G3V[7]	G3V[6]	G3V[5]	G3V[4]	G3V[3]	G3V[2]	G3V[1]	G3V[0]
AVAR5	RD	G3V[15]	G3V[14]	G3V[13]	G3V[12]	G3V[11]	G3V[10]	G3V[9]	G3V[8]

Table 46. Auxiliary Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AVBR0	RD	G4V[7]	G4V[6]	G4V[5]	G4V[4]	G4V[3]	G4V[2]	G4V[1]	G4V[0]
AVBR1	RD	G4V[15]	G4V[14]	G4V[13]	G4V[12]	G4V[11]	G4V[10]	G4V[9]	G4V[8]
AVBR2	RD	G5V[7]	G5V[6]	G5V[5]	G5V[4]	G5V[3]	G5V[2]	G5V[1]	G5V[0]
AVBR3	RD	G5V[15]	G5V[14]	G5V[13]	G5V[12]	G5V[11]	G5V[10]	G5V[9]	G5V[8]
AVBR4	RD	REF[7]	REF[6]	REF[5]	REF[4]	REF[3]	REF[2]	REF[1]	REF[0]
AVBR5	RD	REF[15]	REF[14]	REF[13]	REF[12]	REF[11]	REF[10]	REF[9]	REF[8]

Table 47. Status Register Group A

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STAR0	RD	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
STAR1	RD	SC[15]	SC[14]	SC[13]	SC[12]	SC[11]	SC[10]	SC[9]	SC[8]
STAR2	RD	ITMP[7]	ITMP[6]	ITMP[5]	ITMP[4]	ITMP[3]	ITMP[2]	ITMP[1]	ITMP[0]
STAR3	RD	ITMP[15]	ITMP[14]	ITMP[13]	ITMP[12]	ITMP[11]	ITMP[10]	ITMP[9]	ITMP[8]
STAR4	RD	VA[7]	VA[6]	VA[5]	VA[4]	VA[3]	VA[2]	VA[1]	VA[0]
STAR5	RD	VA[15]	VA[14]	VA[13]	VA[12]	VA[11]	VA[10]	VA[9]	VA[8]

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Table 48. Status Register Group B

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STBR0	RD	VD[7]	VD[6]	VD[5]	VD[4]	VD[3]	VD[2]	VD[1]	VD[0]
STBR1	RD	VD[15]	VD[14]	VD[13]	VD[12]	VD[11]	VD[10]	VD[9]	VD[8]
STBR2	RD	C4OV	C4UV	C3OV	C3UV	C2OV	C2UV	C1OV	C1UV
STBR3	RD	C8OV	C8UV	C7OV	C7UV	C6OV	C6UV	C5OV	C5UV
STBR4	RD	C12OV	C12UV	C11OV	C11UV	C10OV	C10UV	C9OV	C9UV
STBR5	RD	REV[3]	REV[2]	REV[1]	REV[0]	RSVD	RSVD	MUXFAIL	THSD

Table 49. COMM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMM0	RD/WR	ICOM0[3]	ICOM0[2]	ICOM0[1]	ICOM0[0]	D0[7]	D0[6]	D0[5]	D0[4]
COMM1	RD/WR	D0[3]	D0[2]	D0[1]	D0[0]	FCOM0[3]	FCOM0[2]	FCOM0[1]	FCOM0[0]
COMM2	RD/WR	ICOM1[3]	ICOM1[2]	ICOM1[1]	ICOM1[0]	D1[7]	D1[6]	D1[5]	D1[4]
COMM3	RD/WR	D1[3]	D1[2]	D1[1]	D1[0]	FCOM1[3]	FCOM1[2]	FCOM1[1]	FCOM1[0]
COMM4	RD/WR	ICOM2[3]	ICOM2[2]	ICOM2[1]	ICOM2[0]	D2[7]	D2[6]	D2[5]	D2[4]
COMM5	RD/WR	D2[3]	D2[2]	D2[1]	D2[0]	FCOM2[3]	FCOM2[2]	FCOM2[1]	FCOM2[0]

Table 50. S Control Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SCTRL0	RD/WR	SCTL2[3]	SCTL2[2]	SCTL2 [1]	SCTL2[0]	SCTL1[3]	SCTL1[2]	SCTL1[1]	SCTL1[0]
SCTRL1	RD/WR	SCTL4[3]	SCTL4[2]	SCTL4[1]	SCTL4[0]	SCTL3[3]	SCTL3[2]	SCTL3[1]	SCTL3[0]
SCTRL2	RD/WR	SCTL6[3]	SCTL6[2]	SCTL6[1]	SC6TL[0]	SCTL5[3]	SCTL5[2]	SCTL5[1]	SCTL5[0]
SCTRL3	RD/WR	SCTL8[3]	SCTL8[2]	SCTL8[1]	SCTL8[0]	SCTL7[3]	SCTL7[2]	SCTL7[1]	SCTL7[0]
SCTRL4	RD/WR	SCTL10[3]	SCTL10[2]	SCTL10[1]	SCTL10[0]	SCTL9[3]	SCTL9[2]	SCTL9[1]	SCTL9[0]
SCTRL5	RD/WR	SCTL12[3]	SCTL12[2]	SCTL12[1]	SCTL12[0]	SCTL11[3]	SCTL11[2]	SCTL11[1]	SCTL11[0]

Table 51. PWM Register Group

REGISTER	RD/WR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWMR0	RD/WR	PWM2[3]	PWM2[2]	PWM2 [1]	PWM2[0]	PWM1[3]	PWM1[2]	PWM1[1]	PWM1[0]
PWMR1	RD/WR	PWM4[3]	PWM4[2]	PWM4[1]	PWM4[0]	PWM3[3]	PWM3[2]	PWM3[1]	PWM3[0]
PWMR2	RD/WR	PWM6[3]	PWM6[2]	PWM6[1]	PWM6[0]	PWM5[3]	PWM5[2]	PWM5[1]	PWM5[0]
PWMR3	RD/WR	PWM8[3]	PWM8[2]	PWM8[1]	PWM8[0]	PWM7[3]	PWM7[2]	PWM7[1]	PWM7[0]
PWMR4	RD/WR	PWM10[3]	PWM10[2]	PWM10[1]	PWM10[0]	PWM9[3]	PWM9[2]	PWM9[1]	PWM9[0]
PWMR5	RD/WR	PWM12[3]	PWM12[2]	PWM12[1]	PWM12[0]	PWM11[3]	PWM11[2]	PWM11[1]	PWM11[0]

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Table 52. Memory Bit Descriptions

NAME	DESCRIPTION	VALUES
GPIOx	GPIOx Pin Control	Write: 0 -> GPIOx Pin Pull-Down ON; 1-> GPIOx Pin Pull-Down OFF (Default) Read: 0 -> GPIOx Pin at Logic 0; 1 -> GPIOx Pin at Logic 1
REFON	References sPowered Up	1 -> References Remain Powered Up Until Watchdog Timeout 0 -> References Shut Down After Conversions (Default)
DTEN	Discharge Timer Enable (READ ONLY)	1 -> Enables the Discharge Timer for Discharge Switches 0 -> Disables Discharge Timer
ADCOPT	ADC Mode Option Bit	ADCOPT: 0 -> Selects Modes 27kHz, 7kHz, 422Hz or 26Hz with MD[1:0] Bits in ADC Conversion Commands (Default) 1 -> Selects Modes 14kHz, 3kHz, 1kHz or 2kHz with MD[1:0] Bits in ADC Conversion Commands
VUV	Undervoltage Comparison Voltage*	Comparison Voltage = (VUV + 1) • 16 • 100µV Default: VUV = 0x000
VOV	Overvoltage Comparison Voltage*	Comparison Voltage = VOV • 16 • 100µV Default: VOV = 0x000
DCC[x]	Discharge Cell x	x = 1 to 12 1 -> Turn ON Shorting Switch for Cell x 0 -> Turn OFF Shorting Switch for Cell x (Default)

DCTO	Discharge Time Out Value																	
		DCTO (Write)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		Time (Min)	Disabled	0.5	1	2	3	4	5	10	15	20	30	40	60	75	90	120
		DCTO (Read)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		Time Left (Min)	Disabled or Timeout	0 to 0.5	0.5 to 1	1 to 2	2 to 3	3 to 4	4 to 5	5 to 10	10 to 15	15 to 20	20 to 30	30 to 40	40 to 60	60 to 75	75 to 90	90 to 120

CxV	Cell x Voltage*	x = 1 to 12 16-Bit ADC Measurement Value for Cell x Cell Voltage for Cell x = CxV • 100µV CxV is Reset to 0xFFFF on Power-Up and After Clear Command
GxV	GPIO x Voltage*	x = 1 to 5 16-Bit ADC Measurement Value for GPIOx Voltage for GPIOx = GxV • 100µV GxV is Reset to 0xFFFF on Power-Up and After Clear Command
REF	2nd Reference Voltage*	16-Bit ADC Measurement Value for 2nd Reference Voltage for 2nd Reference = REF • 100µV **Normal Range is within 2.99V to 3.01V, Allowing for Variations of V_{REF2} Voltage and ADC TME as Well as Additional Margin to Prevent a False Fault from Being Reported**
SC	Sum of All Cells Measurement*	16-Bit ADC Measurement Value of the Sum of All Cell Voltages Sum of All Cells Voltage = SC • 100µV • 20
ITMP	Internal Die Temperature*	16-Bit ADC Measurement Value of Internal Die Temperature **Temperature Measurement (°C) = ITMP • 100µV/7.5mV/°C – 273°C**
VA	Analog Power Supply Voltage*	16-Bit ADC Measurement Value of Analog Power Supply Voltage Analog Power Supply Voltage = VA • 100µV **The value of VA is set by external components and should be in the range 4.5V to 5.5V for normal operation**
VD	Digital Power Supply Voltage*	16-bit ADC Measurement Value of Digital Power Supply Voltage Digital Power Supply Voltage = VD • 100µV **Normal Range is within 2.7V to 3.6V**
CxOV	Cell x Overvoltage Flag	x = 1 to 12 Cell Voltage Compared to VOV Comparison Voltage 0 -> Cell x Not Flagged for Overvoltage Condition; 1-> Cell x Flagged

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NAME	DESCRIPTION	VALUES					
CxUV	Cell x Undervoltage Flag	x = 1 to 12 Cell Voltage Compared to VUV Comparison Voltage 0 -> Cell x Not Flagged for Undervoltage Condition; 1-> Cell x Flagged					
REV	Revision Code	Device Revision Code					
RSVD	Reserved Bits	Read: Read Back Value Is Always 0					
MUXFAIL	Multiplexer Self Test result	Read: 0 -> Multiplexer Passed Self Test; 1 -> Multiplexer Failed Self Test					
THSD	Thermal Shutdown Status	Read: 0 -> Thermal Shutdown Has Not Occurred; 1 -> Thermal Shutdown Has Occurred THSD Bit Cleared to 0 on Read of Status Register Group B					
SCTLx[x]	S Pin Control Bits	0000 – Drive S Pin High (De-asserted) 0001 – Send 1 High Pulse on S Pin 0010 – Send 2 High Pulses on S Pin 0011 – Send 3 High Pulses on S Pin 0100 – Send 4 High Pulses on S Pin 0101 – Send 5 High Pulses on S Pin 0110 – Send 6 High Pulses on S Pin 0111 – Send 7 High Pulses on S Pin 1XXX – Drive S Pin Low (Asserted)					
PWMx[x]	PWM Discharge Control	0000 – Selects 0% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired 0001 – Selects 6.7% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired 0010 – Selects 13.3% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired … 1110 – Selects 93.3% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired 1111 – Selects 100% Discharge Duty Cycle if DCCx = 1 and Watchdog Timer Has Expired					
ICOMn	Initial Communication Control Bits	Write	I^2C	0110	0001	0000	0111
				START	STOP	BLANK	NO TRANSMIT
			SPI	1000	1010	1001	1111
				CSB Low	CSB Falling Edge	CSB High	NO TRANSMIT
		Read	I^2C	0110	0001	0000	0111
				START from Master	STOP from Master	SDA Low Between Bytes	SDA High Between Bytes
			SPI	0111			
Dn	I^2C/SPI Communication Data Byte	Data Transmitted (Received) to (from) I^2C/SPI Slave Device					
FCOMn	Final Communication Control Bits	Write	I^2C	0000		1000	1001
				Master ACK		Master NACK	Master NACK + STOP
			SPI	X000		1001	
				CSB Low		CSB High	
		Read	I^2C	0000	0111	1111	0001	1001
				ACK from Master	ACK from Slave	NACK from Slave	ACK from Slave + STOP from Master	NACK from Slave + STOP from Master
			SPI	1111				

*Voltage equations use the decimal value of registers, 0 to 4095 for 12 bits and 0 to 65535 for 16 bits.

APPLICATIONS INFORMATION

PROVIDING DC POWER

Simple Linear Regulator

The primary supply pin for the LTC6811 is the 5V (±0.5V) V_{REG} input pin. To generate the required 5V supply for V_{REG}, the DRIVE pin can be used to form a discrete regulator with the addition of a few external components, as shown in Figure 32. The DRIVE pin provides a 5.7V output, capable of sourcing 1mA. When buffered with an NPN transistor, this provides a stable 5V over temperature. The NPN transistor should be chosen to have a sufficient Beta over temperature (>40) to supply the necessary supply current. The peak V_{REG} current requirement of the LTC6811 approaches 30mA when simultaneously communicating over isoSPI and making ADC conversions. If the V_{REG} pin is required to support any additional load, a transistor with an even higher Beta may be required.

The NPN collector can be powered from any voltage source that is a minimum 6V above V^-. This includes the cells that are being monitored, or an unregulated power supply. A 100Ω/100nF RC decoupling network is recommended for the collector power connection to protect the NPN from transients. The emitter of the NPN should be bypassed with a 1µF capacitor. Larger capacitance should be avoided since this will increase the wake-up time of the LTC6811. Some attention should be given to the thermal characteristic of the NPN, as there can be significant heating with a high collector voltage.

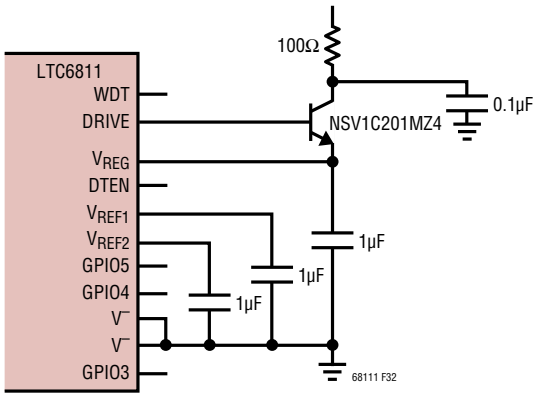

Figure 32. Simple V_{REG} Power Source Using NPN Pass Transistor

Improved Regulator Power Efficiency

For improved efficiency when powering the LTC6811 from the cell stack, V_{REG} may be powered from a DC/DC converter, rather than the NPN pass transistor. An ideal circuit is based on Linear Technology's LT3990 step-down regulator, as shown in Figure 33. A 470Ω resistor is recommended between the battery stack and the LT3990 input; this will prevent in-rush current when connecting to the stack and it will reduce conducted EMI. The EN/UVLO pin should be connected to the DRIVE pin, which will put the LT3990 into a low power state when the LTC6811 is in the SLEEP state.

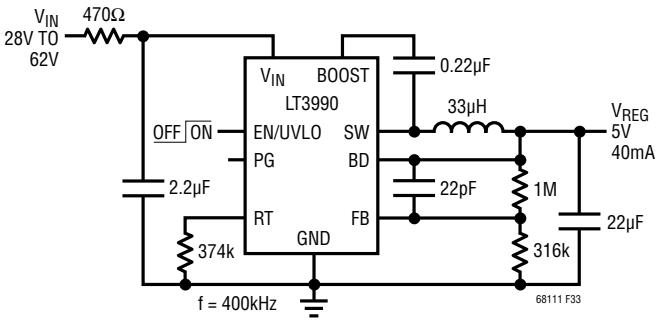

Figure 33. V_{REG} Powered From Cell Stack with High Efficiency Regulator

Fully Isolated Power

A DC/DC converter can provide isolated power for either the LTC6811 V^+, V_{REG} or both. The circuit in Figure 34, along with the isoSPI transformer isolation, provides an example where the LTC6811 circuitry is completely isolated. Furthermore, using a DC/DC converter minimizes the current drain on the battery and minimizes battery imbalance due to electronic loading.

A simple DC/DC converter is shown in Figure 35 using Linear Technology's LT3999 DC/DC converter and a high-isolation-rated transformer. Other topologies including flyback converters are possible with a suitable transformer. The NPN is retained to handle the flyback converter regulation effects at light loads.

Using Linear Technology's LT8301 isolated flyback converter as shown in Figure 36 provides an isolated high

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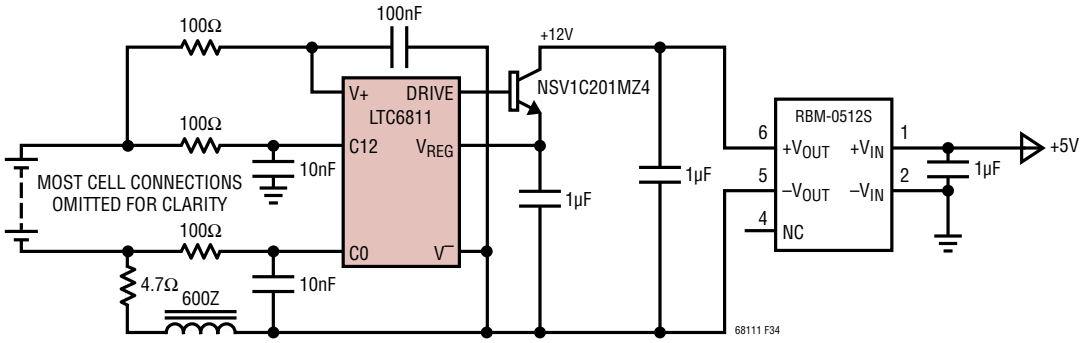

Figure 34. DC/DC Converter Module to Power V_{REG}

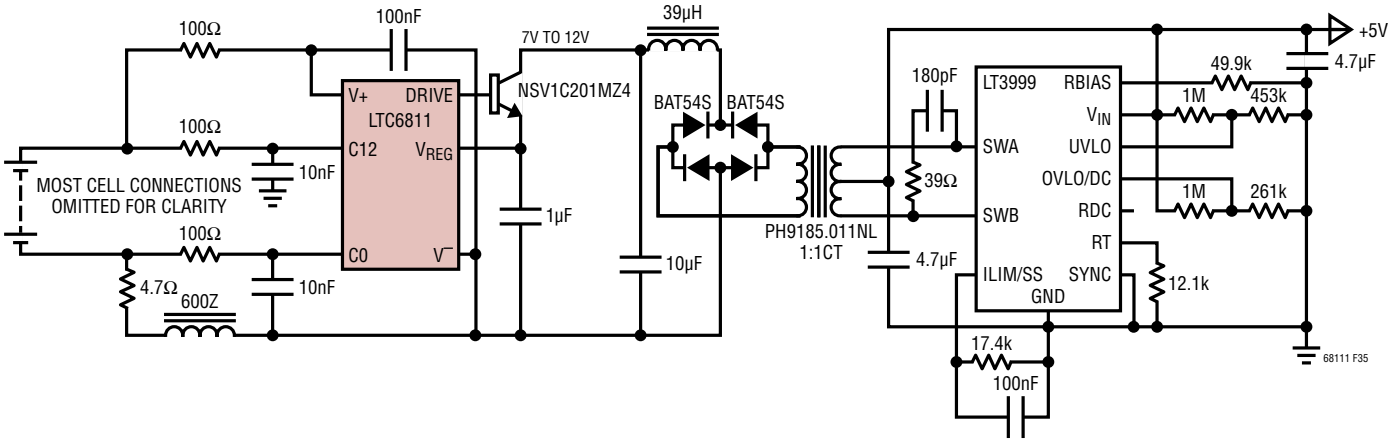

Figure 35. Push-Pull DC/DC Converter Circuit to Power V_{REG}

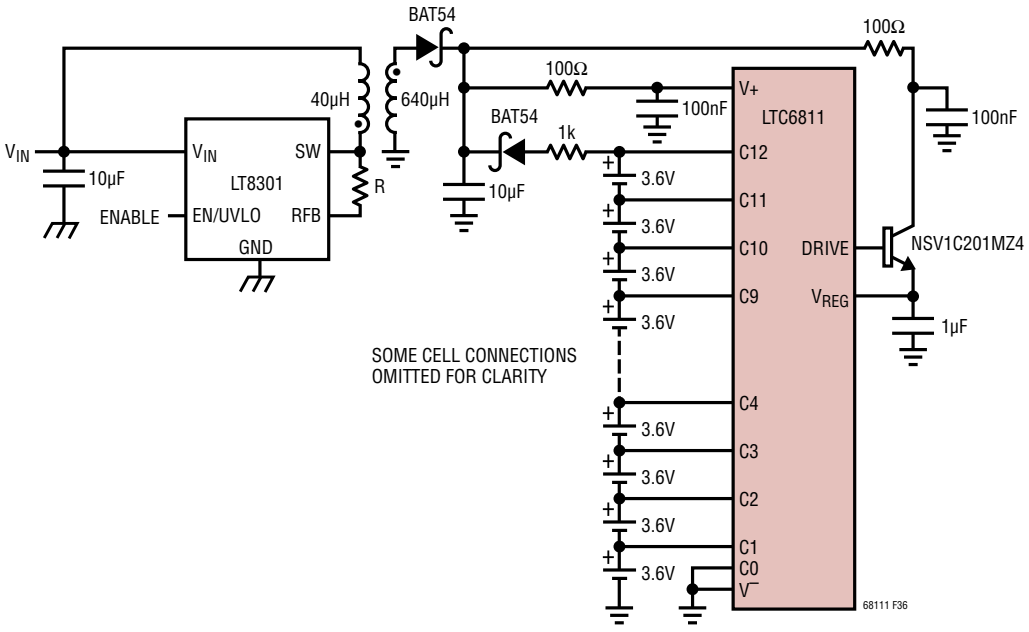

Figure 36. Flyback Converter to Power V^+ and V_{REG}

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voltage for the V^+ pin. The circuit still uses the DRIVE pin to generate V_{REG}. This circuit minimizes the system imbalance from the LTC6811 since the supply current will only be drawn from the batteries during shutdown. It is critical to add a diode between the top monitored cell and V^+ so that supply current will not conduct through parasitic paths inside the IC during shutdown.

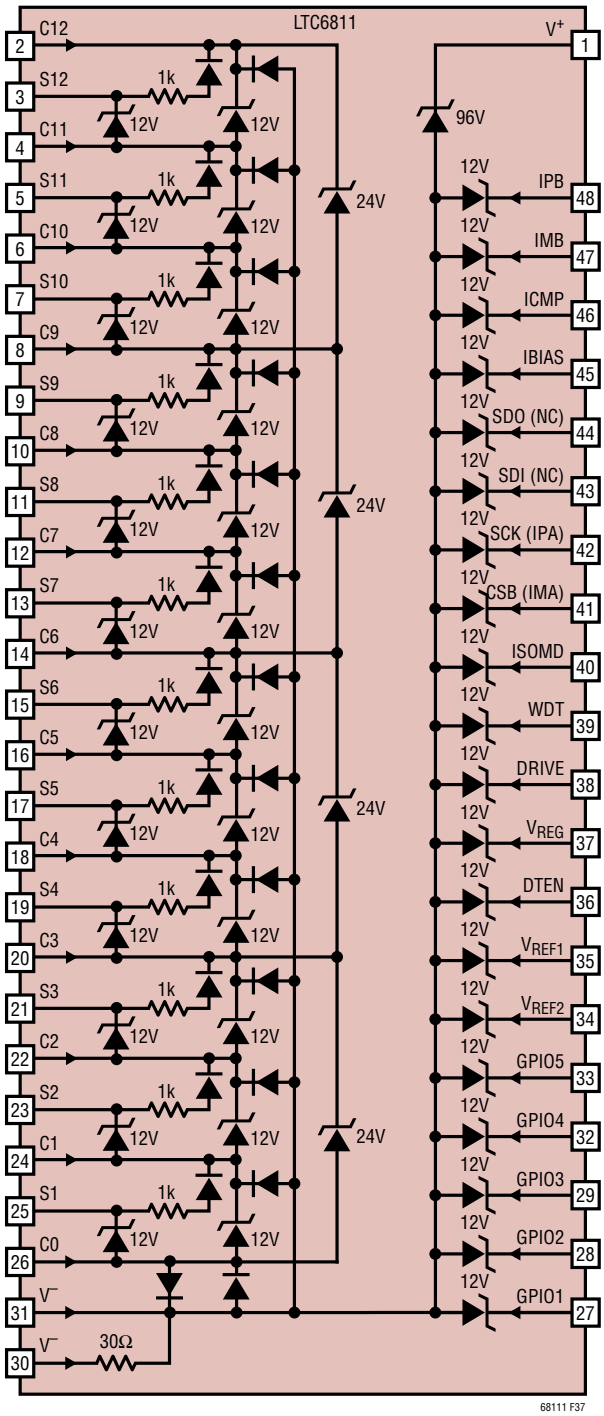
INTERNAL PROTECTION AND FILTERING

Internal Protection Features

The LTC6811 incorporates various ESD safeguards to ensure robust performance. An equivalent circuit showing the specific protection structures is shown in Figure 37. While pins 43 to 48 have different functionality for the –1 and –2 variants, the protection structure is the same. Zener-like suppressors are shown with their nominal clamp voltage, while the unmarked diodes exhibit standard PN junction behavior.

Filtering of Cell and GPIO Inputs

The LTC6811 uses a delta-sigma ADC, which includes a delta-sigma modulator followed by a SINC3 finite impulse response (FIR) digital filter. This greatly relaxes input filtering requirements. Furthermore, the programmable oversampling ratio allows the user to determine the best trade-off between measurement speed and filter cutoff frequency. Even with this high order low pass filter, fast transient noise can still induce some residual noise in measurements, especially in the faster conversion modes. This can be minimized by adding an RC low pass decoupling to each ADC input, which also helps reject potentially damaging high energy transients. Adding more than about 100Ω to the ADC inputs begins to introduce a systematic error in the measurement, which can be improved by raising the filter capacitance or mathematically compensating in software with a calibration procedure. For situations that demand the highest level of battery voltage ripple rejection, grounded capacitor filtering is recommended. This configuration has a series resistance and capacitors that decouple HF noise to V^-. In systems where noise is less



NOTE: NOT SHOWN ARE PN DIODES TO ALL OTHER PINS FROM PIN 35

Figure 37. Internal ESD Protection Structures of the LTC6811

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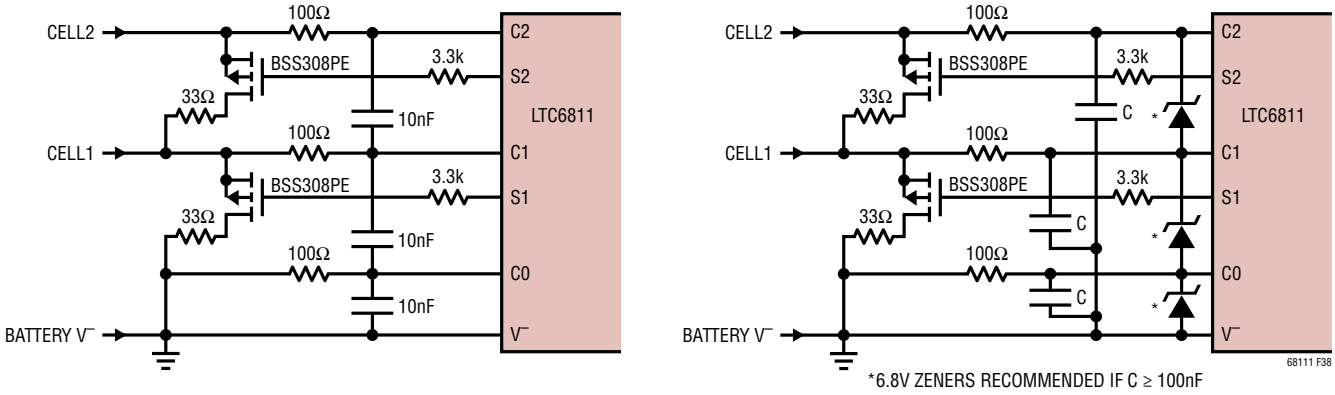
periodic or higher oversample rates are in use, a differential capacitor filter structure is adequate. In this configuration there are series resistors to each input, but the capacitors connect between the adjacent C pins. However, the differential capacitor sections interact. As a result, the filter response is less consistent and results in less attenuation than predicted by the RC, by approximately a decade. Note that the capacitors only see one cell of applied voltage (thus smaller and lower cost) and tend to distribute transient energy uniformly across the IC (reducing stress events on the internal protection structure). Figure 38 shows the two methods schematically. ADC accuracy varies with R, C as shown in the Typical Performance curves, but error is minimized if R = 100Ω and C = 10nF. The GPIO pins will always use a grounded capacitor configuration because the measurements are all with respect to V⁻.

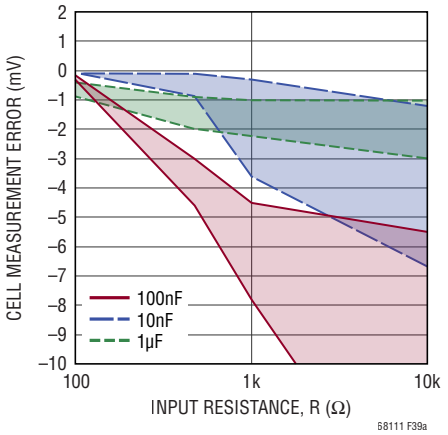
Using Nonstandard Cell Input Filters

A cell pin filter of 100Ω and 10nF is recommended for all applications. This filter provides the best combination of noise rejection and the Total Measurement Error (TME) performance. In applications that use C pin RC filters larger than 100Ω/10nF there may be additional measurement error. Figure 39a shows how both total TME and TME variation increase as the RC time constant increases. The increased error is related to the MUX settling. It is possible

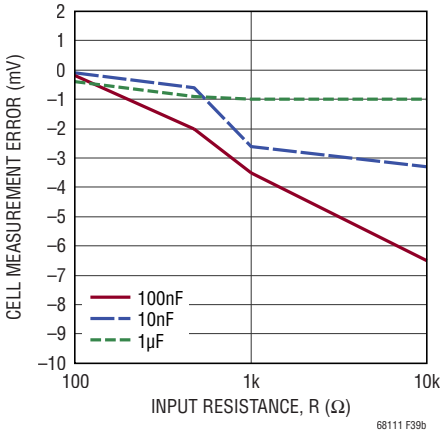


Differential Capacitor Filter **Grounded Capacitor Filter**

Figure 38. Input Filter Structure Configurations



(a) Cell Measurement Error Range vs Input RC Values



(b) Cell Measurement Error vs Input RC Values (Extra Conversion and Delay Before Measurement)

Figure 39. Cell Measurement TME

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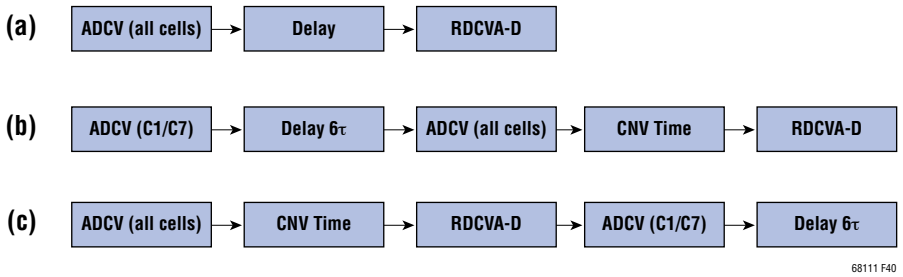


Figure 40. ADC Command Order

to reduce TME levels to near data sheet specifications by implementing an extra single channel conversion before issuing a standard all channel ADCV command. Figure 40a shows the standard ADCV command sequence. Figure 40b and Figure 40c show recommended command sequence and timing that will allow the MUX to settle. The purpose of the modified procedure is to allow the MUX to settle at C1/C7 before the start of the measurement cycle. The delay between the C1/C7 ADCV command and the All Channel ADCV command is dependent on the time constant of the RC being used, the general guidance is to wait 6τ between the C1/C7 ADCV command and the All Channel ADCV command. Figure 39b shows the expected TME when using the recommended command sequence.

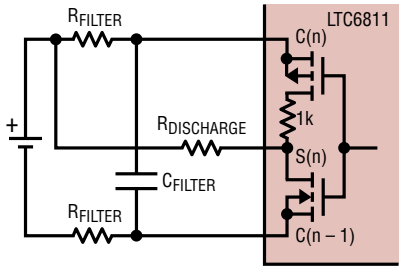
CELL BALANCING

Cell Balancing with Internal MOSFETs

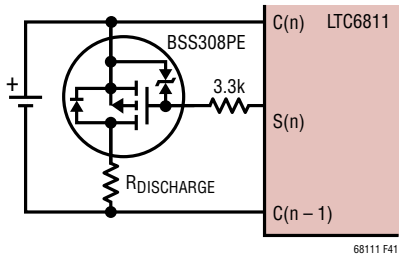
With passive balancing, if one cell in a series stack becomes overcharged, an S output can slowly discharge this cell by connecting it to a resistor. Each S output is connected to an internal N-channel MOSFET with a maximum on resistance of 25Ω. An external resistor should be connected in series with these MOSFETs to allow most of the heat to be dissipated outside of the LTC6811 package, as illustrated in Figure 41a.

The internal discharge switches (MOSFETs) S1 through S12 can be used to passively balance cells as shown in Figure 41a with balancing current of 60mA or less. Balancing current larger than 60mA is not recommended for the internal switches due to excessive die heating. When discharging cells with the internal discharge switches, the die temperature should be monitored. See the Thermal Shutdown section.

Note that the anti-aliasing filter resistor is part of the discharge path, so it should be removed or reduced. Use of an RC for added cell voltage measurement filtering is OK but the filter resistor must remain small, typically around 10Ω, to reduce the effect on the balance current.



a) Internal Discharge Circuit



b) External Discharge Circuit

Figure 41. Internal/External Discharge Circuits

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Cell Balancing with External Transistors

For applications that require balancing currents above 60mA or large cell filters, the S outputs can be used to control external transistors. The LTC6811 includes an internal pull-up PMOS transistor with a 1k series resistor. The S pins can act as digital outputs suitable for driving the gate of an external MOSFET as illustrated in Figure 41b. Figure 38 shows external MOSFET circuits that include RC filtering. For applications with very low cell voltages the PMOS in Figure 41b can be replaced with a PNP. When a PNP is used, the resistor in series with the base should be reduced.

Choosing a Discharge Resistor

When sizing the balancing resistor it is important to know the typical battery imbalance and the allowable time for cell balancing. In most small battery applications it is reasonable for the balancing circuitry to be able to correct for a 5% SOC (State Of Charge) error with 5 hours of balancing. For example a 5Ah battery with a 5% SOC imbalance will have approximately 250mAh of imbalance. Using a 50mA balancing current this could be corrected in 5 hours. With a 100mA balancing current, the error would be corrected in 2.5h. In systems with very large batteries,it becomes difficult to use passive balancing to correct large SOC imbalances in short periods of time. The excessive heat created during balancing generally limits the balancing current. In large capacity battery applications, if short balancing times are required, an active balancing solution should be considered. When choosing a balance resistor, the following equations can be used to help determine a resistor value:

$$\text{Balance Current} = \frac{\%\text{SOC\_Imbalance} \bullet \text{Battery Capacity}}{\text{Number of Hours to Balance}}$$

$$\text{Balance Resistor} = \frac{\text{Nominal Cell Voltage}}{\text{Balance Current}}$$

Active Cell Balancing

Applications that require 1A or greater of cell balancing current should consider implementing an active balancing system. Active balancing allows for much higher balancing currents without the generation of excessive heat. Active balancing also allows for energy recovery since most of the balance current will be redistributed back to the battery pack. Figure 42 shows a simple active balancing implementation using Linear Technology's LT8584. The LT8584 also has advanced features which can be controlled via the LTC6811. See the S Pin Pulsing Using the S Control Register Group section and the LT®8584 data sheet for more details.

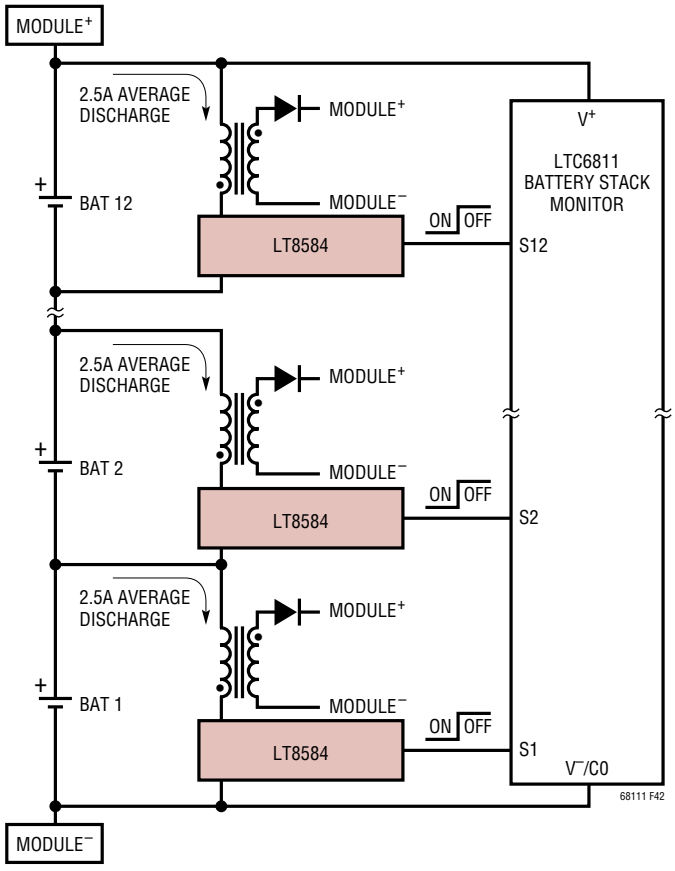

Figure 42. 12-Cell Battery Stack Module with Active Balancing

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DISCHARGE CONTROL DURING CELL MEASUREMENTS

If the discharge permitted (DCP) bit is high at the time of a cell measurement command, the S pin discharge states do not change during cell measurements. If the DCP bit is low, S pin discharge states will be disabled while the corresponding cell or adjacent cells are being measured. If using an external discharge transistor, the relatively low 1kΩ impedance of the internal LTC6811 PMOS transistors should allow the discharge currents to fully turn off before the cell measurement. Table 53 illustrates the ADCV command with DCP = 0. In this table, OFF indicates that the S pin discharge is forced off irrespective of the state of the corresponding DCC[x] bit. ON indicates that the S pin discharge will remain on during the measurement period if it was ON prior to the measurement command.

Battery Module Balancing

In some large battery systems, cells are grouped by BMS ICs. It is common for these groups of cells to become out of balance as compared to the other groups of cells in the battery pack. The circuit shown in Figure 43 is a system to balance groups of cells connected to a single LTC6811. This design is beneficial in combination with the individual, lower current internal discharge switches: A high module (total stack) balancing current can be implemented while lower current, lower cost, individual cell balancing is accomplished with the internal balancing switches shown in Figure 41a.

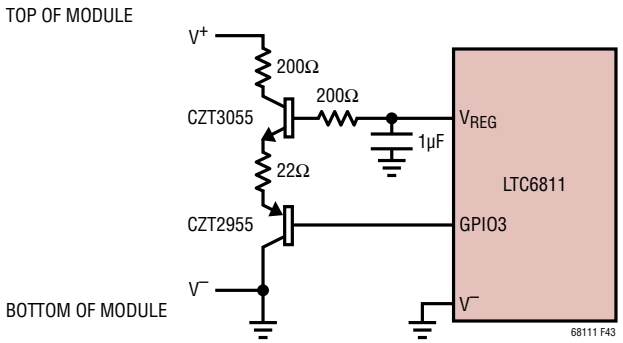

Figure 43. 200mA Module Balancer

Table 53. Discharge Control During an ADCV Command with DCP = 0

	CELL MEASUREMENT PERIODS						CELL CALIBRATION PERIODS					
	CELL1/7	CELL2/8	CELL3/9	CELL4/10	CELL5/11	CELL6/12	CELL1/7	CELL2/8	CELL3/9	CELL4/10	CELL5/11	CELL6/12
DISCHARGE PIN	t_0 to t_{1M}	t_{1M} to t_{2M}	t_{2M} to t_{3M}	t_{3M} to t_{4M}	t_{4M} to t_{5M}	t_{5M} to t_{6M}	t_{6M} to t_{1C}	t_{1C} to t_{2C}	t_{2C} to t_{3C}	t_{3C} to t_{4C}	t_{4C} to t_{5C}	t_{5C} to t_{6C}
S1	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S2	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S3	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S4	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
S5	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S6	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
S7	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF
S8	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON
S9	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON
S10	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	ON
S11	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
S12	OFF	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF

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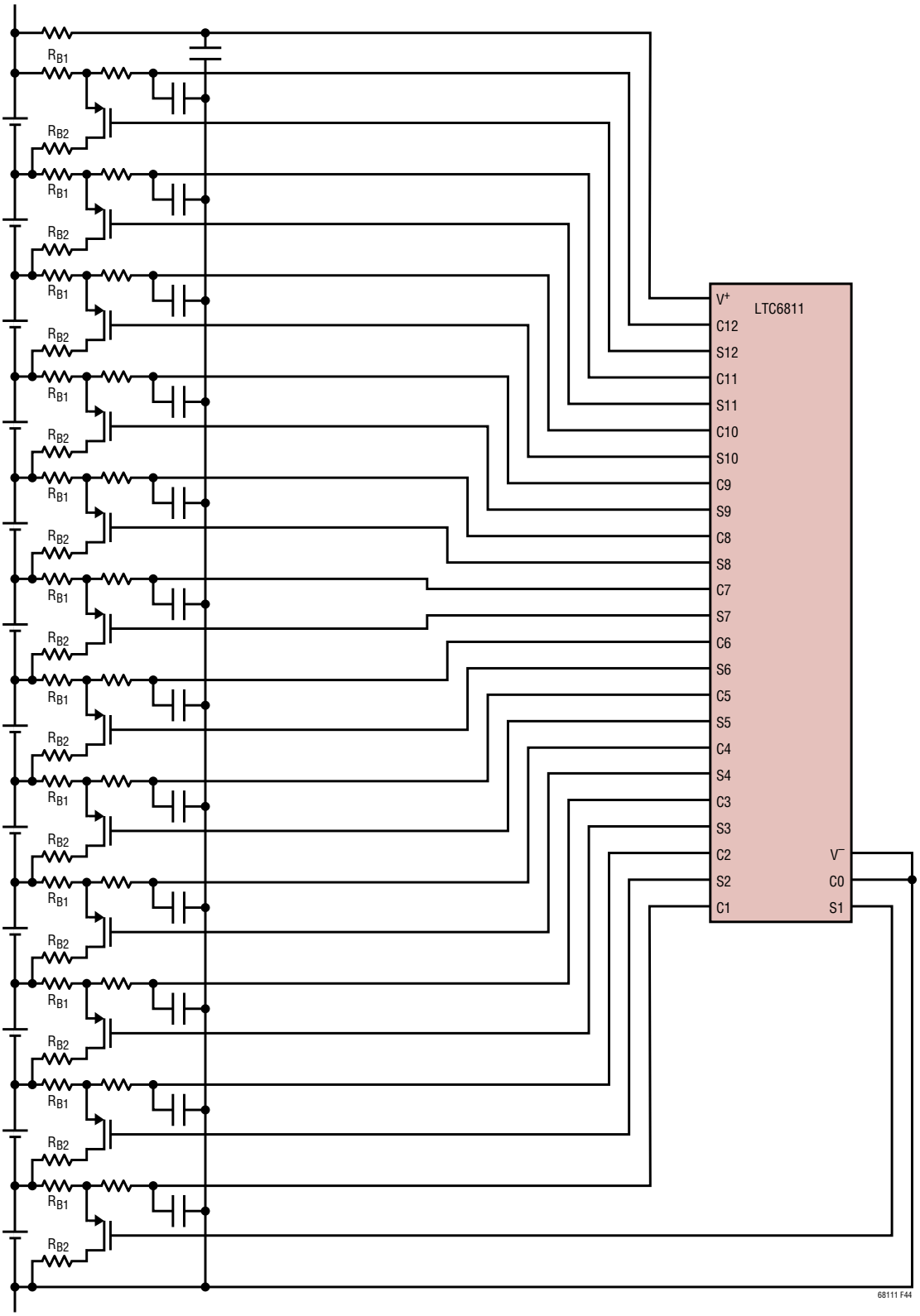

Figure 44. Balancing Self Test Circuit

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Method to Verify Discharge Circuits

The functionality of the discharge circuits can be verified by conducting cell measurements. As shown in Figure 44, a resistor between the battery cell and the source of the discharge MOSFET will cause a decrease in cell voltage measurements. The amount of this measurement decrease depends on the resistor value and the MOSFET on resistance. The following algorithm can be used in conjunction with Figure 44 to verify each discharge circuit:

1. Measure all cells with no discharging (all S outputs off) and read and store the results.
2. Turn on S1 and S7.
3. Measure C1-C0, C7-C6.
4. Turn off S1 and S7.
5. Turn on S2 and S8.
6. Measure C2-C1, C8-C7.
7. Turn off S2 and S8.

…

17. Turn on S6 and S12.
18. Measure C6-C5, C12-C11.
19. Turn off S6 and S12.
20. Read the Cell Voltage Register Groups to get the results of steps 2 thru 19.
21. Compare new readings with old readings. Each cell voltage reading should have decreased by a fixed percentage set by R_{B1} and R_{B2} (Figure 44). The exact amount of decrease depends on the resistor values and MOSFET characteristics.

DIGITAL COMMUNICATIONS

PEC Calculation

The Packet Error Code (PEC) can be used to ensure that the serial data read from the LTC6811 is valid and has not been corrupted. This is a critical feature for reliable communication, particularly in environments of high noise. The LTC6811 requires that a PEC be calculated for all data being read from, and written to, the LTC6811. For this reason it is important to have an efficient method for calculating the PEC.

The C code on page 76 provides a simple implementation of a lookup-table-derived PEC calculation method. There are two functions. The first function init_PEC15_Table() should only be called once when the microcontroller starts and will initialize a PEC15 table array called pec15Table[]. This table will be used in all future PEC calculations. The PEC15 table can also be hard coded into the microcontroller rather than running the init_PEC15_Table() function at startup. The pec15() function calculates the PEC and will return the correct 15-bit PEC for byte arrays of any given length.

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/*******************************
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INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS. IN NO
EVENT SHALL LTC BE LIABLE FOR ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL
DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM ANY USE OF SAME, INCLUDING
ANY LOSS OF USE OR DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE
OR OTHER TORTUOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR
PERFORMANCE OF THIS SOFTWARE.
*******************************************************/
int16 pec15Table[256];
int16 CRC15_POLY = 0x4599;
void init_PEC15_Table()
{
   for (int i = 0; i < 256; i++)
   {
      remainder = i << 7;
      for (int bit = 8; bit > 0; --bit)
      {
         if (remainder & 0x4000)
         {
            remainder = ((remainder << 1));
            remainder = (remainder ^ CRC15_POLY)
         }
         else
         {
            remainder = ((remainder << 1));
         }
      }
      pec15Table[i] = remainder&0xFFFF;
   }
}
unsigned int16 pec15 (char *data , int len)
{
   int16 remainder,address;
   remainder = 16;//PEC seed
   for (int i = 0; i < len; i++)
   {
      address = ((remainder >> 7) ^ data[i]) & 0xff;//calculate PEC table address
      remainder = (remainder << 8 ) ^ pec15Table[address];
   }
   return (remainder*2);//The CRC15 has a 0 in the LSB so the final value must be multiplied by 2
}
```

isoSPI IBIAS and ICMP Setup

The LTC6811 allows the isoSPI links of each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed I_B current, which controls the isoSPI signaling currents. Bias current I_B can range from 100µA to 1mA. Internal circuitry scales up this bias current to create the isoSPI signal currents equal to 20 • I_B. A low I_B reduces the isoSPI power consumption in the READY and ACTIVE states, while a high I_B increases the amplitude of the differential signal voltage V_A across the matching termination resistor, R_M. The I_B current is programmed by the sum of the R_{B1} and R_{B2} resistors connected between the 2V IBIAS pin and GND as shown in Figure 45. The receiver input threshold is set by the ICMP voltage that is programmed with the resistor divider created by the R_{B1} and R_{B2} resistors. The receiver threshold will be half of the voltage present on the ICMP pin.

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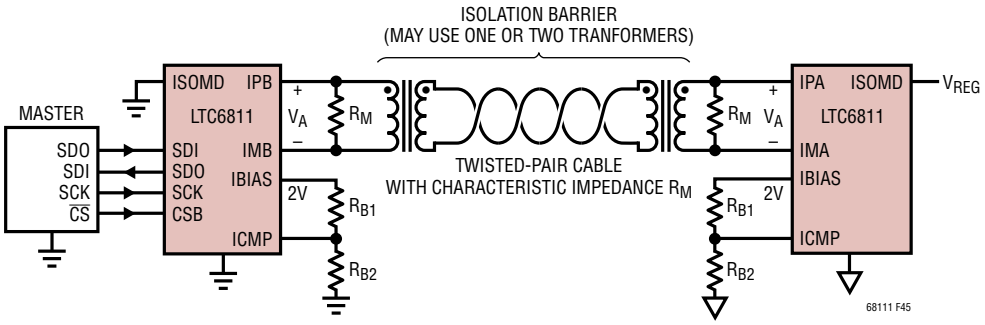


Figure 45. isoSPI Circuit

The following guidelines should be used when setting the bias current (100µA to 1mA) I_B and the receiver comparator threshold voltage $V_{ICMP}/2$:

R_M = Transmission Line Characteristic Impedance Z_0

Signal Amplitude $V_A = (20 \bullet I_B) \bullet (R_M/2)$

V_{TCMP} (Receiver Comparator Threshold) = $K \bullet V_A$

V_{ICMP} (voltage on ICMP pin) = $2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$R_{B1} = (2/I_B) – R_{B2}$

Select I_B and K (Signal Amplitude V_A to Receiver Comparator Threshold ratio) according to the application:

For lower power links: I_B = 0.5mA and K = 0.5

For full power links: I_B = 1mA and K = 0.5

For long links (>50m): I_B = 1mA and K = 0.25

For addressable multi-drop: I_B = 1mA and K = 0.4

For applications with little system noise, setting I_B to 0.5mA is a good compromise between power consumption and noise immunity. Using this I_B setting with a 1:1 transformer and R_M = 100Ω, R_{B1} should be set to 3.01k and R_{B2} set to 1k. With typical CAT5 twisted pair, these settings will allow for communication up to 50m. For applications in very noisy environments or that require cables longer than 50m it is recommended to increase I_B to 1mA. Higher drive current compensates for the increased insertion loss in the cable and provides high noise immunity. When using cables over 50m and a transformer with a 1:1 turns ratio and R_M = 100Ω, R_{B1} would be 1.5k and R_{B2} would be 499Ω.

The maximum clock rate of an isoSPI link is determined by the length of the isoSPI cable. For cables 10 meters or less, the maximum 1MHz SPI clock frequency is possible. As the length of the cable increases, the maximum possible SPI clock rate decreases. This dependence is a result of the increased propagation delays that can create possible timing violations. Figure 46 shows how the maximum data rate reduces as the cable length increases when using a CAT5 twisted pair.

Cable delay affects three timing specifications: t_{CLK}, t_6 and t_7. In the Electrical Characteristics table, each of these specifications is de-rated by 100ns to allow for 50ns of cable delay. For longer cables, the minimum timing parameters may be calculated as shown below:

t_{CLK}, t_6 and $t_7 > 0.9\mu s + 2 \bullet t_{CABLE}$(0.2m per ns)

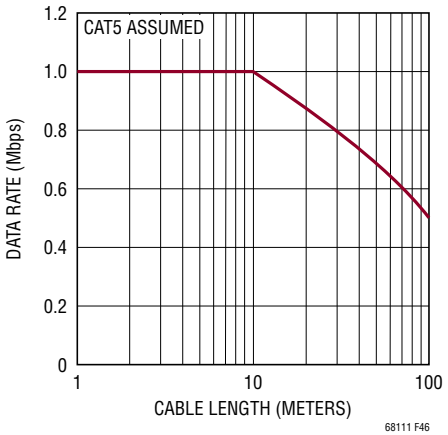


Figure 46. Data Rate vs Cable Length

APPLICATIONS INFORMATION

Implementing a Modular isoSPI Daisy Chain

The hardware design of a daisy-chain isoSPI bus is identical for each device in the network due to the daisy-chain point-to-point architecture. The simple design as shown in Figure 45 is functional, but inadequate for most designs. The termination resistor R_M should be split and bypassed with a capacitor as shown in Figure 47. This change provides both a differential and a common mode termination, and as such, increases the system noise immunity.

The use of cables between battery modules, particularly in automotive applications, can lead to increased noise susceptibility in the communication lines. For high levels of electromagnetic interference (EMC), additional filtering is recommended. The circuit example in Figure 47 shows the use of common mode chokes (CMC)to add common mode noise rejection from transients on the battery lines. The use of a center tapped transformer will also provide additional noise performance. A bypass capacitor connected to the center tap creates a low impedance for common mode noise (Figure 47b). Since transformers without a center tap can be less expensive, they may be preferred. In this case, the addition of a split termination resistor and a bypass capacitor (Figure 47a) can enhance the isoSPI performance. Large center tap capacitors greater than 10nF should be avoided as they may prevent the isoSPI common mode voltage from settling. Common mode chokes similar to those used in Ethernet or CANbus applications are recommended. Specific examples are provided in Table 55.

An important daisy chain design consideration is the number of devices in the isoSPI network. Both the number of devices in a daisy chain and the length of wire between devices determines the serial timing and affects data latency and throughput.

For a daisy chain, it is necessary to extend minimum required t_5, the time from a rising chip select to the next falling chip select (between commands), from 0.65µs to 2µs (see Figure 25).

This timing for t_5 is set by the MCU on the SPI interface of LTC6820 or the SPI interface of the bottom LTC6811 device if it is configured to operate in SPI mode. If necessary, LTC6811 will internally adjust the timing for t_6 and t_5 while transmitting on the Master isoSPI port such that t_6 (Master port) > $t_{6(GOV)}$ and t_5 (Master port) > $t_{5(GOV)}$. This satisfies the timing requirement for the Slave port of the next device.

If the t_5 requirement of 2µs is satisfied on the SPI interface, there is no strict limitation on the maximum number of devices in the daisy chain.

However, it is important to note that the serial read back time, and the increased current consumption, might dictate a practical limitation in the size of the network.

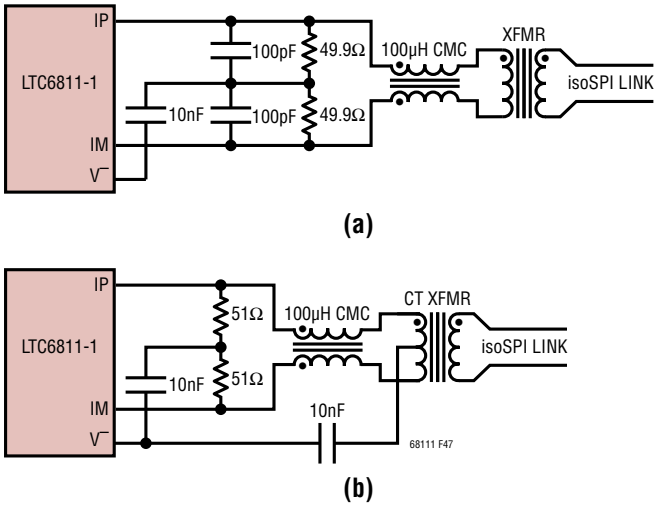
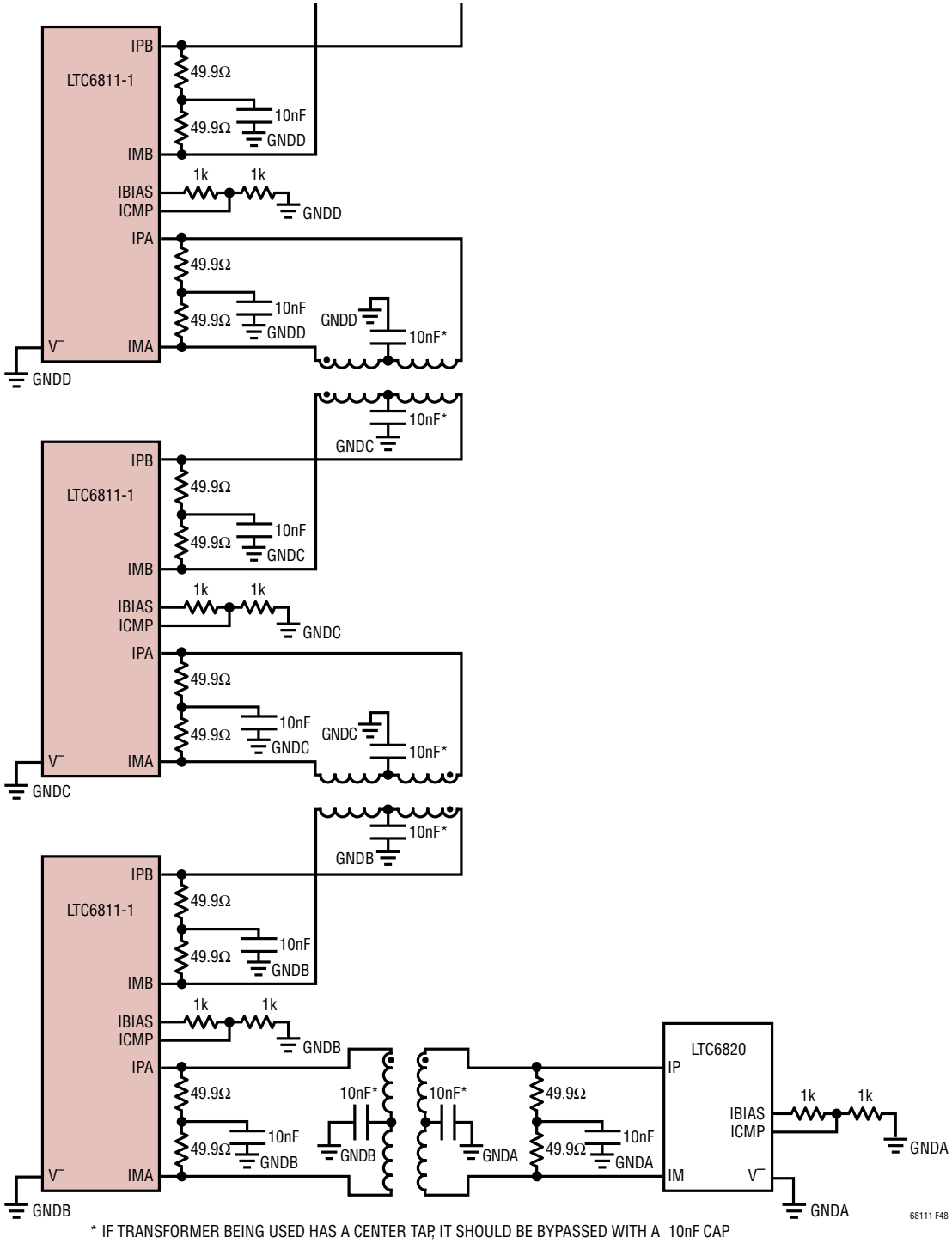


Figure 47. Daisy Chain Interface Components

APPLICATIONS INFORMATION



* IF TRANSFORMER BEING USED HAS A CENTER TAP, IT SHOULD BE BYPASSED WITH A 10nF CAP

Figure 48. Daisy Chain Interface Components on Single Board

APPLICATIONS INFORMATION

Connecting Multiple LTC6811-1s on the Same PCB

When connecting multiple LTC6811-1 devices on the same PCB, only a single transformer is required between the LTC6811-1 isoSPI ports. The absence of the cable also reduces the noise levels on the communication lines and often only a split termination is required. Figure 48 shows an example application that has multiple LTC6811-1s on the same PCB, communicating to the bottom MCU through an LTC6820 isoSPI driver. If a transformer with a center tap is used, a capacitor can be added for better noise rejection. Additional noise filtering can be provided with discrete common mode chokes (not shown) placed to both sides of the single transformer.

On single board designs with low noise requirements, it is possible for a simplified capacitor-isolated coupling as shown in Figure 49 to replace the transformer.

In this circuit, the transformer is directly replaced by two 10nF capacitors. A common mode choke (CMC) provides noise rejection similar to application circuits using transformers. The circuit is designed to use IBIAS/ICMP settings identical to the transformer circuit.

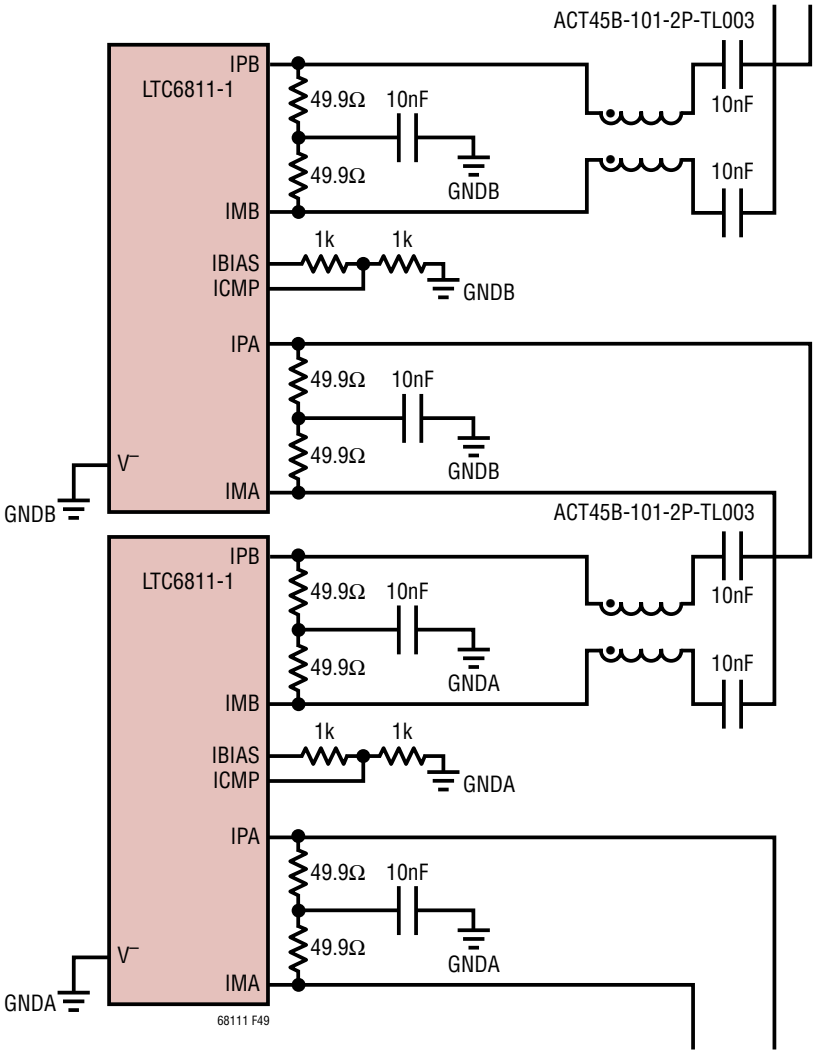


Figure 49. Capacitive Isolation Coupling for LTC6811-1s on the Same PCB

APPLICATIONS INFORMATION

Connecting an MCU to an LTC6811-1 with an isoSPI Data Link

The LTC6820 will convert standard 4-wire SPI into a 2-wire isoSPI link that can communicate directly with the LTC6811. An example is shown in Figure 50. The LTC6820 can be used in applications to provide isolation between the microcontroller and the stack of LTC6811s. The LTC6820 also enables system configurations that have the BMS controller at a remote location relative to the LTC6811 devices and the battery pack.

Configuring the LTC6811-2 in a Multi–Drop isoSPI Link

The addressing feature of the LTC6811-2 allows multiple devices to be connected to a single isoSPI master by distributing them along one twisted pair, essentially creating a large parallel SPI network. A basic multi-drop system is shown in Figure 51; the twisted pair is terminated only at the beginning (master) and the end of the cable. In between, the additional LTC6811-2s are connected to short stubs on the twisted pair. These stubs should be kept short, with as little capacitance as possible, to avoid degrading the termination along the isoSPI wiring.

When an LTC6811-2 is not addressed, it will not transmit data pulses. This scheme eliminates the possibility for collisions since only the addressed device returns data to the master. Generally, multi-drop systems are best confined to compact assemblies where they can avoid excessive isoSPI pulse-distortion and EMC pickup.

Basic Connection of the LTC6811-2 in a Multi-Drop Configuration

In a multi-drop isoSPI bus, placing the termination at the ends of the transmission line provides the best performance (with 100Ω typically). Each of the LTC6811 isoSPI ports should couple to the bus with a resistor network, as shown in Figure 52a. Here again, a center-tapped transformer offers the best performance and a common mode choke (CMC) increases the noise rejection further, as shown in Figure 52b. Figure 52b also shows the use of an RC snubber at the IC connections as a means to suppress resonances (the IC capacitance provides sufficient out-of-band rejection). When using a non-center-tapped transformer, a virtual CT can be generated by connecting a CMC as a voltage-splitter. Series resistors are recommended to decouple the LTC6811 and board parasitic capacitance from the transmission line. Reducing these parasitics on the transmission line will minimize reflections.

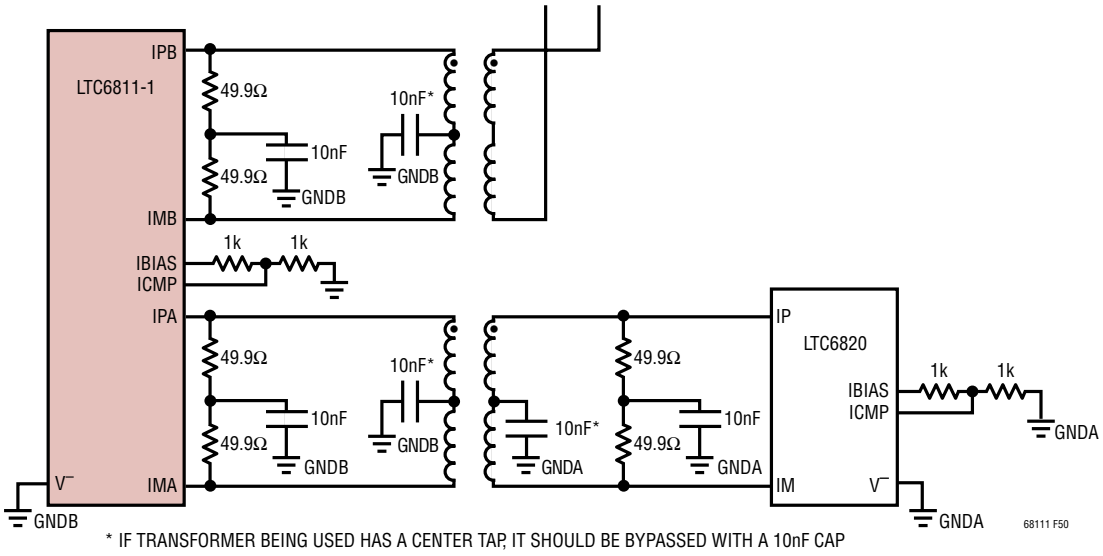


Figure 50. Interfacing an LTC6811-1 with a µC Using an LTC6820 for Isolated SPI Control

APPLICATIONS INFORMATION

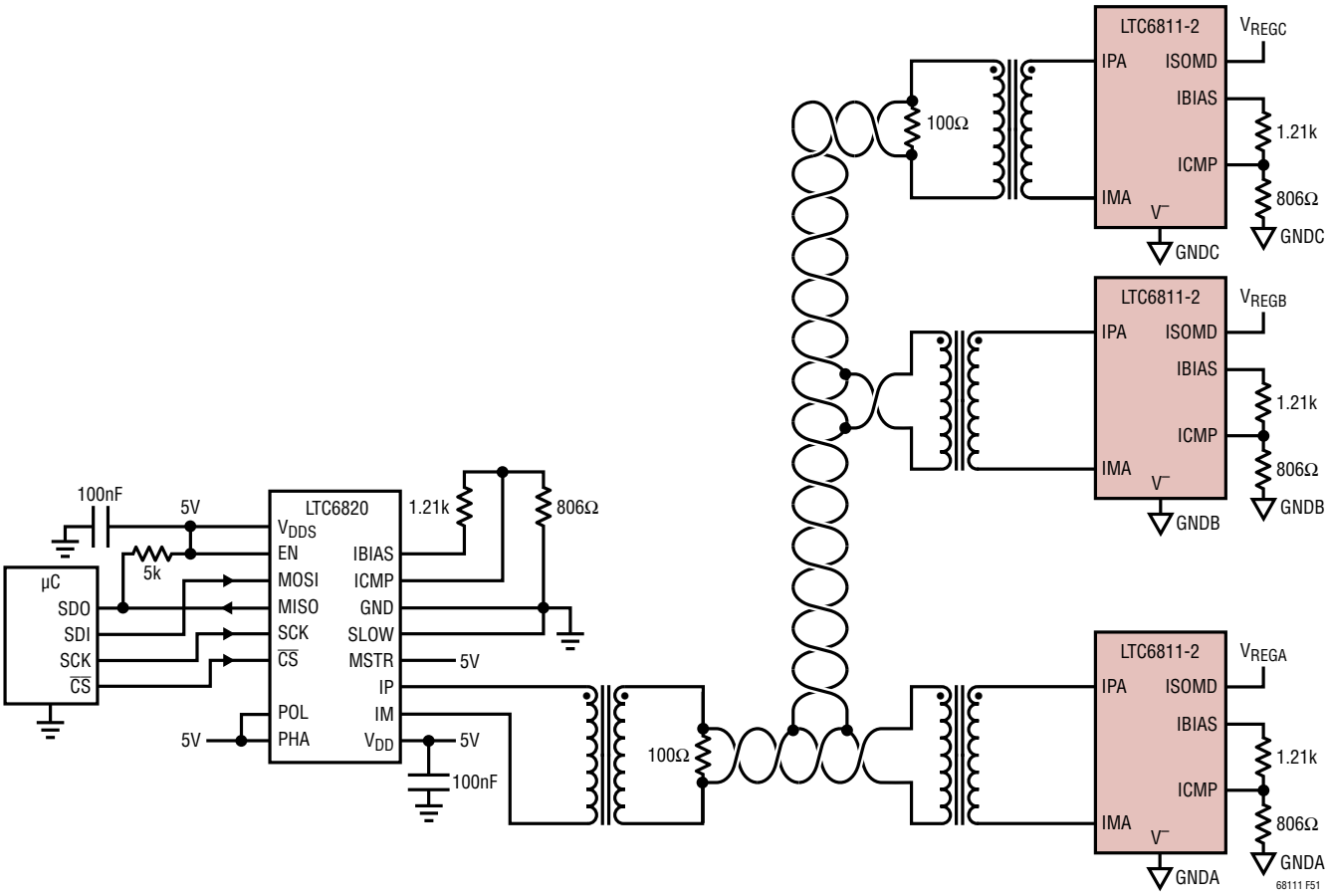


Figure 51. Connecting the LTC6811-2 in a Multi-Drop Configuration

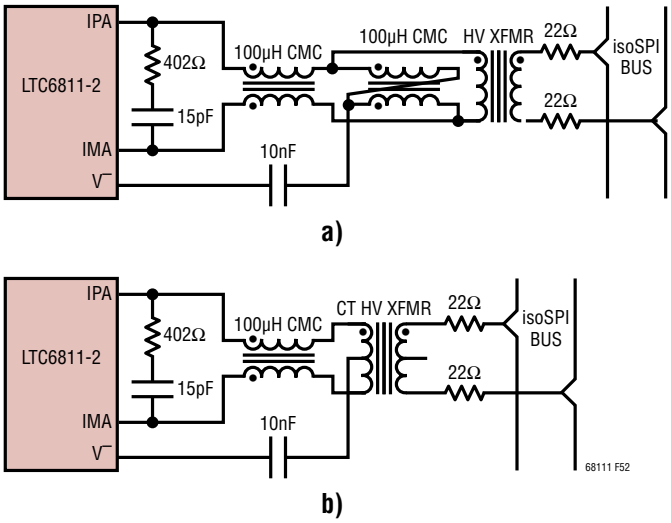


Figure 52. Preferred isoSPI Bus Couplings For Use With LTC6811-2

APPLICATIONS INFORMATION

Table 54. Recommended Transformers

SUPPLIER	PART NUMBER	TEMPERATURE RANGE	$V_{WORKING}$	V_{HIPOT}/60s	CT	CMC	H	L	W (W/LEADS)	PINS	AEC–Q200
Recommended Dual Transformers											
Bourns	SM91501AL	–40°C to 125°C	1000V	4.3kVdc	●	●	5.0mm	15.0mm	14.7mm	12SMT	●
Bourns	SM13105L (AS4562)	–40°C to 125°C	1600V	4.3kVrms	●	●	5.0mm	15.0mm	27.9mm	12SMT	–
Bourns	US4374	–40°C to 125°C	950V	4.3kVdc	●	●	4.9mm	15.6mm	24.0mm	12SMT	●
Jingweida	S12502BA	–40°C to 125°C	1000V	4.3kVdc	●	●	5.0mm	14.8mm	14.8mm	12SMT	●
Halo	TG110-AE050N5LF	–40°C to 85/125°C	60V (est)	1.5kVrms	●	●	6.4mm	12.7mm	9.5mm	16SMT	●
Sumida	CLP178-C20114	–40°C to 125°C	1000V (est)	3.75kVrms	●	●	9mm	17.5mm	15.1mm	12SMT	–
Sumida	CLP0612-C20115		600Vrms	3.75kVrms	●	–	5.7mm	12.7mm	9.4mm	16SMT	–
Pulse	HM2100NL	–40°C to 105°C	1000V	4.3kVdc	–	●	3.5mm	14.7mm	15.0mm	10SMT	●
Pulse	HM2112ZNL	–40°C to 125°C	1600V	4.3kVdc	●	●	3.5mm	14.7mm	15.5mm	12SMT	●
Pulse	HX1188FNL	–40°C to 85°C	60V (est)	1.5kVrms	●	●	6.0mm	12.7mm	9.7mm	16SMT	–
Pulse	HX0068ANL	–40°C to 85°C	60V (est)	1.5kVrms	●	●	2.1mm	12.7mm	9.7mm	16SMT	–
Wurth	7490140110	–40°C to 85°C	250Vrms	4kVrms	●	●	10.9mm	24.6mm	17.0mm	16SMT	–
Wurth	7490140111	0°C to 70°C	1000V (est)	4.5kVrms	●	–	8.4mm	17.1mm	15.2mm	12SMT	–
Wurth	749014018	0°C to 70°C	250Vrms	4kVrms	●	●	8.4mm	17.1mm	15.2mm	12SMT	–
Recommended Single Transformers											
Bourns	SM91502AL	–40°C to 125°C	1000V	4.3kVdc	●	●	6.5mm	8.5mm	8.9mm	6SMT	●
Bourns	SM13102AL (US4195)	–40°C to 125°C	800V	4kVrms	●	●	3.8mm	11.6mm	21.1mm	6SMT	–
Halo	TD04-QXLTAW	–40°C to 85°C	1000V (est)	5kVrms	●	–	8.6mm	8.9mm	16.6mm	6TH	–
Halo	TGR04-6506V6LF	–40°C to 125°C	300V	3kVrms	●	–	10mm	9.5mm	12.1mm	6SMT	–
Halo	TGR04-A6506NA6NL	–40°C to 125°C	300V	3kVrms	●	–	9.4mm	8.9mm	12.1mm	6SMT	●
Halo	TDR04-A550ALLF	–40°C to 105°C	1000V	5kVrms	●	–	6.4mm	8.9mm	16.6mm	6TH	●
Jingweida	S06107BA	–40°C to 125°C	1000V (est)	4.3kVdc	●	●	6.3mm	7.6mm	9.9mm	6SMT	–
Pulse	HM2101NL	–40°C to 105°C	1000V	4.3kVdc	–	●	5.7mm	7.6mm	9.3mm	6SMT	●
Pulse	HM2113ZNL	–40°C to 125°C	1600V	4.3kVdc	●	●	3.5mm	9mm	15.5mm	6SMT	●
Sumida	CEEH96BNP-LTC6804/11	–40°C to 125°C	600V	2.5kVrms	–	–	7mm	9.2mm	12.0mm	4SMT	
Sumida	CEP99NP-LTC6804	–40°C to 125°C	600V	2.5kVrms	●	–	10mm	9.2mm	12.0mm	8SMT	–
Sumida	ESMIT-4180/A	–40°C to 105°C	250Vrms	3kVrms	–	–	3.5mm	5.2mm	9.1mm	4SMT	●
Sumida	ESMIT-4187	–40°C to 105°C	>400Vrms (est)	2.5kVrms	–	–	3.5mm	7.5mm	12.8mm	4SMT	●
TDK	VMT40DR-201S2P4	–40°C to 125°C	600V (est)	3.4kVdc	●	–	4.0mm	8.5mm	13.8mm	6SMT	●
TDK	ALT4532V-201-T001	–40°C to 105°C	80V	~1kV	●	–	2.9mm	3.2mm	4.5mm	6SMT	●
TDK	VGT10/9EE-204S2P4	–40°C to 125°C	700V	2.8kVrms	●	–	10.6mm	10.4mm	12.6mm	8SMT	●
Sunlord	ALTW0806C-C03	–40°C to 125°C	300V (est)	3kVrms	●	–	8.8mm	6.3mm	8.9mm	6SMT	●
Wurth	750340848	–40°C to 105°C	250V	3kVrms	–	–	2.2mm	4.4mm	9.1mm	4SMT	–
XFMRS	XFBMC29-BA09	–40°C to 85°C	1600V (est)	2.9kVrms	●	●	5.0mm	10.0mm	19.5mm	6SMT	●

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Transformer Selection Guide

As shown in Figure 45, a transformer or pair of transformers isolates the isoSPI signals between two isoSPI ports. The isoSPI signals have programmable pulse amplitudes up to $1.6V_{P-P}$ and pulse widths of 50ns and 150ns. To be able to transmit these pulses with the necessary fidelity the system requires that the transformers have primary inductances above 60µH and a 1:1 turns ratio. It is also necessary to use a transformer with less than 2.5µH of leakage inductance. In terms of pulse shape the primary inductance will mostly affect the pulse droop of the 50ns and 150ns pulses. If the primary inductance is too low, the pulse amplitude will begin to droop and decay over the pulse period. When the pulse droop is severe enough, the effective pulse width seen by the receiver will drop substantially, reducing noise margin. Some droop is acceptable as long as it is a relatively small percentage of the total pulse amplitude. The leakage inductance primarily affects the rise and fall times of the pulses. Slower rise and fall times will effectively reduce the pulse width. Pulse width is determined by the receiver as the time the signal is above the threshold set at the ICMP pin. Slow rise and fall times cut into the timing margins. Generally it is best to keep pulse edges as fast as possible. When evaluating transformers, it is also worth noting the parallel winding capacitance. While transformers have very good CMRR at low frequency, this rejection will degrade at higher frequencies, largely due to the winding to winding capacitance. When choosing a transformer, it is best to pick one with less parallel winding capacitance when possible.

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When choosing a transformer, it is equally important to pick a part that has an adequate isolation rating for the application. The working voltage rating of a transformer is a key spec when selecting a part for an application. Interconnecting daisy-chain links between LTC6811-1 devices see <60V stress in typical applications; ordinary pulse and LAN type transformers will suffice. Multi-drop connections and connections to the LTC6820, in general, may need much higher working voltage ratings for good long-term reliability. Usually, matching the working voltage to the voltage of the entire battery stack is conservative. Unfortunately, transformer vendors will often only specify one-second HV testing, and this is not equal to the long-term ("permanent") rating of the part. For example, according to most safety standards a 1.5kV rated transformer is expected to handle 230V continuously, and a 3kV device is capable of 1100V long-term, though manufacturers may not always certify to those levels (refer to actual vendor data for specifics). Usually, the higher voltage transformers are called "high-isolation" or "reinforced insulation" types by the suppliers. Table 54 shows a list of transformers that have been evaluated in isoSPI links.

Table 55. Recommended Common Mode Chokes

MANUFACTURER	PART NUMBER
TDK	ACT45B-101-2P
Murata	DLW43SH101XK2

In most applications a common mode choke is also necessary for noise rejection. Table 55 includes a list of suitable CMCs if the CMC is not already integrated into the transformer being used.

isoSPI Layout Guidelines

Layout of the isoSPI signal lines also plays a significant role in maximizing the noise immunity of a data link. The following layout guidelines are recommended:

1. The transformer should be placed as close to the isoSPI cable connector as possible. The distance should be kept less than 2cm. The LTC6811 should be placed close to but at least 1cm to 2cm away from the transformer to help isolate the IC from magnetic field coupling.
2. A V^- ground plane should not extend under the transformer, the isoSPI connector or in between the transformer and the connector.
3. The isoSPI signal traces should be as direct as possible while isolated from adjacent circuitry by ground metal or space. No traces should cross the isoSPI signal lines, unless separated by a ground plane on an inner layer.

System Supply Current

The LTC6811 has various supply current specifications for the different states of operation. The average supply current depends on the control loop in the system. It is necessary to know which commands are being executed

Table 56. Daisy Chain Serial Time Equations

COMMAND TYPE	CMD BYTES + CMD PEC	DATA BYTES + DATA PEC PER IC	TOTAL BITS	COMMUNICATION TIME
Read	4	8	(4 + (8 • #ICs)) • 8	Total Bits • Clock Period
Write	4	8	(4 + (8 • #ICs)) • 8	Total Bits • Clock Period
Operation	4	0	4 • 8 = 32	32 • Clock Period

Table 57. Multi-Drop Serial Time Equations

COMMAND TYPE	CMD BYTES + CMD PEC	DATA BYTES + DATA PEC PER IC	TOTAL BITS	COMMUNICATION TIME
Read	4	8	((4 + 8) • #ICs) • 8	Total Bits • Clock Period
Write	4	8	((4 + 8) • #ICs) • 8	Total Bits • Clock Period
Operation	4	0	4 • 8 = 32	32 • Clock Period

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each control loop cycle, and the duration of the control loop cycle. From this information it is possible to determine the percentage of time the LTC6811 is in the MEASURE state versus the low power SLEEP state. The amount of isoSPI or SPI communication will also affect the average supply current.

Calculating Serial Throughput

For any given LTC6811 the calculation to determine communication time is simple: it is the number of bits in the transmission multiplied by the SPI clock period being used. The control protocol of the LTC6811 is very uniform so almost all commands can be categorized as a write, read or an operation. Table 56 and Table 57 can be used to determine the number of bits in a given LTC6811 command. Table 56 can be used for daisy chains and Table 57 for multi-drop networks.

ENHANCED APPLICATIONS

Using the LTC6811 With Fewer Than 12 Cells

Internally the 12 cell inputs monitored by the LTC6811 are split into two groups of six cells and are measured using two internal multiplexers and two ADCs. To optimize measurement synchronization in applications with fewer than twelve cells, the unused C pins may be equally distributed between the top of the second MUX (C12) and the top of the first MUX (C6). See Figure 53. If there are an odd number of cells being measured, the top MUX should have fewer cells connected. The unused cell inputs should be tied to the other unused inputs on the same MUX and then connected to the battery stack through a 100Ω resistor. The unused inputs will result in a reading of 0.0V for those cells.

It is also acceptable to connect cells in the conventional sequence with all unused inputs at the top left open-circuit.

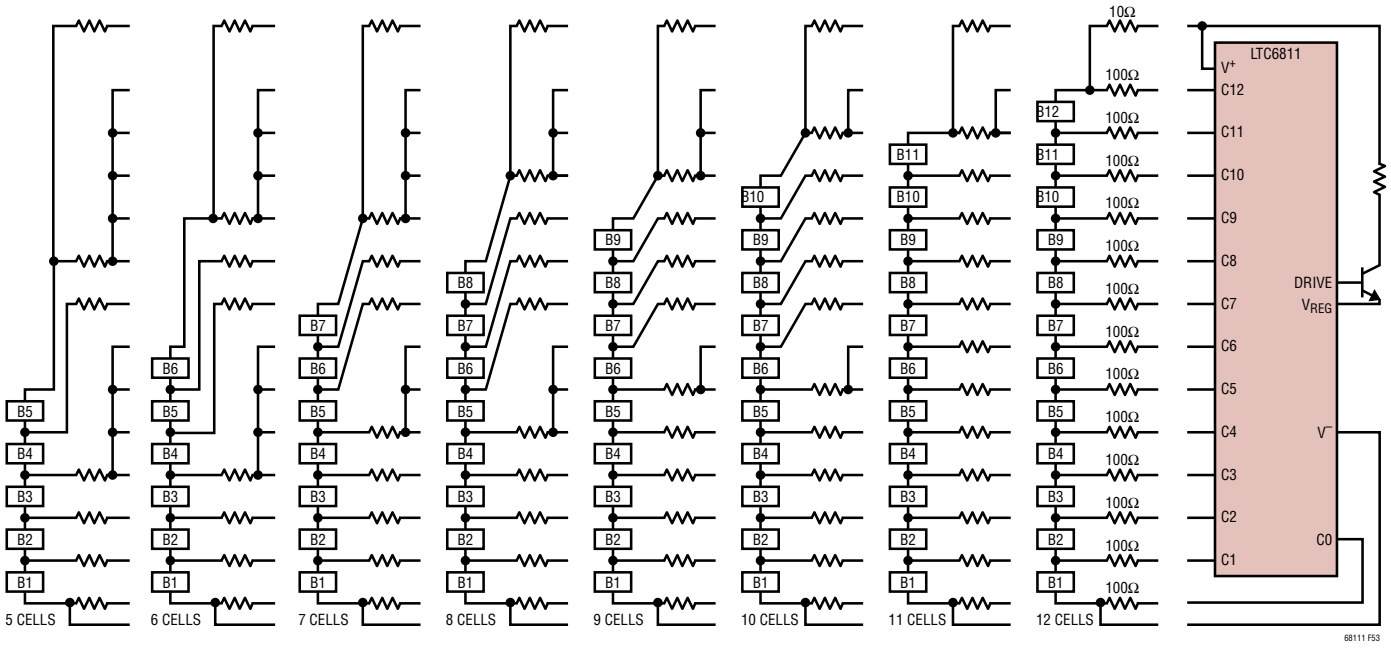


Figure 53. Cell Connection Schemes for 5 to 12 Cells

APPLICATIONS INFORMATION

Monitoring Fewer than 5 Cells

In applications using four cells or fewer, the V^+ must be provided by a separate supply to guarantee that the LTC6811 will operate over the cells entire voltage range. Figure 54 shows an application circuit to monitor 4 cells. The LT8301 is used to generate an isolated 18V supply. It is important that the converter produces a V^+ that is at a higher potential than the cell stack potential. In this case an 18V supply will allow the LTC6811 to operate with four cell voltages between 2V and 4.5V.

Current Measurement with a Hall-Effect Sensor

The LTC6811 auxiliary ADC inputs (GPIO pins) may be used for any analog signal, including active sensors with 0V to 5V analog outputs. For battery current measurements, Hall-effect sensors provide an isolated, low power solution. Figure 55 shows schematically a typical Hall-effect sensor that produces two outputs that proportion to the V_{CC} provided. The sensor in the figure has two bidirectional outputs centered at half of V_{CC}, CH1 is a 0A to 50A low range and CH2 is a 0A to 200A high range. The sensor is

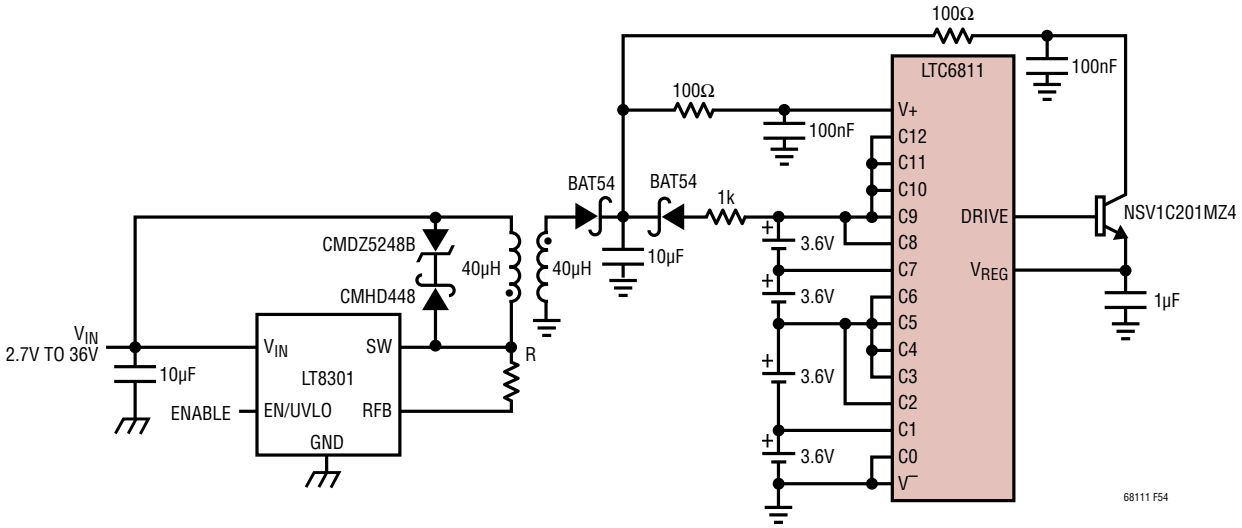


Figure 54. Powering the LTC6811 When Monitoring 4 Cells

APPLICATIONS INFORMATION

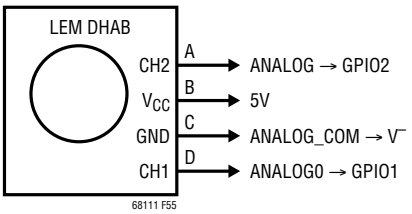


Figure 55. Interfacing a Typical Hall-Effect Battery Current Sensor to Auxiliary ADC Inputs

powered from a 5V source and produces analog outputs that are connected to GPIO pins or inputs of the MUX application shown in Figure 58. The use of GPIO1 and GPIO2 as the ADC inputs has the possibility of being digitized within the same conversion sequence as the cell inputs (using the ADCVAX command), thus synchronizing cell voltage and cell current measurements.

Low Side Current Sense

Many battery current sense applications require a bidirectional measurement that has both high accuracy and a wide dynamic range. Hall-effect sensors often have 2 outputs with different ranges to accommodate this requirement. For current sense solutions, using a small sense resistor shunt and a programmable gain amplifier provides a wide dynamic rage solution. Linear Technology's LTC6915 Digitally Programmable Instrumentation Amplifier is a good choice for this application because of its low 10µV offset and virtually no temperature coefficient. This allows the amplifier to work well with shunts of 100µΩ or greater. Figure 56 shows the LTC6915 configured to monitor bidirectional current on a low side shunt. Because of the low side architecture, a charge pump is needed to provide a negative rail for the amplifier to measure the shunt current during battery discharge.

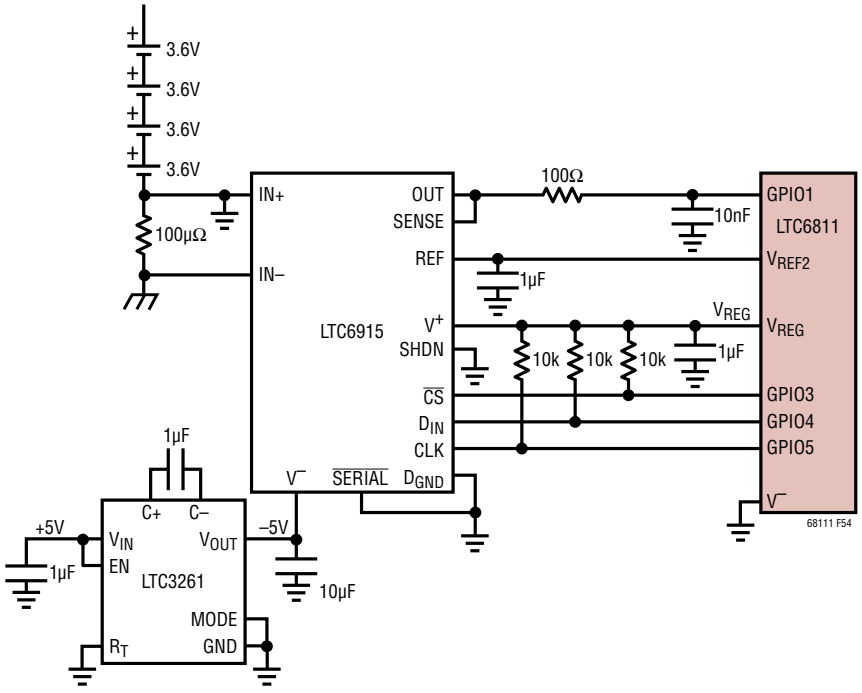


Figure 56. Low Side Current Sense

APPLICATIONS INFORMATION

READING EXTERNAL TEMPERATURE PROBES

Figure 57 shows the typical biasing circuit for a negative-temperature-coefficient (NTC) thermistor. The 10k at 25°C is the most popular sensor value and the V_{REF2} output stage is designed to provide the current required to bias several of these probes. The biasing resistor is selected to correspond to the NTC value so the circuit will provide 1.5V at 25°C (V_{REF2} is 3V nominal). The overall circuit response is approximately –1%/°C in the range of typical cell temperatures, as shown in the chart of Figure 57.

Expanding the Number of Auxiliary Measurements

The LTC6811 has five GPIO pins that can be used as ADC inputs. In applications that need to measure more than five signals a multiplexer (MUX) circuit can be implemented to expand the analog measurements to sixteen different signals (Figure 58). The GPIO1 ADC input is used for measurement and MUX control is provided by the I^2C port on GPIO 4 and 5. The buffer amplifier was selected for fast settling and will increase the usable throughput rate.

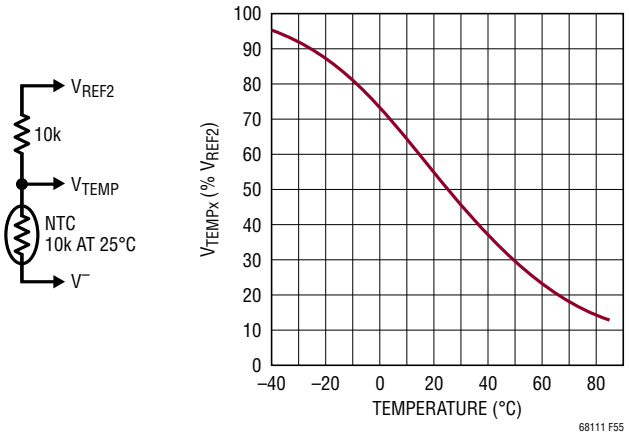


Figure 57. Typical Temperature Probe Circuit and Relative Output

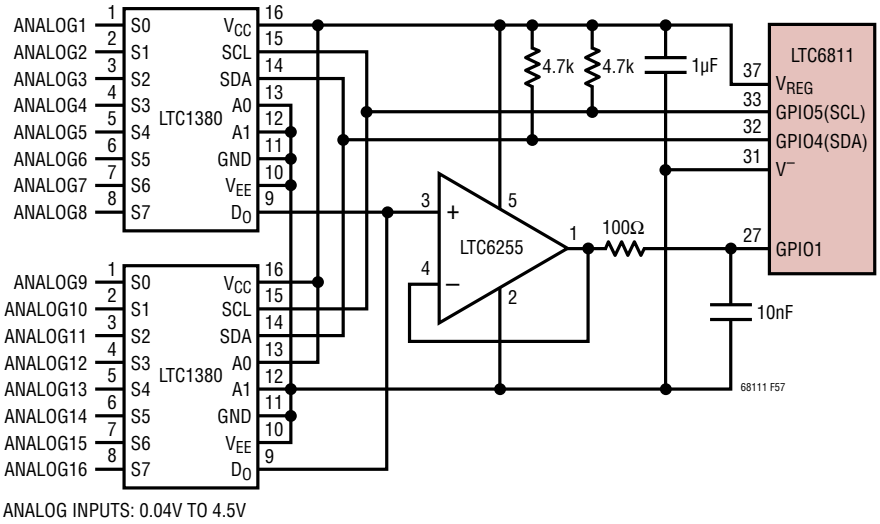
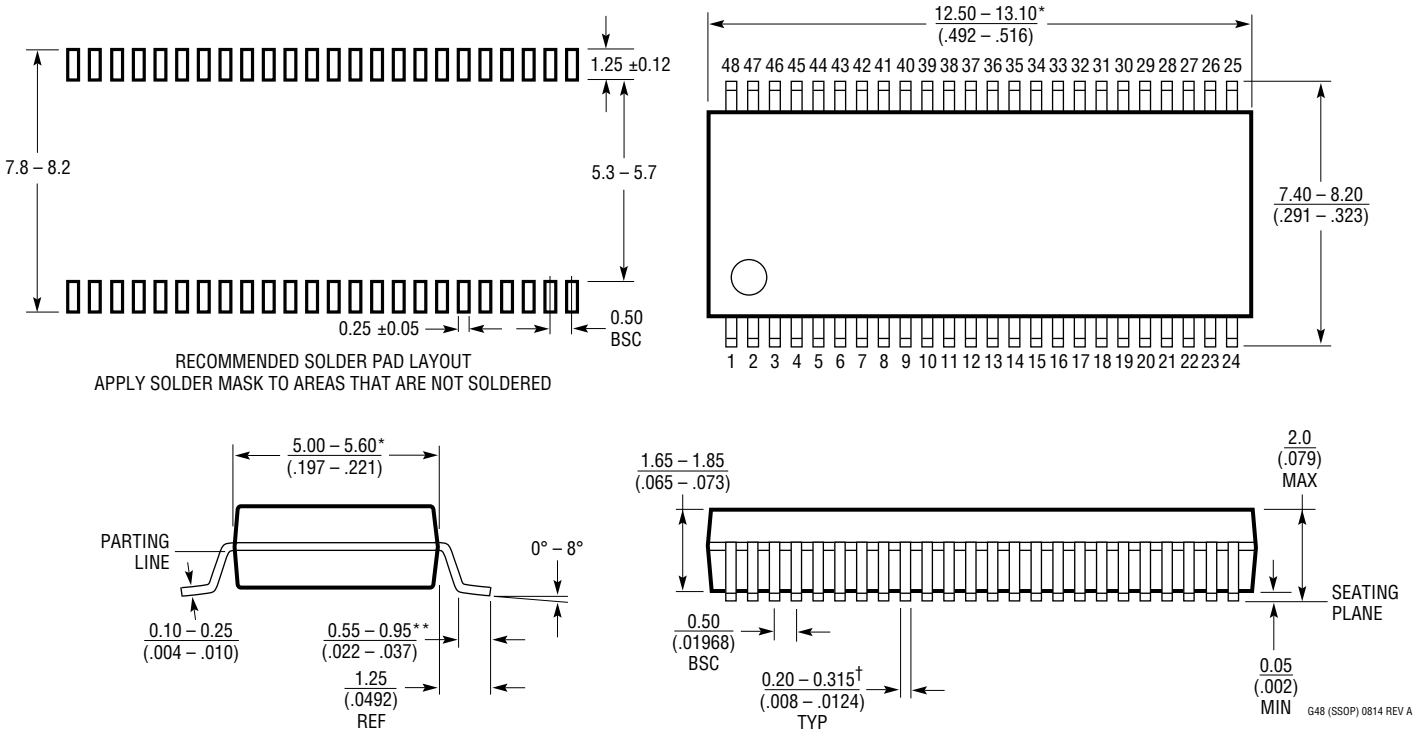


Figure 58. MUX Circuit Supports Sixteen Additional Analog Measurements

PACKAGE DESCRIPTION

G Package
48-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1887 Rev A)



NOTE:
1.DRAWING IS NOT A JEDEC OUTLINE
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
4. DRAWING NOT TO SCALE
5. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH SHALL NOT EXCEED .15mm PER SIDE

**LENGTH OF LEAD FOR SOLDERRING TO A SUBSTRATE

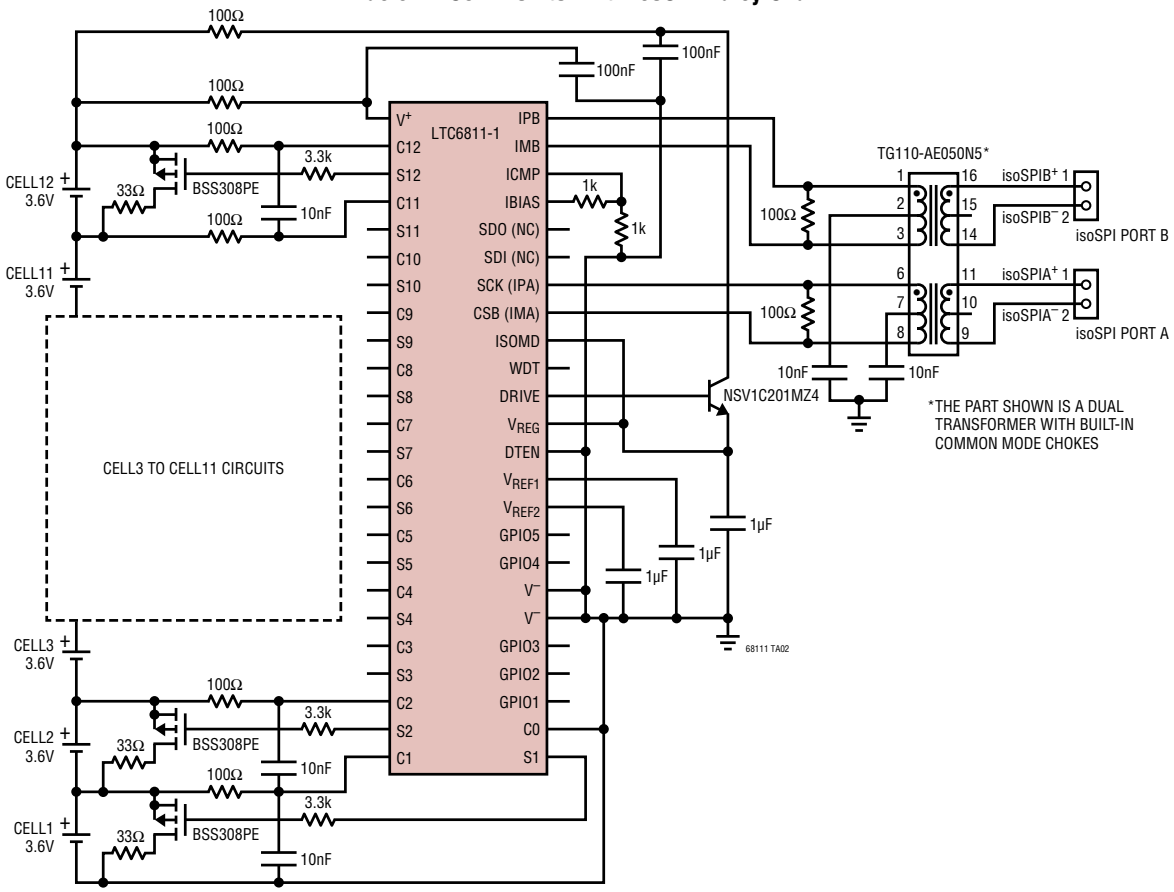
†THE MAXIMUM DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS DO NOT EXCEED 0.13mm PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/17	t_{SKEW2} specification correction: MIN = 211µs.	7
		t_{5GOV} specification correction: MIN = 0.6µs, MAX = 0.82µs.	9
		t_{6GOV} specification correction: MIN = 0.6µs, MAX = 1.05µs.	9
		Typical Performance Characteristics curve “isoSPI Comparator Threshold Gain (Port A/Port B) vs I_{BIAS} Current” renamed “isoSPI Comparator Threshold Gain (Port A/Port B) vs Receiver Common Mode”.	15
		Clarification to the impact statement of the Absolute Maximum spefications for the comparison of the LTC6811 Restriction vs LTC6804.	19
		Corrections to “Table 1. Core Supply Current”: STANDBY, $I_{REG(CORE)}$ = 40µA; REFUP, I_{VP} = 550µA, $I_{REG(CORE)}$ = 450µA; MEASURE, I_{VP} = 550µA.	21
		Corrections to the “Overlap Cell Measurement (ADOL Command)” section: After an ADOL command, the result from ADC2 is placed in Cell Voltage Register Group C and the result from ADC1 is placed in Cell Voltage Register Group C.	31
			62
		Correction to “Table 52. Memory Bit Descriptions”: DTEN description updated to include READ ONLY.	67
		Addition of the “Using Non-Standard Cell Input Filters” section and Figures 38 through 40.	67-88
		All Figures beginning with Figure 38 and above renumbered.	80
		“Table 54. Recommended Transformers” updated.	
B	08/17	Updated Drive Output Voltage specifications.	7
C	11/19	Added AEC-Qualification Indicator.	1
		Added Section “Reset Behaviors” into the Table of Contents.	2
		Device ESD Classifications Added.	3
		Order Information Updated Format.	4
		Renamed Sum of Cells to “Sum of All Cells”.	4, 5, 19, 29-31, 65
		Rewrite to section entitled “CORE LTC6811 STATE DESCRIPTIONS”.	20
		Rewrite to section entitled “Auxiliary(GPIO) Measurements with Digital Redundancy (ADAXD Command)”.	27
		Rewrite to section entitled “Measuring Internal Device Parameters with Digital Redundancy (ADSTATD Command)”.	30
		Added Section “RESET BEHAVIORS”.	37
		Correction to Table 52, section REF, Normal Range description.	65
		Rewrite to section entitled “Implementing a Modular isoSPI Daisy Chain”.	78
		Rewrite to section entitled “Connecting Multiple LTC6811-1s on the Same PCB”.	80
		Update to Table 54. Recommended Transformers.	83
		Rewrite to section entitled “Related Parts”.	92

TYPICAL APPLICATION

Basic 12-Cell Monitor with isoSPI Daisy Chain



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6810-1/ LTC6810-2	4th Generation 6-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 6 Series Battery Cells. Daisy-Chain Capability Allows Multiple Devices to Be Connected to Measure Many Battery Cells Simultaneously. The isoSPI Bus Can Operate Up to 1MHz and Can Be Operated Bidirectionally for Fault Conditions, Such As a Broken Wire or Connector. Includes Internal Passive Cell Balancing of up to 150mA.
LTC6812-1	4th Generation 15-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 15 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to Be Interconnected to Measure Many Battery Cells Simultaneously. The isoSPI Bus Can Operate Up to 1MHz and Can Be Operated Bidirectionally for Fault Conditions, Such As a Broken Wire or Connector. Includes Internal Passive Cell Balancing Capability of Up to 200mA.
LTC6813-1	4th Generation 18-Cell Battery Stack Monitor and Balancing IC	Measures Cell Voltages for Up to 18 Series Battery Cells. The isoSPI Daisy-Chain Capability Allows Multiple Devices to be Interconnected for Measuring Many Battery Cells Simultaneously. The isoSPI Bus can Operate Up to 1MHz and can be Operated Bidirectionally for Fault Conditions, such as a Broken Wire or Connector. Includes Internal Passive Cell Balancing Capability of Up to 200mA.
LTC6820	isoSPI Isolated Communications Interface	Provides an Isolated Interface for SPI Communication Up to 100 Meters, Using a Twisted Pair. Companion to the LTC6804, LTC6806, LTC6811, LTC6812 and LTC6813.