80V Synchronous 4-Switch Buck-Boost DC/DC Slave Controller for LT8708 Multiphase System

FEATURES

- **Slave Chip of LT8708 to Deliver Additional Power**
- **Good Current Matching to the Average Output Current of LT8708 Through Current Regulation**
- **Easily Paralleled with LT8708 Through Four Pins**
- **Synchronized Start-Up with LT8708**
- **Same Conduction Modes as LT8708**
- **Synchronous Rectification: Up to 98% Efficiency**
- Frequency Range: 100kHz to 400kHz
- Available in 40-Lead (5mm × 8mm) QFN with High Voltage Pin Spacing and 64-Lead (10mm × 10mm) eLQFP
- AEC-Q100 in Progress

APPLICATIONS

- High Voltage Buck-Boost Converters
- Bidirectional Charging Systems
- Automotive 48V Systems

DESCRIPTION

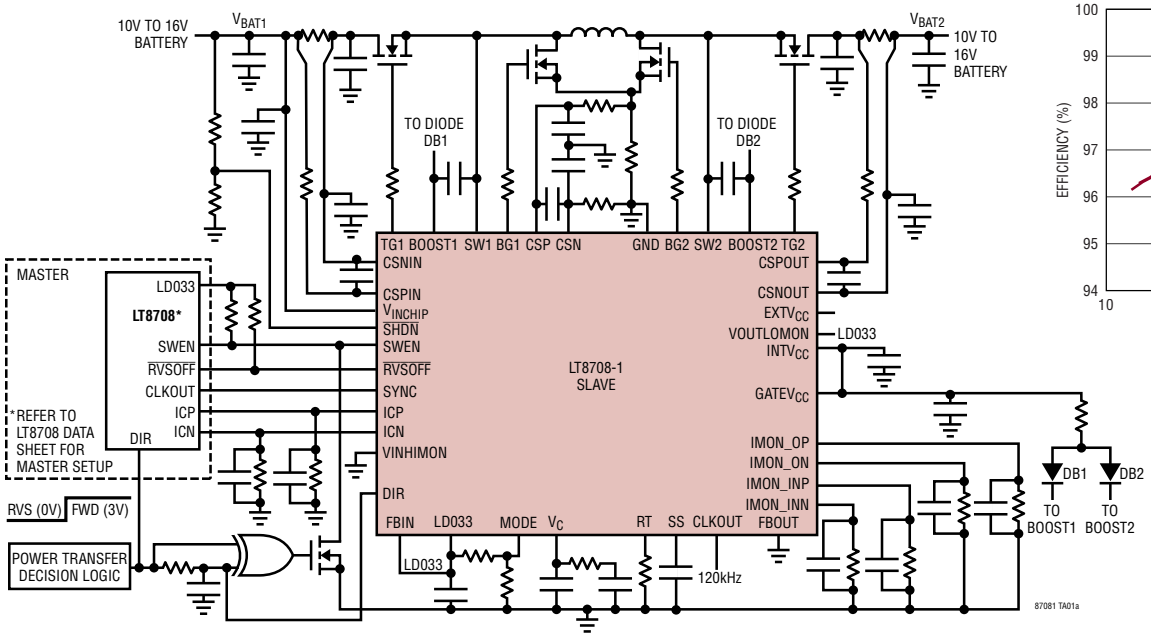
The LT®8708-1 is a high performance buck-boost switching regulator controller that is paralleled with the LT8708 to add power and phases to an LT8708 system. The LT8708-1 always operates as a slave to the master LT8708 and has the capability of delivering as much current or power as the master. One or more slaves can be connected to a single master, proportionally increasing power and current capability of the system.

The LT8708-1 has the same conduction modes as LT8708, allowing the LT8708-1 to conduct current and power in the same direction(s) as the master. The master controls the overall current and voltage limits for an LT8708 multiphase system, and the slaves comply with these limits.

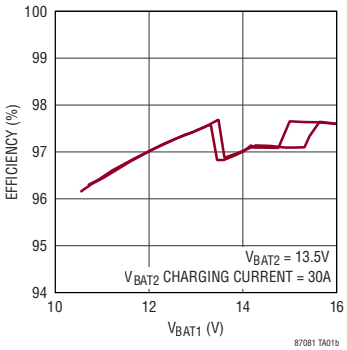
LT8708-1s can be easily paralleled with the LT8708 by connecting four signals together. Two additional current limits (forward V_{IN} current and reverse V_{IN} current) are available on each slave that can be set independently.

TYPICAL APPLICATION

The LT8708-1 Two-Phase 12V Bidirectional Dual Battery System with FHCM and RHCM



Efficiency



Rev A

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V_C Voltage (Note 2) ..... –0.3V to 2.2V
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IMON_INP, IMON_INN, IMON_OP, IMON_ON, ICP, ICN Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
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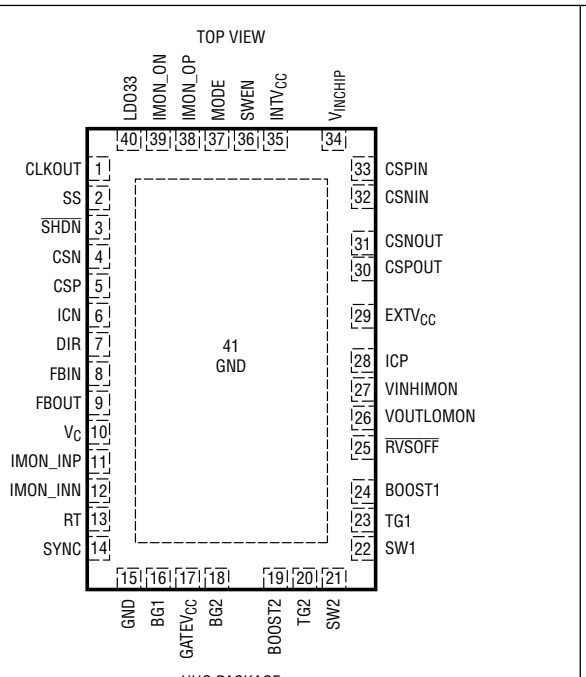
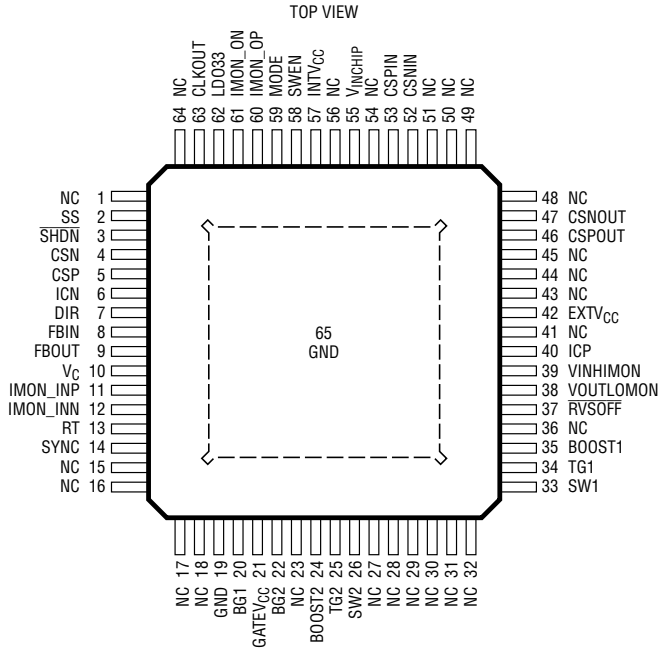
LT8708-1H (Notes 3, 8) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHG PACKAGE
40-LEAD (5mm × 8mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 36°C/W, θ_{JC} = 38°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB



LWE PACKAGE
64-LEAD (10mm × 10mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 17°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8708EUHG-1#PBF	LT8708EUHG-1#TRPBF	87081	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708IUHG-1#PBF	LT8708IUHG-1#TRPBF	87081	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708HUHG-1#PBF	LT8708HUHG-1#TRPBF	87081	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8708EUHG-1#WPBF	LT8708EUHG-1#WTRPBF	87081	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708IUHG-1#WPBF	LT8708IUHG-1#WTRPBF	87081	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 125°C
LT8708HUHG-1#WPBF	LT8708HUHG-1#WTRPBF	87081	40-Lead (5mm × 8mm) Plastic QFN	–40°C to 150°C

TRAY	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE
LT8708ELWE-1#PBF	LT8708LWE-1	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708ILWE-1#PBF	LT8708LWE-1	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708HLWE-1#PBF	LT8708LWE-1	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 150°C
AUTOMOTIVE PRODUCTS**				
LT8708ELWE-1#WPBF	LT8708LWE-1	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708ILWE-1#WPBF	LT8708LWE-1	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 125°C
LT8708HLWE-1#WPBF	LT8708LWE-1	64-Lead (10mm × 10mm) Plastic eLQFP	3	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{INCHIP} =12V, $\overline{SHDN}$ = 3V, DIR = 3.3V unless otherwise noted. (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supplies and Regulators						
V_{INCHIP} Operating Voltage Range	$EXTV_{CC}$ = 0V $EXTV_{CC}$ = 7.5V	● ●	5.5 2.8		80 80	V V
V_{INCHIP} Quiescent Current	Not Switching, V_{EXTVCC} = 0 SWEN = 3.3V SWEN = 0V			 4.7 2.45	 7.5 4.5	 mA mA
V_{INCHIP} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = –20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.2		V
$INTV_{CC}$ Current Limit	Max Current Draw from $INTV_{CC}$ and LDO33 Pins Combined. Regulated from V_{INCHIP} or $EXTV_{CC}$ (12V) $INTV_{CC}$ = 5.25V $INTV_{CC}$ = 4.4V	 ● ●	 90 28	 127 42	 165 55	 mA mA
$INTV_{CC}$ Voltage	Regulated from V_{INCHIP}, I_{INTVCC} = 20mA Regulated from $EXTV_{CC}$ (12V), I_{INTVCC} = 20mA	● ●	6.1 6.1	6.3 6.3	6.5 6.5	V V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 50mA			–0.5	–1.5	%
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling, $GATEV_{CC}$ Connected to $INTV_{CC}$	●	4.45	4.65	4.85	V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout Hysteresis	$GATEV_{CC}$ Connected to $INTV_{CC}$			160		mV
$INTV_{CC}$ Regulator Dropout Voltage	$V_{INCHIP} – V_{INTVCC}$, I_{INTVCC} = 20mA			245		mV
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			–0.25	–1	%
LDO33 Pin Current Limit	SYNC = 3V	●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
Maximum Current Sense Threshold ($V_{CSP} – V_{CSN}$)	Boost Mode, Minimum M3 Switch Duty Cycle	●	76	93	110	mV
Maximum Current Sense Threshold ($V_{CSN} – V_{CSP}$)	Buck Mode, Minimum M2 Switch Duty Cycle	●	68	82	97	mV
Maximum Current Sense Threshold ($V_{CSN} – V_{CSP}$)	Boost Mode, Minimum M3 Switch Duty Cycle	●	79	93	108	mV
Maximum Current Sense Threshold ($V_{CSP} – V_{CSN}$)	Buck Mode, Minimum M2 Switch Duty Cycle	●	72	84	96	mV
Gain from V_C to Max Current Sense Voltage ($V_{CSP} – V_{CSN}$) (A5 in the Block Diagram)	Boost Mode Buck Mode			135 –135		mV/V mV/V
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device QFN LWE	 ● ●	 1.175 1.175	 1.221 1.221	 1.275 1.29	 V V
$\overline{SHDN}$ Input Voltage High Hysteresis				40		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current (LT8708E-1, LT8708I-1) (LT8708H-1)	 ● ●			 0.35 0.3	 V V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 14	1 22	µA µA
SWEN Rising Threshold Voltage		●	1.156	1.208	1.256	V
SWEN Threshold Voltage Hysteresis				22		mV
SWEN Output Voltage Low	I_{SWEN} = 200µA $\overline{SHDN}$ = 0V or V_{INCHIP} = 0V $\overline{SHDN}$ = 3V	 ● ●		 0.9 0.2	 1.1 0.5	 V V
SWEN Internal Pull-Down Release Voltage	$\overline{SHDN}$ = 3V	●	0.75	0.8		V
MODE Pin Continuous Conduction Mode (CCM) Threshold		●	0.4			V
MODE Pin Hybrid DCM/CCM Mode (HCM) Range		●	0.8		1.2	V
MODE Pin Discontinuous Conduction Mode (DCM) Range		●	1.6		2.0	V
MODE Pin Burst Mode Operation Threshold		●			2.4	V
DIR Pin Forward Operation Threshold		●	1.6			V
DIR Pin Reverse Operation Threshold		●			1.2	V
$\overline{RVSOFF}$ Output Voltage Low	$I_{\overline{RVSOFF}}$ = 200µA	●		0.08	0.5	V
$\overline{RVSOFF}$ Falling Threshold Voltage		●	1.155	1.209	1.275	V
$\overline{RVSOFF}$ Threshold Voltage Hysteresis				165		mV
Soft-Start Charging Current	V_{SS} = 0V V_{SS} = 0.5V		13 21	19 31	25 41	µA µA
IMON_ON Rising Threshold for FDCM Operation	MODE = 1V (HCM), DIR = 3.3V	●	235	255	280	mV
IMON_ON Falling Threshold for CCM Operation	MODE = 1V (HCM), DIR = 3.3V	●	185	205	235	mV
IMON_INP Rising Threshold for RDCM Operation	MODE = 1V (HCM), DIR = 0V	●	235	255	280	mV
IMON_INP Falling Threshold for CCM Operation	MODE = 1V (HCM), DIR = 0V	●	185	205	235	mV

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ICP Rising Threshold for Start Switching		●	485	510	536	mV
ICN Rising Threshold for Start Switching		●	485	510	536	mV
ICP Rising Threshold for Enabling Non-CCM Offset Current		●	680	704	730	mV
ICP Falling Threshold for Disabling Non-CCM Offset Current		●	500	530	560	mV
ICN Rising Threshold for Enabling Non-CCM Offset Current		●	680	704	730	mV
ICN Falling Threshold for Disabling Non-CCM Offset Current		●	500	530	560	mV
Voltage Regulation Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltage for FBOUT	Regulate V_C to 1.2V	●	1.193	1.207	1.222	V
Regulation Voltage for FBIN	Regulate V_C to 1.2V	●	1.184	1.205	1.226	V
Line Regulation for FBOUT and FBIN Error Amp Reference Voltage	V_{INCHIP} = 12V to 80V, Not Switching			0.002	0.005	%/V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBOUT Error Amp EA4 g_m				345		µmho
FBOUT Error Amp EA4 Voltage Gain				245		V/V
VOUTLOMON Voltage Activation Threshold	Falling	●	1.185	1.207	1.225	V
VOUTLOMON Threshold Voltage Hysteresis				24		mV
VOUTLOMON Pin Bias Current	$V_{VOUTLOMON}$ = 1.24V, Current Into Pin $V_{VOUTLOMON}$ = 1.17V, Current Into Pin	 ●	 0.8	0.01 1	 1.2	µA µA
FBIN Pin Bias Current	Current Out of Pin			10		nA
FBIN Error Amp EA3 g_m				235		µmho
FBIN Error Amp EA3 Voltage Gain				150		V/V
VINHIMON Voltage Activation Threshold	Rising	●	1.185	1.207	1.23	V
VINHIMON Threshold Voltage Hysteresis				24		mV
VINHIMON Pin Bias Current	$V_{VINHIMON}$ = 1.17V, Current Into Pin $V_{VINHIMON}$ = 1.24V, Current Out of Pin	 ●	 0.8	0.01 1	 1.2	µA µA
Current Regulation Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltages for IMON_INP and IMON_OP	V_C = 1.2V	●	1.185	1.209	1.231	V
Regulation Voltages for IMON_INN	V_C = 1.2V	●	1.185	1.21	1.24	V
Line Regulation for IMON_INP, IMON_INN and IMON_OP Error Amp Reference Voltage	V_{INCHIP} = 12V to 80V			0.002	0.005	%/V
CSPIN Bias Current	V_{CSPIN} = 12V V_{CSPIN} = 1.5V			0.01 0.01		µA µA
CSNIN Bias Current	BOOST Capacitor Charge Control Block Not Active V_{SWEN} = 3.3V, V_{CSPIN} = V_{CSNIN} = 12V V_{SWEN} = 3.3V, V_{CSPIN} = V_{CSNIN} = 1.5V V_{SWEN} = 0V			 84 4.25 0.01		 µA µA µA
CSPIN, CSNIN Common Mode Operating Voltage Range		●	0		80	V
CSPIN, CSNIN Differential Mode Operating Voltage Range		●	–100		100	mV
IMON_INP Output Current	V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSNIN} = 5V V_{CSPIN} – V_{CSNIN} = 50mV, V_{CSNIN} = 5V V_{CSPIN} – V_{CSNIN} = 5mV, V_{CSNIN} = 5V V_{CSPIN} – V_{CSNIN} = 5mV, V_{CSNIN} = 5V	 ● ●	67 64.5 22.5 20	70 70 25 25	73 75.5 27.5 30	µA µA µA µA
IMON_INN Output Current	V_{CSNIN} – V_{CSPIN} = 50mV, V_{CSNIN} = 5V V_{CSNIN} – V_{CSPIN} = 50mV, V_{CSNIN} = 5V V_{CSNIN} – V_{CSPIN} = 5mV, V_{CSNIN} = 5V V_{CSNIN} – V_{CSPIN} = 5mV, V_{CSNIN} = 5V	 ● ●	66 65 19 18	70 70 25 25	74 75 30.5 32	µA µA µA µA

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
IMON_INP and IMON_INN Max Output Current			●	120			µA
IMON_INP Error Amp EA5 g_m					190		µmho
IMON_INP Error Amp EA5 Voltage Gain					130		V/V
IMON_INN Error Amp EA1 g_m	FBIN = 0V, FBOUT = 3.3V				190		µmho
IMON_INN Error Amp EA1 Voltage Gain	FBIN = 0V, FBOUT = 3.3V				130		V/V
CSPOUT Bias Current	V_{CSPOUT} = 12V V_{CSPOUT} = 1.5V				0.01 0.01		µA µA
CSNOUT Bias Current	BOOST Capacitor Charge Control Block Not Active V_{SWEN} = 3.3V, V_{CSPOUT} = V_{CSNOUT} = 12V V_{SWEN} = 3.3V, V_{CSPOUT} = V_{CSNOUT} = 1.5V V_{SWEN} = 0V				 83 4.25 0.01		 µA µA µA
CSPOUT, CSNOUT Common Mode Operating Voltage Range			●	0		80	V
CSPOUT, CSNOUT Differential Mode Operating Voltage Range			●	–100		100	mV
IMON_ON Output Current	V_{CSNOUT} – V_{CSPOUT} = 50mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = 50mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = 5mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = 5mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = –5mV, V_{CSNOUT} = 5V V_{CSNOUT} – V_{CSPOUT} = –5mV, V_{CSNOUT} = 5V		 ● ● ●	67 65 22.5 20.5 12.5 10.5	70 70 25 25 15 15	73 75 27.5 29 17.5 19.5	µA µA µA µA µA µA
IMON_ON Max Output Current			●	120			µA
CSPOUT–CSNOUT Regulation Voltage	Regulate V_C to 1.2V R_{IMON_OP} = 17.4kΩ V_{CSNOUT} = 12V	ICP = 1.218V, ICN = 0V	●	43	50	55	mV
		ICP = 0V, ICN = 1.218V	●	–55	–50	–44	mV
		ICP = ICN = 0.348V	●	–6	0	6	mV
NMOS Gate Drivers							
TG1, TG2 Rise Time	C_{LOAD} = 3300pF (Note 4)				20		ns
TG1, TG2 Fall Time	C_{LOAD} = 3300pF (Note 4)				20		ns
BG1, BG2 Rise Time	C_{LOAD} = 3300pF (Note 4)				20		ns
BG1, BG2 Fall Time	C_{LOAD} = 3300pF (Note 4)				20		ns
TG1 Off to BG1 On Delay	C_{LOAD} = 3300pF Each Driver				90		ns
BG1 Off to TG1 On Delay	C_{LOAD} = 3300pF Each Driver				80		ns
TG2 Off to BG2 On Delay	C_{LOAD} = 3300pF Each Driver				90		ns
BG2 Off to TG2 On Delay	C_{LOAD} = 3300pF Each Driver				80		ns
Min On-Time for Main Switch in Boost Operation ($t_{ON(M3,MIN)}$)	Switch M3, C_{LOAD} = 3300pF				200		ns
Min On-Time for Synchronous Switch in Buck Operation ($t_{ON(M2,MIN)}$)	Switch M2, C_{LOAD} = 3300pF				200		ns
Min Off-Time for Main Switch in Steady-State Boost Operation	Switch M3, C_{LOAD} = 3300pF				230		ns
Min Off-Time for Synchronous Switch in Steady-State Buck Operation	Switch M2, C_{LOAD} = 3300pF				230		ns
Oscillator							
Switch Frequency Range	SYNCing or Free Running			100		400	kHz
Switching Frequency, f_{OSC}	R_T = 365k R_T = 215k R_T = 124k		● ● ●	102 170 310	120 202 350	142 235 400	kHz kHz kHz
SYNC High Level for Synchronization			●	1.3			V
SYNC Low Level for Synchronization			●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V			20		80	%
Recommended Min SYNC Ratio f_{SYNC}/f_{OSC}					3/4		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{INCHIP} =12V, $\overline{SHDN}$ = 3V, DIR = 3.3V unless otherwise noted. (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLKOUT Output Voltage High	$V_{LDO33} – V_{CLKOUT}$, 1mA Out of CLKOUT Pin, I_{LDO33} = 0µA			100	250	mV
CLKOUT Output Voltage Low	1mA Into CLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.7 44.1 77		% % %
CLKOUT Rise Time	C_{LOAD} = 200pF			20		ns
CLKOUT Fall Time	C_{LOAD} = 200pF			20		ns
CLKOUT Phase Delay	SYNC Rising to CLKOUT Rising, f_{OSC} = 100kHz	●	160	180	200	Degree

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8708E-1 is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8708I-1 is guaranteed over the full –40°C to 125°C junction temperature range. The LT8708H-1 is guaranteed over the full –40°C to 150°C operating junction temperature range.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

Note 6: Negative voltages on the SW1 and SW2 pins are limited, in an application, by the body diodes of the external NMOS devices, M2 and M3, or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

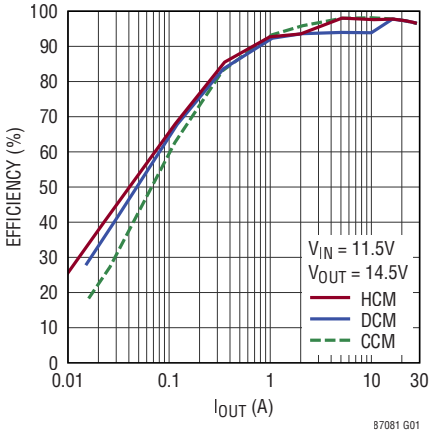
Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 8: Do not force voltage or current into these pins.

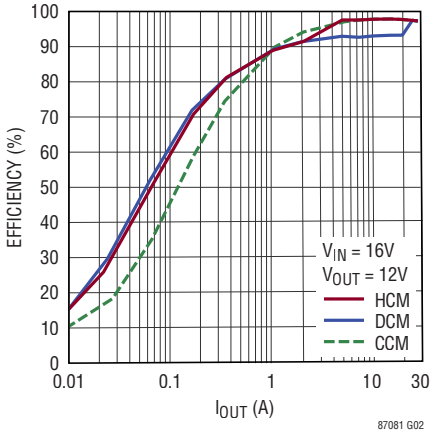
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

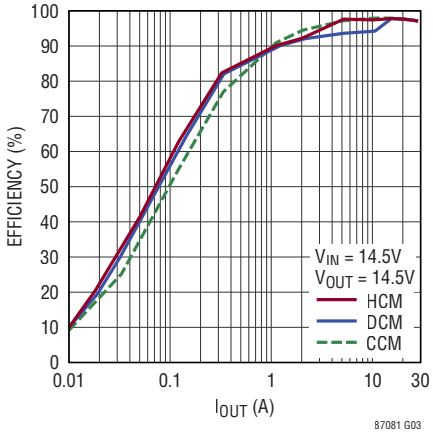
Efficiency vs Output Current (Boost Region – Page 32)



Efficiency vs Output Current (Buck Region – Page 32)

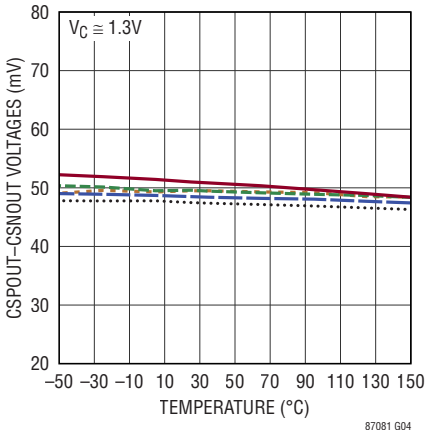


Efficiency vs Output Current (Buck-Boost Region – Page 32)

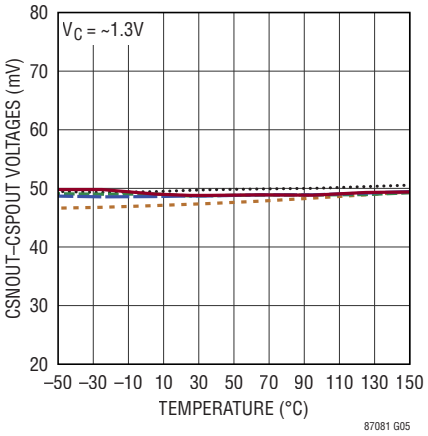


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

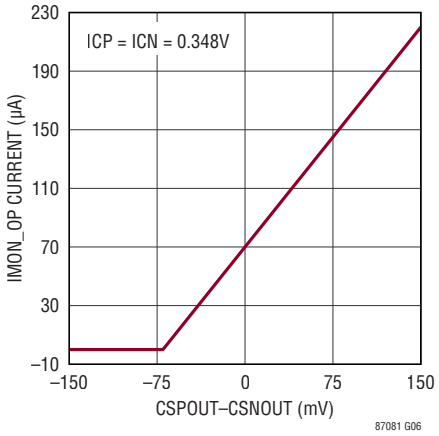
CSPOUT – CSNOUT Voltages (ICP = 1.218V, ICN = 0V) (Five Parts)



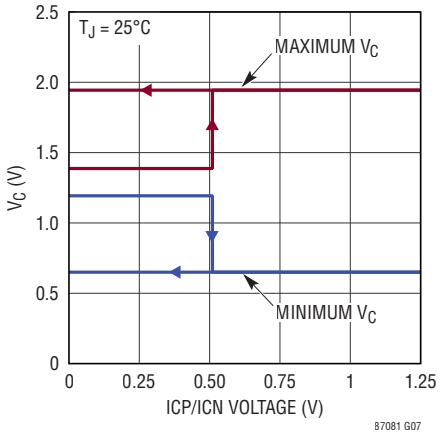
CSNOUT – CSPOUT Voltages (ICP = 1.218V, ICN = 0V) (Five Parts)



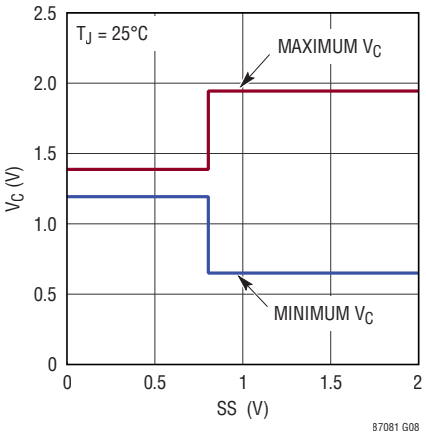
IMON_OP Output Current



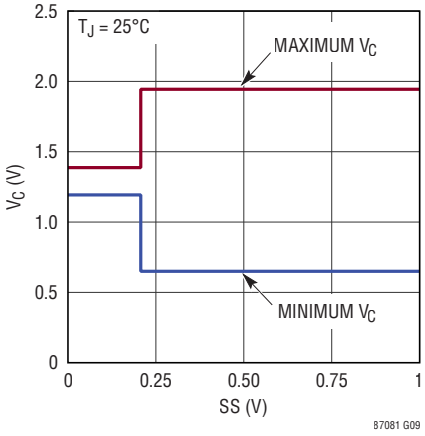
Maximum and Minimum V_C vs ICP_ICN (SS = 0)



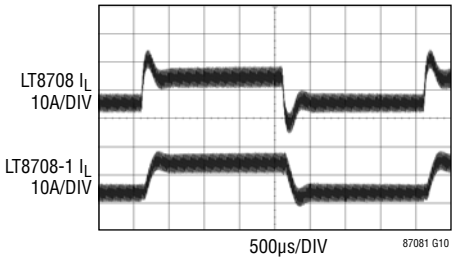
Maximum and Minimum V_C vs SS (ICP = ICN =0.348V)



Maximum and Minimum V_C vs SS (ICP or ICN = 1V)

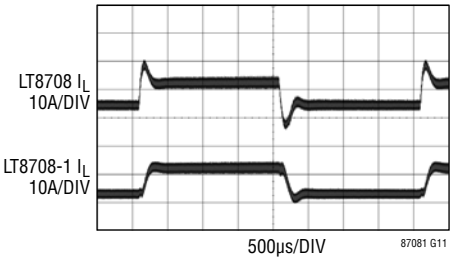


Load Step (Page 32) V_{IN} = 12V V_{OUT} = 14.5V



V_{BAT1} = 12V, V_{BAT2} REGULATED TO 14.5V
LOAD STEP = 10A TO 25A
LOAD APPLIED AT V_{BAT2} WITH
BATTERY DISCONNECTED

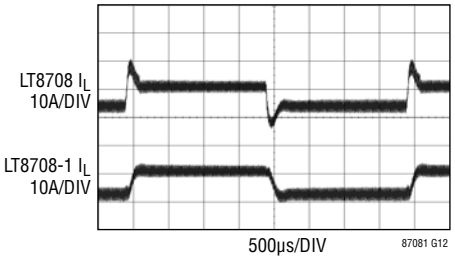
Load Step (Page 32) V_{IN} = 14.5V V_{OUT} = 14.5V



V_{BAT1} = 14.5V, V_{BAT2} REGULATED TO 14.5V
LOAD STEP = 10A TO 25A
LOAD APPLIED AT V_{BAT2} WITH
BATTERY DISCONNECTED

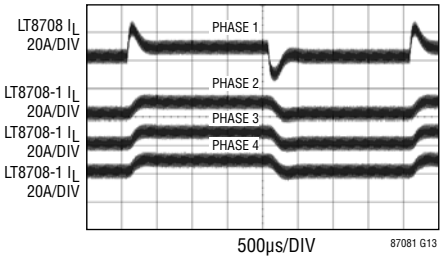
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Load Step (Page 32) V_{IN} = 16V V_{OUT} = 14.5V



V_{BAT1} = 16V, V_{BAT2} REGULATED TO 14.5V
LOAD STEP = 10A TO 25A
LOAD APPLIED AT V_{BAT2} WITH
BATTERY DISCONNECTED

Load Step (Page 33) V_{IN} = 48V V_{OUT} = 14.5V



V_{BAT1} = 48V, V_{BAT2} REGULATED TO 14.5V
LOAD STEP = 20A TO 55A
LOAD APPLIED AT V_{BAT2} WITH
BATTERY DISCONNECTED

PIN FUNCTIONS (QFN/eLQFP)

CLKOUT (Pin 1/Pin 63): Clock Output Pin. Use this pin to synchronize one or more compatible switching regulator ICs. CLKOUT toggles at the same frequency as the internal oscillator or as the SYNC pin, but is approximately 180° out of phase. CLKOUT may also be used as a temperature monitor since the CLKOUT duty cycle varies linearly with the part's junction temperature. The CLKOUT pin can drive capacitive loads up to 200pF.

SS (Pin 2/Pin 2): Soft-Start Pin. Place a capacitor from this pin to ground. A capacitor identical to the SS pin capacitor used on the master LT8708 is recommended. Upon start-up, this pin will be charged by an internal resistor to 3.3V.

$\overline{SHDN}$ (Pin 3/Pin 3): Shutdown Pin. Tie high to enable chip. Ground to shut down and reduce quiescent current to a minimum. Do not float this pin.

CSN (Pin 4/Pin 4): The (–) Input to the Inductor Current Sense and DCM Detect Comparator.

CSP (Pin 5/Pin 5): The (+) Input to the Inductor Current Sense and DCM Detect Comparator. The V_C pin voltage and built-in offsets between CSP and CSN pins, in conjunction with the R_{SENSE} value, set the inductor current trip threshold. It is recommended to use the same value R_{SENSE} as the master LT8708.

ICN (Pin 6/Pin 6): Negative V_{OUT} Current Command Pin. The voltage on this pin determines the negative V_{OUT} current for LT8708-1 to regulate to. Connect this pin to the master LT8708's ICN pin. See the Applications Information section for more information.

DIR (Pin 7/Pin 7): Direction pin when MODE is set for DCM (discontinuous conduction mode) or HCM (hybrid conduction mode) operation. Otherwise this pin is ignored. Connect the pin to GND to process power from the V_{OUT} to V_{IN}. Connect the pin to LDO33 to process power from the V_{IN} to V_{OUT}. Drive this pin with the same control signal, or connect this pin to the same voltages as the master LT8708.

FBIN (Pin 8/Pin 8): V_{IN} Feedback Pin. This pin is connected to the input of error amplifier EA3. Typically, connect this pin to LDO33 to disable the EA3.

FBOUT (Pin 9/Pin 9): V_{OUT} Feedback Pin. This pin is connected to the input of error amplifier EA4. Typically, connect this pin to GND to disable the EA4.

V_C (Pin 10/Pin 10): Error Amplifier Output Pin. Tie external compensation network to this pin.

IMON_INP (Pin 11/Pin 11): Positive V_{IN} Current Monitor and Limit Pin. The current out of this pin is 20µA plus a current proportional to the positive average V_{IN} current. IMON_INP also connects to error amplifier EA5 and can

PIN FUNCTIONS (QFN/eLQFP)

be used to limit the maximum positive V_{IN} current. See the Applications Information section for more information.

IMON_INN (Pin 12/Pin 12): Negative V_{IN} Current Monitor and Limit Pin. The current out of this pin is 20µA plus a current proportional to the negative average V_{IN} current. IMON_INN also connects to error amplifier EA1 and can be used to limit the maximum negative V_{IN} current. See the Applications Information section for more information.

RT (Pin 13/Pin 13): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the frequency. It is recommended to use the same value R_T resistor as the master LT8708. Do not float this pin.

SYNC (Pin 14/Pin 14): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. In a two-phase system, connect this pin to the master LT8708's CLKOUT pin to have a 180° phase shift. See the Applications Information section for more information.

BG1, BG2 (Pin 16/Pin 20, Pin 18/Pin 22): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFETs between ground and $GATEV_{CC}$.

$GATEV_{CC}$ (Pin 17/Pin 21): Power supply for bottom gate drivers. Must be connected to the $INTV_{CC}$ pin. Do not power from any other supply. Locally bypass to GND. It is recommended to use the same value bypass cap as the master LT8708.

BOOST1, BOOST2 (Pin 24/Pin 35, Pin 19/Pin 24): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{IN} + $GATEV_{CC}$. The BOOST2 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{OUT} + $GATEV_{CC}$.

TG1, TG2 (Pin 23/Pin 34, Pin 20/Pin 25): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to $GATEV_{CC}$ superimposed on the switch node voltages.

SW1, SW2 (Pin 22/Pin 33, Pin 21/Pin 26): Switch Nodes. The (–) terminals of the bootstrap capacitors connect here.

$\overline{RVSOFF}$ (Pin 25/Pin 37): Reverse Conduction Disable Pin. This is an input/output open-drain pin that requires a pull-up resistor. Pulling this pin low disables reverse current operation. Typically, connect this pin to the LT8708's $\overline{RVSOFF}$ pin. See the Unidirectional and Bidirectional Conduction section for more information.

VOUTLOMON (Pin 26/Pin 38): V_{OUT} Low Voltage Monitor Pin. Connect a ±1% resistor divider between V_{OUT}, VOUTLOMON and GND to set an undervoltage level on V_{OUT}. When V_{OUT} is lower than this level, reverse conduction is disabled to prevent drawing current from V_{OUT}. See the Applications Information section for more information.

VINHIMON (Pin 27/Pin 39): V_{IN} High Voltage Monitor Pin. Connect a ±1% resistor divider between V_{IN}, VINHIMON and GND in order to set an overvoltage level on V_{IN}. When V_{IN} is higher than this level, reverse conduction is disabled to prevent current flow into V_{IN}. See the Applications Information section for more information.

ICP (Pin 28/Pin 40): Positive V_{OUT} Current Command Pin. The voltage on this pin determines the positive V_{OUT} current for LT8708-1 to regulate to. Connect this pin to LT8708's ICP pin. See the Applications Information section for more information.

$EXTV_{CC}$ (Pin 29/Pin 42): External V_{CC} Input. When $EXTV_{CC}$ exceeds 6.4V (typical), $INTV_{CC}$ will be powered from this pin. When $EXTV_{CC}$ is lower than 6.4V, the $INTV_{CC}$ will be powered from V_{INCHIP}. It is recommended to use the same value bypass cap as the master LT8708.

CSPOUT (Pin 30/Pin 46): The (+) Input to the V_{OUT} Current Monitor Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor, R_{SENSE2}, to provide the V_{OUT} current signals. It is recommended to use the same value R_{SENSE2} between the CSPOUT and CSNOUT pins as the master LT8708. See Applications Information section for proper use of this pin.

CSNOUT (Pin 31/Pin 47): The (–) Input to the V_{OUT} Current Monitor Amplifier. See Applications Information section for proper use of this pin.

CSNIN (Pin 32/Pin 52): The (–) Input to the V_{IN} Current Monitor Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor, R_{SENSE1}, to provide

PIN FUNCTIONS (QFN/eLQFP)

the V_{IN} current signals. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

CSPIN (Pin 33/Pin 53): The (+) Input to the V_{IN} Current Monitor Amplifier. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

V_{INCHIP} (Pin 34/Pin 55): Main Input Supply Pin for the LT8708-1. It must be locally bypassed to ground. It is recommended to use the same value bypass cap as the master LT8708.

$INTV_{CC}$ (Pin 35/Pin 57): 6.35V Regulator Output. Must be connected to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{INCHIP}. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor. It is recommended to use the same value bypass cap as the master LT8708.

SWEN (Pin 36/Pin 58): Switching Regulator Enable Pin. Tie high through a resistor to enable the switching. Ground to disable switching. This pin is pulled down during shutdown, a thermal lockout or when an internal UVLO (Under Voltage Lockout) is detected. Do not float this pin. Connect this pin to the LT8708's SWEN pin for synchronized start-up. See the Start-Up: SWEN Pin section for more details.

MODE (Pin 37/Pin 59): Conduction Mode Select Pin. The voltage applied to this pin sets the conduction mode of the controller. Apply less than 0.4V to enable continuous conduction mode (CCM). Apply 0.8V to 1.2V to enable the hybrid conduction mode (HCM). Apply 1.6V to 2.0V to enable the discontinuous conduction mode (DCM). Apply more than 2.4V to enable Burst Mode operation. It is recommended to drive this pin with the same control signal, or connect this pin to the same value resistor dividers or voltages as the master LT8708.

IMON_OP (Pin 38/Pin 60): Average V_{OUT} Current Regulation Pin. This pin servos to 1.207V to regulate the average output current based on the ICP and ICN voltages. Always connect a 17.4k resistor in parallel with a compensation network from this pin to GND. See the Applications Information section for more information.

IMON_ON (Pin 39/Pin 61): Negative V_{OUT} Current Monitor Pin. The current out of this pin is 20µA plus a current proportional to the negative average V_{OUT} current. See the Applications Information section for more information.

LDO33 (Pin 40/Pin 62): 3.3V Regulator Output. Bypass this pin to ground with a minimum 0.1µF ceramic capacitor. It is recommended to use the same value bypass cap as the master LT8708.

GND (Pin 15/Pin 19, Exposed Pad Pin 41/Pin 65): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM

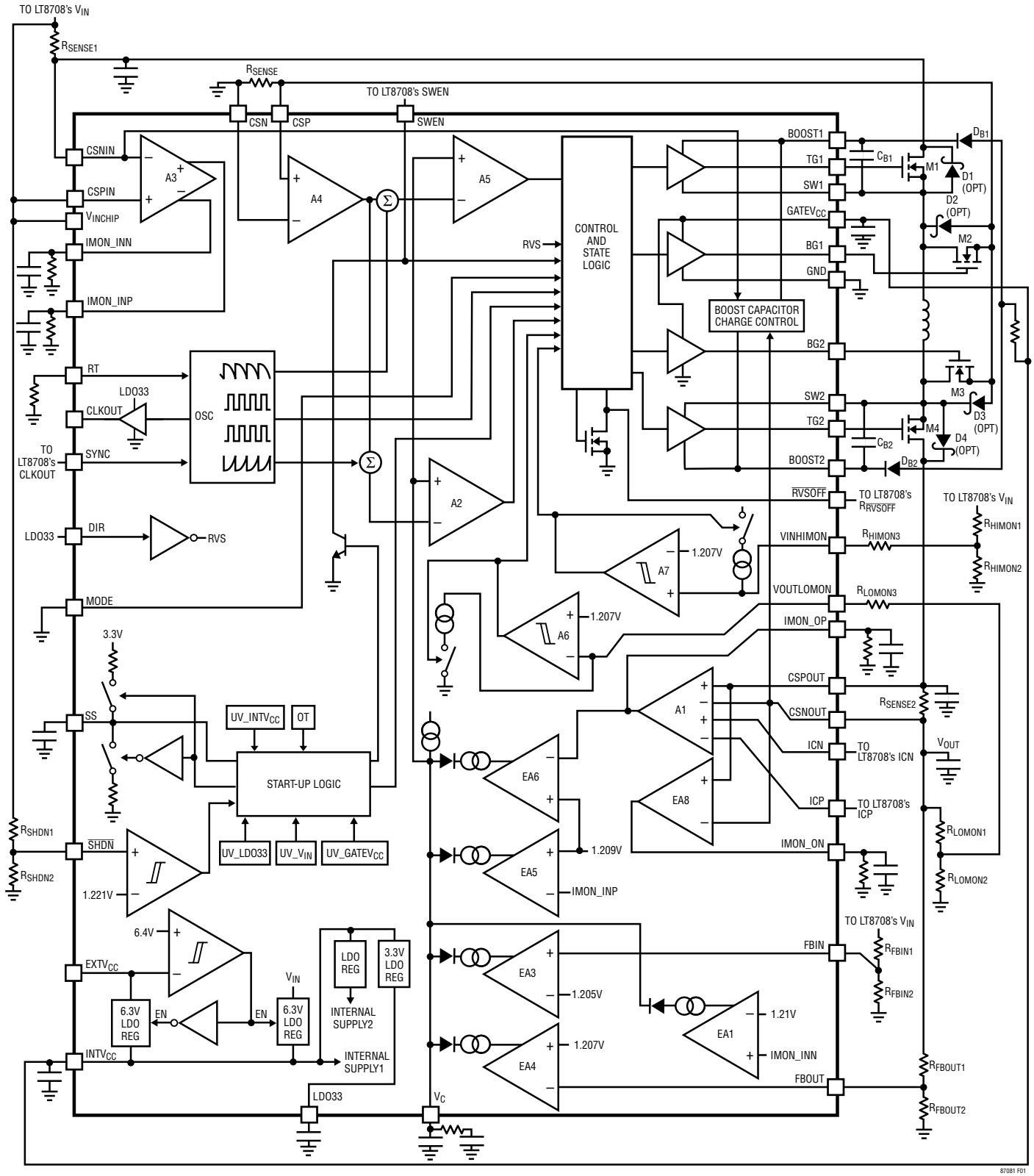


Figure 1. Block Diagram

OPERATION

The LT8708-1 is a high performance 4-switch buck-boost slave controller that is paralleled with the master LT8708 to increase power capability. Using LT8708-1(s) with the LT8708, an application can command power to be delivered from V_{IN} to V_{OUT} or from V_{OUT} to V_{IN} as needed.

COMMON LT8708-1 AND LT8708 FEATURES

The LT8708-1 and LT8708 share many common functions and features that are already documented in the LT8708 data sheet. Table 1 lists the LT8708 data sheet sections that also apply to the LT8708-1. For some of these features, additional LT8708-1 specific information is provided in this data sheet, as indicated in Table 1.

The focus of this data sheet is on how to use the LT8708-1 to increase the number of switching phases in an LT8708-based application. As such, functionality that is identical in both the LT8708 and LT8708-1 will not necessarily be repeated here. It is assumed that readers of this data sheet are already familiar with the LT8708.

Table 1. LT8708 Data Sheet Sections that Apply to the LT8708-1

LT8708 DATA SHEET SECTION	ADDITIONAL INFORMATION IN THIS DATA SHEET
Operation	
Start-Up: $\overline{SHDN}$ Pin	
Power Switch Control	
Unidirectional and Bidirectional Conduction	Yes
$INTV_{CC}$/$EXTV_{CC}$/$GATEV_{CC}$/LDO33 Power	
CLKOUT and Temperature Sensing	
Applications Information	
Internal Oscillator	
SYNC Pin and Clock Synchronization	
CLKOUT Pin and Clock Synchronization	
Inductor Current Sensing and Slope Compensation	
R_{SENSE} Selection and Maximum Current	
R_{SENSE} Filtering	
Inductor (L) Selection	
Power MOSFET Selection	
Schottky Diode (D1, D2, D3, D4) Selection	
Topside MOSFET Driver Supply (C_{B1}, D_{B1}, C_{B2}, D_{B2})	
VINHIMON, VOUTLOMON and $\overline{RVSOFF}$	Yes
$INTV_{CC}$ Regulators and $EXTV_{CC}$ Connection	
LDO33 Regulator	
Voltage Lockouts	Yes
Junction Temperature Measurement	
Thermal Shutdown	
Efficiency Considerations	
Circuit Board Layout Checklist	Yes

ADDING PHASES TO AN LT8708 APPLICATION

In a multiphase LT8708 application, a single LT8708 is the master of the system. One or more LT8708-1s are slaves that provide additional current as needed. As the master of the multiphase system, the LT8708 and its respective error amplifiers, determine the current necessary to regulate the V_{IN} voltage, V_{OUT} voltage, V_{IN} current and V_{OUT} current. The slave LT8708-1 operates by sensing the $I_{OUT(MASTER)}$ (see Figure 2) and delivering a proportional amount of $I_{OUT(SLAVE)}$. Again, since $I_{OUT(SLAVE)}$ is proportional to $I_{OUT(MASTER)}$, the master LT8708 is in control of setting regulation voltages and current limits to the system.

Each LT8708 and LT8708-1, connected in parallel, is hereon referred to as a phase, the master and slave V_{IN} current is referred to as $I_{IN(MASTER)}$ and $I_{IN(SLAVE)}$, respectively. For multiphase operation, the LT8708 should be configured according to the LT8708 data sheet. Configuration of LT8708-1s should follow instructions in this data sheet. Figure 2 shows a simplified drawing of a multiphase system with one LT8708 and multiple LT8708-1s. It illustrates the basic connections needed to add LT8708-1s to a multiphase system.

Adding Phases: The Master LT8708

The master controls the overall current delivered by the multiphase system. For example, the LT8708 controls the V_{IN} and V_{OUT} regulation voltages through its FBIN and FBOUT pins. Since the slaves primarily duplicate the master's $I_{OUT(MASTER)}$ current, the slave's FBIN and FBOUT pins and related circuitry are typically not used. See the Error Amplifiers section on how they can affect V_C and how to disable them.

OPERATION

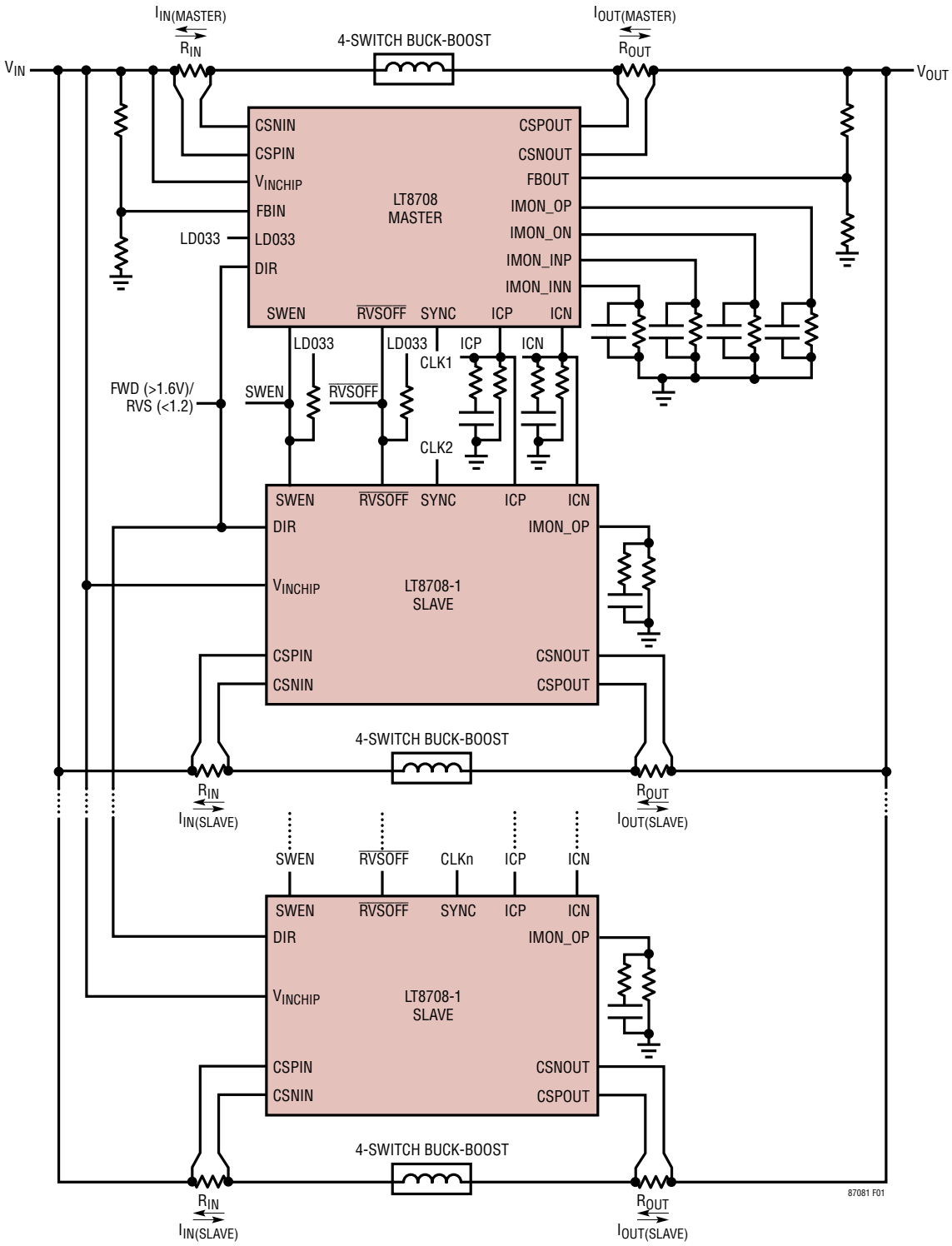


Figure 2. Simplified Multiphase Configuration Diagram

OPERATION

As another example, the master LT8708's current regulation pins (IMON_INP, IMON_INN, IMON_OP, IMON_ON) monitor and limit the per-phase V_{IN} current and V_{OUT} current. The LT8708-1 complies with these limits by regulating the $I_{OUT(SLAVE)}$ proportionally. The slave's IMON pins are typically used differently than on the LT8708. See the $I_{OUT(SLAVE)}$: Configuration section and the Current Monitoring and Limiting section for more information.

Finally, the VINHIMON and VOUTLOMON pins can be used to set up V_{IN} overvoltage and V_{OUT} undervoltage lockouts on both the LT8708 and the LT8708-1. Typically, however, divider networks are only necessary on the master LT8708 since activation of the VINHIMON or VOUTLOMON comparator, on any phase, is communicated to all phases through the shared $\overline{RVSOFF}$ pin connection. Utilizing the VINHIMON and VOUTLOMON pins on additional phases offers redundancy for those functions. See the VINHIMON, VOUTLOMON and $\overline{RVSOFF}$ section for more details.

Adding Phases: The Slave LT8708-1

Further information about the LT8708-1 in Figure 2 is as follows:

- The ICP and ICN signals connect between the LT8708 and all the LT8708-1s. They are used to deliver the positive and negative $I_{OUT(MASTER)}$ information from the LT8708 to the LT8708-1(s), and hence set the average regulated $I_{OUT(SLAVE)}$.
- Typically, the LT8708-1 operates by regulating its $I_{OUT(SLAVE)}$ to a proportion of the $I_{OUT(MASTER)}$. The LT8708-1's IMON_OP pin regulates to 1.209V as a part of this regulation. This IMON_OP function differs from the LT8708 in that the LT8708-1's IMON_OP is not part of the positive $I_{OUT(SLAVE)}$ monitor function. Always connect a 17.4k resistor in parallel with a compensation network from this pin to ground on the LT8708-1.
- The IMON_ON pin is used to monitor the negative $I_{OUT(SLAVE)}$. The current limiting function of this pin on LT8708-1 is disabled and is instead controlled by the master LT8708.
- The LT8708 and LT8708-1 employ different soft-start mechanisms, and the SS pins ramp up differently. See the Start-Up: Soft-Start of Switching Regulator section for more details.

Apart from the information explained above from Figure 2, a few other pins also need to be considered when configuring a multiphase system. A summary of pins and their recommended usage is provided in Table 2.

Table 2. Summary of Pin Connections

SHORT PINS BETWEEN LT8708 AND LT8708-1	PIN NAME(S)	NOTES
YES	SWEN, $\overline{RVSOFF}$	Open-drain communication between all phases. Keeps LT8708/ LT8708-1(s) in same states.
	ICP, ICN	Send LT8708's $I_{OUT(SLAVE)}$ information to LT8708-1.
MAYBE	MODE, DIR	Typically, pins are driven to the same states as LT8708.
NO	FBOUT, IMON_INN	Disable these error amps on LT8708-1(s), or set to same or higher limits than LT8708 if used for secondary limits.
	IMON_INP	If using RHCM, connect a 17.4k resistor and parallel filter capacitor from this pin to ground. Otherwise, disable this error amp or set to same or higher limit than LT8708 if used for secondary $I_{IN(SLAVE)}$ limit.
	VINHIMON, VOUTLOMON	Comparator states are shared between LT8708/ LT8708-1(s) through $\overline{RVSOFF}$ pins. Pins on LT8708-1 can be disabled or used as redundant detectors.
	IMON_OP	On LT8708-1, connect a 17.4k resistor and a compensation network from this pin to ground.
	IMON_ON	Limiting function is disabled on LT8708-1. If using FHCM, connect a 17.4k resistor in parallel with a filter capacitor from this pin to ground to properly detect light load.
	SS, RT	Use same value capacitor, resistor as LT8708.
	LDO33, $INTV_{CC}$, $GATEV_{CC}$	Typically would have same capacitors as LT8708.

OPERATION

In addition, all LT8708-1s' V_{IN} and V_{OUT} should be connected to the LT8708's V_{IN} and V_{OUT}, respectively.

See the Quick-Start Multiphase Setup Guidelines section in the Applications Information for a step-by-step design procedure to add LT8708-1s to your system.

START-UP

Figure 3 illustrates the start-up sequence for the LT8708-1.

Start-Up: SWEN Pin

The LT8708-1 and LT8708's SWEN pins share the same functionality. Refer to Start-Up: SWEN Pin of the LT8708 data sheet for more details. SWEN is internally pulled down by the LT8708 and/or LT8708-1(s) when the respective switching regulator is unable or not ready to operate (see CHIP OFF and SWITCHER OFF 1 states in Figure 3).

In a multiphase system, the SWEN pins are connected between all phases. Due to the internal SWEN pull-down on the LT8708 and LT8708-1, the external pull-up for the common SWEN node should always have a current limiting resistor. Typically, the common SWEN node is pulled up, through a resistor, to the LT8708's LDO33 pin. In other cases, the common SWEN node can be digitally driven through a current limiting resistor.

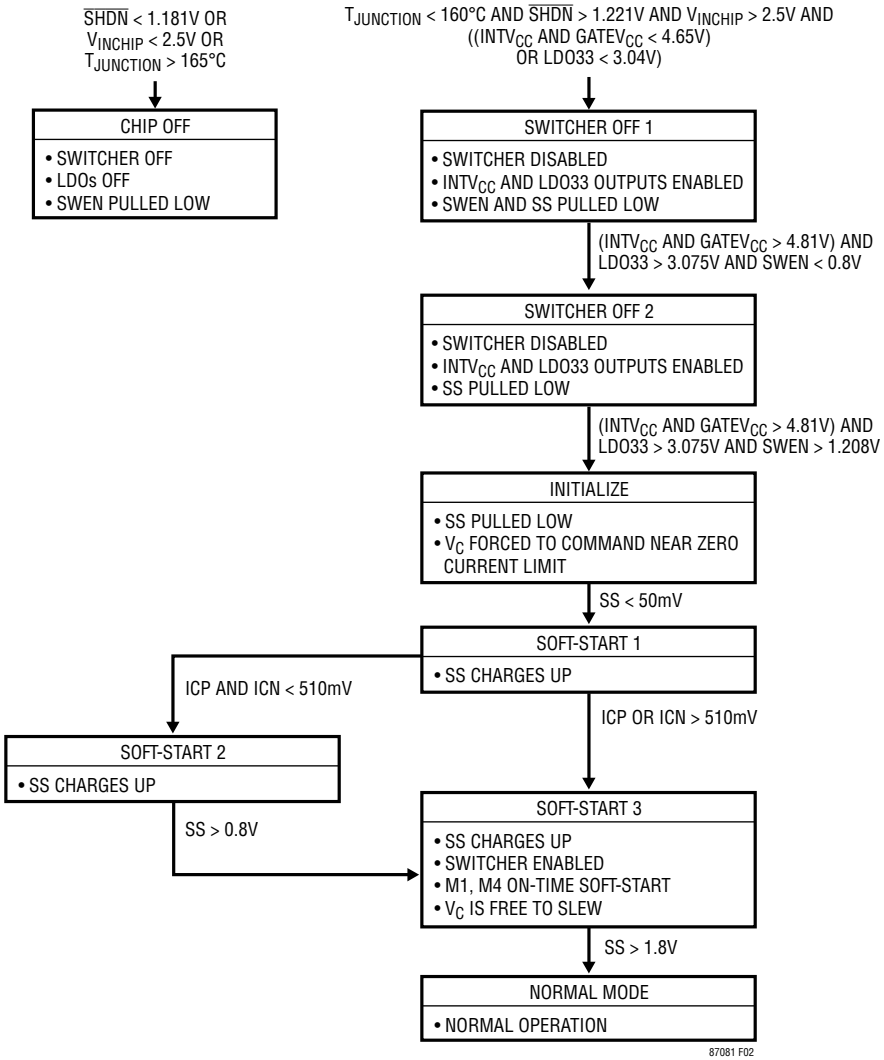


Figure 3. Start-Up Sequence (All Values are Typical)

OPERATION

SWEN is used to synchronize the start-up between all phases of the system. If one or more of the phases is unable to operate, SWEN is pulled low by those chips, thus preventing the entire system from starting. After all phases are ready to operate and SWEN has been pulled down below 0.8V (typical) SWEN rises, due to the pull-up resistor, and start-up proceeds, for all phases, to the SWITCHER OFF 2 state.

When the common SWEN node rises above 1.208V (typical), all the phases proceed to the INITIALIZE state at the same time.

Start-Up: Soft-Start of Switching Regulator

The soft-start sequence, described in this section, happens independently and in parallel for each phase since each phase has its own SS pin, external capacitor and related circuitry. The remaining discussion concerns the LT8708-1 soft-start behavior. The LT8708 soft-start differs slightly.

In the INITIALIZE state, the SS pin is pulled low to prepare for soft-starting the switching regulator. Also, V_C is forced to command near zero current, and IMON_OP is forced to ~1.209V (typical) to improve the transient behavior when the LT8708-1 subsequently starts switching.

After SS has been discharged to less than 50mV, the SOFT-START 1 state begins. In this state, an integrated 180k (typical) resistor from 3.3V pulls SS up. The rising ramp rate of the SS pin voltage is set by this 180k resistor and the external capacitor connected to this pin.

After SS reaches 0.2V (typical), the LT8708-1's integrated pull-up resistor is reduced from 180k to 90k to increase the rising ramp rate of the SS pin voltage. This ensures that the slave chip enters the normal mode in Figure 3 before the master chip, preventing saturation of the regulation loop during start-up.

Switching remains disabled until either (1) ICP or ICN voltage becomes higher than 510mV (typical) (SOFT-START 3) or (2) SS reaches 0.8V (typical) (SOFT-START 2). As soon as switching is enabled, V_C is free to slew under the control of the internal error amplifiers (EA1–EA6). This allows the average $I_{OUT(SLAVE)}$ to quickly follow the average $I_{OUT(MASTER)}$ without saturating the slave's regulation loop. During soft-start the LT8708-1 employs the same switch control mechanism as the LT8708. See the Switch Control: Soft-Start section of the LT8708 data sheet for more information.

When SS reaches 1.8V (typical), the LT8708-1 exits soft-start and enters normal mode. Typical values for the external soft-start capacitor range from 220nF to 2µF. It is recommended to use the same brand and value SS capacitor for all the synchronized LT8708/ LT8708-1(s). Using a slave SS capacitor value significantly higher than the master SS capacitor value can result in undesirable start-up behavior.

CONTROL OVERVIEW

The LT8708-1 is a slave current mode controller that regulates the average $I_{OUT(SLAVE)}$ based on the master's ICP and ICN voltages, or equivalently, the average $I_{OUT(MASTER)}$. The main regulation loop involves EA6 (see Figure 1). In a simple example of $I_{OUT(SLAVE)}$ regulation, the CSPOUT–CSNOUT pins receive the $I_{OUT(SLAVE)}$ feedback signal which is summed with the ICP and ICN signals from the LT8708 to generate the IMON_OP voltage using A1 (see Figure 1). The IMON_OP voltage is compared to the internal reference voltage using EA6. Low IMON_OP voltages raise V_C, which causes $I_{OUT(SLAVE)}$ to become more positive (or less negative) and increases the current out of the IMON_OP pin. Conversely, higher IMON_OP voltages reduce V_C, which causes $I_{OUT(SLAVE)}$ to become less positive (or more negative) and reduces the current flowing out of the IMON_OP pin.

The V_C voltage typically has a Min to Max range of about 1.2V. The maximum V_C voltage commands the most positive inductor current, and thus, commands the most power flow from V_{IN} to V_{OUT}. The minimum V_C voltage commands the most negative inductor current, and thus, commands the most power flow from V_{OUT} to V_{IN}.

V_C is the combined output of five internal error amplifiers EA1–EA6 as shown in Table 3. In a common application, $I_{OUT(SLAVE)}$ would be regulated using the main regulation error amplifier EA6, while error amplifiers EA1 and EA5 are monitoring for excessive input current and EA3 and EA4 are disabled.

OPERATION

Table 3. Error Amplifiers (EA1–EA6)

AMPLIFIER NAME	PIN NAME	USED TO LIMIT OR REGULATE
EA1	IMON_INN	Negative $I_{IN(SLAVE)}$
EA3	FBIN	V_{IN} Voltage
EA4	FBOUT	V_{OUT} Voltage
EA5	IMON_INP	Positive $I_{IN(SLAVE)}$
EA6	IMON_OP	$I_{OUT(SLAVE)}$

Note that the current and power flow can also be restricted to one direction, as needed, by the selected conduction mode discussed in the Unidirectional and Bidirectional Conduction section.

POWER SWITCH CONTROL

The LT8708-1 employs the same power switch control as the LT8708 (see Power Switch Control section of the LT8708 data sheet). Figure 4 shows a simplified diagram of how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and ground.

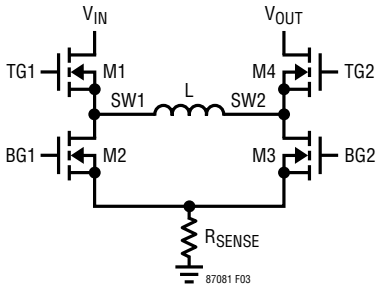


Figure 4. Simplified Diagram of the Buck-Boost Switches

UNIDIRECTIONAL AND BIDIRECTIONAL CONDUCTION

As with the LT8708, the LT8708-1 has one bidirectional and three unidirectional current conduction modes (CCM, HCM, DCM and Burst Mode operation, respectively). The LT8708-1's MODE, DIR and $\overline{\text{RVSOFF}}$ pins operate in the same way as in the LT8708 to select the desired conduction modes. (See the Unidirectional and Bidirectional Conduction section of the LT8708 data sheet for details). In general, it is highly recommended to keep all phases of an LT8708 system in the same conduction mode. This is done by setting all MODE and DIR pins to the same states, or shorting all MODE pins together and all DIR pins together. In addition, the $\overline{\text{RVSOFF}}$ pins of all phases should be connected together.

Note that when operating in the forward hybrid conduction mode (FHCM), the LT8708-1 operation differs slightly from the LT8708. Instead of measuring the ICN pin voltage for light load detection, the LT8708-1 measures the IMON_ON pin. Light load is detected when IMON_ON is above 245mV (typical). Therefore, FHCM operation requires a 17.4k resistor, and a parallel filter capacitor, from ground to the IMON_ON pin of the LT8708-1. Reverse hybrid conduction mode (RHCM) operates identically in the LT8708 and LT8708-1. See the Unidirectional and Bidirectional Conduction: HCM section of the LT8708 data sheet for details.

ERROR AMPLIFIERS

Five internal error amplifiers combine to drive V_C according to Table 4, with the highest priority being at the top.

Table 4. Error Amp Priorities

TYPICAL CONDITION		PURPOSE	
if	IMON_INN > 1.21V	then V_C Rises	to Reduce Negative $I_{IN(SLAVE)}$
else if	FBIN < 1.205V or	then V_C Falls	to Reduce Positive $I_{IN(SLAVE)}$ or Increase Negative $I_{IN(SLAVE)}$
	FBOUT > 1.207V or		to Reduce Positive $I_{OUT(SLAVE)}$ or Increase Negative $I_{IN(SLAVE)}$
	IMON_INP > 1.209V or		to Reduce Positive $I_{IN(SLAVE)}$
	IMON_OP > 1.209V		to Reduce Positive $I_{OUT(SLAVE)}$
else		V_C Rises	Default

Note that certain error amplifiers are disabled under the conditions shown in Table 5. A disabled error amplifier is unable to affect V_C and can be treated as if its associated row is removed from Table 4.

Table 5. Automatically Disabled Error Amp Conditions

ERROR AMP	PIN NAME	VOUTLOMON ASSERTED	VINHIMON ASSERTED	RDCM or RHCM
EA1	IMON_INN			
EA3	FBIN		2*	
EA4	FBOUT	1*		3*
EA5	IMON_INP			
EA6	IMON_OP			

OPERATION

A 1* to 3* indicates that the error amplifier listed for that row is disabled under that column's condition. The purposes of disabling the respective amplifiers are:

1* This improves transient response when VOUTLOMON de-asserts.

2* This improves transient response when VINHIMON de-asserts.

3* Since power can only transfer from V_{OUT} to V_{IN}, this prevents higher FBOUT/V_{OUT} voltages from interfering with the FBIN/V_{IN} voltage regulation.

The primary regulation loop for the LT8708-1 involves EA6, which regulates the average $I_{OUT(SLAVE)}$ based on the ICP and ICN input voltages. Therefore, the IMON_OP pin must always have a proper compensation network connected. See the Loop Compensation section for more information.

The remaining error amplifiers can be disabled or used to limit their respective voltages or currents. When unused, the respective input pin(s) should be driven so that they do not interfere with the operation of the remaining amplifiers. Use Table 6 as a guide.

Table 6. Disabling Unused Amplifiers

AMPLIFIER NAME	PIN NAME	TIE TO DISABLE	EXAMPLE DISABLED PIN CONNECTION
EA1	IMON_INN	< 0.9V	GND
EA3	FBIN	> 1.5V	LDO33
EA4	FBOUT	< 0.9V	GND
EA5	IMON_INP		

TRANSFER FUNCTION: $I_{OUT(SLAVE)}$ VS $I_{OUT(MASTER)}$

The LT8708-1 regulates $I_{OUT(SLAVE)}$ proportionally to $I_{OUT(MASTER)}$ following the transfer functions[1] shown in Figure 5 and Figure 6. The currents are measured (sensed) by the differential CSPOUT–CSNOUT pin voltages for each phase and the information is sent from the master to the slaves via the ICP and ICN pins. The transfer functions are represented by the slave's current sense voltage ($V_{(CSPOUT–CSNOUT)S}$) vs the master's current sense voltage ($V_{(CSPOUT–CSNOUT)M}$). To convert the axes of Figure 5 and Figure 6 to $I_{OUT(SLAVE)}$ vs $I_{OUT(MASTER)}$, simply divide

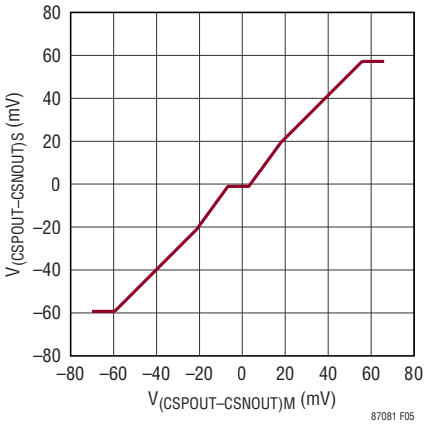


Figure 5. Typical $V_{(CSPOUT–CSNOUT)S}$ vs $V_{(CSPOUT–CSNOUT)M}$ in CCM[1]

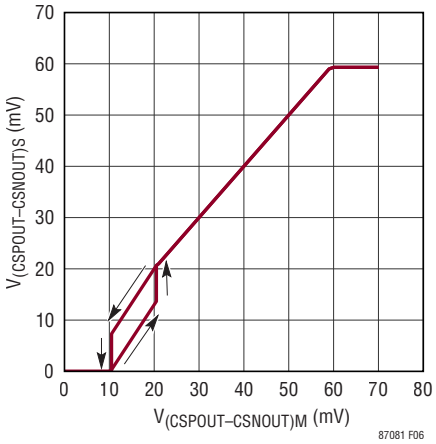


Figure 6. Typical $V_{(CSPOUT–CSNOUT)S}$ vs $V_{(CSPOUT–CSNOUT)M}$ in FDCM, FHCM and Burst Mode Operation[1]

$V_{(CSPOUT–CSNOUT)S}$ and $V_{(CSPOUT–CSNOUT)M}$ by the slave's and master's R_{SENSE2} values, respectively.

Figure 5 shows that increasing the master's average current sense voltage $V_{(CSPOUT–CSNOUT)M}$ above ±60mV results in no additional current from the slave LT8708-1. As such, the average of $V_{(CSPOUT–CSNOUT)M}$ should be limited to ±50mV by connecting appropriate resistors from the IMON_OP and IMON_ON pins of the LT8708 to ground (see the I_{IN} and I_{OUT} Current Monitoring and Limiting section of the LT8708 data sheet).

1. The ICP and ICN pins must be connected between the master and slave chips. 17.4k resistors and appropriate parallel capacitors are also required from those pins to ground.

OPERATION

Transfer Function: CCM

Figure 5 shows the transfer function of the slave's regulated current sense voltage ($V_{(CSPOUT–CSNOUT)S}$) vs the master's current sense voltage ($V_{(CSPOUT–CSNOUT)M}$) when the MODE pin is selecting CCM operation.

At light current levels ($|V_{(CSPOUT–CSNOUT)M}|$<20mV), $I_{OUT(SLAVE)}$ is regulated slightly lower than $I_{OUT(MASTER)}$. This ensures that the LT8708-1 delivers zero current when the master is delivering zero current and also ensures a smooth transition from positive to negative I_{OUT}.

At high current levels ($|V_{(CSPOUT–CSNOUT)M}|$ > 20mV), $I_{OUT(SLAVE)}$ is regulated to be the same as $I_{OUT(MASTER)}$, offering good current sharing and thermal balance between the phases.

Note: If the LT8708-1 is configured to be in CCM while $\overline{RVSOFF}$ is being pulled low, use the FDCM transfer function in the next section.

Transfer Function: DCM, HCM and Burst Mode Operation

Figure 6 shows the transfer function of the slave's regulated current sense voltage ($V_{(CSPOUT–CSNOUT)S}$) vs the master's current sense voltage ($V_{(CSPOUT–CSNOUT)M}$) when the MODE pin is selecting FDCM, FHCM or Burst Mode operation.

The transfer function, in the non-CCM modes, is shown in Figure 6 and has three distinct regions:

1. $V_{(CSPOUT–CSNOUT)M}$ < 10mV: In this region, where the master's current is relatively small, the slave phases deliver zero current.
2. 10mV < $V_{(CSPOUT–CSNOUT)M}$ < 20.5mV: In this region, where the master's current is moderate, the slave phases deliver less current than the master. The transfer function is hysteretic in this region. Therefore, the slave current will operate from 0mV to 13.5mV or from 6.7mV to 20.5mV if the master's $V_{(CSPOUT–CSNOUT)M}$ was most recently below 10mV or above 20.5mV, respectively.
3. $V_{(CSPOUT–CSNOUT)M}$ > 20.5mV: In this region of moderate to high current from the master, the slave delivers the same current as the master.

The transfer function is a mirror image of Figure 6 when operating in the RDCM and RHCM conduction modes for $V_{(CSPOUT–CSNOUT)M}$ < 0mV. Simply multiply the values on the X and Y axes of Figure 6 by –1 to illustrate the transfer function.

CURRENT MONITORING AND LIMITING

Monitoring: $I_{OUT(SLAVE)}$

The LT8708-1 can monitor V_{OUT} current ($I_{OUT(SLAVE)}$) in the negative direction. An external resistor is connected from the IMON_ON pin to ground, and the resulting voltage is linearly proportional to negative $I_{OUT(SLAVE)}$. Unlike the LT8708's IMON_ON pin, the LT8708-1's IMON_ON pin does not regulate or limit $I_{OUT(SLAVE)}$ in the negative direction. See the I_{IN} and I_{OUT} Current Monitoring and Limiting section of the LT8708 data sheet for how to configure the IMON_ON current monitoring.

Monitoring and Limiting: $I_{IN(SLAVE)}$

The LT8708-1 can monitor V_{IN} current ($I_{IN(SLAVE)}$) in both the positive and negative directions by measuring the voltage across a current sense resistor R_{SENSE1} using the CSPIN and CSNIN pins. The voltage is amplified and a proportional current is forced out of the IMON_INP and IMON_INN pins to allow for monitoring and limiting. This function is identical to the LT8708 and more information can be found in the Current Monitoring and Limiting section of the LT8708 data sheet.

As described above, the LT8708-1 has circuitry allowing for independent input current limiting of each phase. This per-phase current limiting is intended to be secondary to the limits imposed by the master. Typically, the master is configured to limit its own input current ($I_{IN(MASTER)}$) thus limiting the command current to the slave. However, since the slave has its own independent input current sensing

OPERATION

and limiting circuitry, it can be configured with redundant current limiting. It is recommended to set the slave input current limit magnitudes to be the same or higher than those set by the master. See the Applications Information section for more information about the $I_{IN(SLAVE)}$ current monitoring and limiting.

As with the LT8708, the LT8708-1 requires a 17.4k resistor and parallel filter capacitor to be connected from ground to the IMON_INP pin when using the RHCM conduction mode. If, in this case, it is also desired to set the LT8708-1's positive $I_{IN(SLAVE)}$ current limit higher than the LT8708's positive $I_{IN(MASTER)}$ limit, reduce the value of the LT8708-1's R_{SENSE1} resistor as compared to the LT8708's R_{SENSE1} value. See Configuring the $I_{IN(SLAVE)}$ Current Limits section for details.

MULTIPHASE CLOCKING

A multiphase application usually has switching regulators operating at the same frequency but at different phases to reduce voltage and current ripple. The SYNC pin can be used to synchronize the LT8708-1's switching frequency at a specific phase relative to the master LT8708 chip. A separate clock chip, e.g., LTC6902, LTC6909 etc., can be used to generate the clock signals and drive the SYNC pins of the LT8708 and LT8708-1(s). If only two phases are needed for the multiphase application, i.e., 0° and 180°, the LT8708-1's SYNC pin can be connected to the LT8708's CLKOUT pin to obtain the 180° phase shift. The master LT8708 can be synchronized to an external source or can be free-running based on the external R_T resistor. It is recommended that the LT8708-1 is always synchronized to the same frequency as the LT8708 through the SYNC pin.

APPLICATIONS INFORMATION

This Applications Information section provides additional details for setting up a multiphase application using the LT8708-1(s) and LT8708. Topics include quick multiphase setup guidelines, choosing the total number of phases, clock synchronization, and selection of various external components. In addition, more information is provided about voltage lockouts, current monitoring, PCB layout considerations. This section wraps up with a design example.

QUICK-START MULTIPHASE SETUP

This section provides a step-by-step summary on how to setup a multiphase system using the LT8708-1(s) and LT8708.

Quick Setup: Design the Master Phase

Design the LT8708 application circuit according to the LT8708 data sheet. Make sure the maximum CSPOUT–CSNOUT current sense voltage is limited to ±50mV by setting the IMON_OP and IMON_ON resistor values equal to or higher than 17.4k. This is the master phase.

Quick Setup: Design the Slave Phase(s)

Step 1 – Power Stage: Apply the same power stage design from the LT8708 application circuit to the LT8708-1 circuit. This includes the inductor, power MOSFETs and their gate resistors, R_{SENSE}, R_{SENSE} filtering, R_{SENSE1}, R_{SENSE2}, CSPIN–CSNIN filtering, CSPOUT–CSNOUT filtering, topside MOSFET driver supply (C_{B1}, D_{B1}, C_{B2}, D_{B2}) and Schottky diodes D1, D2, D3, D4 (if used). See the C_{IN} and C_{OUT} Selection section on how to optimize the capacitor values.

Step 2 – Peripheral Pins: The following components should be identical on the LT8708 as the LT8708-1:

- R_T resistor
- SS pin capacitor
- $INTV_{CC}$, $GATEV_{CC}$, V_{INCHIP} and LDO33 pin bypass capacitors

Connect identical resistor divider networks on $\overline{SHDN}$ as well as on VINHIMON and VOUTLOMON (if used). If not used, connect VINHIMON to GND and/or VOUTLOMON to the LT8708-1's LDO33. Connect the LT8708-1's FBOUT pin to GND and the FBIN pin to the LT8708-1's LDO33 node.

Step 3 – Interconnect: Connect the LT8708-1's ICP, ICN, $EXTV_{CC}$, SWEN and $\overline{RVSOFF}$ pins to their counterparts on the LT8708. Connect the same control signals, or connect the same value resistor dividers or voltages to the MODE pins and the DIR pins of the LT8708 and LT8708-1, respectively. Connect the LT8708's CLKOUT signal or a clock chip's phase shifted clock to the LT8708-1's SYNC pin.

Step 4 – Regulation and Limiting: Connect a 17.4k resistor in parallel with a compensation network from IMON_OP to GND. Connect a resistor in parallel with a filter capacitor from IMON_ON to GND for current monitoring. Connect resistors in parallel with filter capacitors from IMON_INP and IMON_INN to GND, respectively, to set the magnitudes of the $I_{IN(SLAVE)}$ current limits to be equal to or higher than their counterparts on the LT8708.

Step 5: Repeat steps 1 through 4 to add any additional LT8708-1 phases.

Quick Setup: Evaluation

Test and optimize the stability of the multiphase system. See the Loop Compensation section for more details.

CHOOSING THE TOTAL NUMBER OF PHASES

In general, the number of phases needed is selected to meet a multiphase system's total power requirement as well as each phase's thermal requirement. In general, for a given application, the more phases that the system has, the less power that each phase needs to deliver, and the better the thermal performance that each phase has. In many cases, the total number of phases is selected to optimize the total input or output RMS current ripple. See the C_{IN} and C_{OUT} Selection section for more details.

APPLICATIONS INFORMATION

OPERATING FREQUENCY SELECTION

The LT8708-1 uses a constant frequency architecture operating between 100kHz and 400kHz. The LT8708-1 should be synchronized to the same frequency as the LT8708 by connecting a clock signal to the SYNC pin. An appropriate resistor must be placed from the RT pin to ground. In general, use the same value R_T resistor for all the synchronized LT8708 and LT8708-1(s). See the Operating Frequency Selection section of the LT8708 data sheet on how to select the LT8708's switching frequency.

C_{IN} AND C_{OUT} SELECTION

V_{IN} and V_{OUT} capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching spikes. A ceramic capacitor, of at least 1µF at the maximum V_{INCHIP} operating voltage, should also be placed from V_{INCHIP} to GND as close to the LT8708-1 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

C_{IN} and C_{OUT} Selection: V_{IN} Capacitance

Discontinuous V_{IN} current is highest in the buck region due to the M1 switch toggling on and off. Ensure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. Figure 7 shows the total input capacitor RMS ripple current for one to six phases with the V_{OUT} to V_{IN} ratios in buck operation.

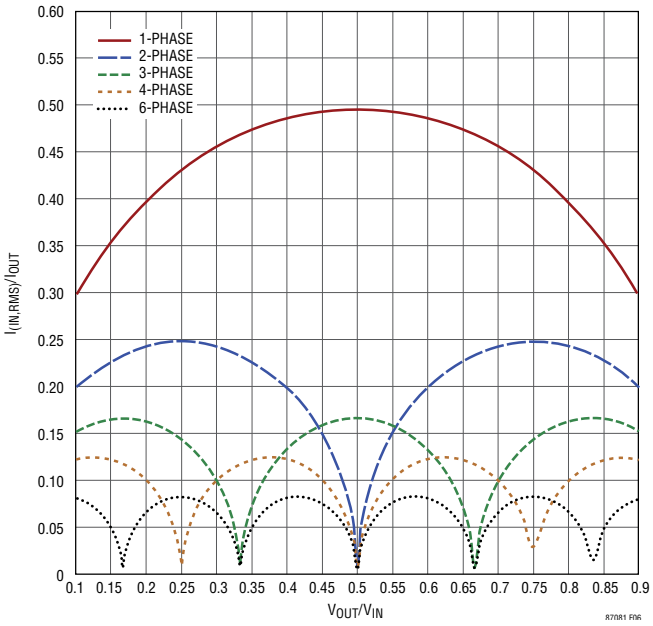


Figure 7. Normalized Total Input RMS Ripple Current vs V_{OUT}/V_{IN} for One to Six Phases in Buck Operation

The total input RMS ripple current $I_{(IN,RMS)}$ is normalized against the total output current of the multiphase system (I_{OUT}). The graph can be used in place of tedious calculations. From the graph, the minimum total input RMS ripple current can be achieved when the product of the number of phases (N) and the output voltage V_{OUT} is approximately equal to integer multiples of the input voltage V_{IN} or:

$$V_{OUT}/V_{IN} = n/N$$

where n = 1, 2,…, N-1

Therefore, the number of phases can be chosen to minimize the input capacitance for given input and output voltages.

Figure 7 also shows the maximum total normalized input RMS current for one to six phases. Choose an adequate C_{IN} capacitor network to handle this RMS current.

C_{IN} is also necessary to reduce the V_{IN} voltage ripple caused by discontinuities and ripple of I_{IN}. The effects of ESR and the bulk capacitance must be considered when choosing the correct capacitor for a given V_{IN} ripple. A low ESR input capacitor sized for the maximum RMS current must be used. Add enough ceramic capacitance to

TYPICAL APPLICATIONS

make sure V_{IN} voltage ripple is adequately low for the application.

C_{IN} and C_{OUT} Selection: V_{OUT} Capacitance

Discontinuous V_{OUT} current is highest in the boost region due to the M4 switch toggling on and off. Make sure that the C_{OUT} capacitor network has low enough ESR and is sized to handle the maximum RMS current. Figure 8 shows the output capacitor RMS ripple current for one to six phases with the (V_{OUT} – V_{IN}) to V_{OUT} ratios in boost operations. The total output RMS ripple current $I_{(OUT,RMS)}$ is normalized against the total output current of the multiphase system (I_{OUT}). The graph can be used in place of tedious calculations. From the graph, the minimum total output RMS ripple current can be achieved when the product of the number of phases (N) and duty cycle (V_{OUT} – V_{IN})/V_{OUT} is approximately equal to integers or:

$$(V_{OUT} - V_{IN})/V_{OUT} = n/N$$

where n = 1,2,…, N-1

Therefore, the number of phases be chosen to minimize the output capacitance for given input and output voltages.

Figure 8 also shows the maximum total normalized output RMS current for one to six phases. Choose an adequate C_{OUT} capacitor network to handle this RMS current.

C_{OUT} is also necessary to reduce the V_{OUT} ripple caused by discontinuities and ripple of I_{OUT}. The effects of ESR and the bulk capacitance must be considered when choosing the right capacitor for a given V_{OUT} ripple. A low ESR input capacitor sized for the maximum RMS current must be used. Add enough ceramic capacitance to make sure V_{OUT} voltage ripple is adequate for the application.

Figure 7 and Figure 8 show that the peak total RMS input current in buck operation and the peak total RMS output current in boost operation are reduced linearly, inversely proportional to the number of phases used. It is important to note that the ESR-related power loss is proportional to the RMS current squared, and therefore a 3-phase implementation results in 90% less power loss when compared to a single-phase design. Battery/input protection fuse resistance (if used) PCB trace and connector resistance losses are also reduced by the reduction of the ripple

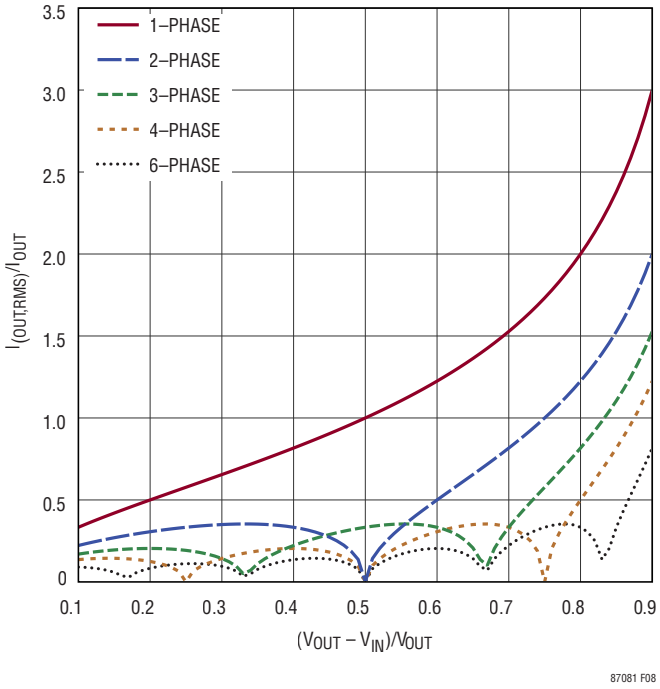


Figure 8. Normalized Output RMS Ripple Current vs (V_{OUT}–V_{IN})/V_{IN} for One to Six Phases in Boost Operation

current in a multiphase system. The required amount of input and output capacitance is further reduced by the factor, N, due to the effective increase in the frequency of the current pulses.

VINHIMON, VOUTLOMON AND $\overline{\text{RVSOFF}}$

VINHIMON and VOUTLOMON offer the identical functions on the LT8708 and LT8708-1(s). See the VINHIMON, VOUTLOMON and $\overline{\text{RVSOFF}}$ section of the LT8708 data sheet for more details. If the VINHIMON and VOUTLOMON functions are used on the LT8708-1(s) as redundant monitoring functions, in general use the same value resistor dividers as on the LT8708. If the VINHIMON and/or VOUTLOMON functions are not used on the LT8708-1(s), tie VINHIMON to GND and/or VOUTLOMON to the respective LT8708-1's LDO33 pin.

The $\overline{\text{RVSOFF}}$ pin has an internal comparator with a rising threshold of 1.374V (typical) and a falling threshold of 1.209V (typical). A low state on this pin inhibits reverse current and power flow. It is recommended to tie the $\overline{\text{RVSOFF}}$ pins of all the synchronized LT8708 and LT8708-1(s) together. In a multiphase system, if one or

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more chips' VINHIMON or VOUTLOMON comparator is triggered, the $\overline{\text{RVSOFF}}$ pin is pulled low to prevent the entire multiphase system from delivering reverse current and power. The multiphase system will exit the $\overline{\text{RVSOFF}}$ operation when all the VINHIMON and VOUTLOMON comparators are de-asserted.

CONFIGURING THE $I_{IN(SLAVE)}$ CURRENT LIMITS

As discussed in the Monitoring and Limiting: $I_{IN(SLAVE)}$ section, the LT8708-1 can monitor and limit the input current independently of the master. The current limiting discussed in this section is intended to be secondary, or redundant, since the master is primarily in control of the amount of current commanded from the slave.

As shown in Figure 9, the LT8708-1 measures $I_{IN(SLAVE)}$ with the CSPIN and CSNIN pins and can independently monitor and limit the current in both positive and negative directions. The operation of the input current monitor circuits is identical to the LT8708. More information about configuring these circuits can be found in the I_{IN} and I_{OUT} Current Monitoring and Limiting section of the LT8708 data sheet.

When setting the $I_{IN(SLAVE)}$ current limits, it is recommended to set them equal to or higher than the magnitudes of the $I_{IN(MASTER)}$ limits. Consider that if the slave reaches input current limiting before the master, the slave can no longer deliver additional current as requested by the master. With equal $I_{IN(SLAVE)}$ and $I_{IN(MASTER)}$ limits, slight output current mismatch, and hence slight thermal imbalance can still happen due to device tolerance. Bench evaluation should be carried out to ensure the selected $I_{IN(SLAVE)}$ limits meet the application's thermal and stability requirements.

REGULATING $I_{OUT(SLAVE)}$

$I_{OUT(SLAVE)}$: Circuit Description

This section describes the control circuitry in the LT8708-1 that regulates the output current $I_{OUT(SLAVE)}$. The master LT8708 sends the ICP and ICN control signals to the slave LT8708-1 to set $I_{OUT(SLAVE)}$. See the Transfer Function: $I_{OUT(SLAVE)}$ vs $I_{OUT(MASTER)}$ section for related information.

Figure 10 shows the primary LT8708-1 circuits involved in the regulation of $I_{OUT(SLAVE)}$. Additional circuitry is shown in Figure 1. $I_{OUT(SLAVE)}$ is regulated by a feedback loop with ICP and ICN setting the desired current. The feedback loop involves the following sections:

- The V_C pin controls the inductor current, thus indirectly controlling $I_{OUT(SLAVE)}$. Higher V_C voltage

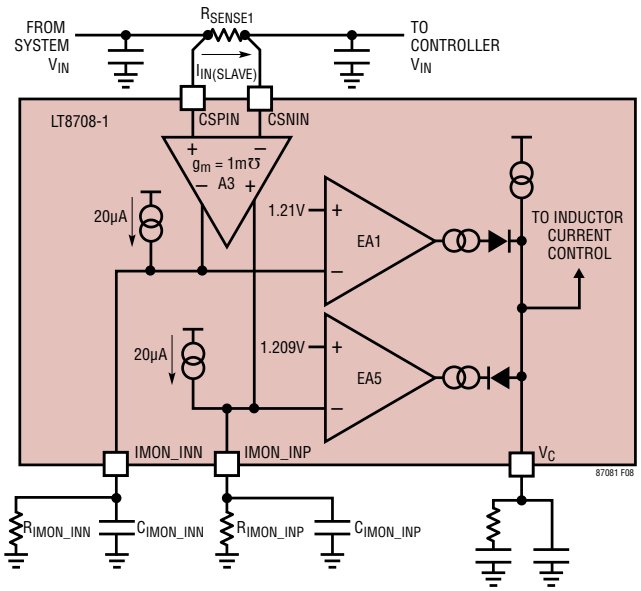


Figure 9. $I_{IN(SLAVE)}$ Current Monitor and Limit

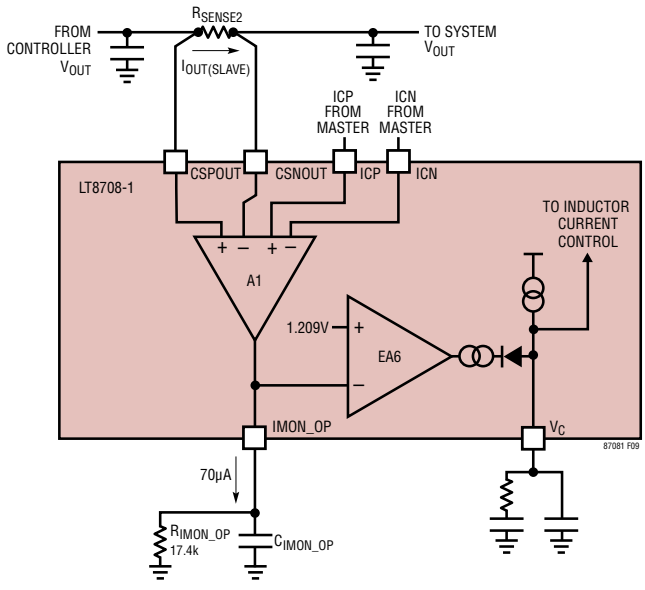


Figure 10. $I_{OUT(SLAVE)}$ Current Regulation and Monitor

TYPICAL APPLICATIONS

results in higher $I_{OUT(SLAVE)}$ current and vice versa. V_C is driven by error amplifier EA6 during $I_{OUT(SLAVE)}$ regulation.

- During regulation, the IMON_OP voltage is very close to the EA6 reference of 1.209V. Small changes in IMON_OP voltage make large adjustments to V_C, and thus the $I_{OUT(SLAVE)}$ current.
- Resistor R_{SENSE2} converts the $I_{OUT(SLAVE)}$ current into a voltage that can be measured by amplifier A1. This voltage is denoted as $V_{(CSPOUT–CSNOUT)S}$ in Figure 10.
- Transconductance amplifier A1 makes sure that $I_{OUT(SLAVE)}$ is equal to the current set by the ICP and ICN signals. If $I_{OUT(SLAVE)}$ becomes higher than requested by ICP and ICN, additional current is delivered out of A1. This raises IMON_OP which reduces V_C and reduces $I_{OUT(SLAVE)}$. Conversely, if $I_{OUT(SLAVE)}$ becomes lower than requested by ICP and ICN, the current out of A1 is reduced. This lowers IMON_OP which raises V_C and increases $I_{OUT(SLAVE)}$.

Figure 11 illustrates, in CCM mode, the typical relationship between the master's output current $I_{OUT(MASTER)}$, the resulting ICP and ICN control voltages, and the further resulting $I_{OUT(SLAVE)}$ current. Figure 11 can best be explained with a few examples.

In these examples, the output current sense resistors are R_{SENSE2} = 10mΩ for the master and the slave devices. First, assume the master's output current $I_{OUT(MASTER)}$ is 4A. This results in the master LT8708 measuring a current sense voltage of $V_{(CSPOUT–VCSNOUT)M}$ = 4A • 10mΩ = 40mV. Locate 40mV along the X-axis of Figure 11. The corresponding ICP and ICN voltages are ~1V and 0V, respectively. These ICP and ICN voltages are sent from the LT8708 to the LT8708-1. As a result, the LT8708-1 regulates $I_{OUT(SLAVE)}$ to:

$$I_{OUT(SLAVE)} = \frac{V_{(CSPOUT– CSNOUT)S}}{R_{SENSE2}} = \frac{40mV\ (from\ Figure\ 10)}{10m\Omega} = 4A$$

Alternatively, if the master's output current $I_{OUT(MASTER)}$ is –2A. Then the master LT8708 will measure a current sense voltage of $V_{(CSPOUT–VCSNOUT)M}$ = –2A • 10mΩ = –20mV. Locate –20mV along the X-axis of Figure 11. The corresponding ICP and ICN voltages are 0V and ~0.7V, respectively. These ICP and ICN voltages are sent from the LT8708 to the LT8708-1. As a result, the LT8708-1 regulates $I_{OUT(SLAVE)}$ to:

$$I_{OUT(SLAVE)} = \frac{V_{(CSPOUT– CSNOUT)S}}{R_{SENSE2}} = \frac{-20mV\ (from\ Figure\ 10)}{10m\Omega} = -2A$$

Figure 12 illustrates the relationship between $I_{OUT(MASTER)}$, ICP, ICN and $I_{OUT(SLAVE)}$ in FDCM, FHCM and Burst Mode operation. Use Figure 12, instead of Figure 11, to understand the control voltage relationships when operating in FDCM, FHCM or Burst Mode Operation. Figure 12 can

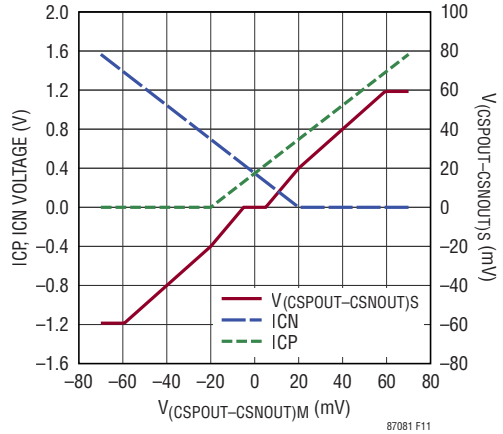


Figure 11. $I_{OUT(SLAVE)}$ Control Voltage Relationships (CCM)

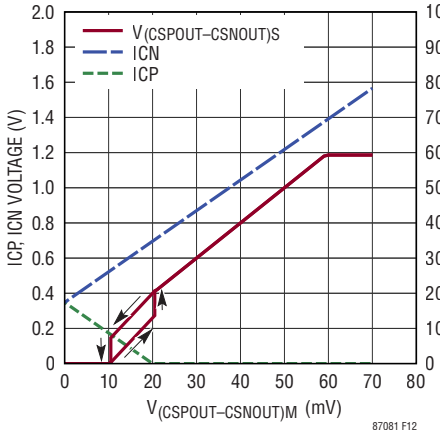


Figure 12. $I_{OUT(SLAVE)}$ Control Voltage Relationships (FDCM, FHCM and Burst Mode Operation)

APPLICATIONS INFORMATION

also be used to understand RDCM and RHCM operation by multiplying the $V_{(CSPOUT–CSNOUT)M}$ and the $V_{(CSPOUT–CSNOUT)S}$ axis values by –1.

As mentioned previously, 17.4k resistors must be connected from the ICP and ICN pins to ground. Proper resistor connections are required to produce the correct ICP and ICN voltages, and result in the correct $I_{OUT(SLAVE)}$ currents.

$I_{OUT(SLAVE)}$: Configuration

$I_{OUT(SLAVE)}$ regulation is the main regulation loop for the LT8708-1 and should always be enabled. Therefore, always connect a 17.4k resistor in parallel with a compensation network from the IMON_OP pin to ground. Note that the IMON_OP pin cannot be used for monitoring the $I_{OUT(SLAVE)}$ current.

Figure 5 and Figure 11 show that increasing the master's average current sense voltage $V_{(CSPOUT–CSNOUT)M}$ above ±60mV results in no additional current from the slave LT8708-1. As such, the target average of $V_{(CSPOUT–CSNOUT)M}$ should be limited to ±50mV by connecting appropriate resistors from the IMON_OP and IMON_ON pins of the LT8708 to ground (see the I_{IN} and I_{OUT} Current Monitoring and Limiting section of the LT8708 data sheet).

In addition, the instantaneous differential voltage $V_{(CSPOUT–CSNOUT)S}$ should remain between –100mV and 100mV due to the limited current that can be driven out of IMON_OP. If the instantaneous $V_{(CSPOUT–CSNOUT)S}$ exceeds these limits but the average $V_{(CSPOUT–CSNOUT)S}$ is between –50mV and 50mV, consider including the current sense filter described in the I_{IN} and I_{OUT} Current Monitoring and Limiting section of the LT8708 data sheet. The filter can reduce the instantaneous voltage while preserving the average. In general, use the same value current sense filter for all the synchronized LT8708 and LT8708-1(s).

Finally, IMON_OP should be compensated and filtered with capacitor C_{IMON_OP}. At least a few nF of capacitance is usually necessary.

LOOP COMPENSATION

To compensate a multiphase system of the LT8708 and LT8708-1(s), most of the initial compensation component selection can be done by analyzing the individual voltage regulator and/or current regulator(s) independently of each other. Use the total input and output bulk capacitance of the multiphase system in the stability analysis for each of the following steps.

1. Analyze the stability of the LT8708 as a single phase without any additional LT8708-1 phases included. This includes all the regulation loops that will be used by the master LT8708, such as voltage regulation (FBOUT, FBIN) and/or current regulation (IMON_INP, IMON_INN, IMON_OP, IMON_ON). Determine the initial values for the V_C pin compensation network, and the relevant IMON_XX pin capacitors for the master LT8708. Further adjustment of these values will be done in Step 4. Adjustment to C_{IN} and C_{OUT} may also be necessary as part of this analysis. See the Loop Compensation section of the LT8708 data sheet for more details. LTspice® transient simulation can be helpful for this step.
2. Analyze the stability of the $I_{OUT(SLAVE)}$ current regulation loop of a standalone LT8708-1 phase. Adjust the V_C and IMON_OP compensation networks of the LT8708-1 to achieve stability and maximum bandwidth. Bench stability evaluation of a standalone LT8708-1 can be carried out by driving the ICP and ICN pins with external voltage sources.

   A similar approach to that used for analyzing the LT8708 in constant-current regulation can be employed in compensating the standalone LT8708-1 current regulator. An IMON_OP capacitor of at least a few nF is necessary to maintain $I_{OUT(SLAVE)}$ regulation loop stability. In addition, adding a resistor of a few hundred Ohms in series with this capacitor can often provide additional phase margin.

   If any of the $I_{IN(SLAVE)}$ regulation loops, i.e. IMON_INP and IMON_INN, is used for secondary or redundant current limiting, carry out the corresponding stability analysis on the standalone LT8708-1. Use the same

TYPICAL APPLICATIONS

approach that is used for compensating the LT8708's input current regulation loops.

3. Complete the multiphase system with the LT8708 and LT8708-1(s). A few nF of capacitance should be placed on the ICP and ICN pins near the LT8708 for proper compensation. In addition, adding a few hundred Ohms in series with these capacitors can often provide extra phase margin to the multiphase system. See Figure 2 as an example.
4. Perform the loop stability analysis in simulation and/or on the bench. Primarily, adjust the LT8708's V_C compensation network for stability. A trim pot and selectable capacitor bank can be used on the V_C pin to determine the optimal values. Typically, the LT8708 should be adjusted to have lower bandwidth than the LT8708-1 phases. This can be achieved by increasing the capacitance and/or reducing the series resistance of the LT8708's V_C compensation network.

   If the LT8708 operates in constant current limit, as set by one or more of the IMON_xx pins, adjust the respective LT8708 IMON_xx filter capacitors as well to achieve optimal loop stability.

VOLTAGE LOCKOUTS

The LT8708-1 offers the same voltage detectors as the LT8708 to make sure the chip is under proper operating conditions. See the Voltage Lockouts section of the LT8708 data sheet for more details.

Although allowed with a standalone LT8708, a resistor divider connected to the SWEN pins should never be used for undervoltage detection in a multiphase system (see the Start-Up: SWEN Pin section for proper ways to connect or drive the SWEN pin in a multiphase system). Instead, an external comparator chip can be used to monitor undervoltage conditions, and its output drives the common SWEN node in a multiphase system through a current limiting resistor.

CIRCUIT BOARD LAYOUT CHECKLIST

The LT8708's circuit board layout guidelines also apply to the LT8708-1(s). Refer to the Circuit Board Layout Checklist section of the LT8708 data sheet for details.

In addition:

- Route the ICP and ICN traces together with minimum PCB trace spacing from the LT8708 to the LT8708-1(s). Avoid having these traces pass through noisy areas, such as switch nodes.
- Star connect the V_{IN} and V_{OUT} power buses as well as the power GND bus to each LT8708/ LT8708-1(s). Minimize the voltage difference between local V_{IN}, V_{OUT} and power GNDs, respectively.

DESIGN EXAMPLE

In this section, we start with the Design Example in the LT8708 data sheet, and expand it into a 2-phase regulator. The design requirements from the LT8708 data sheet are listed below with the total output current (I_{OUT}) and the total input current (I_{IN}) specifications doubled for two phases.

V_{IN} = 8V to 25V

V_{IN_FBIN} = 12V (V_{IN} regulation voltage set by LT8708 FBIN loop)

V_{OUT_FBOUT} = 12V (V_{OUT} regulation voltage set by LT8708 FBOUT loop)

$I_{OUT(MAX,\ FWD)}$ = 10A

$I_{IN(MAX,\ RVS)}$ = 6A

f =150kHz

This design operates in CCM.

Maximum ambient temperature = 60°C

Use the same R_T, R_{SENSE}, R_{SENSE2} resistors, inductor, external MOSFETs and capacitors from the Design Example of the LT8708 data sheet for LT8708-1.

SYNC Pin: Since this is a 2-phase system, the slave chip operates 180° out of phase from the master chip. Connect the LT8708's CLKOUT pin to the LT8708-1's SYNC pin.

APPLICATIONS INFORMATION

MODE Pin: Connect the MODE pin to GND for CCM operation.

SWEN and $\overline{\text{RVSOFF}}$ Pins: Connect the SWEN and $\overline{\text{RVSOFF}}$ pins together for the LT8708 and LT8708-1, respectively. This synchronizes the start-up and operation mode between the two chips.

ICP and ICN Pins: Connect two 17.4k resistors from the ICP and ICN pins to GND, respectively. Place them next to the LT8708 chip and route the ICP and ICN traces to the LT8708-1's counterparts, respectively.

R_{IMON_OP} Selection: Connect 17.4k from IMON_OP to GND for the LT8708-1.

R_{IMON_ON} Selection: LT8708-1's IMON_ON is only used to monitor the $I_{OUT(SLAVE)}$ in the reverse direction. A same value resistor of 24.9k from the LT8708 design example is selected here to provide an IMON_ON reading on the same scale as the one on the LT8708.

R_{SENSE1}, R_{IMON_INP}, R_{IMON_INN} selection: IMON_INP and IMON_INN are used to provide current limits for the LT8708-1 only. They are set to be equal to the maximum per phase V_{IN} current in the forward and reverse directions, respectively.

The maximum slave V_{IN} current in the forward direction is:

$$I_{IN(MAX,FWD,SLAVE)} = \frac{I_{(IMON\_OP,MASTER)} \bullet V_{OUT}}{V_{IN,MIN}}$$

$$= \frac{6A \bullet 12V}{8V} = 9A$$

And the maximum slave V_{IN} current in the reverse direction is:

$$I_{IN(MAX,RVS,SLAVE)} = I_{IN(IMON\_ON,MASTER)} = 3.6A$$

Choose R_{IMON_INP} to be around 17.4k, so that the LT8708 1's $V_{CSPIN–CSNIN}$ limit becomes 50mV, and the R_{SENSE1} is calculated to be:

$$R_{SENSE1} = \frac{50mV}{9A} \cong 6m\Omega$$

Using the equation given in the I_{IN} and I_{OUT} Current Monitoring and Limiting section of the LT8708 data sheet, R_{IMON_INP} is recalculated to be:

$$R_{IMON\_INP} = \frac{1.209}{I_{IN(MAX,\ FWD,SLAVE)} \bullet 1m\frac{A}{V} \bullet R_{SENSE2} + 20\mu A}\Omega \cong 16.2k\Omega$$

And R_{IMON_INN} is calculated to be:

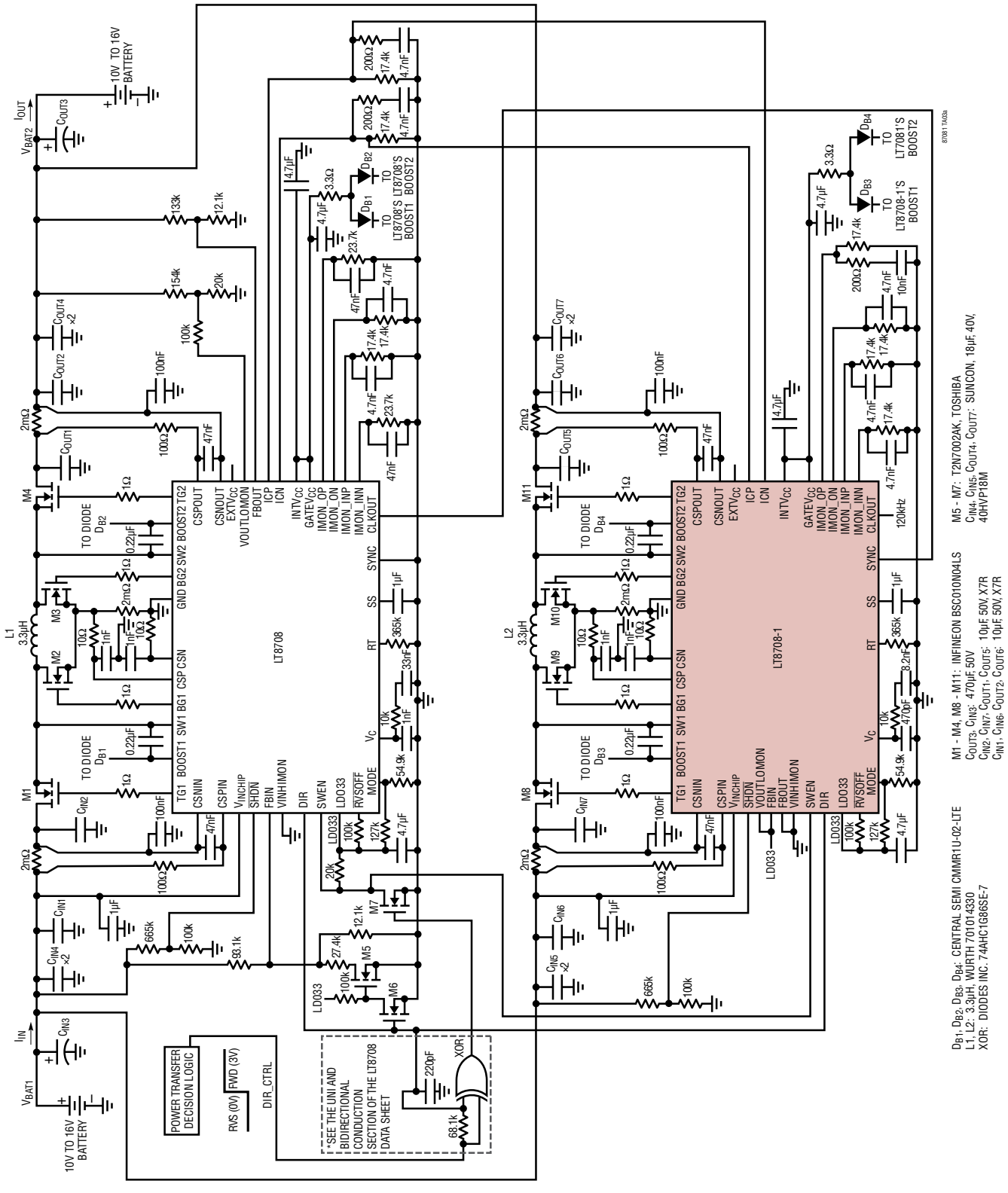
$$R_{IMON\_INN} = \frac{1.21}{I_{IN(MAX,\ RVS,SLAVE)} \bullet 1m\frac{A}{V} \bullet R_{SENSE2} + 20\mu A}\Omega \cong 29.4k\Omega$$

FBOUT Pin: Connect FBOUT pin to GND to disable the FBOUT pin.

FBIN Pin: Connect FBIN pin to LDO33 of the LT8708-1 to disable the FBIN pin.

TYPICAL APPLICATIONS

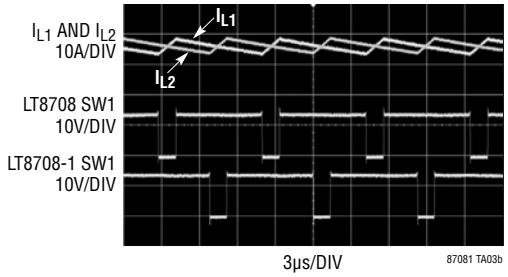
2-Phase 12V Bidirectional Dual Battery System with FHCM and RHCM



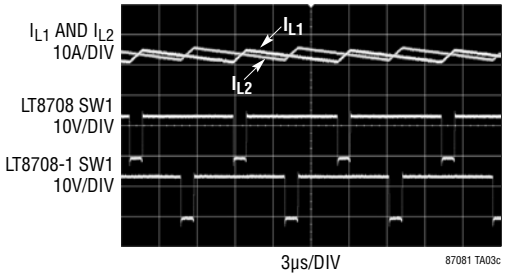
TYPICAL APPLICATIONS

2-Phase 12V Bidirectional Dual Battery System with FHCM and RHCM

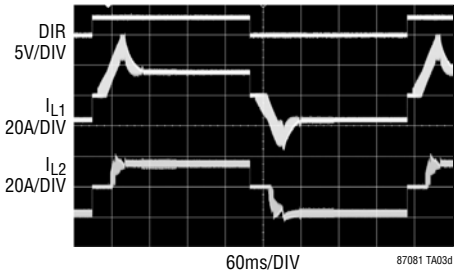
Forward Conduction V_{BAT1} = ~12V, V_{BAT2} = ~14V, I_{OUT} = ~30A



Reverse Conduction V_{BAT1} = ~12V, V_{BAT2} = ~14V, I_{IN} = ~30A

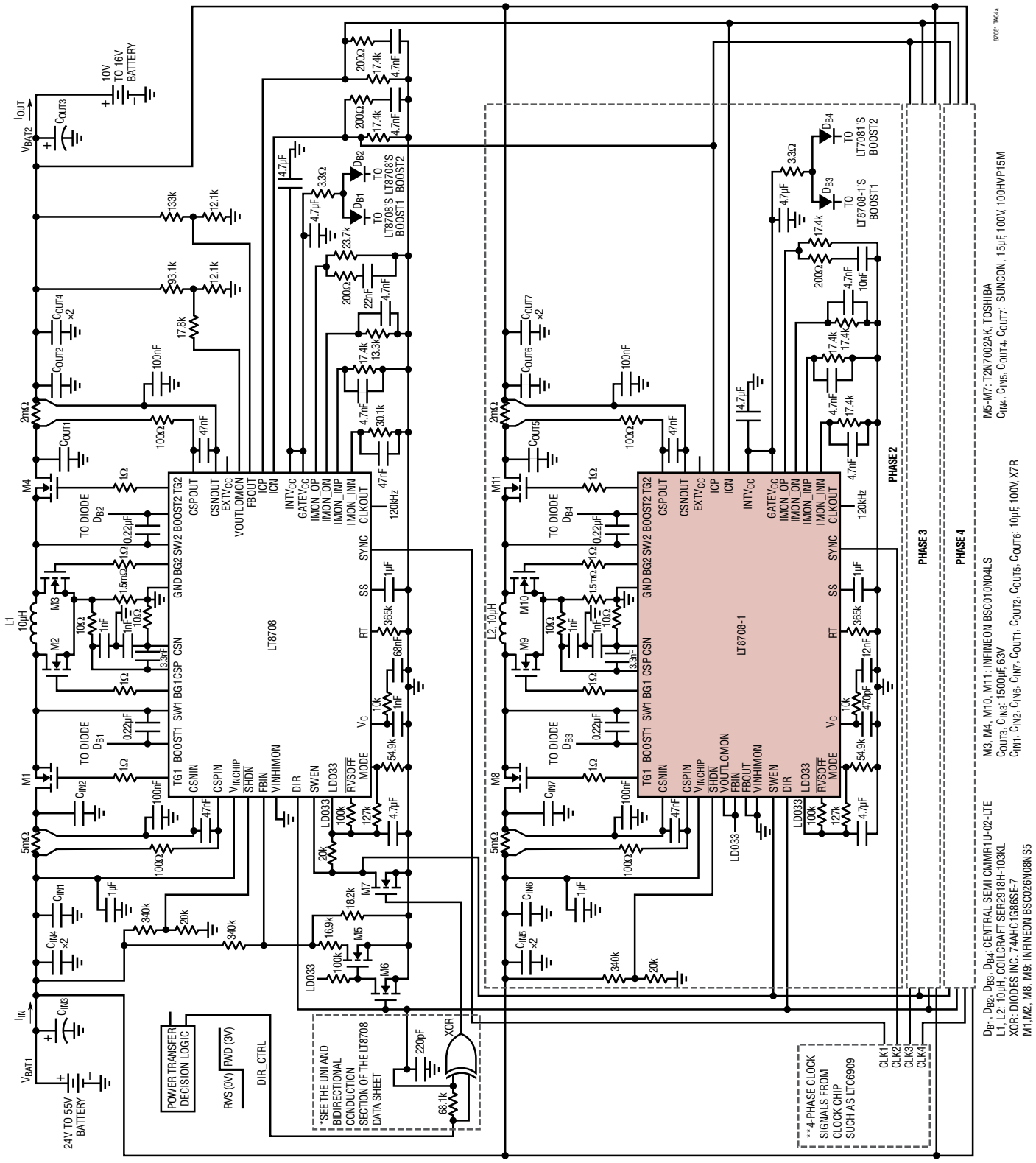


Direction Change with V_{BAT1} = ~12V, V_{BAT2} = ~12V



TYPICAL APPLICATIONS

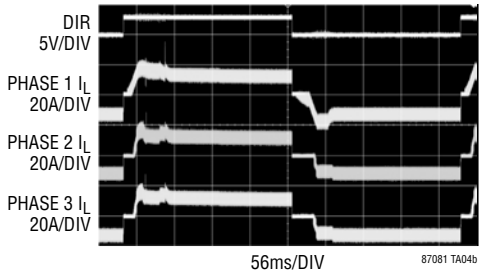
4-Phase 48V to 12V Bidirectional Dual Battery System with FHCM and RHCM



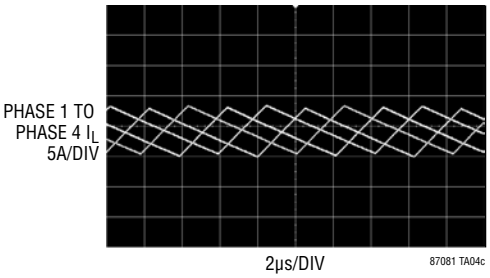
TYPICAL APPLICATIONS

4-Phase 48V to 12V Bidirectional Dual Battery System with FHCM and RHCM

Direction Change

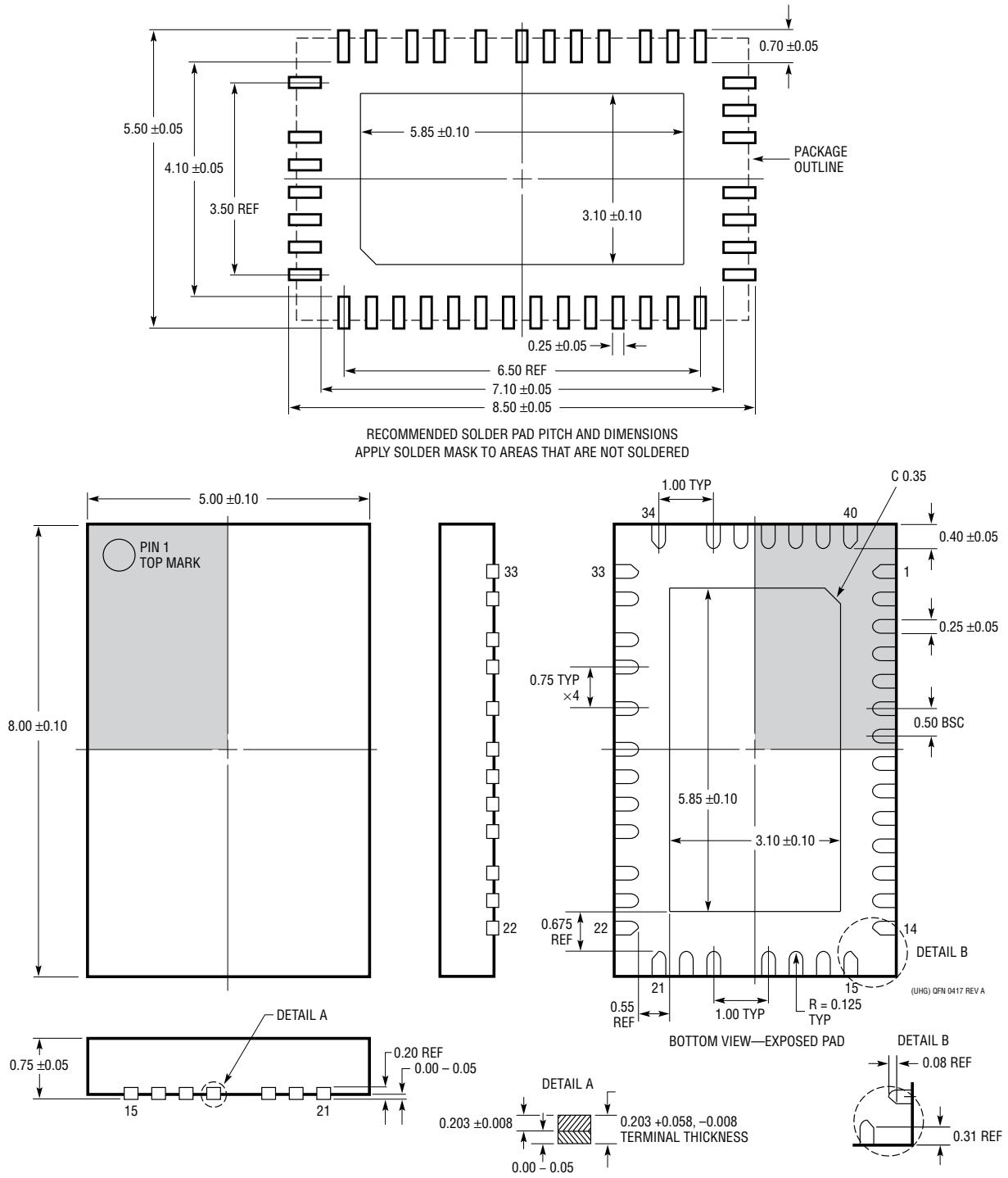


Phase 1 to 4 Inductor Current



PACKAGE DESCRIPTION

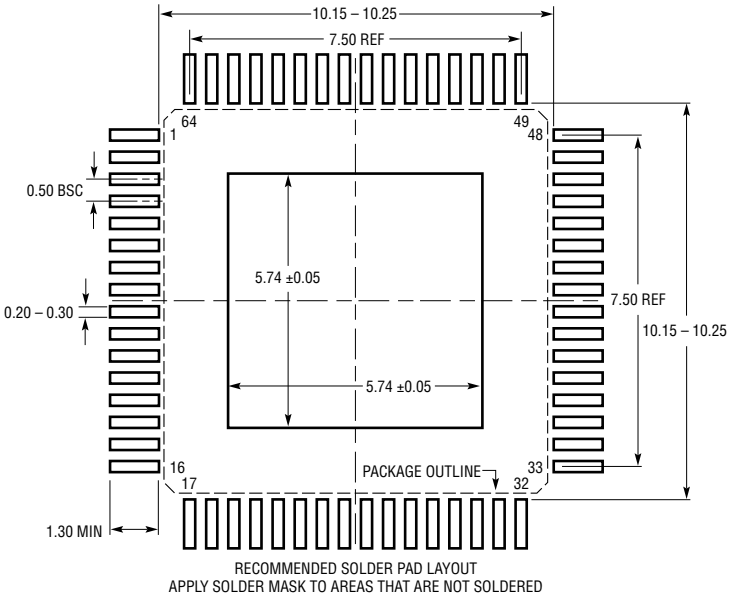
UHG Package
40-Lead Plastic QFN (5mm × 8mm)
(Reference LTC DWG # 05-08-1528 Rev A)

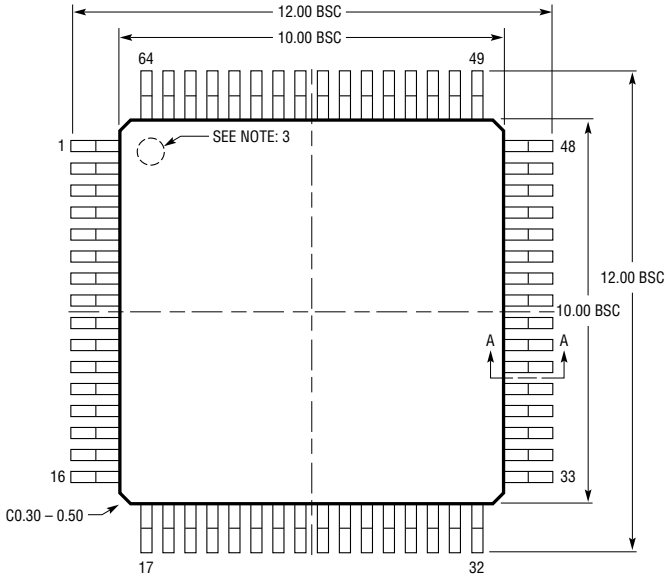


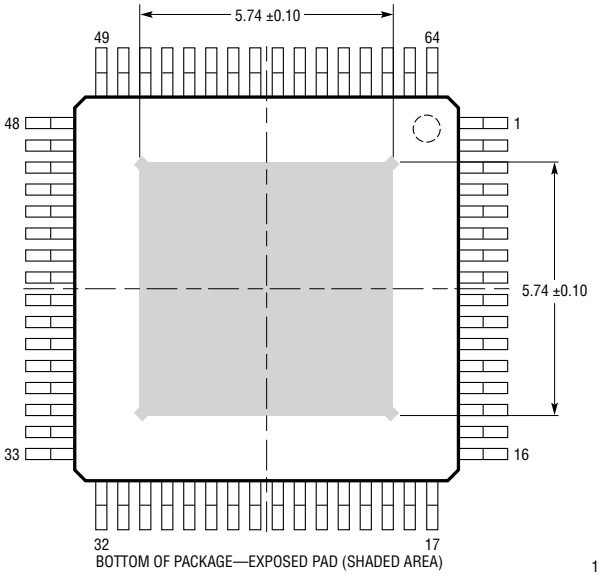
NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08MM.
3. WARPAGE SHALL NOT EXCEED 0.10MM.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. REFER JEDEC M0-220.

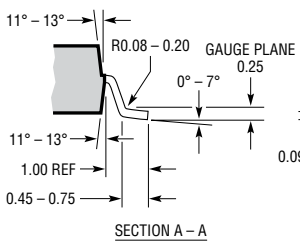
PACKAGE DESCRIPTION

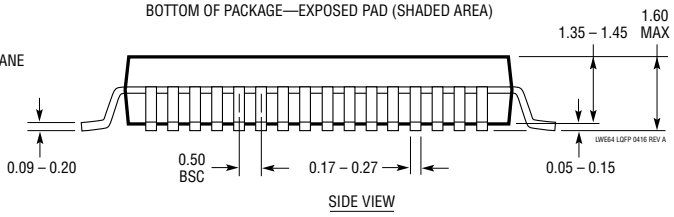
LWE Package
64-Lead Plastic Exposed Pad LQFP (10mm × 10mm)
(Reference LTC DWG #05-08-1982 Rev A)











NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND MAX 0.50mm (20 MILS) ON ANY SIDE OF THE EXPOSED PAD, MAX 0.77mm (30 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
4. DRAWING IS NOT TO SCALE

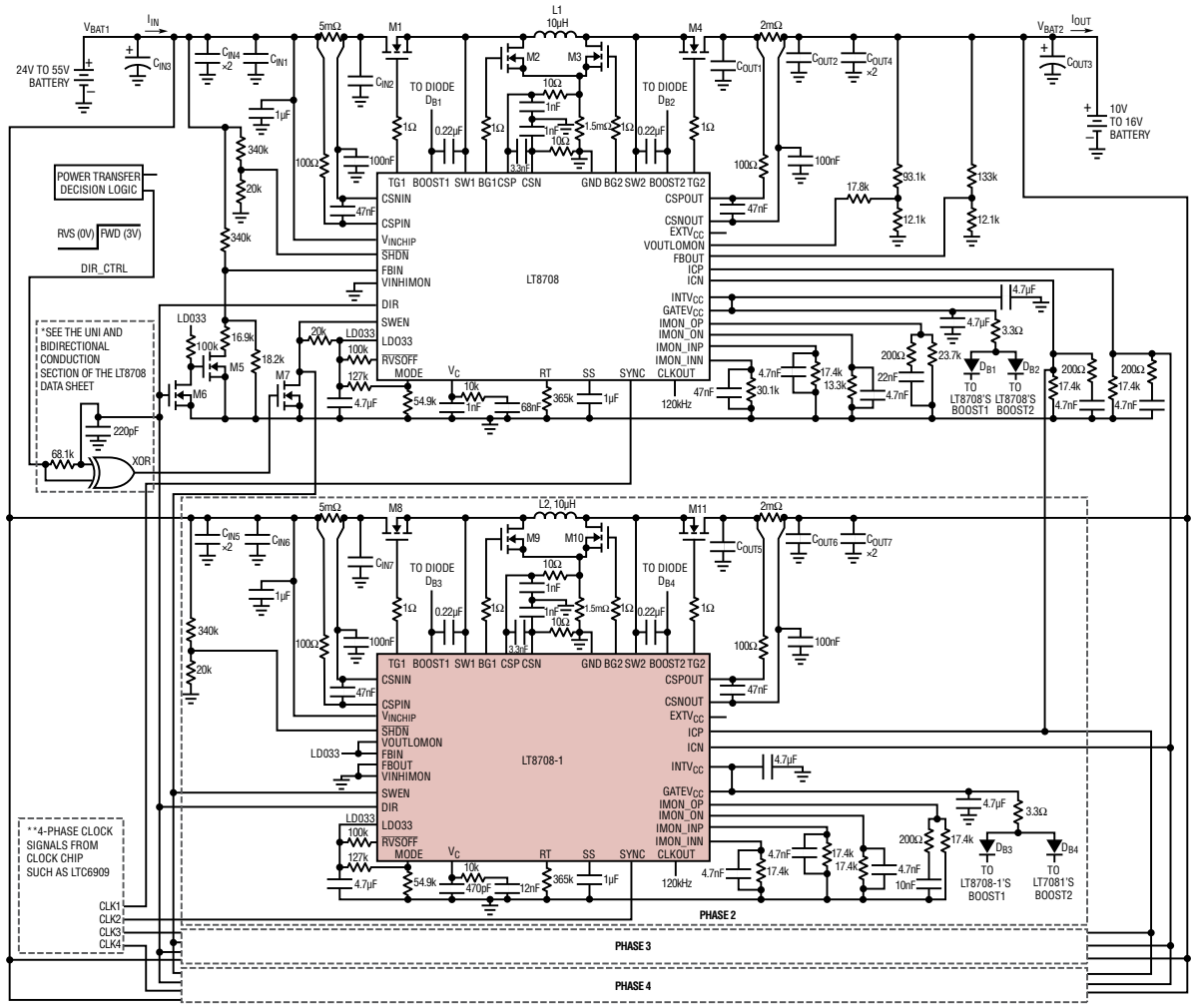
Rev A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/20	Added eLQFP package option.	1, 3, 4, 6, 36, 37
		Corrected Block Diagram.	13
		Corrected components information.	31, 33, 36

TYPICAL APPLICATION

4-Phase 48V to 12V Bidirectional Dual Battery System with FHCM and RHCM



D_{B1}, D_{B2}, D_{B3}, D_{B4}: CENTRAL SEMI CMMR1U-02-LTE
L1, L2: 10µH, COILCRAFT SER2918H-103KL
XOR: DIODES INC. 74AHC1G86SE-7
M1, M2, M8, M9: INFINEON BSC026N08NS5
M3,M4, M10, M11: INFINEON BSC010N04LS
C_{OUT3}, C_{IN3}: 1500µF 63V
C_{IN1}, C_{IN2}, C_{IN6}, C_{IN7}, C_{OUT1}, C_{OUT2}, C_{OUT5}, C_{OUT6}: 10µF, 100V, X7R
M5, M6, M7: T2N7002AK, TOSHIBA
C_{IN4}, C_{IN5}, C_{OUT4}, C_{OUT7}: SUNCON, 15µF, 100V 100HVP15M

SEE MORE DETAILS OF THIS APPLICATION ON PAGE 33.

87081 TA02a

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT8708	80V Synchronous 4-Switch Buck-Boost DC/DC Controller with Flexible Bidirectional Capability	2.8V (Need $EXTV_{CC}$ > 6.4V) ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 80V, 5mm × 8mm, QFN-40 and 10mm × 10mm eLQFP-64 Packages.
LT8705A	80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, Input and Output Current Monitor, 5mm × 7mm QFN-38 and TSSOP-38 Packages
LTC®3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, Up to 99% Efficiency Drives Logic-Level or STD Threshold MOSFETs, TSSOP-38 Package
LTC3899	60V, Triple Output, Buck/Buck/Boost Synchronous Controller with 29µA Burst Mode I_Q	4.5V (Down to 2.2V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, Buck V_{OUT} Range: 0.8V to 60V, Boost V_{OUT} Up to 60V
LTC3895/ LTC7801	150V Low I_Q, Synchronous Step-Down DC/DC Controller with 100% Duty Cycle	4V ≤ V_{IN} ≤ 140V, 150V ABS Max, PLL Fixed Frequency 50kHz to 900kHz, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, I_Q = 40µA, 4mm × 5mm QFN-24, TSSOP-24, TSSOP-38(31) Packages
LTC3871	Bidirectional Multiphase DC/DC Synchronous Buck or Boost On-Demand Controller	V_{IN}/V_{OUT} Up to 100V, Ideal for High Power 48V/12V Automotive Battery Applications