2 A/1.2 A DC-to-DC Switching Regulator with Independent Positive and Negative Outputs

Data Sheet

ADP5071

FEATURES

- Wide input supply voltage range: 2.85 V to 15 V
- Generates well regulated, independently resistor programmable V_{POS} and V_{NEG} outputs
- Boost regulator to generate V_{POS} output
  - Adjustable positive output to 39 V
  - Integrated 2.0 A main switch
  - Optional single-ended primary-inductor converter (SEPIC) configuration for automatic step-up/step-down
- Inverting regulator to generate V_{NEG} output
  - Adjustable negative output to V_{IN} − 39 V
  - Integrated 1.2 A main switch
- True shutdown for both positive and negative outputs
- 1.2 MHz/2.4 MHz switching frequency with optional external frequency synchronization from 1.0 MHz to 2.6 MHz
- Resistor programmable soft start timer
- Slew rate control for lower system noise
- Individual precision enable and flexible start-up sequence control for symmetric start, V_{POS} first, or V_{NEG} first
- Out-of-phase operation
- UVLO, OCP, OVP, and TSD protection
- 4 mm × 4 mm, 20-lead LFCSP and 20-lead TSSOP
- −40°C to +125°C junction temperature range
- Supported by the ADIsimPower tool set

APPLICATIONS

- Bipolar amplifiers, ADCs, DACs, and multiplexers
- Charge-coupled device (CCD) bias supply
- Optical module supply
- RF power amplifier (PA) bias

TYPICAL APPLICATION CIRCUIT

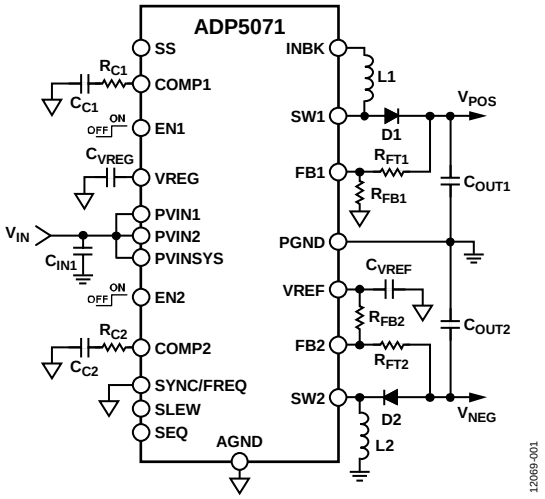

Figure 1.

GENERAL DESCRIPTION

The ADP5071 is a dual high performance dc-to-dc regulator that generates independently regulated positive and negative rails.

The input voltage range of 2.85 V to 15 V supports a wide variety of applications. The integrated main switch in both regulators enables generation of an adjustable positive output voltage up to +39 V and a negative output voltage down to −39 V below input voltage.

The ADP5071 operates at a pin selected 1.2 MHz/2.4 MHz switching frequency. The ADP5071 can synchronize with an external oscillator from 1.0 MHz to 2.6 MHz to ease noise filtering in sensitive applications. Both regulators implement programmable slew rate control circuitry for the MOSFET driver stage to reduce electromagnetic interference (EMI).

Flexible start-up sequencing is provided with the options of manual enable, simultaneous mode, positive supply first, and negative supply first.

The ADP5071 includes a fixed internal or resistor programmable soft start timer to prevent inrush current at power-up. During shutdown, both regulators completely disconnect the loads from the input supply to provide a true shutdown.

Other key safety features in the ADP5071 include overcurrent protection (OCP), overvoltage protection (OVP), thermal shutdown (TSD), and input undervoltage lockout (UVLO).

The ADP5071 is available in a 20-lead LFCSP or in a 20-lead TSSOP and is rated for a −40°C to +125°C junction temperature range.

Table 1. Family Models

Model	Boost Switch (A)	Inverter Switch (A)
ADP5070	1.0	0.6
ADP5071	2.0	1.2

Rev. E
Document Feedback

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2/2015—Revision 0: Initial Version

SPECIFICATIONS

PVIN1 = PVIN2 = PVINSYS = 2.85 V to 15 V, V_{POS} = 15 V, V_{NEG} = −15 V, f_{SW} = 1200 kHz, T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V_{IN}	2.85		15	V	PVIN1, PVIN2, PVINSYS
QUIESCENT CURRENT						
Operating Quiescent Current						
PVIN1, PVIN2, PVINSYS (Total)	I_Q		3.5	4.0	mA	No switching, EN1 = EN2 = high, PVIN1 = PVIN2 = PVINSYS = 5 V
Shutdown Current	I_{SHDN}		5	10	µA	No switching, EN1 = EN2 = low, PVIN1 = PVIN2 = PVINSYS = 5 V
UVLO						
System UVLO Threshold						PVINSYS
Rising	V_{UVLO_RISING}		2.8	2.85	V	
Falling	$V_{UVLO\_FALLING}$	2.5	2.55		V	
Hysteresis	V_{HYS_1}		0.25		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	1.130	1.200	1.270	MHz	SYNC/FREQ = low
		2.240	2.400	2.560	MHz	SYNC/FREQ = high (connect to VREG)
SYNC/FREQ Input						
Input Clock Range	f_{SYNC}	1.000		2.600	MHz	
Input Clock Minimum On Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
Input Clock Minimum Off Pulse Width	$t_{SYNC\_MIN\_OFF}$	100			ns	
Input Clock High Logic	$V_{H\ (SYNC)}$			1.3	V	
Input Clock Low Logic	$V_{L\ (SYNC)}$	0.4			V	
PRECISION ENABLING (EN1, EN2)						
High Level Threshold	V_{TH_H}	1.125	1.15	1.175	V	
Low Level Threshold	V_{TH_L}	1.025	1.05	1.075	V	
Shutdown Mode	V_{TH_S}	0.4			V	Internal circuitry disabled to achieve ISHDN
Pull-Down Resistance	R_{EN}		1.48		MΩ	
INTERNAL REGULATOR						
VREG Output Voltage	V_{REG}		4.25		V	
BOOST REGULATOR						
Feedback Voltage	V_{FB1}		0.8		V	
Feedback Voltage Accuracy		−0.5		+0.5	%	T_J = 25°C
		−1.5		+1.5	%	T_J = −40°C to +125°C
Feedback Bias Current	I_{FB1}			0.1	µA	
Overvoltage Protection Threshold	V_{OV1}		0.86		V	At FB1 pin
Load Regulation	$\Delta V_{FB1}/I_{LOAD1}$		0.0003		%/mA	I_{LOAD1}[1] = 5 mA to 150 mA
Line Regulation	$\Delta V_{FB1}/V_{PVIN1}$		0.002		%/V	V_{PVIN1} = 2.85 V to 14.5 V, I_{LOAD1}[1] = 50 mA
Error Amplifier (EA) Transconductance	g_{M1}	270	300	330	µA/V	
Power FET On Resistance	$R_{DS\ (ON)\ BOOST}$		175		mΩ	
Power FET Maximum Drain Source Voltage	$V_{DS\ (MAX)\ BOOST}$		39		V	
Input Disconnect Switch On Resistance	$R_{DS\ (ON)\ INBK}$		210		mΩ	
Current-Limit Threshold	$I_{LIM\ (BOOST)}$	2.0	2.2	2.4	A	
Minimum On Time			50		ns	
Minimum Off Time			25		ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INVERTING REGULATOR						
Reference Voltage	V_{REF}		1.60		V	
Reference Voltage Accuracy		−0.5		+0.5	%	T_J = 25°C
		−1.5		+1.5	%	T_J = −40°C to +125°C
Feedback Voltage	$V_{REF} - V_{FB2}$		0.8		V	
Feedback Voltage Accuracy		−0.5		+0.5	%	T_J = 25°C
		−1.5		+1.5	%	T_J = −40°C to +125°C
Feedback Bias Current	I_{FB2}			0.1	µA	
Overvoltage Protection Threshold	V_{OV2}		0.74		V	At FB2 pin after soft start has completed
Load Regulation	$\Delta(V_{REF} - V_{FB2})/I_{LOAD2}$		0.0004		%/mA	I_{LOAD2}[1] = 5 mA to 75 mA
Line Regulation	$\Delta(V_{REF} - V_{FB2})/V_{PVIN2}$		0.003		%/V	V_{PVIN2} = 2.85 V to 14.5 V, I_{LOAD2}[1] = 25 mA
EA Transconductance	g_{M2}	270	300	330	µA/V	
Power FET On Resistance	$R_{DS\ (ON)\ INVERTER}$		350		mΩ	
Power FET Maximum Drain Source Voltage	$V_{DS\ (MAX)\ INVERTER}$		39		V	
Current-Limit Threshold	$I_{LIM\ (INVERTER)}$	1200	1320	1440	mA	
Minimum On Time			60		ns	
Minimum Off Time			50		ns	
SOFT START						
Soft Start Timer for Boost and Inverting Regulators	t_{SS}		4		ms	SS = open
			32		ms	SS resistor = 50 kΩ to GND
Hiccup Time	t_{HICCUP}		$8 \times t_{SS}$		ms	
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		150		°C	
Hysteresis	T_{HYS}		15		°C	

[1] I_{LOADx} is the current through a resistive load connected across the output capacitor (where x is 1 for the boost regulator load and 2 for the inverting regulator load).

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
PVIN1, PVIN2, PVINSYS	−0.3 V to +18 V
INBK	−0.3 V to PVIN1 + 0.3 V
SW1	−0.3 V to +40 V
SW2	PVIN2 − 40 V to PVIN2 + 0.3 V
PGND, AGND	−0.3 V to +0.3 V
VREG	−0.3 V to lower of PVINSYS + 0.3 V or +6 V
EN1, EN2, FB1, FB2, SYNC/FREQ	−0.3 V to +6 V
COMP1, COMP2, SLEW, SS, SEQ, VREF	−0.3 V to VREG + 0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JT} are based on a 4-layer printed circuit board (PCB) (two signal and two power planes) with nine thermal vias connecting the exposed pad to the ground plane as recommended in the Layout Considerations section. θ_{JC} is measured at the top of the package and is independent of the PCB. The Ψ_{JT} value is more appropriate for calculating junction to case temperature in the application.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JT}	Unit
20-Lead LFCSP	60.2	36.5	0.63	°C/W
20-Lead TSSOP	58.5	35.0	0.60	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

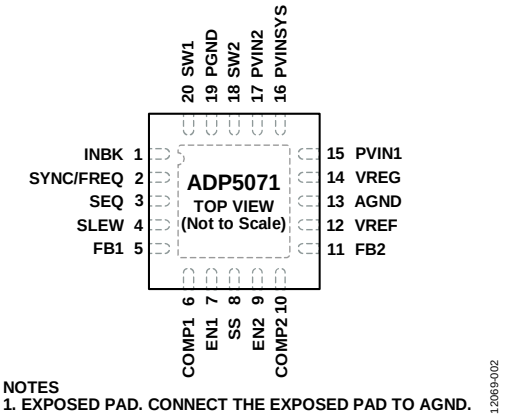


Figure 2. 20-Lead LFCSP Pin Configuration

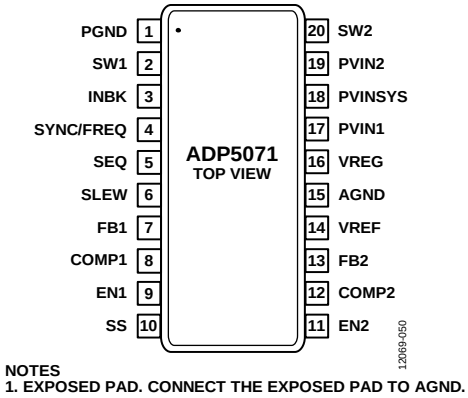


Figure 3. 20-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
LFCSP	**TSSOP**	**Mnemonic**	**Description**
1	3	INBK	Input Disconnect Switch Output for the Boost Regulator.
2	4	SYNC/FREQ	Frequency Setting and Synchronization Input. To set the switching frequency to 2.4 MHz, pull the SYNC/FREQ pin high. To set the switching frequency to 1.2 MHz, pull the SYNC/FREQ pin low. To synchronize the switching frequency, connect the SYNC/FREQ pin to an external clock.
3	5	SEQ	Start-Up Sequence Control. For manual V_{POS}/V_{NEG} startup using an individual precision enabling pin, leave the SEQ pin open. For simultaneous V_{POS}/V_{NEG} startup when the EN2 pin rises, connect the SEQ pin to VREG (the EN1 pin can be used to enable the internal references early, if required). For a sequenced startup, pull the SEQ pin low. Either EN1 or EN2 can be used, and the corresponding supply is the first in sequence; hold the other enable pin low.
4	6	SLEW	Driver Stage Slew Rate Control. The SLEW pin sets the slew rate for the SW1 and SW2 drivers. For the fastest slew rate (best efficiency), leave the SLEW pin open. For normal slew rate, connect the SLEW pin to VREG. For the slowest slew rate (best noise performance), connect the SLEW pin to AGND.
5	7	FB1	Feedback Input for the Boost Regulator. Connect a resistor divider between the positive side of the boost regulator output capacitor and AGND to program the output voltage.
6	8	COMP1	Error Amplifier Compensation for the Boost Regulator. Connect the compensation network between this pin and AGND.
7	9	EN1	Boost Regulator Precision Enable. The EN1 pin is compared to an internal precision reference to enable the boost regulator output.
8	10	SS	Soft Start Programming. Leave the SS pin open to obtain the fastest soft start time. To program a slower soft start time, connect a resistor between the SS pin and AGND.
9	11	EN2	Inverting Regulator Precision Enable. The EN2 pin is compared to an internal precision reference to enable the inverting regulator output.
10	12	COMP2	Error Amplifier Compensation for the Inverting Regulator. Connect the compensation network between this pin and AGND.
11	13	FB2	Feedback Input for the Inverting Regulator. Connect a resistor divider between the negative side of the inverting regulator output capacitor and VREF to program the output voltage.
12	14	VREF	Inverting Regulator Reference Output. Connect a 1.0 µF ceramic filter capacitor between the VREF pin and AGND.
13	15	AGND	Analog Ground.
14	16	VREG	Internal Regulator Output. Connect a 1.0 µF ceramic filter capacitor between the VREG pin and AGND.
15	17	PVIN1	Power Input for the Boost Regulator.
16	18	PVINSYS	System Power Supply for the ADP5071.
17	19	PVIN2	Power Input for the Inverting Regulator.

Pin No.			
LFCSP	TSSOP	Mnemonic	Description
18	20	SW2	Switching Node for the Inverting Regulator.
19	1	PGND	Power Ground for the Boost and Inverting Regulators.
20	2	SW1	Switching Node for the Boost Regulator.
		EPAD	Exposed Pad. Connect the exposed pad to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

Typical performance characteristics are generated using the standard bill of materials for each input/output combination listed in Table 9, Table 10, and Table 11.

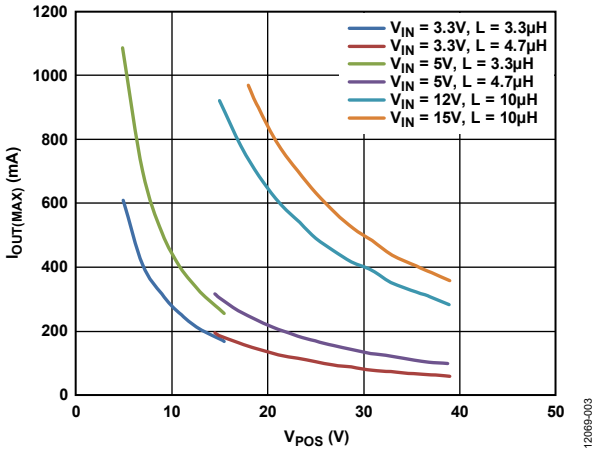


Figure 4. Boost Regulator Maximum Output Current, f_{SW} = 1.2 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (BOOST)}$

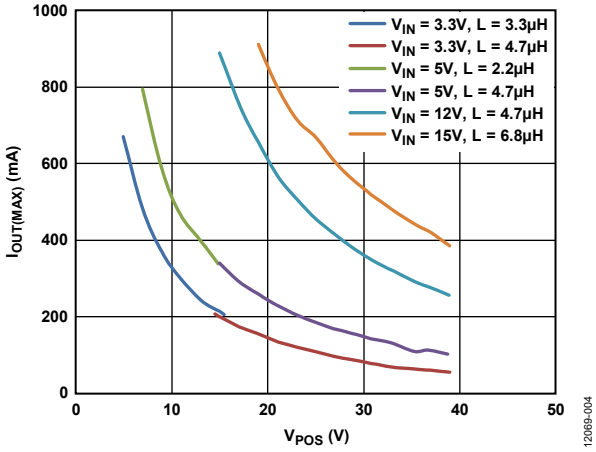


Figure 5. Boost Regulator Maximum Output Current, f_{SW} = 2.4 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (BOOST)}$

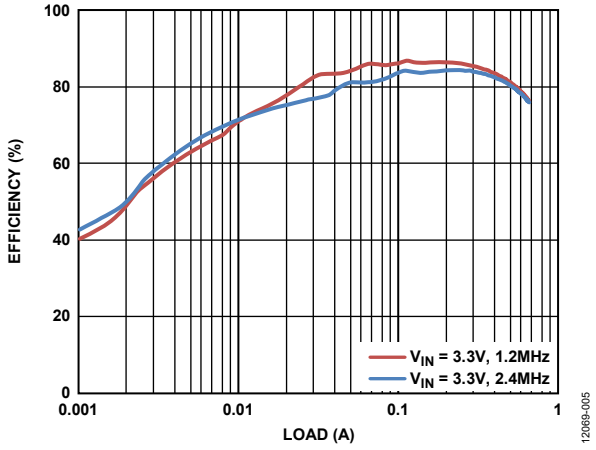


Figure 6. Boost Regulator Efficiency vs. Current Load, V_{IN} = 3.3 V, V_{POS} = 5 V, T_A = 25°C

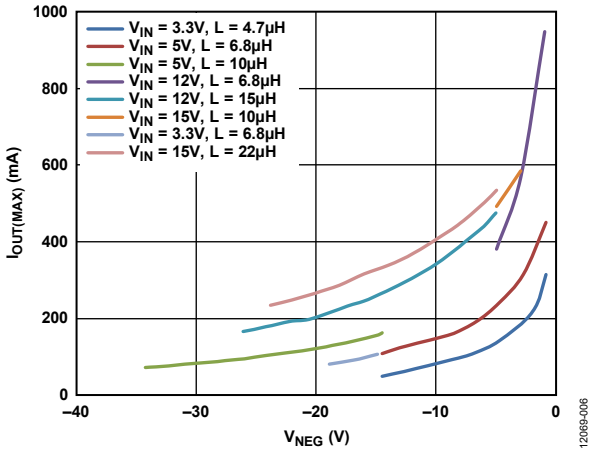


Figure 7. Inverting Regulator Maximum Output Current, f_{SW} = 1.2 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (INVERTER)}$

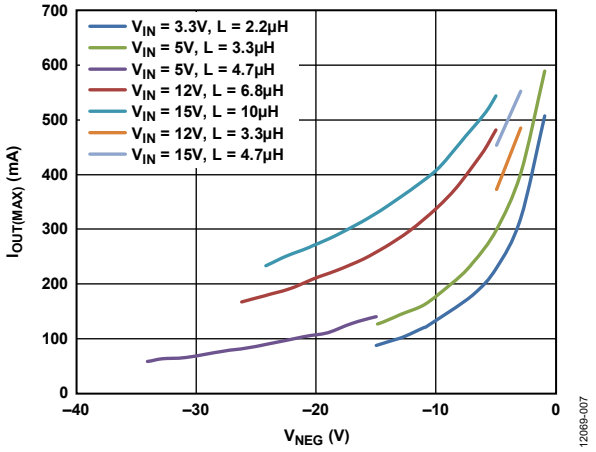


Figure 8. Inverting Regulator Maximum Output Current, f_{SW} = 2.4 MHz, T_A = 25°C, Based on Target of 70% $I_{LIM\ (INVERTER)}$

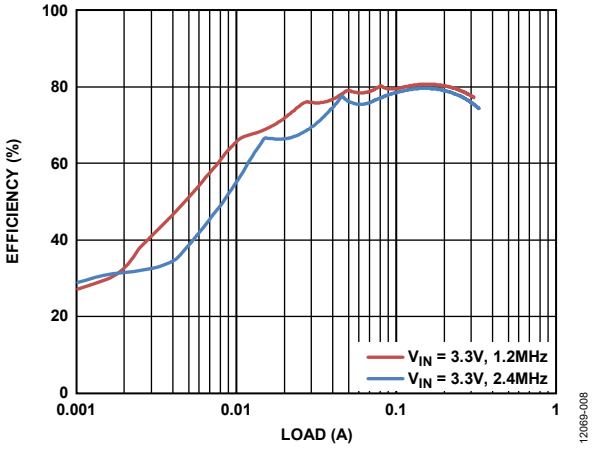


Figure 9. Inverting Regulator Efficiency vs. Current Load, V_{IN} = 3.3 V, V_{NEG} = −5 V, T_A = 25°C

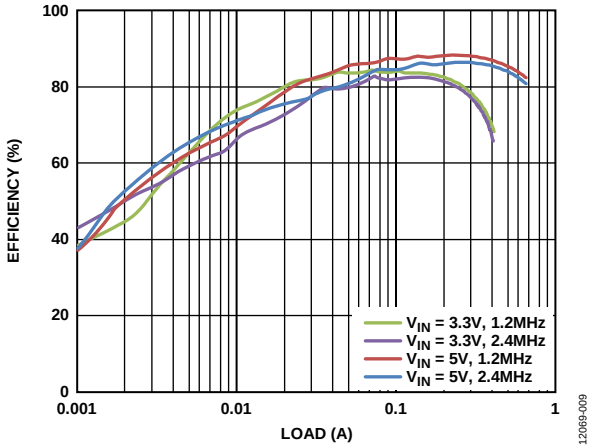


Figure 10. Boost Regulator Efficiency vs. Current Load, V_{POS} = 9 V, T_A = 25°C

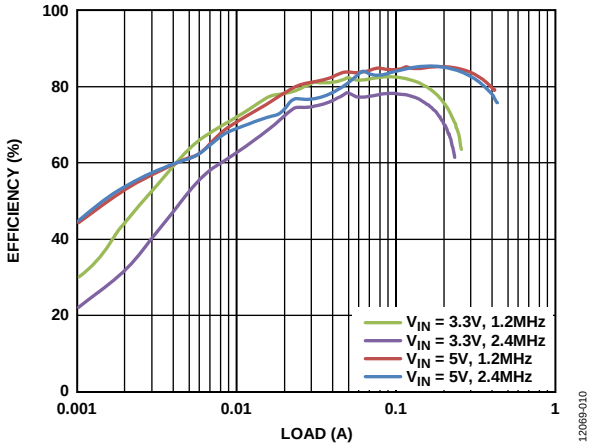


Figure 11. Boost Regulator Efficiency vs. Current Load, V_{POS} = 15 V, T_A = 25°C

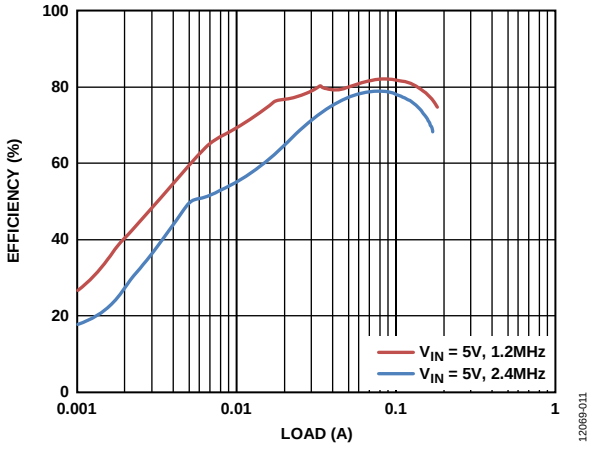


Figure 12. Boost Regulator Efficiency vs. Current Load, V_{POS} = 34 V, T_A = 25°C

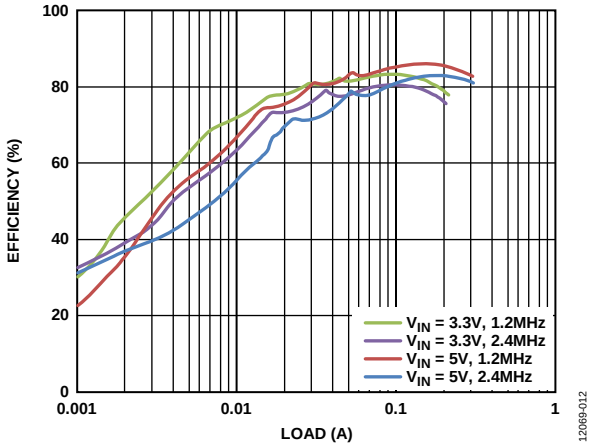


Figure 13. Inverting Regulator Efficiency vs. Current Load, V_{NEG} = −9 V, T_A = 25°C

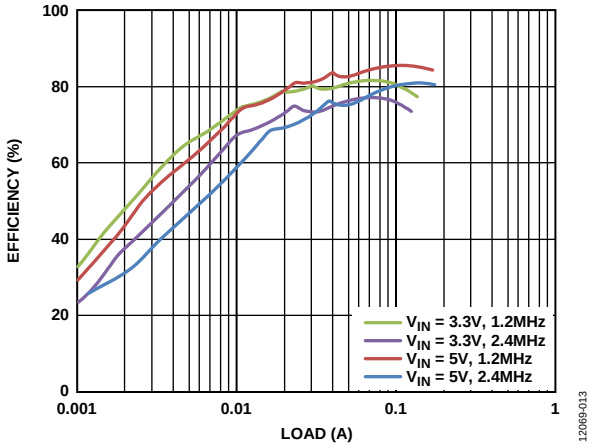


Figure 14. Inverting Regulator Efficiency vs. Current Load, V_{NEG} = −15 V, T_A = 25°C

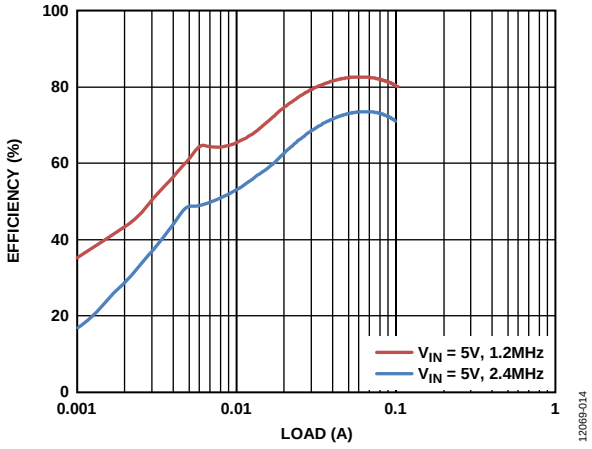


Figure 15. Inverting Regulator Efficiency vs. Current Load, V_{NEG} = −34 V, T_A = 25°C

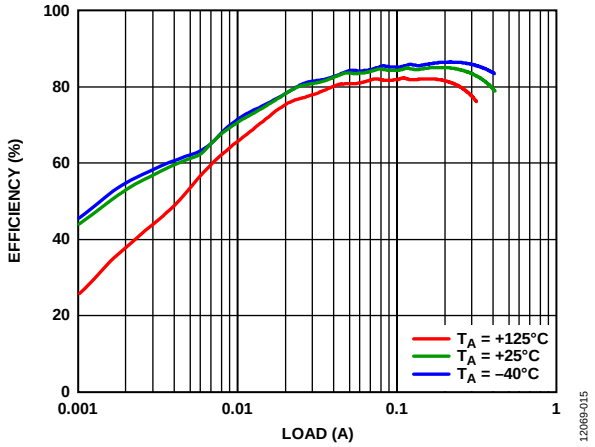


Figure 16. Boost Regulator Efficiency over Temperature, V_{IN} = 5 V, V_{POS} = 15 V, f_{SW} = 1.2 MHz

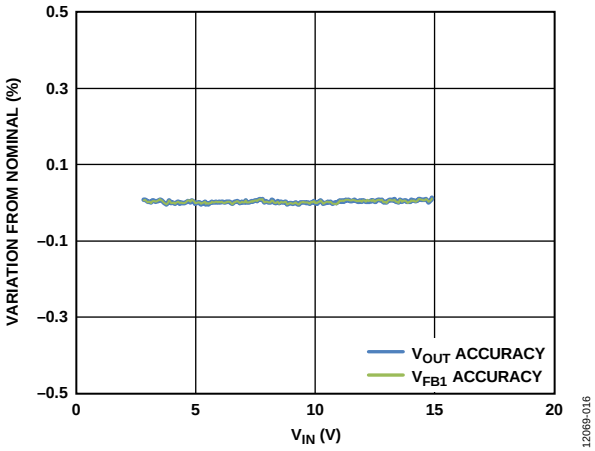


Figure 17. Boost Regulator Line Regulation, V_{POS} = 15 V, f_{SW} = 1.2 MHz, 15 mA Load, T_A = 25°C

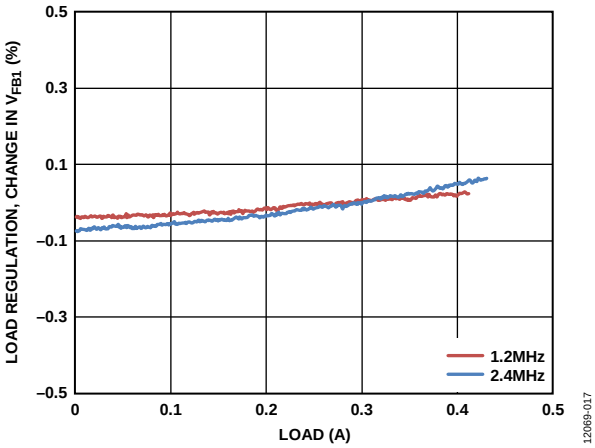


Figure 18. Boost Regulator Load Regulation, V_{IN} = 5 V, V_{POS} = 15 V

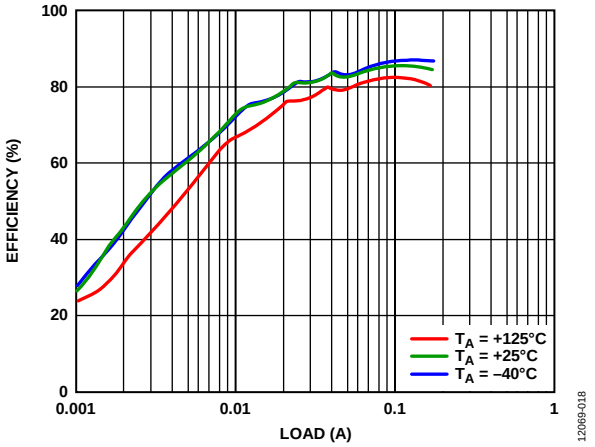


Figure 19. Inverting Regulator Efficiency over Temperature, V_{IN} = 5 V, V_{NEG} = −15 V, f_{SW} = 1.2 MHz

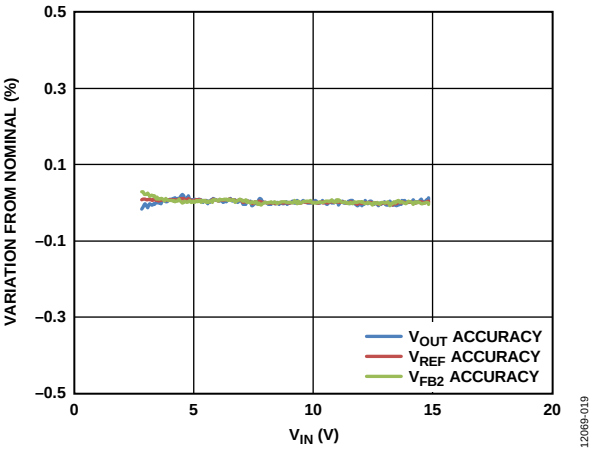


Figure 20. Inverting Regulator Line Regulation, V_{NEG} = −15 V, f_{SW} = 1.2 MHz, 15 mA Load, T_A = 25°C

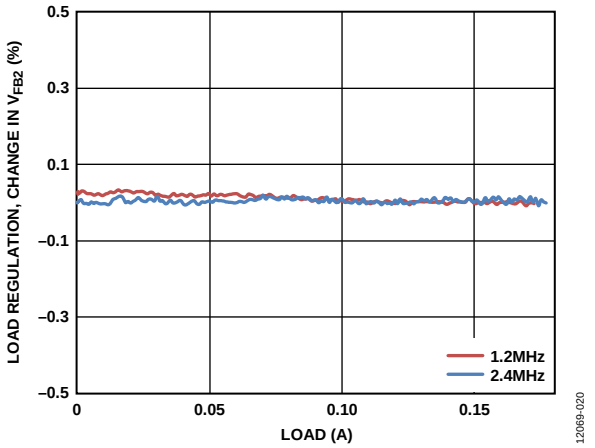


Figure 21. Inverting Regulator Load Regulation, V_{IN} = 5 V, V_{NEG} = −15 V

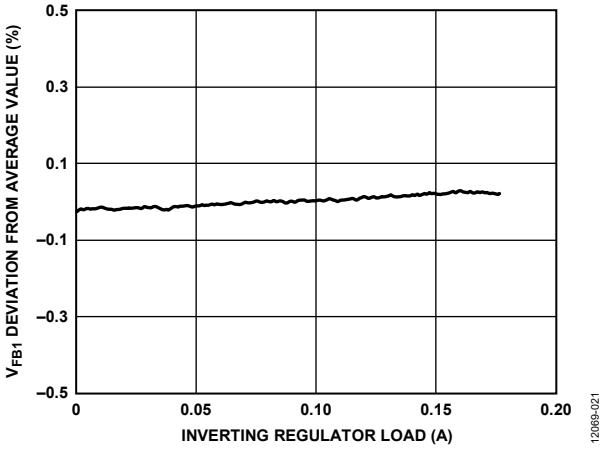


Figure 22. Cross Regulation, Boost Regulator V_{FB1} Regulation over Inverting Regulator Current Load, V_{IN} = 5 V, V_{POS} = 15 V, V_{NEG} = −15 V, f_{SW} = 2.4 MHz, T_A = 25°C, Boost Regulator Run in Continuous Conduction Mode with Fixed Load for Test

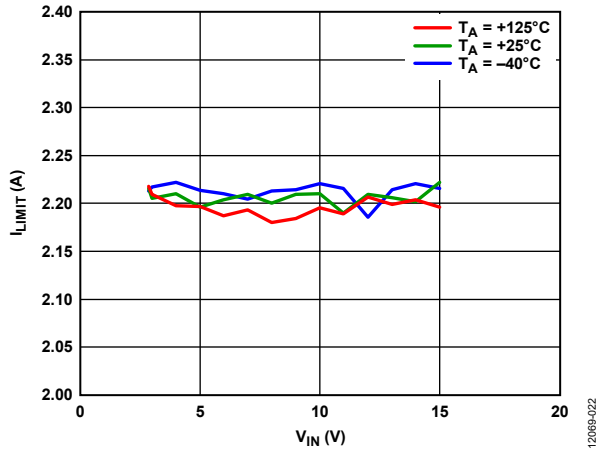


Figure 23. Boost Regulator Current Limit (I_{LIMIT}) vs. Input Voltage (V_{IN}) over Temperature

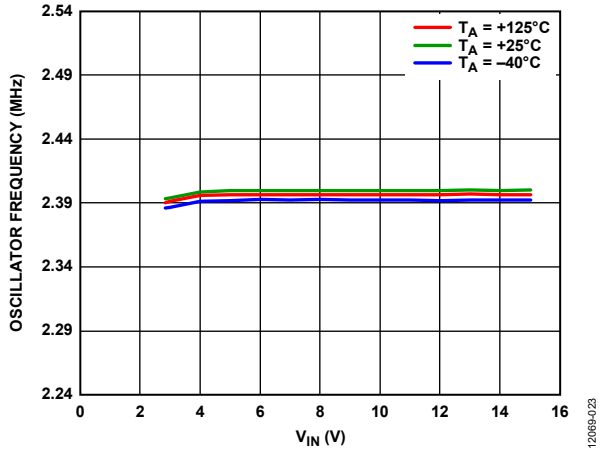


Figure 24. Oscillator Frequency vs. Input Voltage (V_{IN}) over Temperature, SYNC/FREQ Pin = High

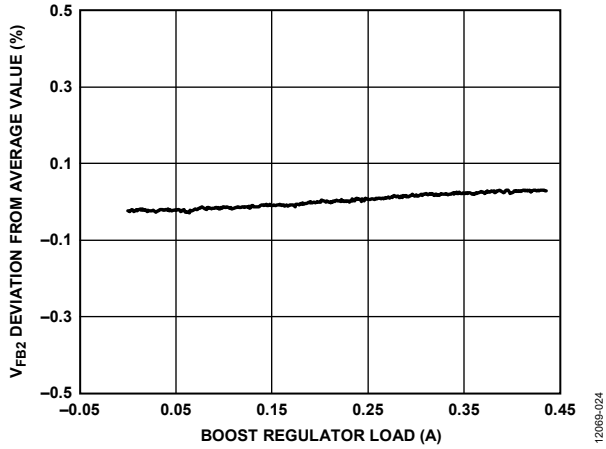


Figure 25. Cross Regulation, Inverting Regulator V_{FB2} Regulation over Boost Regulator Current Load, V_{IN} = 5 V, V_{POS} = 15 V, V_{NEG} = −15 V, f_{SW} = 2.4 MHz, T_A = 25°C, Inverting Regulator Run in Continuous Conduction Mode with Fixed Load for Test

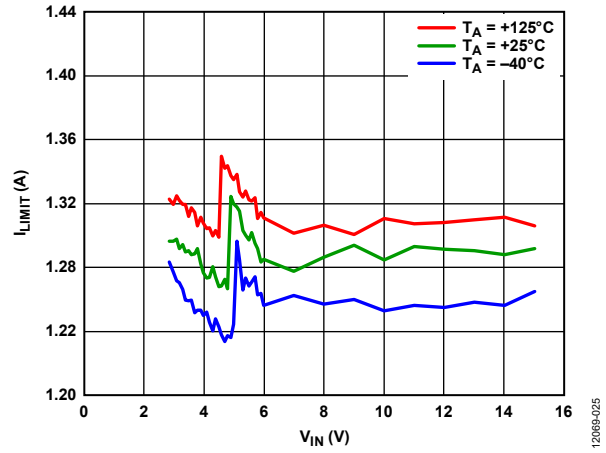


Figure 26. Inverting Regulator Current Limit (I_{LIMIT}) vs. Input Voltage (V_{IN}) over Temperature

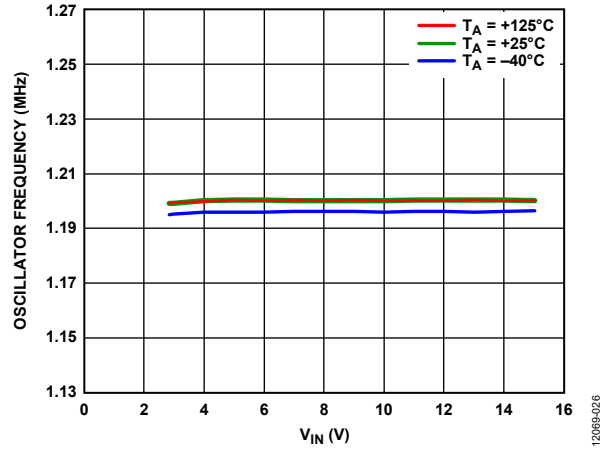


Figure 27. Oscillator Frequency vs. Input Voltage (V_{IN}) over Temperature, SYNC/FREQ Pin = Low

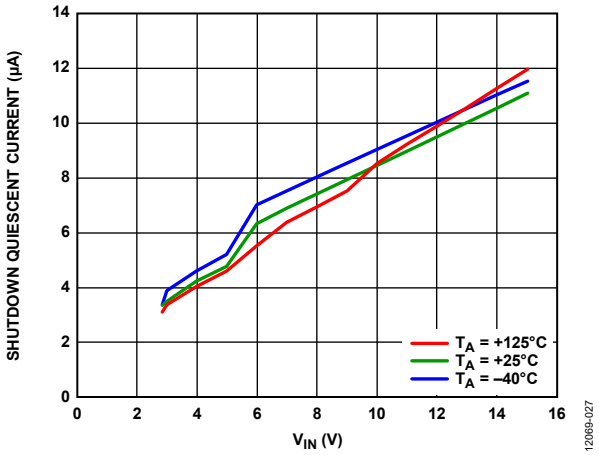


Figure 28. Shutdown Quiescent Current vs. Input Voltage (V_{IN}) over Temperature, Both ENx Pins Below Shutdown Threshold

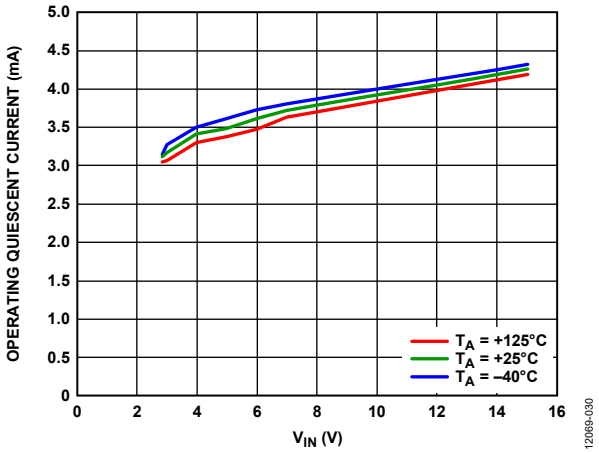


Figure 31. Operating Quiescent Current vs. Input Voltage (V_{IN}) over Temperature, Both ENx Pins On

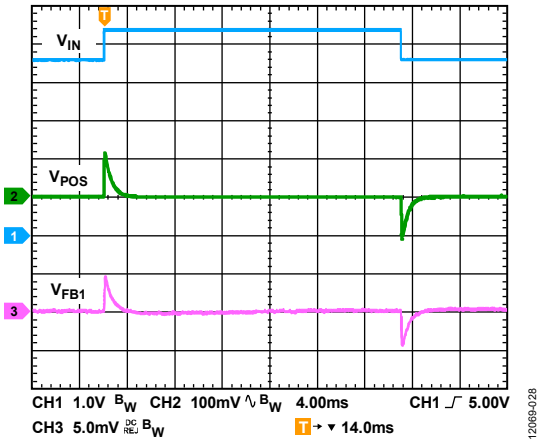


Figure 29. Boost Regulator Line Transient, V_{IN} = 4.5 V to 5.5 V Step, V_{POS} = 15 V, R_{LOAD1} = 300 Ω, f_{SW} = 2.4 MHz, T_A = 25°C

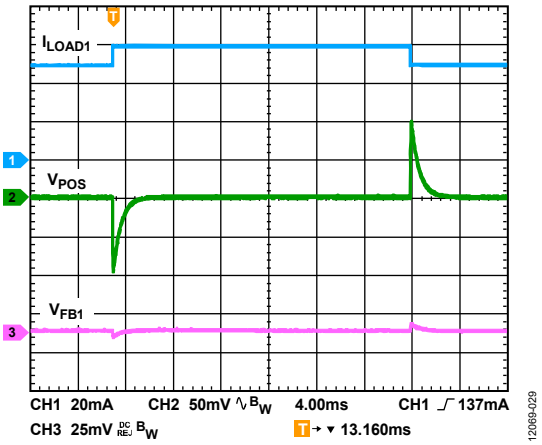


Figure 30. Boost Regulator Load Transient, V_{IN} = 5 V Step, V_{POS} = 15 V, I_{LOAD1} = 120 mA to 150 mA Step, f_{SW} = 2.4 MHz, T_A = 25°C

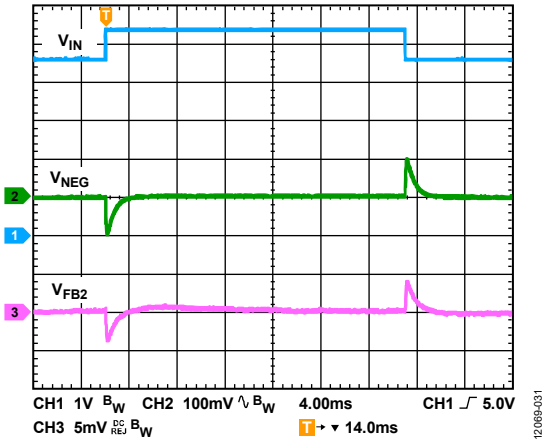


Figure 32. Inverting Regulator Line Transient, V_{IN} = 4.5 V to 5.5 V Step, V_{NEG} = −15 V, R_{LOAD2} = 300 Ω, f_{SW} = 2.4 MHz, T_A = 25°C

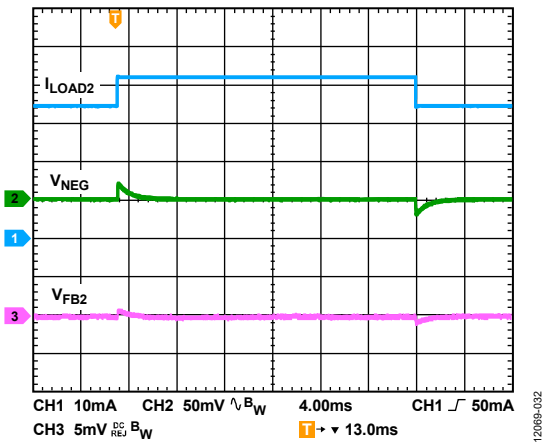


Figure 33. Inverting Regulator Load Transient, V_{IN} = 5 V Step, V_{NEG} = −15 V, I_{LOAD2} = 35 mA to 45 mA Step, f_{SW} = 2.4 MHz, T_A = 25°C

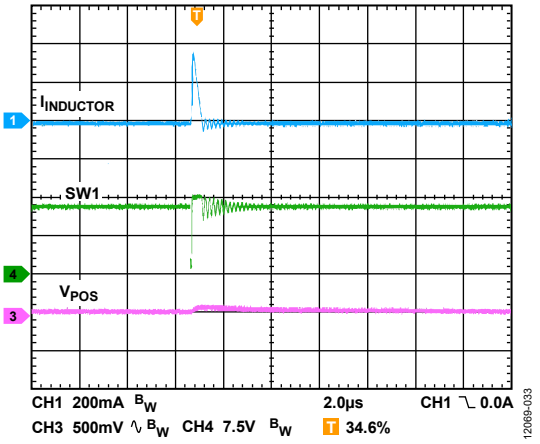


Figure 34. Boost Regulator Skip Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 12 V, V_{POS} = 15 V, I_{LOAD1} = 4 mA, f_{SW} = 2.4 MHz, T_A = 25°C

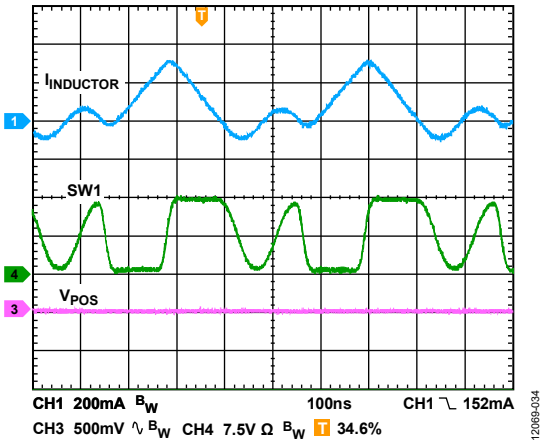


Figure 35. Boost Regulator Discontinuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{POS} = 15 V, I_{LOAD1} = 20 mA, f_{SW} = 2.4 MHz, T_A = 25°C

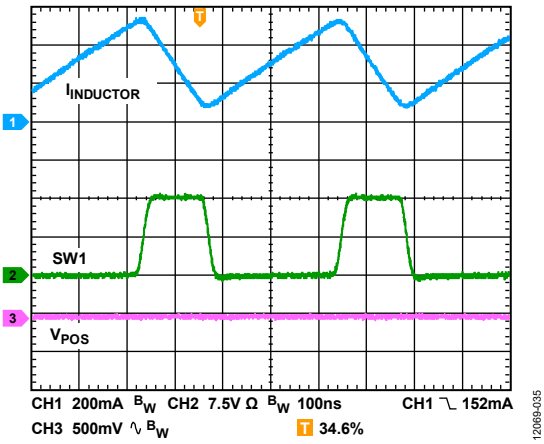


Figure 36. Boost Regulator Continuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{POS} = 15 V, I_{LOAD1} = 90 mA, f_{SW} = 2.4 MHz, T_A = 25°C

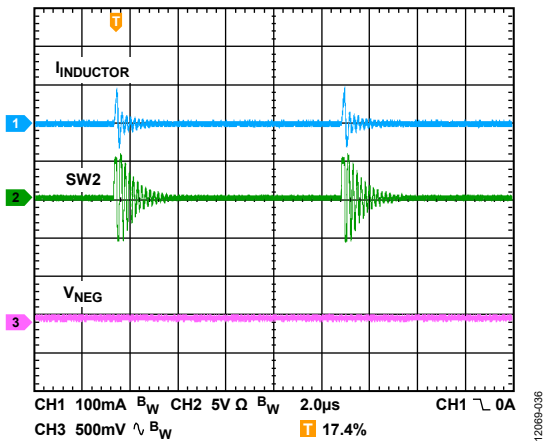


Figure 37. Inverting Regulator Skip Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{NEG} = −5 V, I_{LOAD2} = 1 mA, f_{SW} = 2.4 MHz, T_A = 25°C

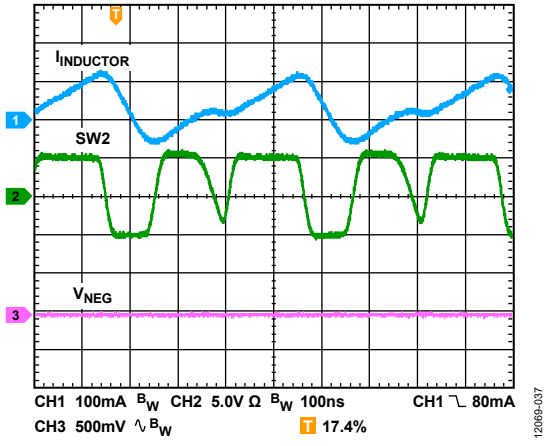


Figure 38. Inverting Regulator Discontinuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{NEG} = −5 V, I_{LOAD2} = 6 mA, f_{SW} = 2.4 MHz, T_A = 25°C

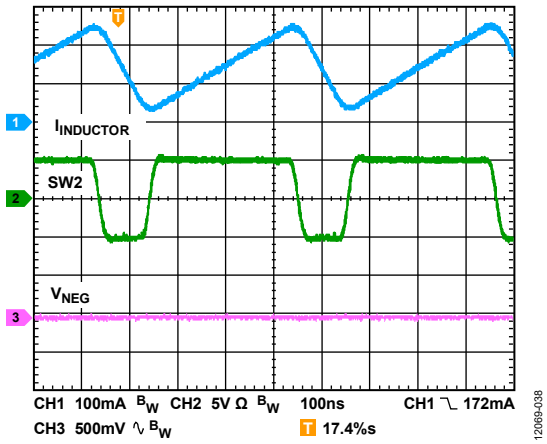


Figure 39. Inverting Regulator Continuous Conduction Mode Operation Showing Inductor Current ($I_{INDUCTOR}$), Switch Node Voltage, and Output Ripple, V_{IN} = 5 V, V_{NEG} = −5 V, I_{LOAD2} = 35 mA, f_{SW} = 2.4 MHz, T_A = 25°C

THEORY OF OPERATION

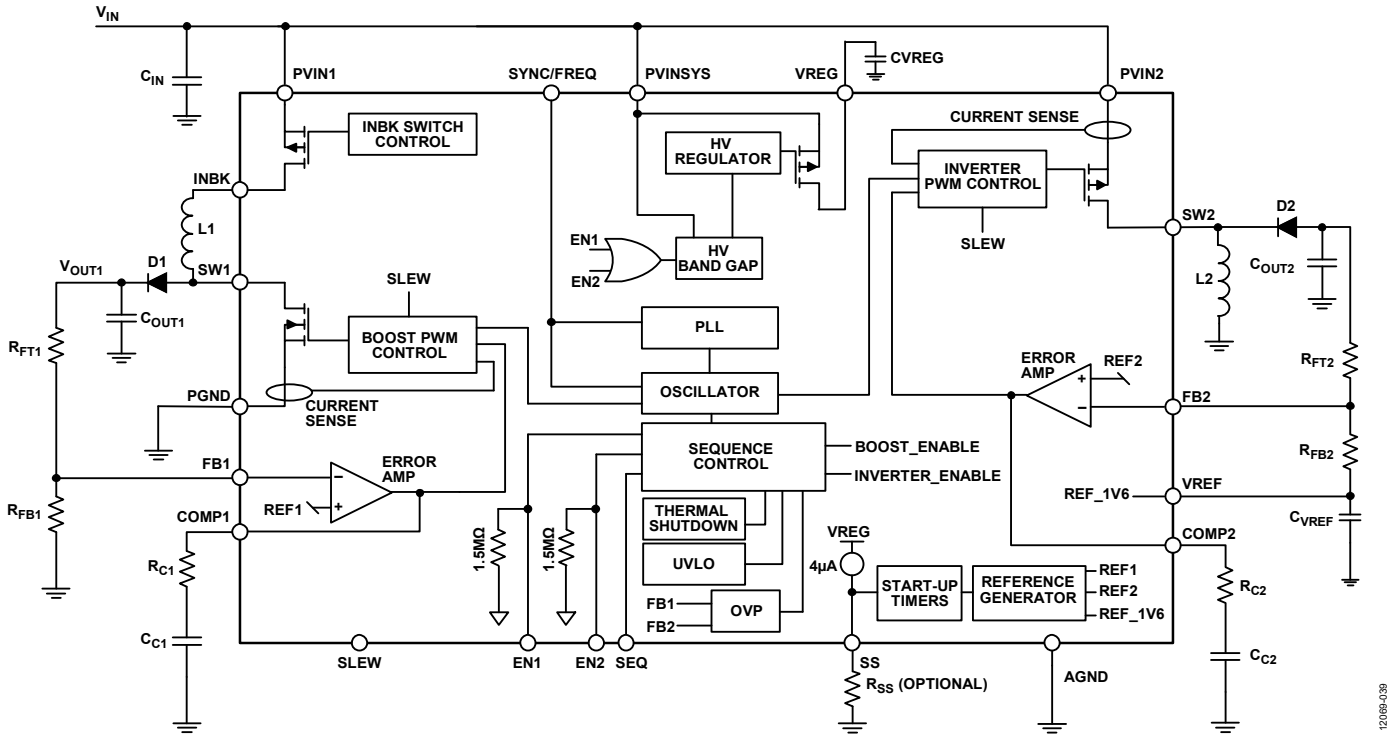


Figure 40. Functional Block Diagram

PWM MODE

The boost and inverting regulators in the ADP5071 operate at a fixed frequency set by an internal oscillator. At the start of each oscillator cycle, the MOSFET switch turns on, applying a positive voltage across the inductor. The inductor current increases until the current sense signal crosses the peak inductor current threshold that turns off the MOSFET switch; this threshold is set by the error amplifier output. During the MOSFET off time, the inductor current declines through the external diode until the next oscillator clock pulse starts a new cycle. It regulates the output voltage by adjusting the peak inductor current threshold.

PSM MODE

During light load operation, the regulators can skip pulses to maintain output voltage regulation. Skipping pulses increases the device efficiency.

UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout circuitry monitors the PVINSYS pin voltage level. If the input voltage drops below the $V_{UVLO\_FALLING}$ threshold, both regulators turn off. After the PVINSYS pin voltage rises above the V_{UVLO_RISING} threshold, the soft start period initiates, and the regulators are enabled.

OSCILLATOR AND SYNCHRONIZATION

The ADP5071 initiates the drive of the boost regulator SW1 pin and the inverting regulator SW2 pin 180° out of phase to reduce peak current consumption and noise.

A phase-locked loop (PLL)-based oscillator generates the internal clock and offers a choice of two internally generated frequency options or external clock synchronization. The switching frequency is configured using the SYNC/FREQ pin options shown in Table 6.

For external synchronization, connect the SYNC/FREQ pin to a suitable clock source. The PLL locks to an input clock within the range specified by f_{SYNC}.

Table 6. SYNC/FREQ Pin Options

SYNC/FREQ Pin	Switching Frequency
High	2.4 MHz
Low	1.2 MHz
External Clock	1 × clock frequency

INTERNAL REGULATORS

The internal VREG regulator in the ADP5071 provides a stable power supply for the internal circuitry. The VREG supply can be used to provide a logic high signal for device configuration pins but must not be used to supply external circuitry.

The VREF regulator provides a reference voltage for the inverting regulator feedback network to ensure a positive feedback voltage on the FB2 pin.

A current-limit circuit is included for both regulators to protect the circuit from accidental loading.

PRECISION ENABLING

The ADP5071 has an individual enable pin for the boost and inverting regulators: EN1 and EN2. The enable pins feature a precision enable circuit with an accurate reference voltage. This reference allows the ADP5071 to be sequenced easily from other supplies. It can also be used as a programmable UVLO input by using a resistor divider.

The enable pins have an internal pull-down resistor that defaults each regulator to off when the pin is floating.

When the voltage at the enable pins is greater than the V_{TH_H} reference level, the regulator is enabled.

SOFT START

Each regulator in the ADP5071 includes soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time is internally set to the fastest rate when the SS pin is open.

Connecting a resistor between SS and AGND allows the adjustment of the soft start delay. The delay length is common to both regulators.

SLEW RATE CONTROL

The ADP5071 employs programmable output driver slew rate control circuitry. This circuitry reduces the slew rate of the switching node as shown in Figure 41, resulting in reduced ringing and lower EMI. To program the slew rate, connect the SLEW pin to the VREG pin for normal mode, to the AGND pin for slow mode, or leave it open for fast mode. This configuration allows the use of an open-drain output from a noise sensitive device to switch the slew rate from fast to slow, for example, during analog-to-digital converter (ADC) sampling.

Note that slew rate control causes a trade-off between efficiency and low EMI.

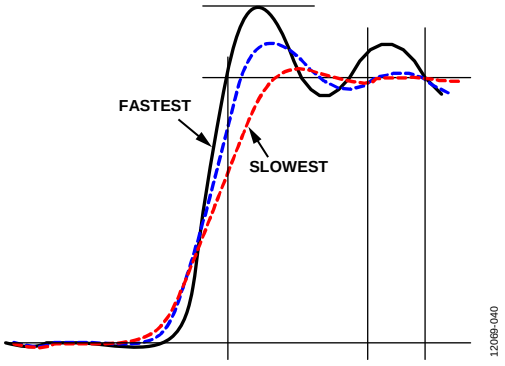


Figure 41. Switching Node at Various Slew Rate Settings

CURRENT-LIMIT PROTECTION

The boost and inverting regulators in the ADP5071 include current-limit protection circuitry to limit the amount of forward current through the MOSFET switch.

When the peak inductor current exceeds the overcurrent limit threshold for a number of clock cycles during an overload or short-circuit condition, the regulator enters hiccup mode. The regulator stops switching and then restarts with a new soft start cycle after t_{HICCUP} and repeats until the overcurrent condition is removed.

OVERVOLTAGE PROTECTION

An overvoltage protection mechanism is present on the FB1 and FB2 pins for the boost and inverting regulators.

On the boost regulator, when the voltage on the FB1 pin exceeds the V_{OV1} threshold, the switching on SW1 stops until the voltage falls below the threshold again. This functionality is permanently enabled on this regulator.

On the inverting regulator, when the voltage on the FB2 pin drops below the V_{OV2} threshold, the switching stops until the voltage rises above the threshold. This functionality is enabled after the soft start period has elapsed.

THERMAL SHUTDOWN

In the event that the ADP5071 junction temperature rises above T_{SHDN}, the thermal shutdown circuit turns off the IC. Extreme junction temperatures can be the result of prolonged high current operation, poor circuit board design, and/or high ambient temperature. Hysteresis is included so that when thermal shutdown occurs, the ADP5071 does not return to operation until the on-chip temperature drops below T_{SHDN} minus T_{HYS}. When resuming from thermal shutdown, a soft start is performed on each enabled channel.

START-UP SEQUENCE

The ADP5071 implements a flexible start-up sequence to meet different system requirements. Three different enabling modes can be implemented via the SEQ pin, as explained in Table 7.

Table 7. SEQ Pin Settings

SEQ Pin	Description
Open	Manual enable mode
VREG	Simultaneous enable mode
Low	Sequential enable mode

To configure the manual enable mode, leave the SEQ pin open. The boost and inverting regulators are controlled separately from their respective precision enable pins.

To configure the simultaneous enable mode, connect the SEQ pin to the VREG pin. Both regulators power up simultaneously when the EN2 pin is taken high. The EN1 pin enable can be used to enable the internal references ahead of enabling the outputs, if desired. The simultaneous enable mode timing is shown in Figure 42.

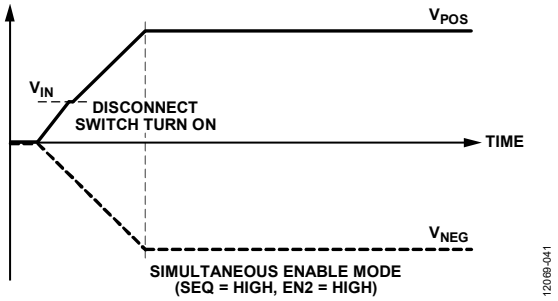


Figure 42. Simultaneous Enable Mode

To configure the sequential enable mode, pull the SEQ pin low. In this mode, either V_{POS} or V_{NEG} can be enabled first by using the respective EN1 pin or EN2 pin. Keep the other pin low. The secondary supply is enabled when the primary supply completes soft start and its feedback voltage reaches approximately 85% of the target value. The sequential enable mode timing is shown in Figure 43.

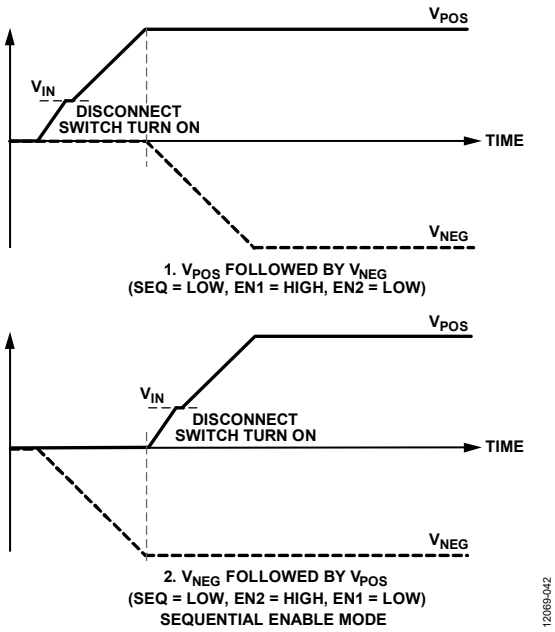


Figure 43. Sequential Enable Mode

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP5071 is supported by the ADIsimPower design toolset. ADIsimPower is a collection of tools that produce complete power designs optimized to a specific design goal. These tools allow the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count while taking into consideration the operating conditions and limitations of the IC and all real external components. The ADIsimPower tool can be found at www.analog.com/adisimpower, and the user can request an unpopulated board through the tool.

COMPONENT SELECTION

Feedback Resistors

The ADP5071 provides an adjustable output voltage for both boost and inverting regulators. An external resistor divider sets the output voltage where the divider output must equal the appropriate feedback reference voltage, V_{FB1} or V_{FB2}. To limit the output voltage accuracy degradation due to feedback bias current, ensure that the current through the divider is at least 10 times I_{FB1} or I_{FB2}.

Set the positive output for the boost regulator by

$$V_{POS} = V_{FB1} \times \left(1 + \frac{R_{FT1}}{R_{FB1}}\right)$$

where:
V_{POS} is the positive output voltage.
V_{FB1} is the FB1 reference voltage.
R_{FT1} is the feedback resistor from V_{POS} to FB1.
R_{FB1} is the feedback resistor from FB1 to AGND.

Set the negative output for the inverting regulator by

$$V_{NEG} = V_{FB2} - \frac{R_{FT2}}{R_{FB2}}(V_{REF} - V_{FB2})$$

where:
V_{NEG} is the negative output voltage.
V_{FB2} is the FB2 reference voltage.
R_{FT2} is the feedback resistor from V_{NEG} to FB2.
R_{FB2} is the feedback resistor from FB2 to VREF.
V_{REF} is the VREF pin reference voltage.

Table 8. Recommended Feedback Resistor Values

	Boost/SEPIC Regulator			Inverting Regulator		
Desired Output Voltage (V)	R_{FT1} (MΩ)	R_{FB1} (kΩ)	Calculated Output Voltage (V)	R_{FT2} (MΩ)	R_{FB2} (kΩ)	Calculated Output Voltage (V)
±1.8	0.143	115	1.795	0.332	102	−1.804
±3	0.316	115	2.998	0.475	100	−3.000
±3.3	0.357	115	3.283	0.523	102	−3.302
±4.2	0.432	102	4.188	0.715	115	−4.174
±5	0.604	115	5.002	1.15	158	−5.023
±9	1.24	121	8.998	1.62	133	−8.944
±12	1.4	100	12.000	1.15	71.5	−12.067
±13	2.1	137	13.063	2.8	162	−13.027
±15	2.43	137	14.990	2.32	118	−14.929
±18	2.15	100	18.000	2.67	113	−18.103
±20	2.55	107	19.865	2.94	113	−20.014
±24	3.09	107	23.903	3.16	102	−23.984
±30	3.65	100	30.000	4.12	107	−30.004
±35	5.9	137	35.253	5.11	115	−34.748

Output Capacitors

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to the output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 25 V or 50 V (depending on output) are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

Calculate the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage using the following equation:

$$C_{EFFECTIVE} = C_{NOMINAL} \times (1 - TEMPCO) \times (1 - DCBIASCO) \times (1 - Tolerance)$$

where:
$C_{EFFECTIVE}$ is the effective capacitance at the operating voltage.
$C_{NOMINAL}$ is the nominal data sheet capacitance.
TEMPCO is the worst-case capacitor temperature coefficient.
DCBIASCO is the dc bias derating at the output voltage.
Tolerance is the worst-case component tolerance.

To guarantee the performance of the device, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

Capacitors with lower effective series resistance (ESR) and effective series inductance (ESL) are preferred to minimize output voltage ripple.

Note that the use of large output capacitors can require a slower soft start to prevent current limit during startup. A 10 µF capacitor is suggested as a good balance between performance and size.

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response.

To minimize supply noise, place the input capacitor as close as possible to the PVINSYS pin, PVIN1 pin, and PVIN2 pin. A low ESR capacitor is recommended.

The effective capacitance needed for stability is a minimum of 10 µF. If the power pins are individually decoupled, it is recommended to use an effective minimum of a 5.6 µF capacitor on the PVIN1 and PVIN2 pins and a 3.3 µF capacitor on the PVINSYS pin. The minimum values specified exclude dc bias, temperature, and tolerance effects that are application dependent and must be taken into consideration.

VREG Capacitor

A 1.0 µF ceramic capacitor (C_{VREG}) is required between the VREG pin and AGND.

VREF Capacitor

A 1.0 µF ceramic capacitor (C_{VREF}) is required between the VREF pin and AGND.

Soft Start Resistor

A resistor can be connected between the SS pin and the AGND pin to increase the soft start time. The soft start time can be set by the resistor between 4 ms (268 kΩ) and 32 ms (50 kΩ). Leaving the SS pin open selects the fastest time of 4 ms. Figure 44 shows the behavior of this operation. Calculate the soft start time using the following formula:

$$t_{SS} = 38.4 \times 10^{-3} - 1.28 \times 10^{-7} \times R_{SS}\ (\Omega)$$

where $50\ k\Omega \le R_{SS} \le 268\ k\Omega$.

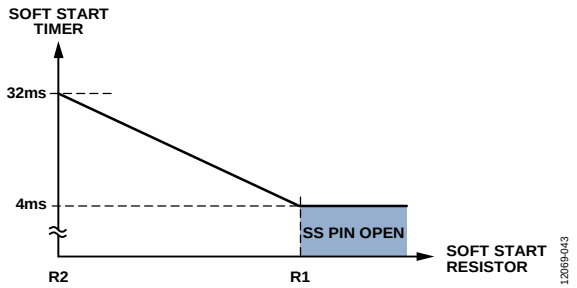


Figure 44. Soft Start Behavior

Diodes

A Schottky diode with low junction capacitance is recommended for D1 and D2. At higher output voltages and especially at higher switching frequencies, the junction capacitance is a significant contributor to efficiency. Higher capacitance diodes also generate more switching noise. As a guide, a diode with less than 40 pF junction capacitance is preferred when the output voltage is above 5 V.

Inductor Selection for the Boost Regulator

The inductor stores energy during the on time of the power switch, and transfers that energy to the output through the output rectifier during the off time. To balance the tradeoffs between small inductor current ripple and efficiency, inductance values in the range of 1 µH to 22 µH are recommended. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in a higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current close to 30% of the maximum dc input current for the application typically yields an optimal compromise.

For the inductor ripple current in continuous conduction mode (CCM) operation, the input (V_{IN}) and output (V_{POS}) voltages determine the switch duty cycle ($DUTY_1$) by the following equation:

$$DUTY_1 = \left(\frac{V_{POS} - V_{IN} + V_{DIODE1}}{V_{POS} + V_{DIODE1}} \right)$$

where V_{DIODE1} is the forward voltage drop of the Schottky diode (D1).

The dc input current in CCM (I_{IN}) can be determined by the following equation:

$$I_{IN} = \frac{I_{OUT1}}{(1 - DUTY_1)}$$

Using the duty cycle ($DUTY_1$) and switching frequency (f_{SW}), determine the on time (t_{ON1}) using the following equation:

$$t_{ON1} = \frac{DUTY_1}{f_{SW}}$$

The inductor ripple current (ΔI_{L1}) in steady state is calculated by

$$\Delta I_{L1} = \frac{V_{IN} \times t_{ON1}}{L1}$$

Solve for the inductance value (L1) using the following equation:

$$L1 = \frac{V_{IN} \times t_{ON1}}{\Delta I_{L1}}$$

Assuming an inductor ripple current of 30% of the maximum dc input current results in

$$L1 = \frac{V_{IN} \times t_{ON1} \times (1 - DUTY_1)}{0.3 \times I_{OUT1}}$$

Ensure that the peak inductor current (the maximum input current plus half the inductor ripple current) is below the rated saturation current of the inductor. Likewise, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

When the ADP5071 boost regulator is operated in CCM at duty cycles greater than 50%, slope compensation is required to stabilize the current mode loop. This slope compensation is built in to the ADP5071 For stable current mode operation, ensure that the selected inductance is equal to or greater than the minimum calculated inductance, L_{MIN1}, for the application parameters in the following equation:

$$L1 > L_{MIN1} = V_{IN} \times \left(\frac{0.13}{(1 - DUTY_1)} - 0.16 \right) (\mu H)$$

Table 10 suggests a series of inductors to use with the ADP5071 boost regulator.

Inductor Selection for the Inverting Regulator

The inductor stores energy during the on time of the power switch, and transfers that energy to the output through the output rectifier during the off time. To balance the tradeoffs between small inductor current ripple and efficiency, inductance values in the range of 1 µH to 22 µH are recommended. In general, lower inductance values have higher saturation current and lower series resistance for a given physical size. However, lower inductance results in a higher peak current that can lead to reduced efficiency and greater input and/or output ripple and noise. A peak-to-peak inductor ripple current close to 30% of the maximum dc current in the inductor typically yields an optimal compromise.

For the inductor ripple current in continuous conduction mode (CCM) operation, the input (V_{IN}) and output (V_{NEG}) voltages determine the switch duty cycle ($DUTY_2$) by the following equation:

$$DUTY_2 = \left(\frac{|V_{NEG}| + V_{DIODE2}}{V_{IN} + |V_{NEG}| + V_{DIODE2}} \right)$$

where V_{DIODE2} is the forward voltage drop of the Schottky diode (D2).

The dc current in the inductor in CCM (I_{L2}) can be determined by the following equation:

$$I_{L2} = \frac{I_{OUT2}}{(1 - DUTY_2)}$$

Using the duty cycle ($DUTY_2$) and switching frequency (f_{SW}), determine the on time (t_{ON2}) by the following equation:

$$t_{ON2} = \frac{DUTY_2}{f_{SW}}$$

The inductor ripple current (ΔI_{L2}) in steady state is calculated by

$$\Delta I_{L2} = \frac{V_{IN} \times t_{ON2}}{L2}$$

Solve for the inductance value (L2) by the following equation:

$$L2 = \frac{V_{IN} \times t_{ON2}}{\Delta I_{L2}}$$

Assuming an inductor ripple current of 30% of the maximum dc current in the inductor results in

$$L2 = \frac{V_{IN} \times t_{ON2} \times (1 - DUTY_2)}{0.3 \times I_{OUT2}}$$

Ensure that the peak inductor current (the maximum input current plus half the inductor ripple current) is below the rated saturation current of the inductor. Likewise, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

When the ADP5071 inverting regulator is operated in CCM at duty cycles greater than 50%, slope compensation is required to stabilize the current mode loop. For stable current mode operation, ensure that the selected inductance is equal to or greater than the minimum calculated inductance, L_{MIN2}, for the application parameters in the following equation:

$$L2 > L_{MIN2} = V_{IN} \times \left(\frac{0.13}{(1 - DUTY_2)} - 0.16 \right) (\mu H)$$

Table 11 suggests a series of inductors to use with the ADP5071 inverting regulator.

LOOP COMPENSATION

The ADP5071 uses external components to compensate the regulator loop, allowing the optimization of the loop dynamics for a given application. It is recommended to use the ADIsimPower tool to calculate compensation components.

Boost Regulator

The boost converter produces an undesirable right half plane zero in the regulation feedback loop. This feedback loop requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right half plane zero. The right half plane zero is determined by the following equation:

$$f_{Z1}(RHP) = \frac{R_{LOAD1}(1 - DUTY_1)^2}{2\pi \times L1}$$

where:
$f_{Z1}(RHP)$ is the right half plane zero frequency.
R_{LOAD1} is the equivalent load resistance or the output voltage divided by the load current.

$$DUTY_1 = \left(\frac{V_{POS} - V_{IN} + V_{DIODE1}}{V_{POS} + V_{DIODE1}} \right)$$

where V_{DIODE1} is the forward voltage drop of the Schottky diode (D1).

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-tenth of the right half plane zero frequency.

The boost regulator loop gain is

$$A_{VL1} = \frac{V_{FB1}}{V_{POS}} \times \frac{V_{IN}}{V_{POS}} \times G_{M1} \times \left| R_{OUT1} \right| \left| Z_{COMP1} \right| \times G_{CS1} \times \left| Z_{OUT1} \right|$$

where:
A_{VL1} is the loop gain.
V_{FB1} is the feedback regulation voltage
V_{POS} is the regulated positive output voltage.
V_{IN} is the input voltage.
G_{M1} is the error amplifier transconductance gain.
R_{OUT1} is the output impedance of the error amplifier and is 33 MΩ.
Z_{COMP1} is the impedance of the series RC network from COMP1 to AGND.
G_{CS1} is the current sense transconductance gain (the inductor current divided by the voltage at COMP1), which is internally set by the ADP5071and is 12.5 A/V.
Z_{OUT1} is the impedance of the load in parallel with the output capacitor.

To determine the crossover frequency (f_{C1}), it is important to note that, at that frequency, the compensation impedance (Z_{COMP1}) is dominated by a resistor (R_{C1}), and the output impedance (Z_{OUT1}) is dominated by the impedance of an output capacitor (C_{OUT1}). Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) is simplified to

$$\left| A_{VL1} \right| = \frac{V_{FB1}}{V_{POS}} \times \frac{V_{IN}}{V_{POS}} \times G_{M1} \times R_{C1} \times G_{CS1} \times \frac{1}{2\pi \times f_{C1} \times C_{OUT1}} = 1$$

where f_{C1} is the crossover frequency.

To solve for R_{C1}, use the following equation:

$$R_{C1} = \frac{2\pi \times f_{C1} \times C_{OUT1} \times (V_{POS})^2}{V_{FB1} \times V_{IN} \times G_{M1} \times G_{CS1}}$$

where G_{CS1} = 12.5 A/V.

Using typical values for V_{FB1} and G_{M1} results in

$$R_{C1} = \frac{2094 \times f_{C1} \times C_{OUT1} \times (V_{POS})^2}{V_{IN}}$$

For better accuracy, it is recommended to use the value of output capacitance, C_{OUT1}, expected for the dc bias conditions under which it operates under in the calculation for R_{C1}.

After the compensation resistor is known, set the zero formed by the compensation capacitor and resistor to one-fourth of the crossover frequency, or

$$C_{C1} = \frac{2}{\pi \times f_{C1} \times R_{C1}}$$

where C_{C1} is the compensation capacitor value.

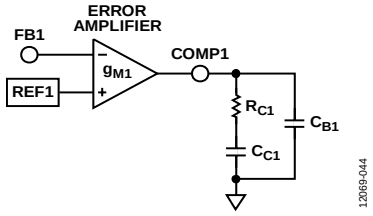


Figure 45. Compensation Components

The capacitor, C_{B1}, is chosen to cancel the zero introduced by the output capacitor ESR. Solve for C_{B1} as follows:

$$C_{B1} = \frac{ESR \times C_{OUT1}}{R_{C1}}$$

For low ESR output capacitance such as with a ceramic capacitor, C_{B1} is optional. For optimal transient performance, R_{C1} and C_{C1} may need to be adjusted by observing the load transient response of the ADP5071. For most applications, R_{C1} must be within the range of 1 kΩ to 200 kΩ, and C_{C1} must be within the range of 1 nF to 68 nF.

Inverting Regulator

The inverting converter, like the boost converter, produces an undesirable right half plane zero in the regulation feedback loop. This feedback loop requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right half plane zero. The right half plane zero frequency is determined by the following equation:

$$f_{Z2}(RHP) = \frac{R_{LOAD2}(1 - DUTY_2)^2}{2\pi \times L2 \times DUTY_2}$$

where:
$f_{Z2}(RHP)$ is the right half plane zero frequency.
R_{LOAD2} is the equivalent load resistance or the output voltage divided by the load current.

$$DUTY_2 = \left(\frac{|V_{NEG}| + V_{DIODE2}}{V_{IN} + |V_{NEG}| + V_{DIODE2}} \right)$$

where V_{DIODE2} is the forward voltage drop of the Schottky diode (D2).

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-tenth of the right half plane zero frequency.

The inverting regulator loop gain is

$$A_{VL2} = \frac{V_{FB2}}{|V_{NEG}|} \times \frac{V_{IN}}{(V_{IN} + 2 \times |V_{NEG}|)} \times G_{M2} \times$$

$$|R_{OUT2}||Z_{COMP2}| \times G_{CS2} \times |Z_{OUT2}|$$

where:
A_{VL2} is the loop gain.
V_{FB2} is the feedback regulation voltage.
V_{NEG} is the regulated negative output voltage.
V_{IN} is the input voltage.
G_{M2} is the error amplifier transconductance gain.
R_{OUT2} is the output impedance of the error amplifier and is 33 MΩ.
Z_{COMP2} is the impedance of the series RC network from COMP2 to AGND.
G_{CS2} is the current sense transconductance gain (the inductor current divided by the voltage at COMP2), which is internally set by the ADP5071 and is 12.5 A/V.
Z_{OUT2} is the impedance of the load in parallel with the output capacitor.

To determine the crossover frequency, it is important to note that, at that frequency, the compensation impedance (Z_{COMP2}) is dominated by a resistor, R_{C2}, and the output impedance (Z_{OUT2}) is dominated by the impedance of the output capacitor, C_{OUT2}. Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) is simplified to

$$|A_{VL2}| = \frac{V_{FB2}}{|V_{NEG}|} \times \frac{V_{IN}}{(V_{IN} + 2 \times |V_{NEG}|)} \times G_{M2} \times$$

$$R_{C2} \times G_{CS} 2 \times \frac{1}{2\pi \times f_{C2} \times C_{OUT2}} = 1$$

where f_{C2} is the crossover frequency.

To solve for R_{C2}, use the following equation:

$$R_{C2} = \frac{2\pi \times f_{C2} \times C_{OUT2} \times |V_{NEG}| \times (V_{IN} + (2 \times |V_{NEG}|)}{V_{FB2} \times V_{IN} \times G_{M2} \times G_{CS2}}$$

where G_{CS2} = 12.5 A/V.

Using typical values for V_{FB2} and G_{M2} results in

$$R_{C2} = \frac{2094 \times f_{C2} \times C_{OUT2} \times |V_{NEG}| \times (V_{IN} + (2 \times |V_{NEG}|)}{V_{IN}}$$

For better accuracy, it is recommended to use the value of output capacitance, C_{OUT2}, expected under the dc bias conditions that it operates under in the calculation for R_{C2}.

After the compensation resistor is known, set the zero formed by the C_{C2} and R_{C2} to one-fourth of the crossover frequency, or

$$C_{C2} = \frac{2}{\pi \times f_{C2} \times R_{C2}}$$

where C_{C2} is the compensation capacitor.

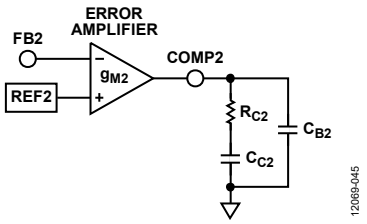


Figure 46. Compensation Component

The capacitor, C_{B2}, is chosen to cancel the zero introduced by output capacitance, ESR.

Solve for C_{B2} as follows:

$$C_{B2} = \frac{ESR \times C_{OUT2}}{R_{C2}}$$

For low ESR output capacitance, such as with a ceramic capacitor, C_{B2} is optional. For optimal transient performance, R_{C2} and C_{C2} may need to be adjusted by observing the load transient response of the ADP5071. For most applications, R_{C2} must be within the range of 1 kΩ to 200 kΩ, and C_{C2} must be within the range of 1 nF to 68 nF.

COMMON APPLICATIONS

Table 9 through Table 11 list a number of common component selections for typical V_{IN} and V_{OUT} conditions. These have been bench tested and provide an off the shelf solution. Note that when pairing a boost and inverting regulator bill of materials, choose the same V_{IN} and switching frequency. To optimize components for an application, it is recommend to use the ADIsimPower toolset.

Figure 47 shows the schematic referenced by Table 9 through Table 11 with example component values for +5 V to ±15 V generation. Table 9 shows the components common to all of the V_{IN} and V_{OUT} conditions.

Table 9. Recommended Common Components Selections

REF	Value	Part Number	Manufacturer
C_{IN1}	10 µF	TMK316B7106KL-TD	Taiyo Yuden
C_{VREG}	1 µF	GRM188R71A105KA61D	Murata
C_{VREF}	1 µF	GRM188R71A105KA61D	Murata

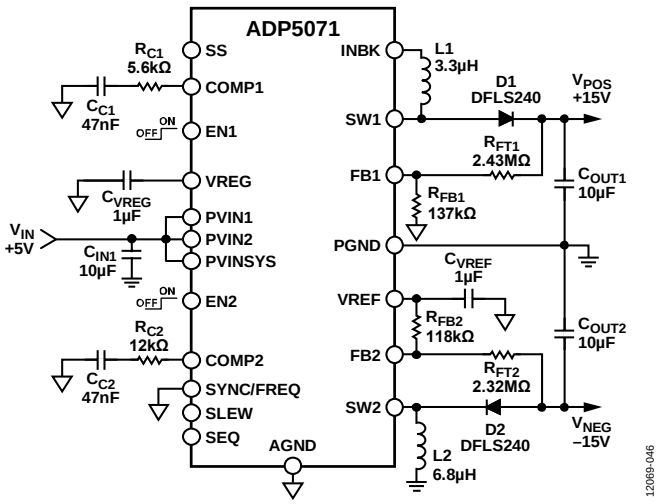


Figure 47. Typical +5 V to ±15 V Application

Table 10. Recommended Boost Regulator Components

V_{IN} (V)	V_{POS} (V)	Freq. (MHz)	L1 (µH)	L1 Manufacturer Part Number		C_{OUT1} (µF)	C_{OUT1}, Murata Part	D1, Diodes, Inc. Part	R_{FT1} (MΩ)	R_{FB1} (kΩ)	C_{C1} (nF)	R_{C1} (kΩ)
				Coilcraft®	Wurth Elektronik							
3.3	5	1.2	2.2	XAL4020-222ME_	74438356022	10	GRM32ER71H106KA12L	DFLS240L	0.604	115	47	4.7
3.3	5	2.4	1	XAL4020-102ME_	74438356010	10	GRM32ER71H106KA12L	DFLS240L	0.604	115	47	4.7
3.3	9	1.2	2.2	XAL4020-222ME_	74438356022	10	GRM32ER71H106KA12L	DFLS240	1.24	121	47	3.3
3.3	9	2.4	1.5	XAL4020-152ME_	74438356015	10	GRM32ER71H106KA12L	DFLS240	1.24	121	47	3.3
3.3	15	1.2	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	2.43	137	47	14
3.3	15	2.4	1.5	XAL4020-152ME_	74438356015	10	GRM32ER71H106KA12L	DFLS240	2.43	137	47	14
3.3	24	1.2	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	3.09	107	47	18
3.3	24	2.4	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	3.09	107	47	18
3.3	34	1.2	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	4.22	102	47	33
3.3	34	2.4	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	4.22	102	47	33
5	9	1.2	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	1.24	121	47	1.8
5	9	2.4	1.5	XAL4020-152ME_	74438356015	10	GRM32ER71H106KA12L	DFLS240	1.24	121	47	2.2
5	15	1.2	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	2.43	137	47	5.6
5	15	2.4	2.2	XAL4020-222ME_	74438356022	10	GRM32ER71H106KA12L	DFLS240	2.43	137	47	8.2
5	24	1.2	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	3.09	107	47	10
5	24	2.4	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	3.09	107	47	10
5	34	1.2	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	4.22	102	47	12
5	34	2.4	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	4.22	102	47	12
12	24	1.2	6.8	XAL4030-682ME_	74438357068	10	GRM32ER71H106KA12L	DFLS240	3.09	107	47	4.7
12	24	2.4	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	3.09	107	47	4.7

Table 11. Recommended Inverting Regulator Components

V_{IN} (V)	V_{NEG} (V)	Freq. (MHz)	L2 (µH)	L2, Manufacturer Part Number		C_{OUT2} (µF)	C_{OUT2}, Murata Part	D2, Diodes, Inc. Part	R_{FT2} (MΩ)	R_{FB2} (kΩ)	C_{C2} (nF)	R_{C2} (kΩ)
				Coilcraft	Wurth Elektronik							
3.3	−5	1.2	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240L	1.15	158	47	8.2
3.3	−5	2.4	2.2	XAL4020-222ME_	74438356022	10	GRM32ER71H106KA12L	DFLS240L	1.15	158	47	8.2
3.3	−9	1.2	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	1.62	133	47	10
3.3	−9	2.4	2.2	XAL4020-222ME_	74438356022	10	GRM32ER71H106KA12L	DFLS240	1.62	133	47	15
3.3	−15	1.2	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	2.32	118	47	18
3.3	−15	2.4	2.2	XAL4020-222ME_	74438356022	10	GRM32ER71H106KA12L	DFLS240	2.32	118	47	18
3.3	−24	1.2	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	3.16	102	47	39
3.3	−24	2.4	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	3.16	102	47	47
3.3	−34	1.2	6.8	XAL4030-682ME_	74438357068	10	GRM32ER71H106KA12L	DFLS240	4.99	115	47	33
3.3	−34	2.4	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	4.99	115	47	33
5	−9	1.2	6.8	XAL4030-682ME_	74438357068	10	GRM32ER71H106KA12L	DFLS240	1.62	133	47	5.6
5	−9	2.4	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	1.62	133	47	5.6
5	−15	1.2	6.8	XAL4030-682ME_	74438357068	10	GRM32ER71H106KA12L	DFLS240	2.32	118	68	12
5	−15	2.4	3.3	XAL4030-332ME_		10	GRM32ER71H106KA12L	DFLS240	2.32	118	47	12
5	−24	1.2	10	XAL4040-103ME_		10	GRM32ER71H106KA12L	DFLS240	3.16	102	47	27
5	−24	2.4	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	3.16	102	47	27
5	−34	1.2	10	XAL4040-103ME_		10	GRM32ER71H106KA12L	DFLS240	4.99	115	47	39
5	−34	2.4	4.7	XAL4030-472ME_	74438357047	10	GRM32ER71H106KA12L	DFLS240	4.99	115	47	39
12	−24	1.2	15	XAL4040-153ME_		10	GRM32ER71H106KA12L	DFLS240	3.16	102	47	15
12	−24	2.4	6.8	XAL4030-682ME_	74438357068	10	GRM32ER71H106KA12L	DFLS240	3.16	102	47	15

SUPER LOW NOISE WITH OPTIONAL LDOS

Low dropout regulators (LDOs) can be added to the ADP5071 output to provide super low noise supplies for high performance ADCs, digital-to-analog converters (DACs), and other precision applications.

Table 12 shows recommended companion devices, and Figure 48 shows a typical application schematic for ±15 V generation from a +5 V supply.

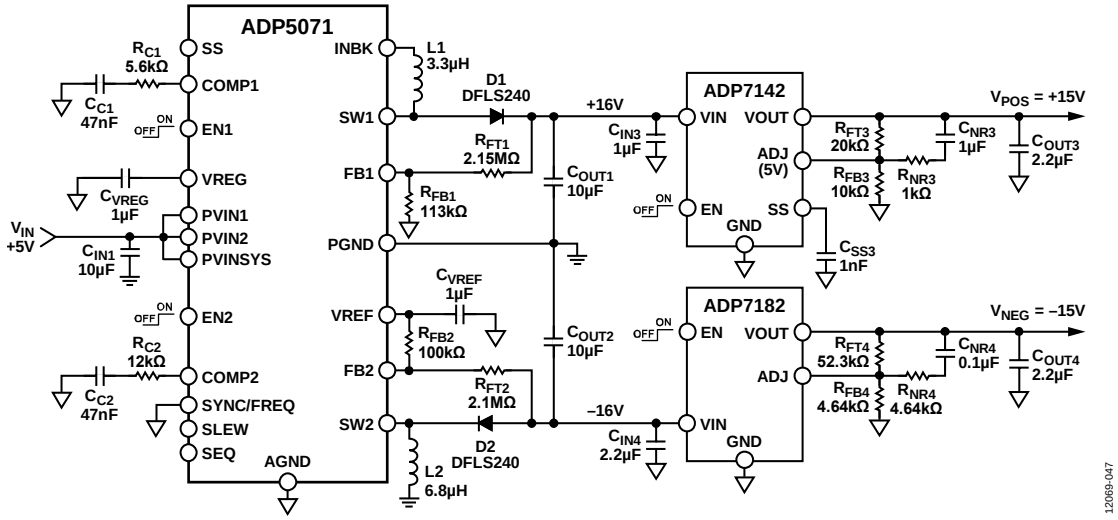


Figure 48. Super Low Noise ±15 V Generation with Post Regulation by the ADP7142 (+40 V, +200 mA, Low Noise LDO) and ADP7182 (–28 V, –200 mA, Low Noise LDO)

Table 12. Recommended LDOs for Super Low Noise Operation

Parameter	ADP7102	ADP7104	ADP7105	ADP7118	ADP7142	ADP7182
V_{IN} Range	3.3 V to 20 V	3.3 V to 20 V	3.3 V to 20 V	2.7 V to 20 V	2.7 V to 40 V	–2.7 V to –28 V
Fixed V_{OUT}	1.5 V to 9 V	1.5 V to 9 V	1.8 V, 3.3 V, 5 V	1.2 V to 5 V	1.2 V to 5 V	–1.8 V to –5 V
Adjustable V_{OUT}	1.22 V to 19 V	1.22 V to 19 V	1.22 V to 19 V	1.2 V to 19 V	1.2 V to 39 V	–1.22 V to–27 V
I_{OUT}	300 mA	500 mA	500 mA	200 mA	200 mA	–200 mA
I_Q at No Load	400 µA	400 µA	400 µA	50 µA	50 µA	–33 µA
I_{SHDN} Typical	40 µA	40 µA	40 µA	2 µA	2 µA	–2 µA
Soft Start	No	No	Yes	Yes	Yes	No
PGOOD	Yes	Yes	Yes	No	No	No
Noise (Fixed), 10 Hz to 100 kHz	15 µV rms	15 µV rms	15 µV rms	11 µV rms	11 µV rms	18 µV rms
PSRR (100 kHz)	60 dB	60 dB	60 dB	68 dB	68 dB	45 dB
PSRR (1 MHz)	40 dB	40 dB	40 dB	50 dB	50 dB	45 dB
Package	8-lead LFCSP, 8-lead SOIC	8-lead LFCSP, 8-lead SOIC	8-lead LFCSP, 8-lead SOIC	6-lead LFCSP, 8-lead SOIC, 5-lead TSOT	6-lead LFCSP, 8-lead SOIC, 5-lead TSOT	6-lead LFCSP, 8-lead LFCSP, 5-lead TSOT

SEPIC STEP-UP/STEP-DOWN OPERATION

SEPIC operation allows the positive output channel to produce a voltage higher or lower than V_{IN}. Both standalone and coupled inductors are supported for this application. SEPIC designs are supported in the ADIsimPower toolset.

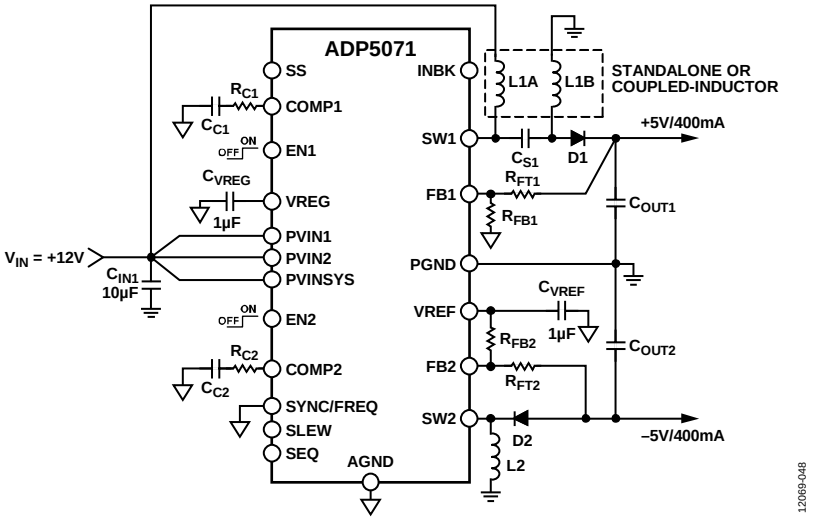


Figure 49. SEPIC Application for +12 V in to ±5 V Output Generation

LAYOUT CONSIDERATIONS

Layout is important for all switching regulators but is particularly important for regulators with high switching frequencies. To achieve high efficiency, good regulation, good stability, and low noise, a well-designed PCB layout is required. Follow these guidelines when designing PCBs:

- Keep the input bypass capacitor, C_{IN1}, close to the PVIN1 pin, the PVIN2 pin, and the PVINSYS pin. Route each of these pins individually to the pad of this capacitor to minimize noise coupling between the power inputs rather than connecting the three pins at the device. A separate capacitor can be used on the PVINSYS pin for the best noise performance.
- Keep the high current paths as short as possible. These paths include the connections between CIN1, L1, L2, D1, D2, COUT1, COUT2, and PGND and their connections to the ADP5071.
- Keep AGND and PGND separate on the top layer of the board. This separation avoids pollution of AGND with switching noise. Do not connect PGND to the EPAD on the top layer of the layout. Connect both AGND and PGND to the board ground plane with vias. Ideally, connect PGND to the plane at a point between the input and output capacitors. Connect the EPAD on its own to this ground layer with vias and connect AGND as near to the pin as possible between the CVREF and CVREG capacitors.
- Keep high current traces as short and wide as possible to minimize parasitic series inductance, which causes spiking and electromagnetic interference (EMI).
- Avoid routing high impedance traces near any node connected to the SW1 and SW2 pins or near Inductors L1and L2 to prevent radiated switching noise injection.
- Place the feedback resistors as close to the FB1 and FB2 pins as possible to prevent high frequency switching noise injection.
- Place the top of the upper feedback resistors, RFT1 and RFT2, or route traces to them from as close as possible to the top of COUT1 and COUT2 for optimum output voltage sensing.
- Place the compensation components as close as possible to COMP1 and COMP2. Do not share vias to the ground plane with the feedback resistors to avoid coupling high frequency noise into the sensitive COMP1 and COMP2 pins.
- Place the CVREF and CVREG capacitors as close to the VREG and VREF pins as possible. Ensure that short traces are used between VREF and R_{FB2}.

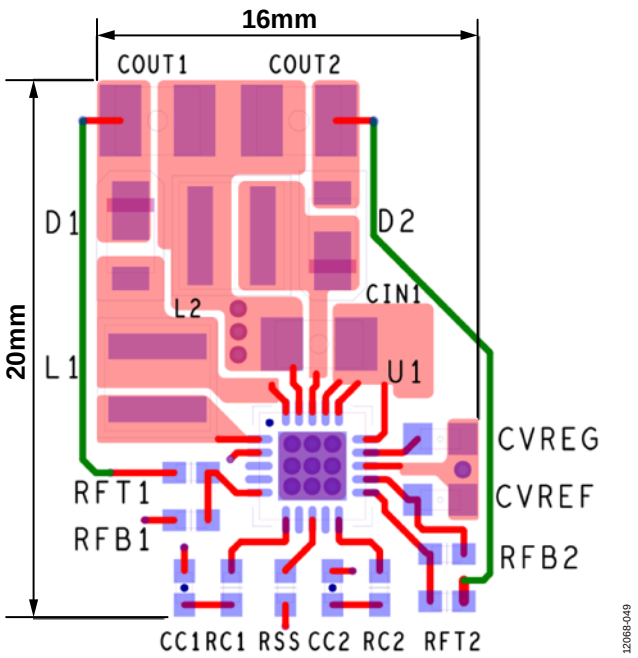


Figure 50. Suggested LFCSP Layout; Vias Connected to the PCB Ground Plane, Not to Scale

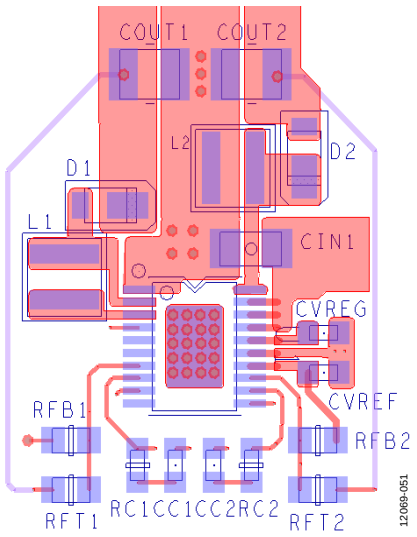
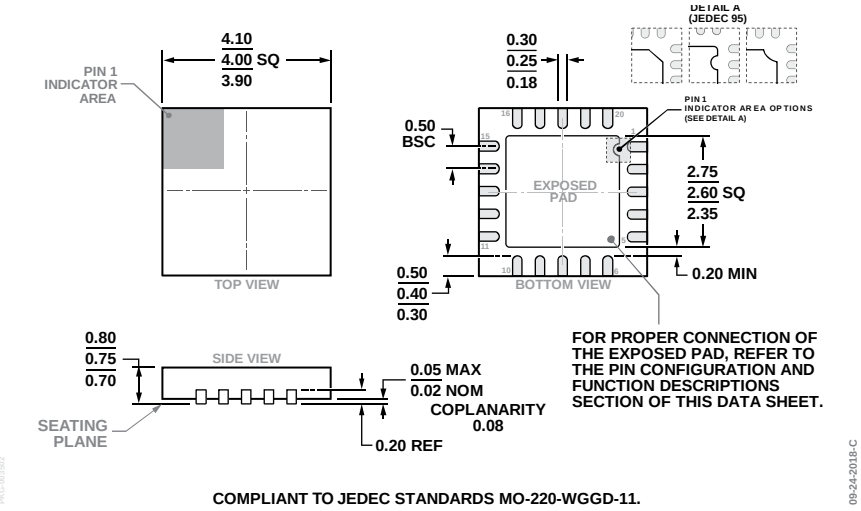


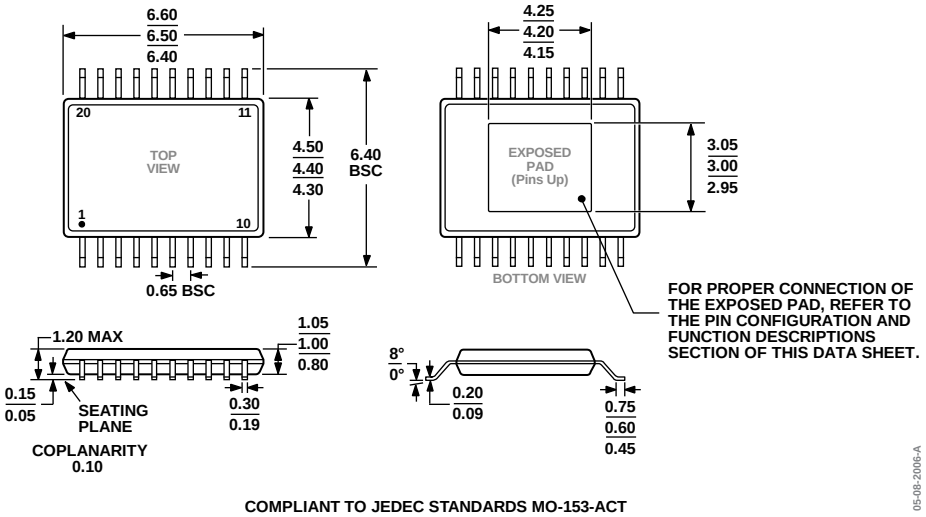
Figure 51. Suggested TSSOP Layout; Vias Connected to the PCB Ground Plane, Not to Scale

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-11.

Figure 52. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-20-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-ACT

Figure 53. 20-Lead Thin Shrink Small Outline With Exposed Pad [TSSOP_EP]
(RE-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5071ACPZ	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
ADP5071ACPZ-R7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP]	CP-20-8
ADP5071AREZ	−40°C to +125°C	20-Lead Thin Shrink Small Outline With Exposed Pad [TSSOP_EP]	RE-20-1
ADP5071AREZ-R7	−40°C to +125°C	20-Lead Thin Shrink Small Outline With Exposed Pad [TSSOP_EP]	RE-20-1
ADP5071CP-EVALZ		Evaluation Board for the LFCSP	
ADP5071RE-EVALZ		Evaluation Board for the TSSOP_EP	

[1] Z = RoHS Compliant Part.