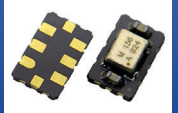


# Jitter Optimized, Factory Programmable $\pm 3$ ppm TCXO



ASGTX5 Series



ESD Sensitive



5.0 x 3.2 x 1.5 mm  
RoHS/RoHS II Compliant  
MSL = 1

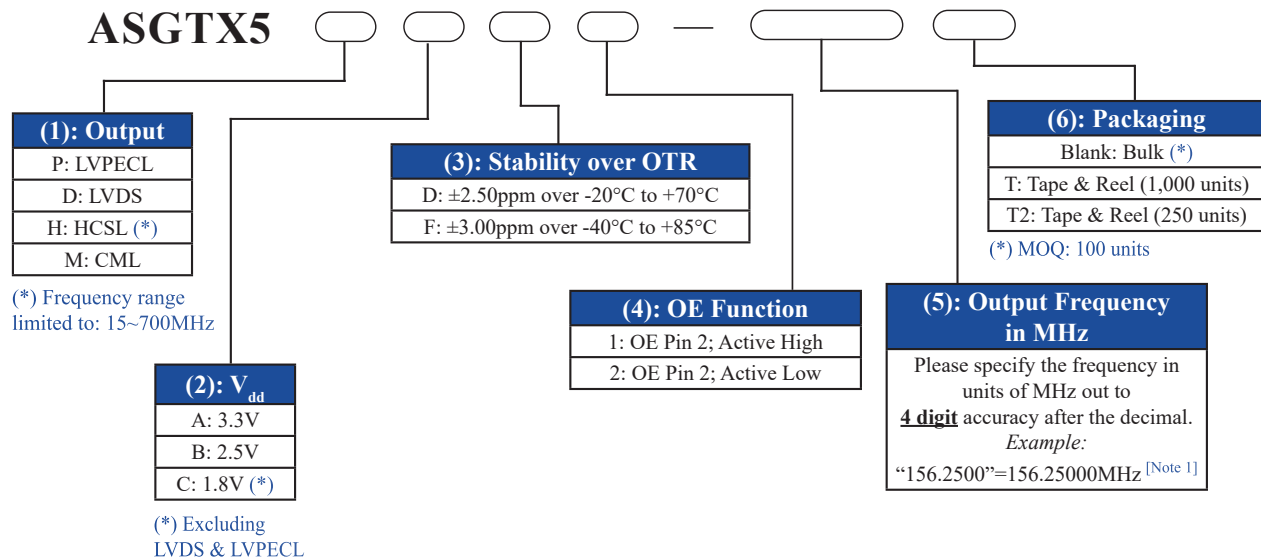
## Features

- Ultra-Low Jitter: 332 fs Typ RMS @ 156.25MHz
- Available with any frequency from 15MHz to 2,100MHz
- Factory programmable; samples available within 1-2 weeks
- Lowest in-class power consumption (75mA Typ LVDS)
- $\pm 3.0$ ppm stability over  $-40$  to  $+85^\circ\text{C}$
- 3.3V, 2.5V, 1.8V  $V_{dd}$  supply voltage
- LVPECL, LVDS, HCSL, & CML differential output options
- Industry standard 5.0 x 3.2mm footprint
- Meets Stratum-IV requirement of  $< \pm 25$ ppm All Inclusive Frequency Stability over product life

## Applications

- Networking & communications
- 10G/40G/100G optical Ethernet
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement

## Options and Part Identification [Note 1]



### Part Number Example:

**ASGTX5PAD1-156.2500T2**

Note 1: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.

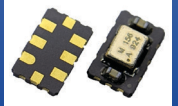


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## Electrical Characteristics

Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range	LVPECL	15		2,100	MHz	Option "P"
	LVDS	15		2,100		Option "D"
	HCSL	15		700		Option "H"
	CML	15		2,100		Option "M"
Supply Voltage ( $V_{dd}$ ) [Note 2]		2.97	3.30	3.63	V	Option "A"
		2.25	2.50	2.75		Option "B"
		1.71	1.80	1.89		Option "C"
Supply Current ( $I_{dd}$ )	LVPECL		100	120	mA	Max @ 2,100MHz; 3.3V
	LVDS		75	90		Max @ 2,100MHz; 3.3V
	HCSL		80	100		Max @ 700MHz; 3.3V
	CML		70	85		Max @ 2,100MHz; 3.3V
Operating Temperature Range		-20		+70	°C	Option "D"
		-40		+85		Option "F"
Storage Temperature		-55		+150	°C	
Frequency Accuracy (Initial Set-Tolerance) [Note 3] at time of shipment (Pre-Reflow) @ +25°C $\pm 3$ °C		-1.00		+1.00	ppm	Relative to carrier
Shift through Reflow Soldering		-1.00		+1.00	ppm	Relative to initial tolerance
Frequency Stability over Operating Temperature Range, relative to post reflow stabilized frequency		-2.5	< $\pm 1.00$	+2.5	ppm	Over -20°C to +70°C
		-3.0	< $\pm 2.00$	+3.0		Over -40°C to +85°C
Aging over first year @ +25°C $\pm 3$ °C		-1.00		+1.00	ppm	
Aging over 20 Year Product Life [Note 4]		-7.00		+7.00	ppm	
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life [Note 4 & 5]		-11.50		+11.50	ppm	Over -20°C to +70°C
		-12.50		+12.50		Over -40°C to +85°C
Rise (Tr) / Fall (Tf) Time (20% to 80% $V_{peak\ to\ peak}$ )				400	ps	
Duty Cycle		45		55	%	@ 50% $V_{dd}$
Powerup Time			< 5.0	10	ms	
Output Enable & Disable Control		0.7*( $V_{dd}$ )			V	Output Enable; or No Connect
				0.3*( $V_{dd}$ )		Output Disable; High Impedance
Output Enable Time				2.50	ms	70% of $V_{dd}$ (min.) to enable output
Output Disable Time				10	$\mu$ s	30% of $V_{dd}$ (max) to disable output

Note 2: Supply Voltage ( $V_{dd}$ ) = 1.8V option not available with LVPECL output

Note 3: Excludes carrier frequencies 122.88MHz, 491.52MHz, 368.4MHz, 614.4MHz, 737.28MHz, 860.16MHz, 983.04MHz, & 1105.92MHz.  
The Frequency Accuracy (Initial Set-Tolerance) at time of shipment (Pre-Reflow) for the above carrier frequencies =  $\pm 10$ ppm MAX.

Note 4: Relative to post reflow measured frequency @ +25°C  $\pm 3$ °C

Note 5: Includes temperature accuracy, shift through reflow, stability over operating temperature, load pulling, frequency pushing and aging over 20 years

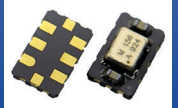


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MSL = 1

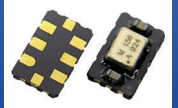
## Electrical Specifications Cont.

Parameters		Min.	Typ.	Max.	Unit	Notes	
Output Disable Current Consumption	LVPECL		99		mA	Max @ 2,100MHz; 3.3V	
	LVDS		74			Max @ 2,100MHz; 3.3V	
	HCSL		79			Max @ 700MHz; 3.3V	
	CML		69			Max @ 2,100MHz; 3.3V	
Output High Voltage ( $V_{OH}$ ) Output Low Voltage ( $V_{OL}$ )	LVPECL	$V_{OH}$	$V_{dd}-1.03$		V	50 $\Omega$ to $V_{dd}-2.0V$ or Thevenin equivalent	
		$V_{OL}$	$V_{dd}-1.85$				$V_{dd}-1.6$
	LVDS	$V_{OH}$		1.4		1.6	100 $\Omega$ between OUT-P and OUT-N
		$V_{OL}$	0.9	1.1			
	HCSL	$V_{OH}$	0.66			1.15	50 $\Omega$ to GND
		$V_{OL}$	0.0			0.15	
	CML	$V_{OH}$	$V_{dd}-0.085$			$V_{dd}$	50 $\Omega$ to $V_{dd}$
		$V_{OL}$	$V_{dd}-0.6$			$V_{dd}-0.32$	

## RMS Phase Jitter (12kHz -20MHz BW) | $V_{dd} = 3.3V$

Carrier F0 (MHz)	Min.	Typ.	Max.	Unit	Notes
15.00 to 50.00		< 500		fsec	All Differential Outputs: LVPECL, LVDS, HCSL & CML
51.00 to 1,200		< 350		fsec	
1,201 to 2,100		< 225		fsec	

# Jitter Optimized, Factory Programmable $\pm 3\text{ppm}$ TCXO



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MSL = 1

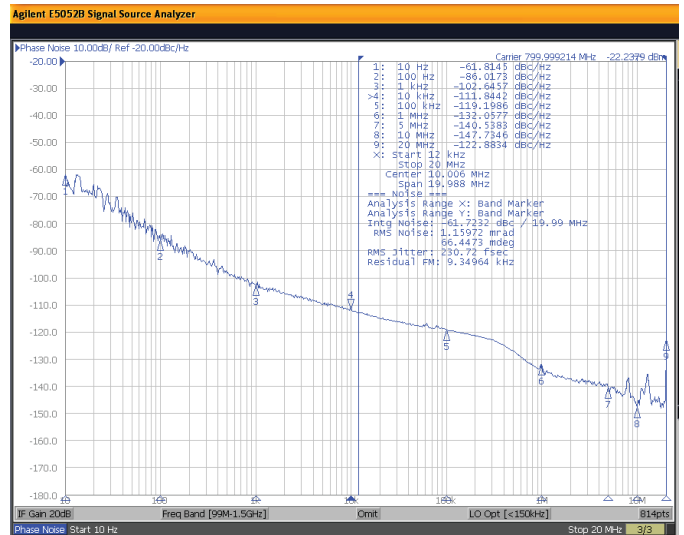
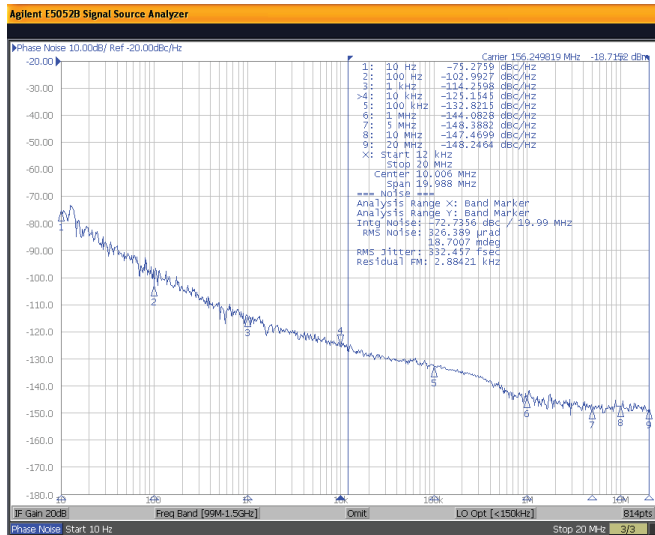
## Phase Noise Test Setup

- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = NOT Omitted (Normalized in dBc/Hz)
- Specified Spur Omission Function = NOT Enabled
- IF Gain = 20dB
- Correlation = 5dB
- Average = 3

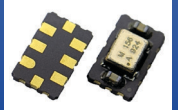
## Representative Phase Noise Plots

$F_0=156.2500\text{MHz}$  |  $V_{dd}=3.3\text{V}$  | LVPECL  
RMS Phase Jitter = 332 fsec

$F=800.0000\text{MHz}$  |  $V_{dd}=3.3\text{V}$  | LVPECL  
RMS Phase Jitter = 231 fsec



# Jitter Optimized, Factory Programmable $\pm 3\text{ppm}$ TCXO



ASGTX5 Series



ESD Sensitive

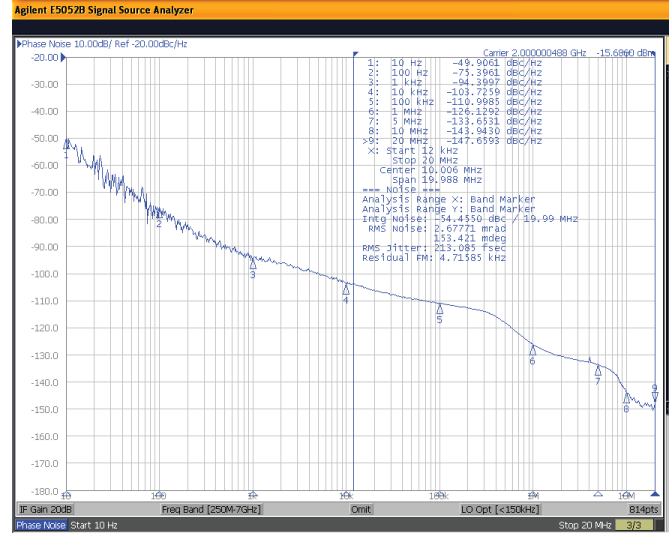
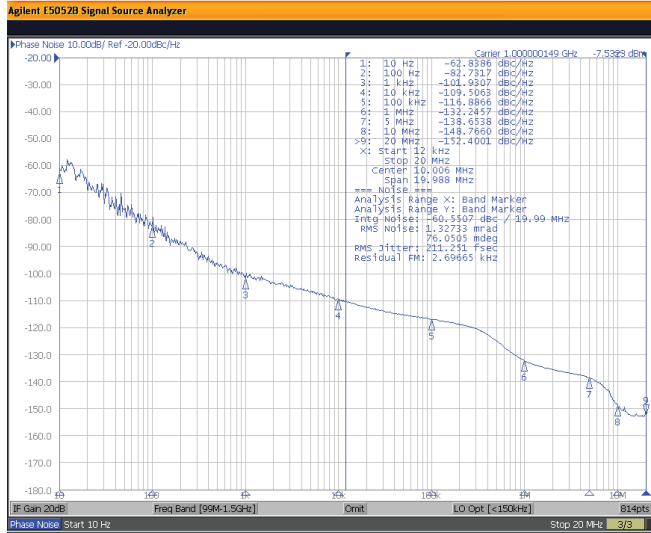


5.0 x 3.2 x 1.5 mm  
RoHS/RoHS II Compliant  
MSL = 1

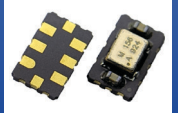
## Representative Phase Noise Plots

**F0=1.0000GHz,  $V_{dd}=3.3\text{V}$ , LVPECL**  
RMS Phase Jitter = 211 fsec

**F0=2.0000GHz,  $V_{dd}=3.3\text{V}$ , LVPECL**  
RMS Phase Jitter = 213 fsec



# Jitter Optimized, Factory Programmable $\pm 3$ ppm TCXO



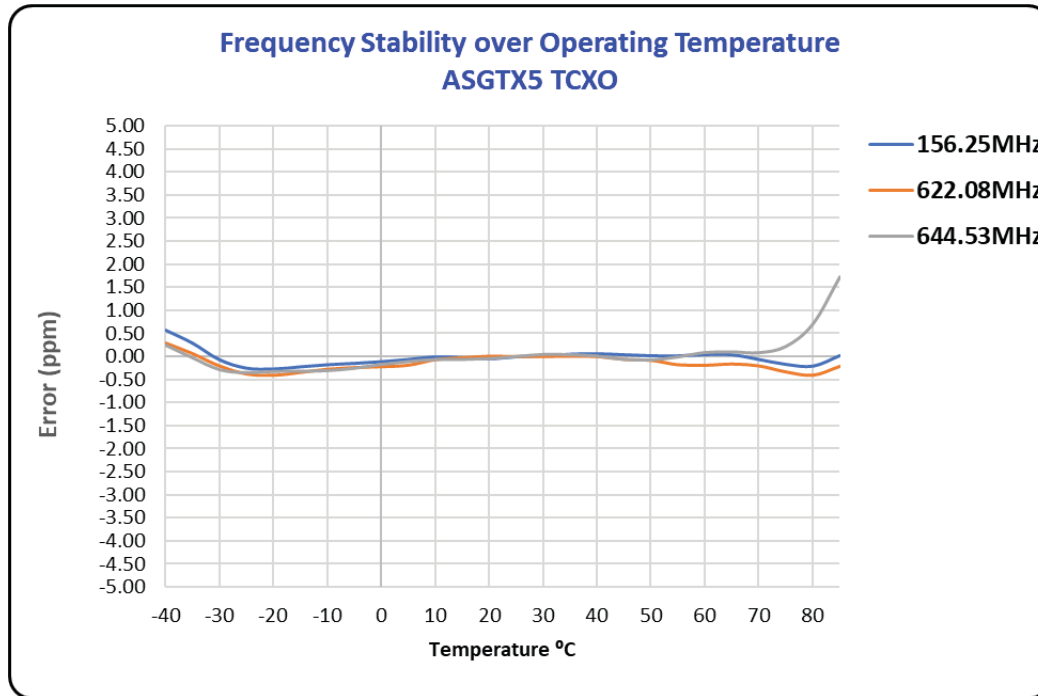
ASGTX5 Series



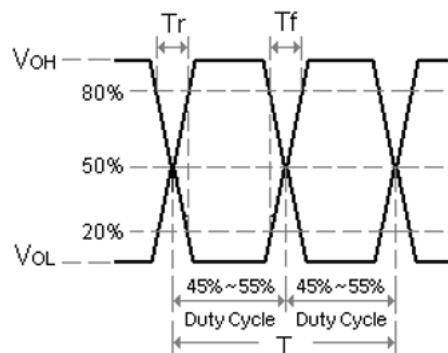
ESD Sensitive

5.0 x 3.2 x 1.5 mm  
RoHS/RoHS II Compliant  
MSL = 1

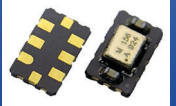
## Typical Frequency vs. Temperature Characteristics



## Differential Output Waveform



# Jitter Optimized, Factory Programmable $\pm 3\text{ppm}$ TCXO



ASGTX5 Series

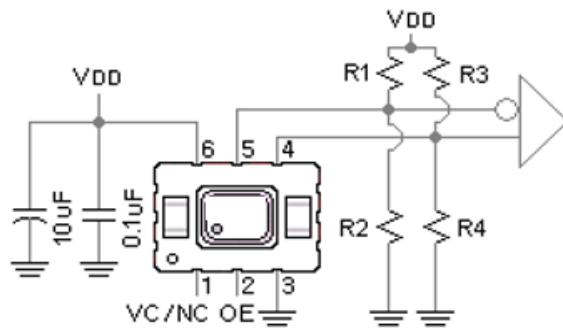


ESD Sensitive

5.0 x 3.2 x 1.5 mm  
RoHS/RoHS II Compliant  
MSL = 1

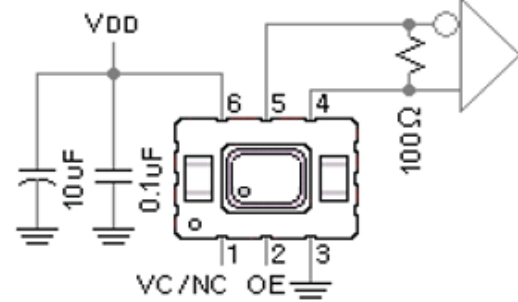
## Recommended Test Circuit

### LVPECL

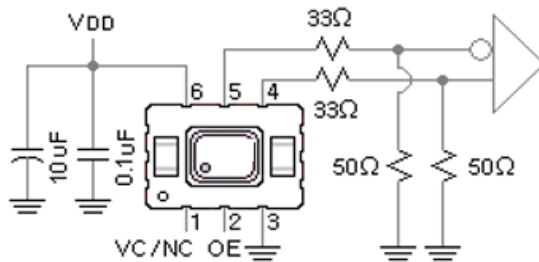


$V_{dd}=3.3\text{V}$ :  $R1=R3=127\Omega$ ;  $R2=R4=82.5\Omega$   
 $V_{dd}=2.5\text{V}$ :  $R1=R3=250\Omega$ ;  $R2=R4=62.5\Omega$

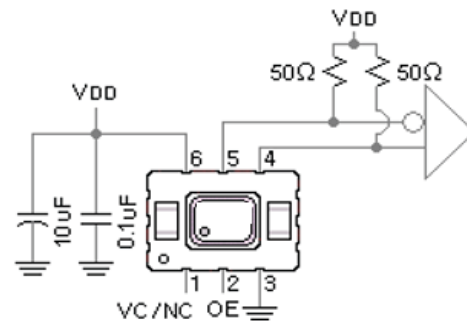
### LVDS



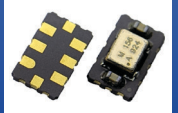
### HCSL



### CML



# Jitter Optimized, Factory Programmable $\pm 3\text{ppm}$ TCXO



ASGTX5 Series

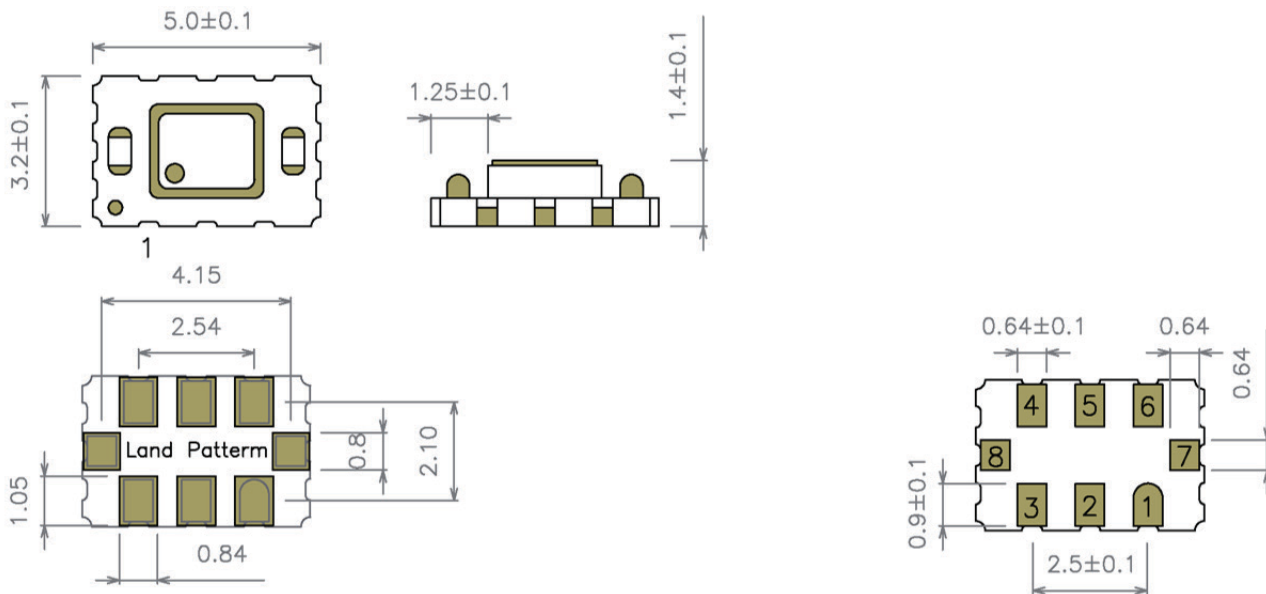


ESD Sensitive



5.0 x 3.2 x 1.5 mm  
RoHS/RoHS II Compliant  
MSL = 1

## Mechanical Dimensions



Pin #	Function
# 1	No Connect (NC) {TCXO Configuration}
# 2	Output Enable / Disable (OE)
# 3	Ground
# 4	RF Output (Q)
# 5	RF Output Complimentary (Q')
# 6	Supply Voltage ( $V_{dd}$ )
# 7	Do Not Connect (leave floating)
# 8	Do Not Connect (leave floating)

Option	OE pin functionality (Pin#2)
1	Output Enable Active HIGH
2	Output Enable Active LOW

Dimensions: inches [mm]



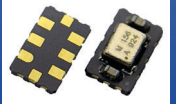
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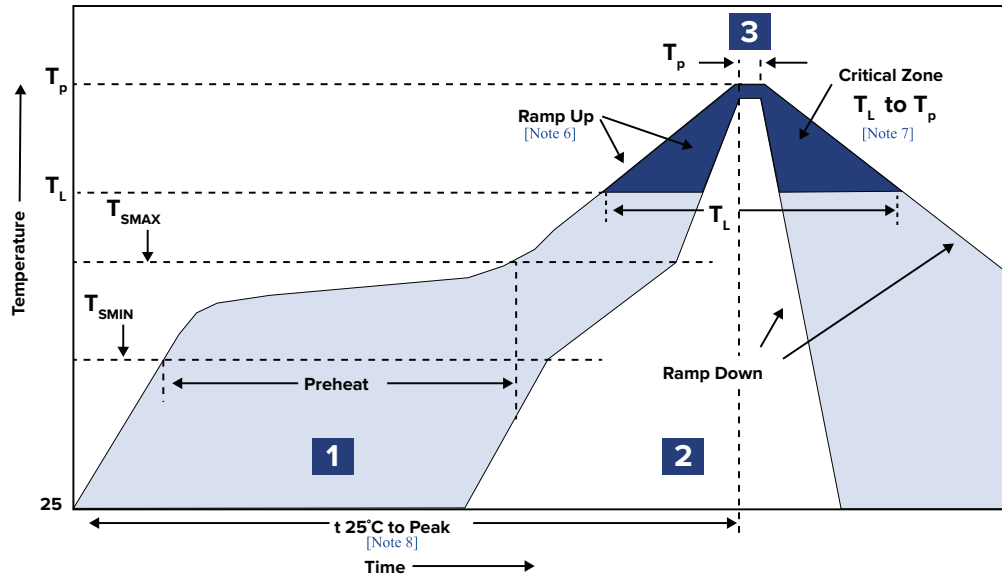
ASGTX5 Series



ESD Sensitive

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MSL = 1

## Recommended Reflow Profile [Note 9]



Zone	Description	Temperature	Time
1	Preheat / Soak	$T_{SMIN} \sim T_{SMAX}$ $150^\circ\text{C} \sim 200^\circ\text{C}$	60 ~ 180 sec.
2	Reflow	$T_L$ $217^\circ\text{C}$	60 ~ 150 sec.
3	Peak heat	$T_P$ $260^\circ\text{C} \pm 5^\circ\text{C}$	20 ~ 40 sec.

Note 6: Ramp Up Rate ( $T_L \rightarrow T_P$ ) =  $3^\circ\text{C} / \text{sec. MAX}$

Note 7: Ramp Down Rate ( $T_P \rightarrow T_L$ ) =  $6^\circ\text{C} / \text{sec. MAX}$

Note 8: Time 25°C to Peak Temperature ( $25^\circ\text{C} \rightarrow T_P$ ) = 8 minutes MAX

Note 9: Can withstand 2 times reflow

All temperatures refer to topside of the package, measured on the package body surface below.

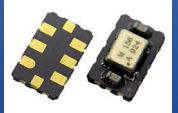


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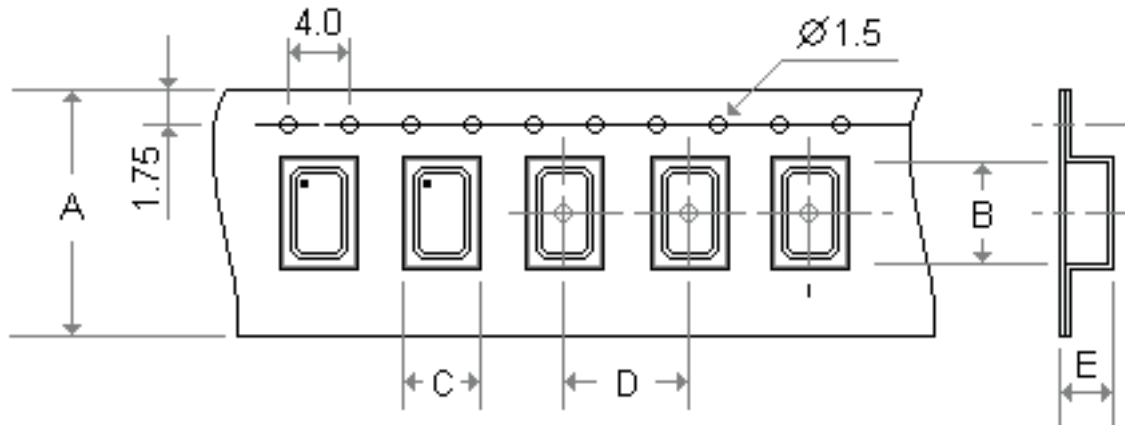
## Packaging

Blank = Bulk (MOQ: 100 units)

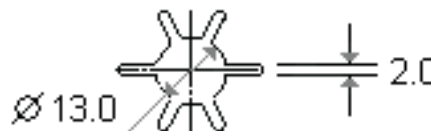
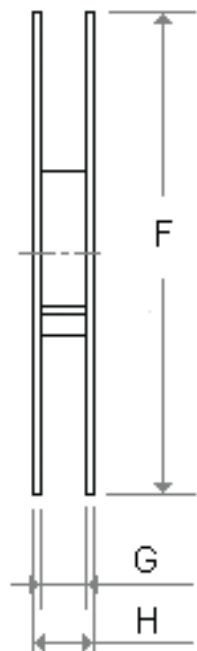
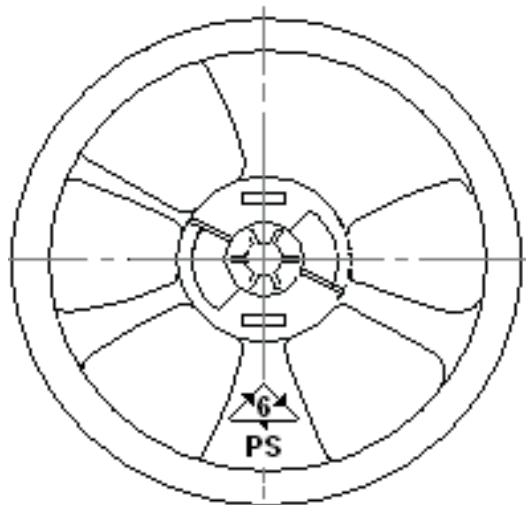
T = Tape & Reel (1000 units/reel)

T2 = Tape & Reel (250 units/reel)

Feeding (PULL) Direction →



Tape Dimensions	
A	12.0
B	5.3
C	3.6
D	8.0
E	1.4
Reel Dimensions	
F	180.0
G	13.0
H	16.0



Dimensions: mm

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