XA2C256 CoolRunner-II Automotive CPLD

DS555 (v1.2) June 22, 2009

Product Specification

Features

- AEC-Q100 device qualification and full PPAP support available in both I-grade and extended temperature Q-grade
- Guaranteed to meet full electrical specifications over T_A = –40°C to +105°C with T_J Maximum = +125°C (Q-grade)
- Optimized for 1.8V systems
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis. Refer to the CoolRunner™-II family data sheet for architecture description.
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
  - 100-pin VQFP with 80 user I/O
  - 144-pin TQFP with 118 user I/O
  - Pb-free only for all packages
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt-trigger input (per pin)
  - Unsurpassed low power management
    - DataGATE enable (DGE) signal control
  - Two separate I/O banks
  - RealDigital 100% CMOS product term generation
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (divide by 2, 4, 6, 8, 10, 12, 14, 16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Advanced design security
  - PLA architecture
    - Superior pinout retention
    - 100% product term routability across function block
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pull-up on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
  - Hot pluggable

  WARNING: Programming temperature range of T_A = 0°C to +70°C.

Description

The CoolRunner-II Automotive 256-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved.

This device consists of sixteen Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt-trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as "direct input" registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchronous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

Circuitry has also been included to divide one externally supplied global clock (GCK2) by eight different selections. This yields divide by even and odd clock frequencies.

The use of the clock divide (division by 2) and DualEDGE flip-flop gives the resultant CoolCLOCK feature.

DataGATE is a method to selectively disable inputs of the CPLD that are not of interest during certain points in time. By mapping a signal to the DataGATE function, lower power can be achieved due to reduction in signal switching.

Another feature that eases voltage translation is I/O banking. Two I/O banks are available on the CoolRunner-II Automotive 256-macrocell device that permit easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II Automotive 256-macrocell CPLD is I/O compatible with various I/O standards (see Table 1). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

RealDigital Design Technology

Xilinx® CoolRunner-II Automotive CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II Automotive CPLDs employ RealDigital, a design technique that makes use of CMOS technology in both the fabrication and design methodology. RealDigital design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II Automotive CPLDs achieve both high-performance and low power operation.

Supported I/O Standards

The CoolRunner-II Automotive 256-macrocell device features LVCMOS and LVTTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general-purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. CoolRunner-II Automotive CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: **I/O Standards for XA2C256**

IOSTANDARD Attribute	Output V_{CCIO}	Input V_{CCIO}
LVTTL	3.3	3.3
LVCMOS33	3.3	3.3
LVCMOS25	2.5	2.5
LVCMOS18	1.8	1.8
LVCMOS15 (1)	1.5	1.5

(1) LVCMOS15 requires Schmitt-trigger inputs.

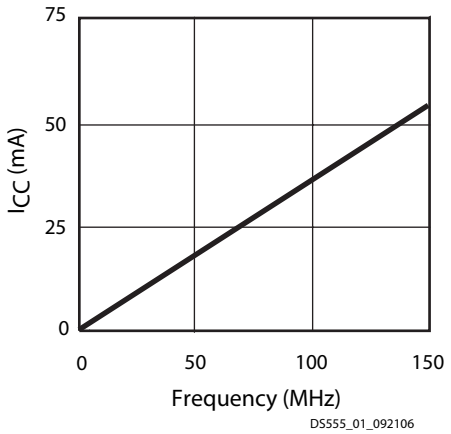


Figure 1: **I_{CC} vs Frequency**

Table 2: **I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)(1)**

	Frequency (MHz)						
	0	30	50	70	100	120	150
Typical I_{CC} (mA)	0.021	11.68	19.40	27.01	38.18	45.54	56.32

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block).

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to ground	–0.5 to 2.0	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 4.0	V
V_{JTAG}(2)	JTAG input voltage limits	–0.5 to 4.0	V
V_{CCAUX}	JTAG input supply voltage	–0.5 to 4.0	V
V_{IN}(1)	Input voltage relative to ground	–0.5 to 4.0	V
V_{TS}(1)	Voltage applied to 3-state output	–0.5 to 4.0	V
T_{STG}(3)	Storage Temperature (ambient)	–65 to +150	°C
T_J	Junction Temperature	+125	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to –2.0v or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Valid over commercial temperature range.
3. For soldering guidelines and thermal considerations, see the Device Package User Guide. For Pb-free packages, see XAPP427.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply voltage for internal logic and input buffers	Industrial T_A = –40°C to +85°C	1.7	1.9	V
		Q-Grade T_A = –40°C to +105°C T_J Maximum = +125°C	1.7	1.9	V
V_{CCIO}	Supply voltage for output drivers @ 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers @ 2.5V operation		2.3	2.7	V
	Supply voltage for output drivers @ 1.8V operation		1.7	1.9	V
	Supply voltage for output drivers @ 1.5V operation		1.4	1.6	V
V_{CCAUX}	JTAG programming		1.7	3.6	V

DC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Typical	Max.	Units
I_{CCSB}	Standby current Industrial	V_{CC} = 1.9V, V_{CCIO} = 3.6V	54	300	µA
I_{CCSB}	Standby current Q-grade	V_{CC} = 1.9V, V_{CCIO} = 3.6V	54	2.5	mA
I_{CC}	Dynamic current	f = 1 MHz	-	3.0	mA
		f = 50 MHz	-	30	mA
C_{JTAG}	JTAG input capacitance	f = 1 MHz	-	10	pF
C_{CLK}	Global clock input capacitance	f = 1 MHz	-	12	pF
C_{IO}	I/O capacitance	f = 1 MHz	-	10	pF
I_{IL}(2)	Input leakage current	V_{IN} = 0V or V_{CCIO} to 3.9V	-	±10	µA
I_{IH}(2)	I/O High-Z leakage	V_{IN} = 0V or V_{CCIO} to 3.9V	-	±10	µA

Notes:
1. 16-bit up/down, resettable binary counter (one counter per function block) tested at V_{CC}= V_{CCIO} = 1.9V

LVCMOS 3.3V and LVTTL 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	3.0	3.6	V
V_{IH}	High level input voltage	-	2	3.9	V
V_{IL}	Low level input voltage	-	–0.3	0.8	V
V_{OH}	High level output voltage, Industrial grade	I_{OH} = –8 mA, V_{CCIO} = 3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 3V	V_{CCIO} – 0.2V	-	V
	High level output voltage, Q-grade	I_{OH} = –4 mA, V_{CCIO} = 3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 3V	V_{CCIO} – 0.2V	-	V
V_{OL}	High level output voltage, Industrial grade	I_{OL} = 8 mA, V_{CCIO} = 3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 3V	-	0.2	V
	High level output voltage, Q-grade	I_{OL} = 4 mA, V_{CCIO} = 3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 3V	-	0.2	V

LVCMOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	2.3	2.7	V
V_{IH}	High level input voltage	-	1.7	V_{CCIO} + 0.3(1)	V
V_{IL}	Low level input voltage	-	–0.3	0.7	V
V_{OH}	High level output voltage, Industrial grade	I_{OH} = –8 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.2V	-	V
	High level output voltage, Q-grade	I_{OH} = –4 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.4V	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 2.3V	V_{CCIO} – 0.2V	-	V
V_{OL}	High level output voltage, Industrial grade	I_{OL} = 8 mA, V_{CCIO} = 2.3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 2.3V	-	0.2	V
	High level output voltage, Q-grade	I_{OL} = 4 mA, V_{CCIO} = 2.3V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 2.3V	-	0.2	V

1. The V_{IH} Max value represents the JEDEC specification for LVCMOS25. The CoolRunner-II input buffer can tolerate up to 3.9V without physical damage.

LVCMOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	1.7	1.9	V
V_{IH}	High level input voltage	-	0.65 x V_{CCIO}	V_{CCIO} + 0.3(1)	V
V_{IL}	Low level input voltage	-	–0.3	0.35 x V_{CCIO}	V
V_{OH}	High level output voltage, Industrial grade	I_{OH} = –8 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.2	-	V
	High level output voltage, Q-grade	I_{OH} = –4 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.7V	V_{CCIO} – 0.2	-	V

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OL}	High level output voltage, Industrial grade	I_{OL} = 8 mA, V_{CCIO} = 1.7V	-	0.45	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.7V	-	0.2	V
	High level output voltage, Q-grade	I_{OL} = 4 mA, V_{CCIO} = 1.7V	-	0.45	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.7V	-	0.2	V

1. The V_{IH} Max value represents the JEDEC specification for LVCMOS18. The CoolRunner-II input buffer can tolerate up to 3.9V without physical damage.

LVCMOS 1.5V DC Voltage Specifications(1)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	1.4	1.6	V
V_{T+}	Input hysteresis threshold voltage	-	0.5 x V_{CCIO}	0.8 x V_{CCIO}	V
V_{T-}		-	0.2 x V_{CCIO}	0.5 x V_{CCIO}	V
V_{OH}	High level output voltage, Industrial grade	I_{OH} = –8 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.2	-	V
	High level output voltage, Q-grade	I_{OH} = –4 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.45	-	V
		I_{OH} = –0.1 mA, V_{CCIO} = 1.4V	V_{CCIO} – 0.2	-	V
V_{OL}	High level output voltage, Industrial grade	I_{OL} = 8 mA, V_{CCIO} = 1.4V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.4V	-	0.2	V
	High level output voltage, Q-grade	I_{OL} = 4 mA, V_{CCIO} = 1.4V	-	0.4	V
		I_{OL} = 0.1 mA, V_{CCIO} = 1.4V	-	0.2	V

Notes:
1. Hysteresis used on 1.5V inputs.

Schmitt Trigger Input DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{CCIO}	Input source voltage	-	1.4	3.9	V
V_{T+}	Input hysteresis threshold voltage	-	0.5 x V_{CCIO}	0.8 x V_{CCIO}	V
V_{T-}		-	0.2 x V_{CCIO}	0.5 x V_{CCIO}	V

AC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	-7		-8		Units
		Min.	Max.	Min.	Max.	
T_{PD1}	Propagation delay single p-term	-	7.0	-	7.0	ns
T_{PD2}	Propagation delay OR array	-	7.5	-	7.5	ns
T_{SUD}	Direct input register clock setup time	3.0	-	3.0	-	ns
T_{SU1}	Setup time (single p-term)	2.8	-	3.4	-	ns
T_{SU2}	Setup time (OR array)	3.3	-	3.9	-	ns
T_{HD}	Direct input register hold time	0	-	0.4	-	ns
T_H	P-term hold time	0	-	0.4	-	ns
T_{CO}	Clock to output	-	6.0	-	6.0	ns

Symbol	Parameter	-7		-8		Units
		Min.	Max.	Min.	Max.	
F_{TOGGLE}(1)	Internal toggle rate	-	300	-	300	MHz
$F_{SYSTEM1}$(2)	Maximum system frequency	-	152	-	139	MHz
$F_{SYSTEM2}$(2)	Maximum system frequency	-	141	-	130	MHz
F_{EXT1}(3)	Maximum external frequency	-	114	-	106	MHz
F_{EXT2}(3)	Maximum external frequency	-	108	-	101	MHz
T_{PSUD}	Direct input register p-term clock setup time	1.7	-	2.0	-	ns
T_{PSU1}	P-term clock setup time (single p-term)	1.5	-	1.9	-	ns
T_{PSU2}	P-term clock setup time (OR array)	2.0	-	2.4	-	ns
T_{PHD}	Direct input register p-term clock hold time	1.2	-	1.8	-	ns
T_{PH}	P-term clock hold	1.0	-	1.3	-	ns
T_{PCO}	P-term clock to output	-	7.3		8.4	ns
T_{OE}/T_{OD}	Global OE to output enable/disable	-	7.0	-	7.0	ns
T_{POE}/T_{POD}	P-term OE to output enable/disable	-	8.0	-	9.1	ns
T_{MOE}/T_{MOD}	Macrocell driven OE to output enable/disable	-	9.9	-	9.9	ns
T_{PAO}	P-term set/reset to output valid	-	8.1	-	8.6	ns
T_{AO}	Global set/reset to output valid	-	7.6	-	7.6	ns
T_{SUEC}	Register clock enable setup time	3.1	-	3.5	-	ns
T_{HEC}	Register clock enable hold time	0.0	-	0.0	-	ns
T_{CW}	Global clock pulse width High or Low	1.6	-	1.6	-	ns
T_{PCW}	P-term pulse width High or Low	7.5	-	7.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	7.5	-	7.5	-	ns
T_{DGSU}	Set-up before DataGATE latch assertion	0.0	-	0.0	-	ns
T_{DGH}	Hold to DataGATE latch assertion	6.0	-	6.0	-	ns
T_{DGR}	DataGATE recovery to new data	-	9.0	-	9.3	ns
T_{DGW}	DataGATE low pulse width	3.5	-	3.5	-	ns
T_{CDRSU}	CDRST setup time before falling edge GCLK2	2.0	-	2.0	-	ns
T_{CDRH}	Hold time CDRST after falling edge GCLK2	0.0	-	0.0	-	ns
T_{CONFIG}(4)	Configuration time	-	150	-	150	µs

Notes:

1. F_{TOGGLE} is the maximum clock frequency to which a T flip-flop can reliably toggle (see the CoolRunner-II Automotive CPLD family data sheet for more information).
2. $F_{SYSTEM1}$ ($1/T_{CYCLE}$) is the internal operating frequency for a device fully populated with one 16-bit counter through one p-term per macrocell while $F_{SYSTEM2}$ is through the OR array.
3. F_{EXT1} ($1/T_{SU1}+T_{CO}$) is the maximum external frequency using one p-term while F_{EXT2} is through the OR array.
4. Typical configuration current during T_{CONFIG} is approximately 7.7 mA.

Internal Timing Parameters

Symbol	Parameter[2]	-7		-8		Units
		Min.	Max.	Min.	Max.	
Buffer Delays						
T_{IN}	Input buffer delay	-	2.6	-	2.6	ns
T_{DIN}	Direct data register input delay	-	3.9	-	3.3	ns
T_{GCK}	Global Clock buffer delay	-	2.7	-	2.7	ns
T_{GSR}	Global set/reset buffer delay	-	3.5	-	4.1	ns
T_{GTS}	Global 3-state buffer delay	-	3.0	-	3.0	ns
T_{OUT}	Output buffer delay	-	2.6	-	2.6	ns
T_{EN}	Output buffer enable/disable delay	-	4.0	-	4.0	ns
P-term Delays						
T_{CT}	Control term delay	-	1.4	-	2.5	ns
T_{LOGI1}	Single P-term delay adder	-	1.1	-	1.1	ns
T_{LOGI2}	Multiple P-term delay adder	-	0.5	-	0.5	ns
Macrocell Delay						
T_{PDI}	Input to output valid	-	0.7	-	0.7	ns
T_{LDI}	Setup before clock (transparent latch)	-	2.5	-	2.5	ns
T_{SUI}	Setup before clock	1.8	-	2.4	-	ns
T_{HI}	Hold after clock	0.0	-	0.0	-	ns
T_{ECSU}	Enable clock setup time	1.8	-	1.1	-	ns
T_{ECHO}	Enable clock hold time	0.0	-	0.0	-	ns
T_{COI}	Clock to output valid	-	0.7	-	0.7	ns
T_{AOI}	Set/reset to output valid	-	1.5	-	0.9	ns
Feedback Delays						
T_{F}	Feedback delay	-	3.0	-	3.0	ns
T_{OEM}	Macrocell to global OE delay	-	2.5	-	2.5	ns
I/O Standard Time Adder Delays 1.5V CMOS						
T_{HYS15}	Hysteresis input adder	-	4.0	-	4.0	ns
T_{OUT15}	Output adder	-	1.0	-	1.0	ns
T_{SLEW15}	Output slew rate adder	-	5.0	-	5.0	ns
I/O Standard Time Adder Delays 1.8V CMOS						
T_{HYS18}	Hysteresis input adder	-	3.0	-	3.0	ns
T_{OUT18}	Output adder	-	0.0	-	0.0	ns
T_{SLEW}	Output slew rate adder	-	4.0	-	4.0	ns

Internal Timing Parameters *(Continued)*

Symbol	Parameter[2]	-7		-8		Units
		Min.	Max.	Min.	Max.	
I/O Standard Time Adder Delays 2.5V CMOS						
T_{IN25}	Standard input adder	-	0.7	-	0.7	ns
T_{HYS25}	Hysteresis input adder	-	3.0	-	3.0	ns
T_{OUT25}	Output adder	-	1.0	-	1.0	ns
T_{SLEW25}	Output slew rate adder	-	4.0	-	4.0	ns
I/O Standard Time Adder Delays 3.3V CMOS/TTL						
T_{IN33}	Standard input adder	-	0.7	-	0.7	ns
T_{HYS33}	Hysteresis input adder	-	3.0	-	3.0	ns
T_{OUT33}	Output adder	-	1.6	-	1.6	ns
T_{SLEW33}	Output slew rate adder	-	4.0	-	4.0	ns

Notes:
1. 1.5 ns input pin signal rise/fall.

Switching Characteristics

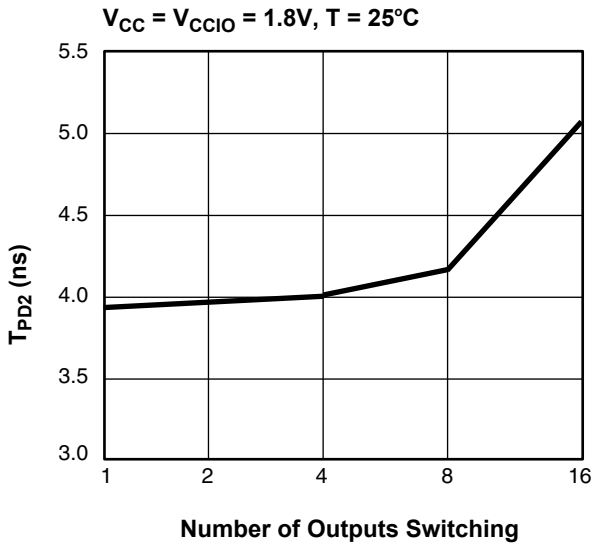
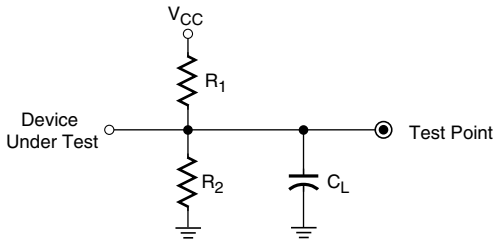


Figure 2: **Derating Curve for T_{PD}**

AC Test Circuit



Output Type	R_1	R_2	C_L
LVTTL33	268Ω	235Ω	35 pF
LVCMOS33	275Ω	275Ω	35 pF
LVCMOS25	188Ω	188Ω	35pF
LVCMOS18	112.5Ω	112.5Ω	35pF
LVCMOS15	150Ω	150Ω	35pF

C_L includes test fixtures and probe capacitance.
1.5 nsec maximum rise/fall times on inputs.

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Figure 3: **AC Load Circuit**

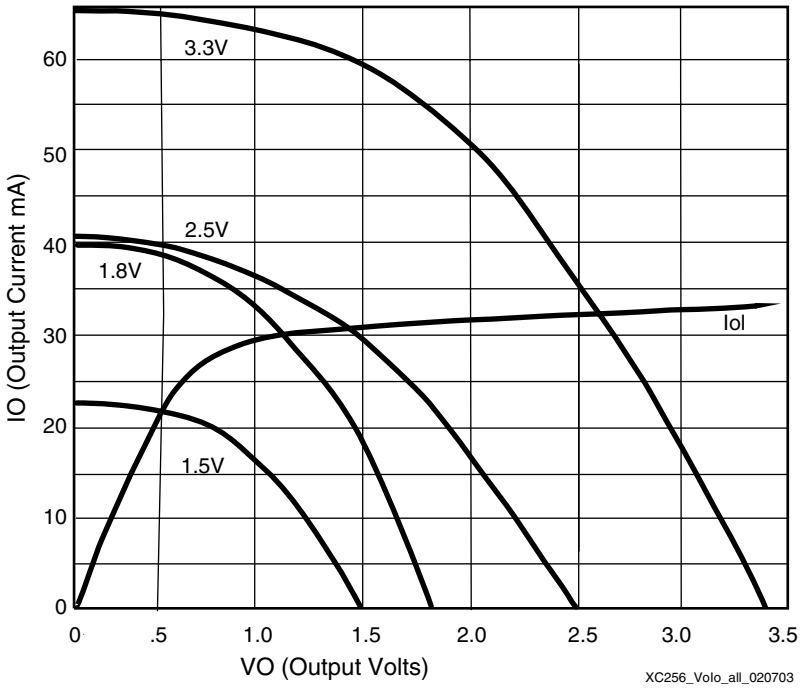


Figure 4: **Typical I/V Curve for XA2C256**

Pin Descriptions

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
1	1	-	-	2
1	2	-	-	2
1(GSR)	3	99	143	2
1	4	-	142	2
1	5	-	-	2
1	6	97	140	2
1	7	-	-	-
1	8	-	-	-
1	9	-	-	-
1	10	-	-	-
1	11	-	-	-
1	12	96	139	2
1	13	95	138	2
1	14	94	137	2
1	15	-	-	2
1	16	-	-	2
2(GTS2)	1	1	2	2
2	2	-	-	2
2(GTS3)	3	2	3	2
2	4	-	4	2
2(GTS0)	5	3	5	2
2	6	-	-	2
2	7	-	-	-
2	8	-	-	-
2	9	-	-	-
2	10	-	-	-
2	11	-	-	-
2(GTS1)	12	4	6	2
2	13	-	7	2
2	14	6	9	2
2	15	7	10	2
2	16	-	-	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
3	1	-	136	2
3	2	-	135	2
3	3	-	134	2
3	4	-	-	2
3	5	93	133	2
3	6			2
3	7	-	-	-
3	8	-	-	-
3	9	-	-	-
3	10	-	-	-
3	11	-	-	-
3	12	92	-	2
3	13	-	-	2
3	14	91	132	2
3	15	-	-	2
3	16	90	131	2
4	1	8	11	2
4	2	9	12	2
4	3	10	13	2
4	4	-	14	2
4	5	11	15	2
4	6	12	16	2
4	7	-	-	-
4	8	-	-	-
4	9	-	-	-
4	10	-	-	-
4	11	-	-	-
4	12	-	17	2
4	13	13	-	2
4	14	-	18	2
4	15	-	-	2
4	16	-	-	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
5	1	-	-	1
5	2	-	33	1
5	3	-	-	1
5(GCK1)	4	23	32	1
5	5		31	1
5(GCK0)	6	22	30	1
5	7	-	-	-
5	8	-	-	-
5	9	-	-	-
5	10	-	-	-
5	11	-	-	-
5	12	-	-	1
5	13	-	-	1
5	14	-	28	1
5	15	-	-	1
5	16	-	-	1
6	1	-	34	1
6 (CDRST)	2	24	35	1
6	3	-	-	1
6(GCK2)	4	27	38	1
6	5	-	-	1
6	6	-	-	1
6	7	-	-	-
6	8	-	-	-
6	9	-	-	-
6	10	-	-	-
6	11	-	-	-
6(DGE)	12	28	39	1
6	13	-	40	1
6	14	29	41	1
6	15	-	42	1
6	16	30	43	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
7	1	-	-	1
7	2	-	-	1
7	3	-	-	1
7	4	-	-	1
7	5	19	26	1
7	6	18	25	1
7	7	-	-	-
7	8	-	-	-
7	9	-	-	-
7	10	-	-	-
7	11	17	24	1
7	12	16	23	1
7	13	15	22	1
7	14	14	21	1
7	15	-	20	1
7	16	-	19	1
8	1	-	44	1
8	2	-	45	1
8	3	-	46	1
8	4	-	-	1
8	5	-	48	1
8	6	32	49	1
8	7	-	-	-
8	8	-	-	-
8	9	-	-	-
8	10	-	-	-
8	11	33	50	1
8	12	34	51	1
8	13	35	52	1
8	14	36	-	1
8	15	37	-	1
8	16	-	-	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
9	1	78	112	2
9	2	79	113	2
9	3	-	-	2
9	4	80	114	2
9	5			2
9	6	81	115	2
9	7	-	-	-
9	8	-	-	-
9	9	-	-	-
9	10	-	-	-
9	11	-	-	2
9	12	82	116	2
9	13	-	117	2
9	14	-	118	2
9	15	-	119	2
9	16	-	-	2
10	1	77	111	2
10	2	76	110	2
10	3	74	107	2
10	4	73	106	2
10	5	72	105	2
10	6	71	104	2
10	7	-	-	-
10	8	-	-	-
10	9	-	-	-
10	10	-	-	-
10	11			2
10	12	70	103	2
10	13	-	-	2
10	14	-	102	2
10	15	-	-	2
10	16	-	101	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
11	1	-	-	2
11	2	-	-	2
11	3	-	-	2
11	4	-	-	2
11	5	-	120	2
11	6	-	121	2
11	7	-	-	-
11	8	-	-	-
11	9	-	-	-
11	10	-	-	-
11	11	85	124	2
11	12	86	125	2
11	13	87	126	2
11	14	89	128	2
11	15	-	129	2
11	16	-	130	2
12	1	-	-	2
12	2	-	100	2
12	3	-	-	2
12	4	-	-	2
12	5	-	-	2
12	6	-	-	2
12	7	-	-	-
12	8	-	-	-
12	9	-	-	-
12	10	-	-	-
12	11	68	98	2
12	12	-	97	2
12	13	67	96	2
12	14	66	95	2
12	15	65	94	2
12	16	-	-	2

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
13	1	-	75	1
13	2	53	76	1
13	3	-	77	1
13	4	54	-	1
13	5	-	78	1
13	6	55	79	1
13	7	-	-	-
13	8	-	-	-
13	9	-	-	-
13	10	-	-	-
13	11	-	-	-
13	12	-	80	1
13	13	56	81	1
13	14	-	82	1
13	15	-	-	1
13	16	-	-	1
14	1	52	74	1
14	2	-	71	1
14	3	50	70	1
14	4	-	69	1
14	5	49	-	1
14	6	-	68	1
14	7	-	-	-
14	8	-	-	-
14	9	-	-	-
14	10	-	-	-
14	11	-	-	-
14	12	-	-	1
14	13	-	66	1
14	14	46	64	1
14	15	44	-	1
14	16	-	61	1

Pin Descriptions *(Continued)*

Function Block	Macro-cell	VQG100	TQG144	I/O Bank
15	1	-	-	1
15	2	-	83	1
15	3	-	-	1
15	4	-	-	1
15	5	-	-	1
15	6	-	-	1
15	7	-	-	-
15	8	-	-	-
15	9	-	-	-
15	10	-	-	-
15	11	58	85	1
15	12	59	86	1
15	13	60	87	1
15	14	61	88	1
15	15	63	91	1
15	16	64	92	1
16	1	-	-	1
16	2	-	-	1
16	3	-	-	1
16	4	-	-	1
16	5	43	60	1
16	6	42	59	1
16	7	-	-	-
16	8	-	-	-
16	9	-	-	-
16	10	-	-	-
16	11	41	58	1
16	12	40	57	1
16	13	39	56	1
16	14	-	-	1
16	15	-	54	1
16	16	-	53	1

Notes:

1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.
2. GTS, GSR and GCK pins can be used for general purpose I/O.

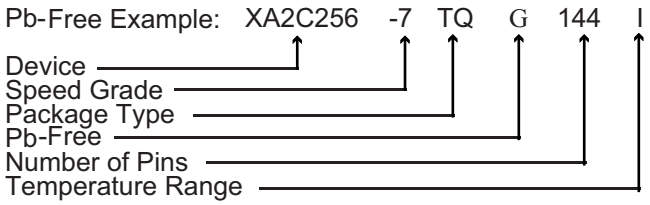
XA2C256 JTAG, Power/Ground, No Connect Pins and Total User I/O

Pin Type	VQG100	TQG144
TCK	48	67
TDI	45	63
TDO	83	122
TMS	47	65
V_{CCAUX} (JTAG supply voltage)	5	8
Power internal (V_{CC})	26, 57	1, 37, 84
Power Bank 1 I/O (V_{CCIO1})	20, 38, 51	27, 55, 73, 93
Power Bank 2 I/O (V_{CCIO2})	88, 98	109, 127, 141
Ground	21, 25, 31, 62, 69, 75, 84, 100	29, 36, 47, 62, 72, 89, 90, 99, 108, 123, 144
No connects	-	-
Total user I/O	80	118

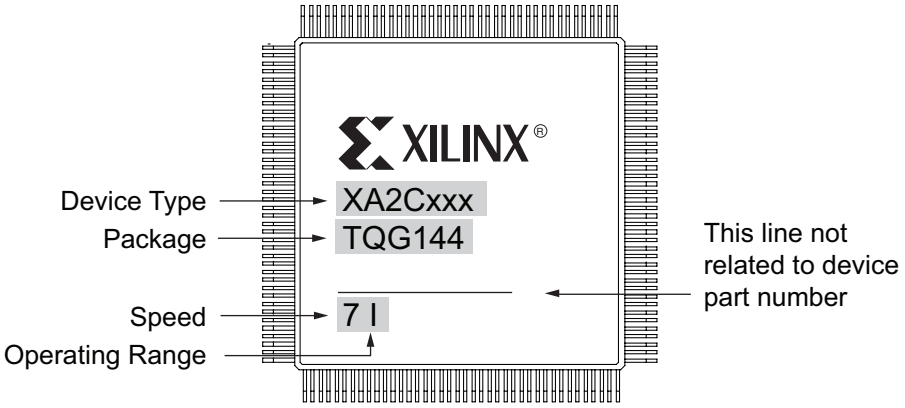
Ordering Information

Part Number	Pin/Ball Spacing	θ_{JA} (C/Watt)	θ_{JC} (C/Watt)	Package Type	Package Body Dimensions	I/O	Industrial (I)[1] Hi-T (Q)
XA2C256-7VQG100I	0.5mm	43.1	10.9	Very Thin Quad Flat Pack; Pb-free	14mm x 14mm	80	I
XA2C256-8VQG100Q	0.5mm	43.1	10.9	Very Thin Quad Flat Pack; Pb-free	14mm x 14mm	80	Q
XA2C256-7TQG144I	0.5mm	37.2	7.2	Thin Quad Flat Pack; Pb-free	20mm x 20mm	118	I
XA2C256-8TQG144Q	0.5mm	37.2	7.2	Thin Quad Flat Pack; Pb-free	20mm x 20mm	118	Q

Notes:
1. I = Industrial (T_A = –40°C to +85°C); Q = Automotive (T_A = –40°C to +105°C with T_J Maximum = +125°C).



Device Part Marking



Part Marking for all non chip scale packages

Figure 5: **Sample Package with Part Marking**

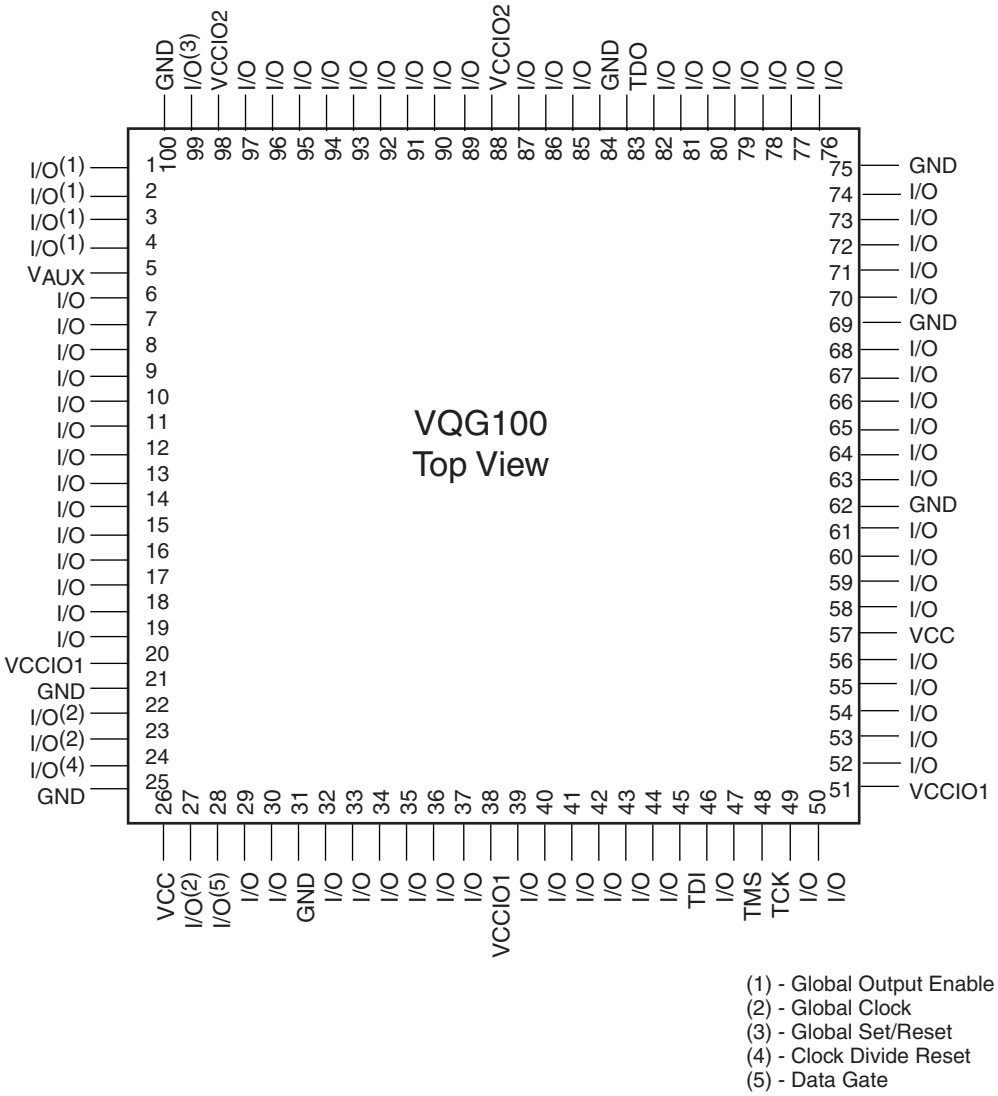


Figure 6: **VQG100 Very Thin Quad Flat Pack**

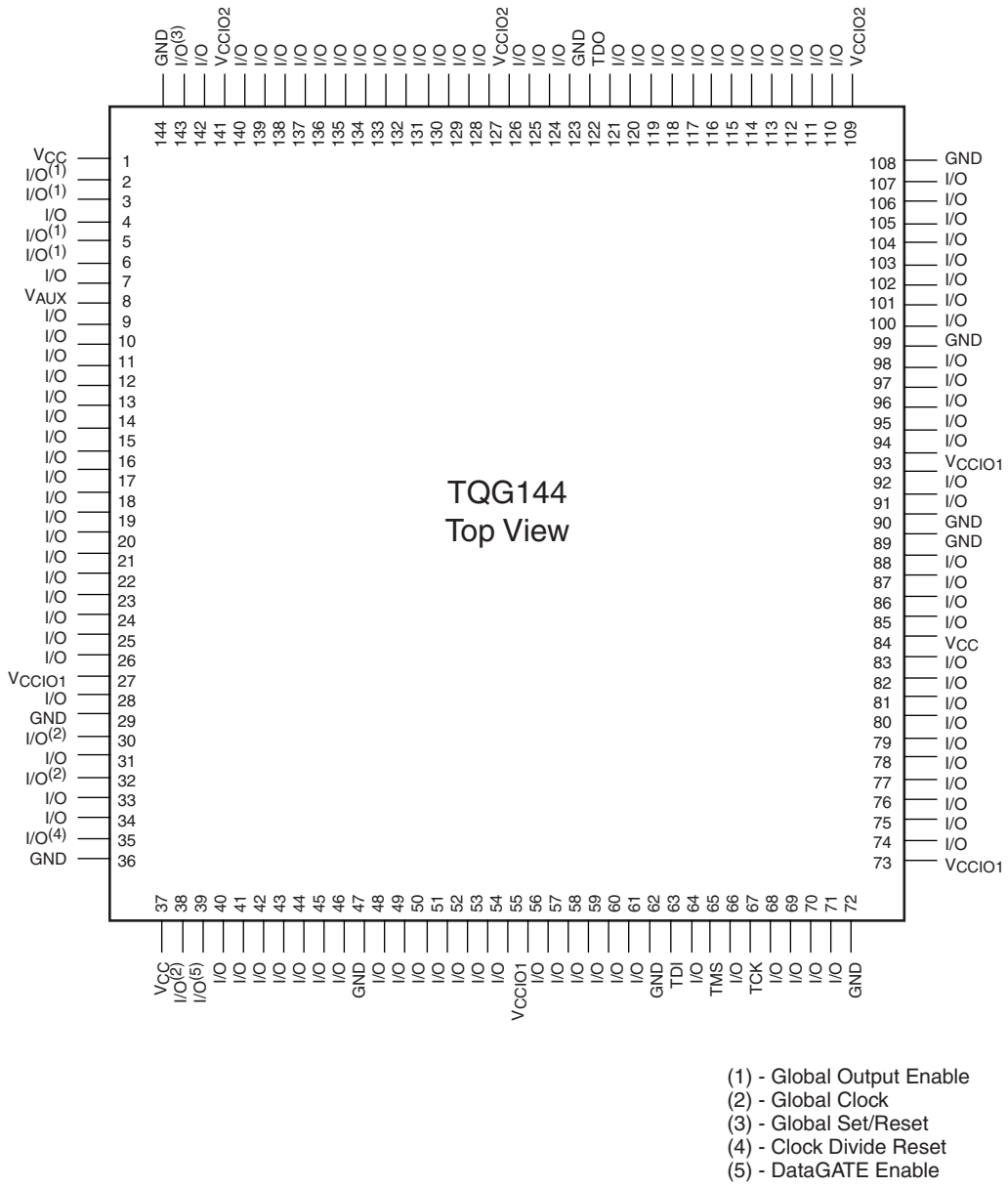


Figure 7: **TQG144 Thin Quad Flat Pack**

CoolRunner-II Automotive Requirements and Recommendations

Requirements

The following requirements are for all automotive applications:

1. Use a monotonic, fast ramp power supply to power up CoolRunner-II. A V_{CC} ramp time of less than 1 ms is required.
2. Do not float I/O pins during device operation. Floating I/O pins can increase I_{CC} as input buffers will draw 1–2 mA per floating input. In addition, when I/O pins are floated, noise can propagate to the center of the CPLD. I/O pins should be appropriately terminated with bus-hold or pull-up. Unused I/Os can also be configured as C_{GND} (programmable GND).
3. Do not drive I/O pins without V_{CC}/V_{CCIO} powered.
4. Sink current when driving LEDs. Because all Xilinx CPLDs have N-channel pull-down transistors on outputs, it is required that an LED anode is sourced through a resistor externally to V_{CC}. Consequently, this will give the brightest solution.

5. Avoid pull-down resistors. Always use external pull-up resistors if external termination is required. This is because the CoolRunner-II Automotive CPLD, which includes some I/O driving circuits beyond the input and output buffers, may have contention with external pull-down resistors, and, consequently, the I/O will not switch as expected.
6. Do not drive I/Os pins above the V_{CCIO} assigned to its I/O bank.
   a. The current flow can go into V_{CCIO} and affect a user voltage regulator.
   b. It can also increase undesired leakage current associated with the device.
   c. If done for too long, it can reduce the life of the device.
7. Do not rely on the I/O states before the CPLD configures. During power up, the CPLD I/Os may be affected by internal or external signals.
8. Use a voltage regulator which can provide sufficient current during device power up. As a rule of thumb, the regulator needs to provide at least three times the peak current while powering up a CPLD in order to guarantee the CPLD can configure successfully.
9. Ensure external JTAG terminations for TMS, TCK, TDI, TDO should comply with the IEEE 1149.1. All Xilinx CPLDs have internal weak pull-ups on TDI, TMS, and TCK.
10. Attach all CPLD V_{CC} and GND pins in order to have necessary power and ground supplies around the CPLD.
11. Decouple all V_{CC} and V_{CCIO} pins with capacitors of 0.01 µF and 0.1 µF closest to the pins for each V_{CC}/V_{CCIO}-GND pair.
12. Configure I/Os properly. CoolRunner-II Automotive CPLDs have I/O banks; therefore, signals must be assigned to appropriate banks (LVCMOS33, LVCMOS18 …).

Recommendations

The following recommendations are for all automotive applications.

1. Use strict synchronous design (only one clocking event) if possible. A synchronous system is more robust than an asynchronous one.
2. Include JTAG stakes on the PCB. JTAG stakes can be used to test the part on the PCB. They add benefit in reprogramming part on the PCB, inspecting chip internals with INTEST, identifying stuck pins, and inspecting programming patterns (if not secured).
3. CoolRunner-II Automotive CPLDs work with any power sequence, but it is preferable to power the V_{CCI} (internal V_{CC}) before the V_{CCIO} for the applications in which any glitches from device I/Os are unwanted.
4. Do not disregard report file warnings. Software identifies potential problems when compiling, so the report file is worth inspecting to see exactly how your design is mapped onto the logic.
5. Understand the Timing Report. This report file provides a speed summary along with warnings. Read the timing file (*.tim) carefully. Analyze key signal chains to determine limits to given clock(s) based on logic analysis.
6. Review Fitter Report equations. Equations can be shown in ABEL-like format, or can also be displayed in Verilog or VHDL formats. The Fitter Report also includes switch settings that are very informative of other device behaviors.
7. Let design software define pinouts if possible. Xilinx CPLD software works best when it selects the I/O pins and manages resources for users. It can spread signals around and improve pin-locking. If users must define pins, plan resources in advance.
8. Perform a post-fit simulation for all speeds to identify any possible problems (such as race conditions) that might occur when fast-speed silicon is used instead of slow-speed silicon.
9. Distribute SSOs (Simultaneously Switching Outputs) evenly around the CPLD to reduce switching noise.
10. Terminate high speed outputs to eliminate noise caused by very fast rising/falling edges.

Additional Information

Additional information is available for the following CoolRunner-II topics:

- **XAPP784**: Bulletproof CPLD Design Practices
- **XAPP375**: Timing Model
- **XAPP376**: Logic Engine
- **XAPP378**: Advanced Features
- **XAPP382**: I/O Characteristics
- **XAPP389**: Powering CoolRunner-II
- **XAPP399**: Assigning VREF Pins

These and other application notes can be accessed at:

CoolRunner-II Documentation

Package specifications can be accessed at:

Device Packages

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/31/06	1.0	Initial Xilinx release.
05/05/07	1.1	Change to V_{IH} specification for 3.3V, 2.5V and 1.8V LVCMOS.
06/22/09	1.2	Updated Figure 7.

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