CMOS single-chip 8-bit MCU with 12-bit A/D converter

Main features

- **8-bit Microcontroller With High Speed 8051 CPU**
- **Basic MCU Function**
  - 4Kbytes Flash Code Memory
  - 256bytes IRAM
- **Built-in Analog Function**
  - Power-On Reset and Low Voltage Detect Reset
  - Internal 8MHz RC Oscillator (±2.0%, T_A= 0 ~ +50°C)
  - Internal 200kHz RC Oscillator (±3.0%, T_A= -20 ~ +85°C)
  - Watchdog Timer RC Oscillator (5kHz)
- **Peripheral Features**
  - 12-bit Analog to Digital Converter (8 inputs)
  - USART(UART + SPI) 1set
  - I2C 8-bit x 1-ch
  - 16-bit CRC/Checksum Generator
- **I/O and Packages**
  - Up to 18 Programmable I/O lines with 20 pin package.
  - 8 SOP, 10 SSOP, 16 SOPN, 20 SOP, 20 TSSOP
  - Pb-free package
- **Operating Conditions**
  - 1.8V to 5.5V Wide Voltage Range
  - -40°C to 85°C Temperature Range
- **Application**
  - Small Home Appliance

MC96F8204

Data Sheet

V 1.6

Revised 29 September, 2017

Revision history

Version	Date	Revision list
1.0	2016.03.14	Published this book.
1.1	2016.04.08	Change tR spec max value form 5.0V/ms to 30.0V/ms in 7.4 Power-On Reset. Add a chapter 7.23 Recommended Circuit and Layout with SMPS Power. Modify the program tips in Chapter 15. Flash Memory. Add an appendix about “Flash Protection for invalid Erase/Write” Fix typos.
1.2	2016.05.17	Fix typo of 8SOP package device name (MC96F8104M). Fix typos of I2C Status Register in chapter 11.9 I2C.
1.3	2016.09.08	Remove packages the 20 QFN, 16 TSSOP, 16 QFN, 8 PDIP. Modify package from 16 SOP to 16 SOPN.
1.4	2016.12.21	Updated OCD dongle image and writing tool images in chapter 1.3 Development tools. Fix typos of T0/T1/T2.
1.5	2017.01.20	Added the note on the flash memory erase and write in chapter 15. Flash Memory. Fix typos of I2C Status Register in chapter 11.9 I2C.
1.6	2017.09.29	Revised this book. Added the maximum allowable current (I_{IK}) in chapter 7.1 Absolute Maximum Ratings. Updated package diagrams in chapter 4. Package Diagram.

Version 1.6

Published by FAE team

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1 Overview

1.1 Description

The MC96F8204 is advanced CMOS 8-bit microcontroller with 4 Kbytes of FLASH. This is powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 4k bytes of FLASH, 256 bytes of IRAM, general purpose I/O, basic interval timer, watchdog timer, 8/16-bit timer/counter, 16-bit PPG output, watch timer, USART(UART + SPI), I2C, 12-bit A/D converter, Flash CRC/Checksum Generator, on-chip POR, LVR, LVI, on-chip oscillator and clock circuitry. The MC96F8204 also supports power down modes to reduce power consumption.

Device Name	FLASH	IRAM	ADC	I/O PORT	Package
MC96F8204D	4 Kbytes FLASH	256 bytes	8 inputs	18	20 SOP
MC96F8204R			8 inputs	18	20 TSSOP
MC96F8204M			8 inputs	14	16 SOPN
MC96F8104S			8 inputs	8	10 SSOP
MC96F8104M			6 inputs	6	8 SOP

Table 1.1 Ordering Information of MC96F8204

1.2 Features

- **CPU**
  - 8-bit CISC core (M8051, 2 clocks per cycle)
- **ROM (FLASH) Capacity**
  - 4 Kbytes Flash with self read/write capability
  - On Chip debug and In-System Programming(ISP)
  - Endurance : 10,000 times
  - Retention : 10 years
- **256bytes IRAM**
- **General Purpose I/O (GPIO)**
  - Normal I/O : 18 Ports (P0, P1, P2[1:0])
- **Timer/Counter**
  - Basic Interval Timer (BIT) 8-bit× 1-ch
  - Watch Dog Timer (WDT) 8-bit × 1-ch 5kHz internal RC oscillator for WDT
  - 8-bit× 1-ch(T0), 16-bit× 2-ch (T1/T2)
- **Programmable Pulse Generation**
  - Pulse generation (by T1/T2)
- **Watch Timer (WT)**
  - 3.91ms/0.25s/0.5s/1s /1min interval at 32.768kHz
- **USART**
  - 8Bit UART × 1ch, 8Bit SPI x 1ch
- **I2C**
  - 8-bit× 1-ch
- **12-bit A/D Converter**
  - 8 Input channels
- **16-Bit CRC/Checksum Generator**
  - Auto and User CRC/Checksum mode
- **Power On Reset**
  - Reset release level (1.4V)
- **Low Voltage Reset**
  - 14 level detect (1.60/ 2.05/ 2.15/ 2.25/ 2.37/ 2.50/ 2.65/ 2.82/ 3.01/ 3.22/ 3.47/ 3.76/ 4.10/ 4.51V)
- **Low Voltage Indicator**
  - 13 level detect (2.05/ 2.15/ 2.25/ 2.37/ 2.50/ 2.65/ 2.82/ 3.01/ 3.22/ 3.47/ 3.76/ 4.10/ 4.51V)
- **Interrupt Sources**
  - External Interrupts (EINT0/1/10/11/12) (5)
  - Timer(0/1/2) (3)
  - WT (1)
  - WDT (1)
  - BIT (1)
  - USART (2)
  - I2C(1)
  - ADC (1)
- **Internal RC Oscillator**
  - Low frequency: 200kHz ± 3.0% (TA = -20 to +85 °C)
  - High frequency: 8MHz ± 2.0% (TA = 0 to +50 °C)
- **Power Down Mode**
  - STOP, IDLE mode
- **Operating Voltage and Frequency**
  - 1.8V~ 5.5V (@32 ~ 38kHz with X-tal)
  - 1.8V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal, Ceramic)
  - 2.0V ~ 5.5V (@ 0.4 ~ 4.2MHz with X-tal, Crystal)
  - 2.7V ~ 5.5V (@ 0.4 ~ 12.0MHz with X-tal)
  - 1.8V ~ 5.5V (@ 0.5 ~ 8.0MHz with HFIRC)
  - 1.8V ~ 5.5V (@ 25.0 ~ 200kHz with LFIRC)
  - Voltage dropout converter included for core
- **Minimum Instruction Execution Time**
  - 167ns (@12MHz main clock)
  - 61us (@ 32.768kHz sub clock)
- **Operating Temperature**
  - –40 ~ +85℃
- **Oscillator Type**
  - 0.4-12MHz Crystal or Ceramic for main clock
- **Package Type**
  - 20 SOP/TSSOP
  - 16 SOPN
  - 10 SSOP
  - 8 SOP
  - Pb-free package

1.3 Development tools

1.3.1 Compiler

We do not provide the compiler. Please contact the third parties.

The core of MC96F8204 is Mentor 8051. And, device ROM size is smaller than 64k bytes. Developer can use all kinds of third party's standard 8051 compiler.

1.3.2 OCD(On-chip debugger) emulator and debugger

The OCD (On Chip Debug) emulator supports ABOV Semiconductor's 8051 series MCU emulation.

The OCD interface uses two-wire interfacing between PC and MCU which is attached to user's system. The OCD can read or change the value of MCU internal memory and I/O peripherals. And the OCD also controls MCU internal debugging logic, it means OCD controls emulation, step run, monitoring, etc.

The OCD Debugger program works on all Microsoft-Windows operating system.

If you want to see more details, please refer to OCD debugger manual. You can download debugger S/W and manual from our web-site(http://www.abov.co.kr).

Connection:

- DSCL (MC96F8204 P01 port)
- DSDA (MC96F8204 P00 port)

OCD connector diagram: Connect OCD with user system

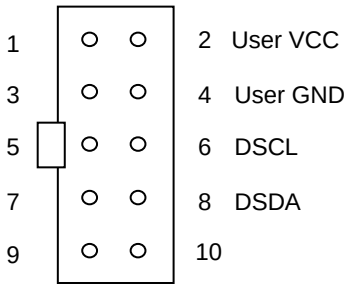


Figure 1.1 Debugger(OCD1/OCD2) and Pin description

1.3.3 Programmer

Single programmer :

E-PGM+ : It programs MCU device directly.

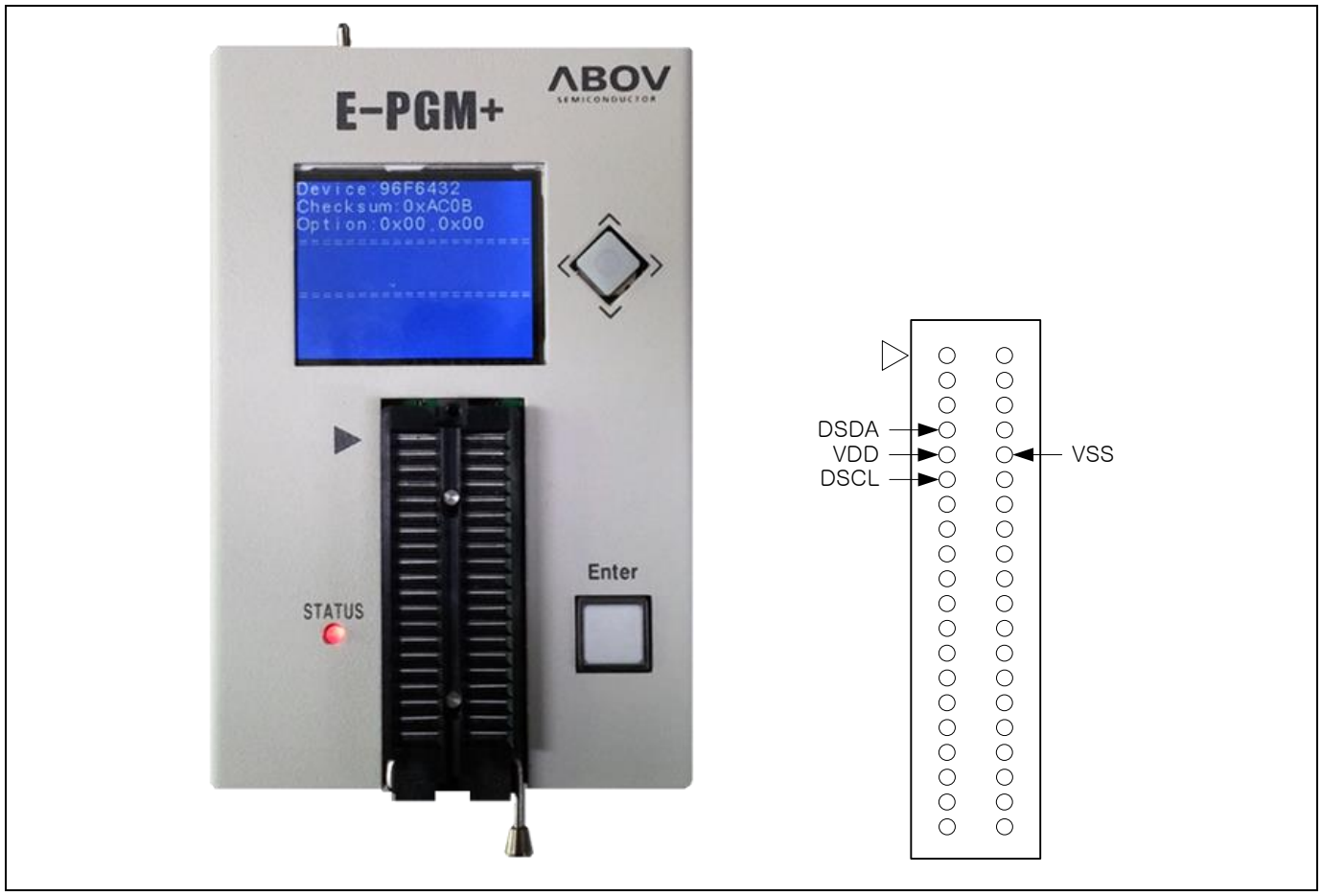


Figure 1.2 E-PGM+ (Single writer)

OCD emulator:

It can write code to MCU device too, because OCD debugger supports ISP (In System Programming).It does not require additional H/W, except developer's target system.

Gang programmer: E-GANG4 and E-GANG6

- It can run PC controlled mode.
- It can run standalone without PC control too.
- USB interface is supported.
- Easy to connect to the handler.

Figure 1.3 E-GANG4 and E-GANG6 (for Mass Production)

1.4 MTP programming

1.4.1 Overview

The program memory of MC96F8204 is MTP Type. This flash is accessed by serial data format. There are four pins(DSCL, DSDA, VDD, VSS) for programming/reading the flash.

Pin name	Main chip pin name	During programming	
		I/O	Description
DSCL	P01	I	Serial clock pin. Input only pin.
DSDA	P00	I/O	Serial data pin. Output port when reading and input port when programming. Can be assigned as input/push-pull output port.
VDD, VSS	VDD, VSS	-	Logic power supply pin.

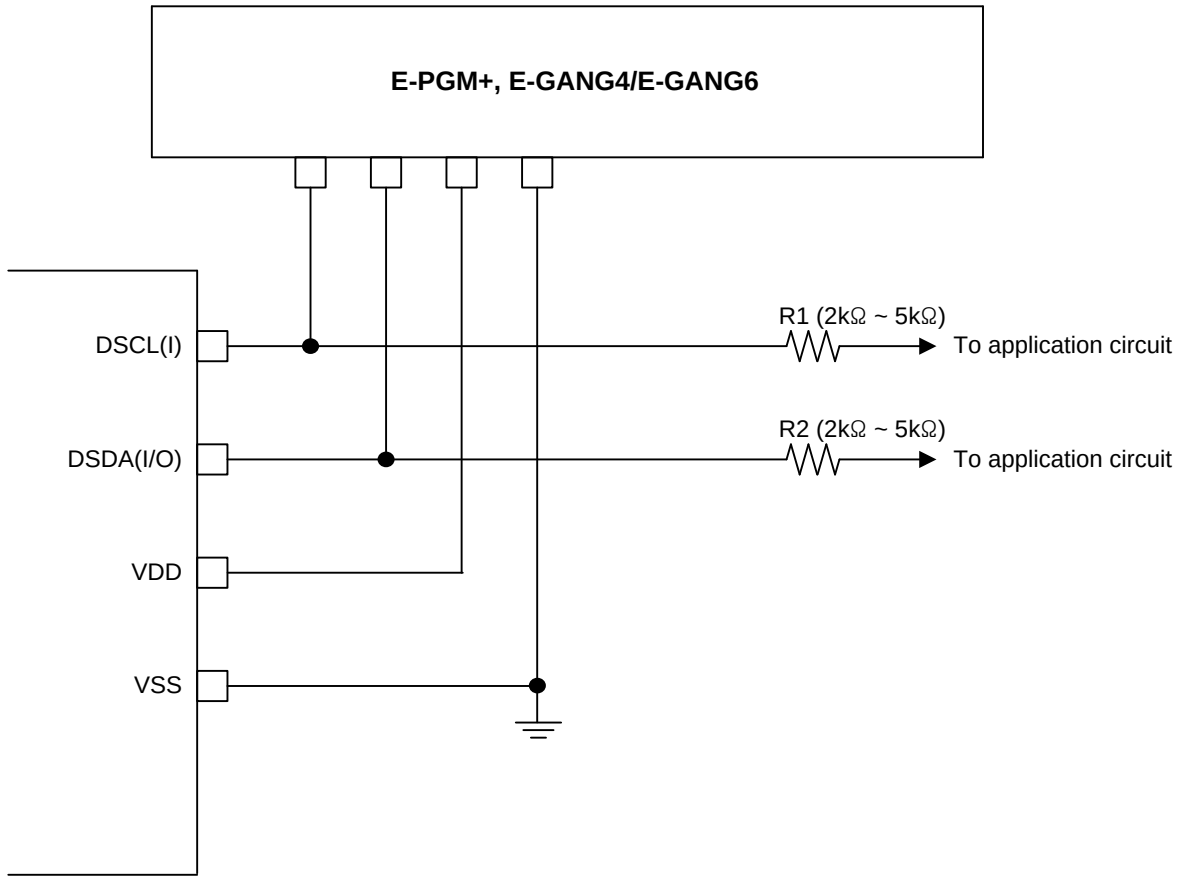
Table 1.2 Descriptions of pins which are used to programming/reading the Flash

1.4.2 On-Board programming

The MC96F8204 needs only four signal lines including VDD and VSS pins for programming FLASH with serial protocol. Therefore the on-board programming is possible if the programming signal lines are considered when the PCB of application board is designed.

1.4.3 Circuit Design Guide

At the FLASH programming, the programming tool needs 4 signal lines that are DSCL, DSDA, VDD, and VSS. When you design the PCB circuits, you should consider the usage of these signal lines for the on-board programming. Please be careful to design the related circuit of these signal pins because rising/falling timing of DSCL and DSDA is very important for proper programming.



NOTE)

1. In on-board programming mode, very high-speed signal will be provided to pin DSCL and DSDA. And it will cause some damages to the application circuits connected to DSCL or DSDA port if the application circuit is designed as high speed response such as relay control circuit. If possible, the I/O configuration of DSDA, DSCL pins had better be set to input mode.
2. The value of R1 and R2 is recommended value. It varies with circuit of system.

Figure 1.4 PCB design guide for on board programming

2 Block diagram

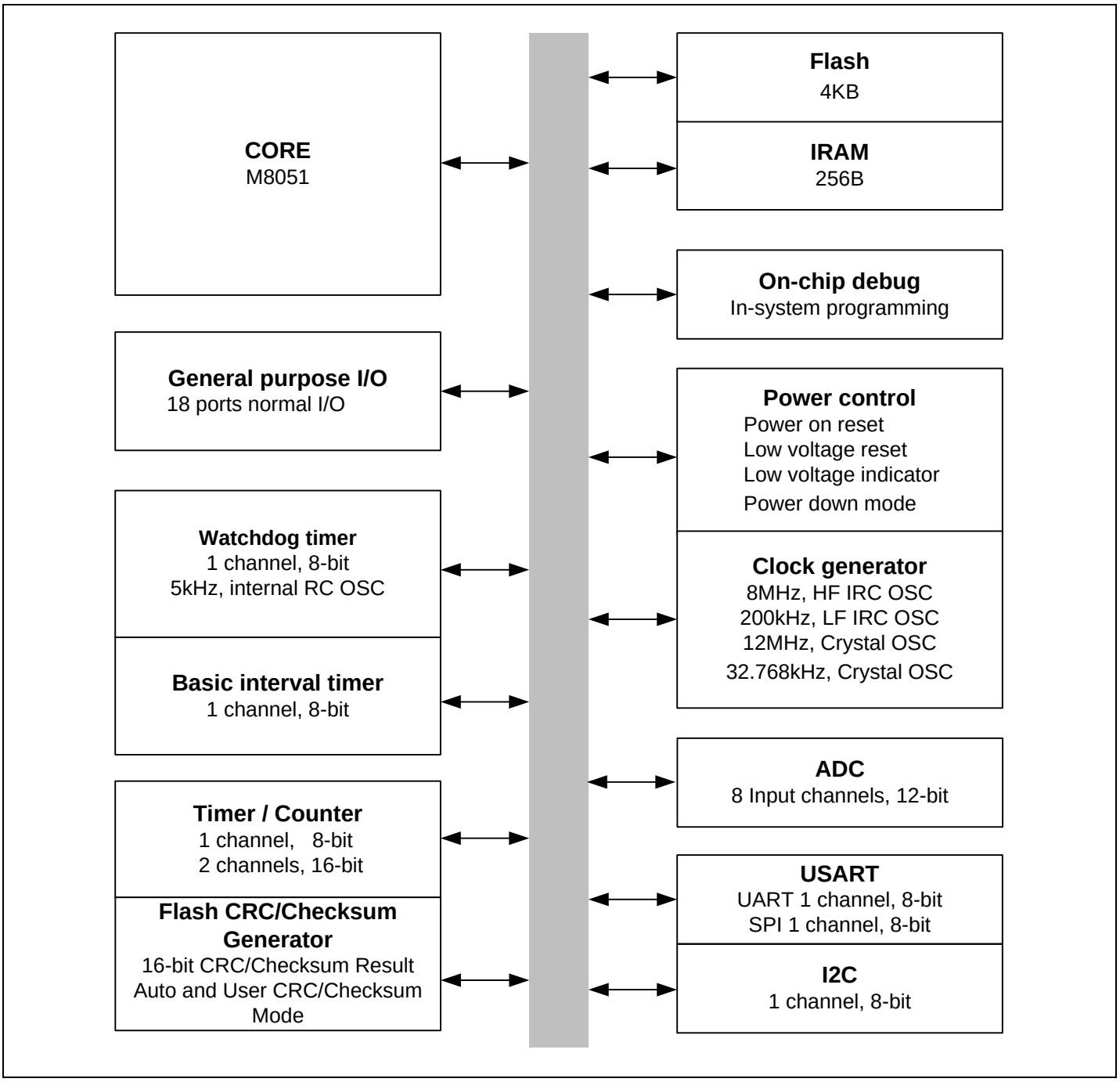
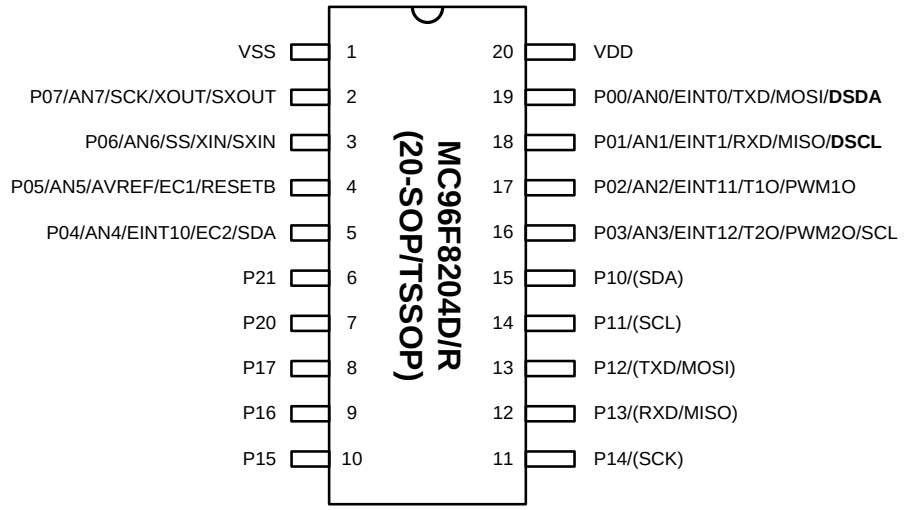


Figure 2.1 Block diagram of MC96F8204

NOTE)

1. The P16-P17 and P20-P21 are not in the 16-Pin package.
2. The P10-P17 and P20-P21 are not in the 10-Pin package.
3. The P03-P04, P10-P17 and P20-P21 are not in the 8-Pin package.

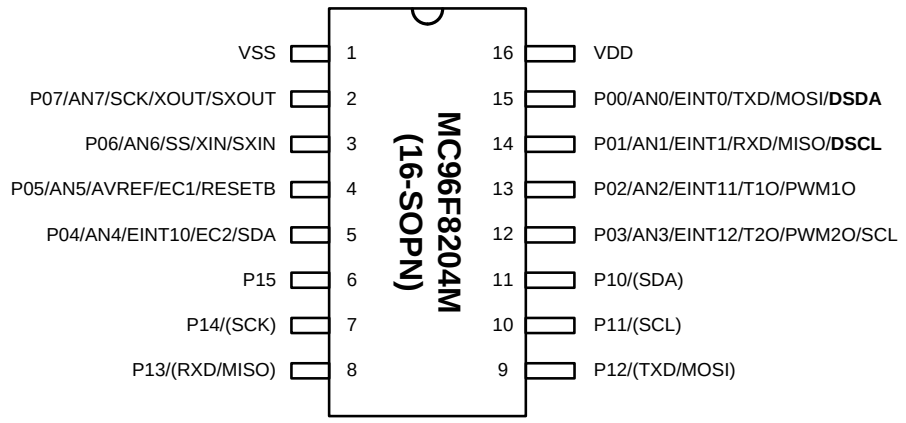
3 Pin assignment



NOTE)

1. On On-Chip Debugging, ISP uses P0[1:0] pin as DSCL, DSDA.

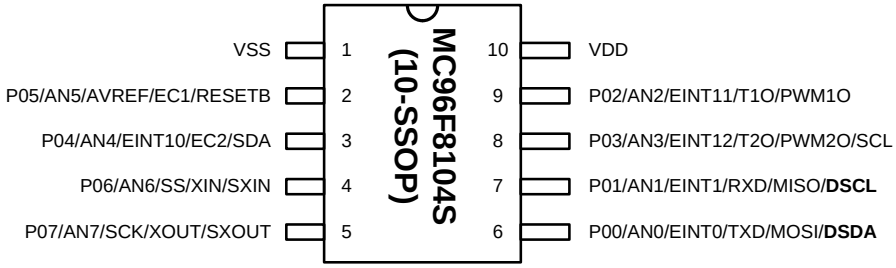
Figure 3.1 MC96F8204D 20SOP/TSSOP Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P0[1:0] pin as DSCL, DSDA.
2. The P16-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 16-pin package is used.

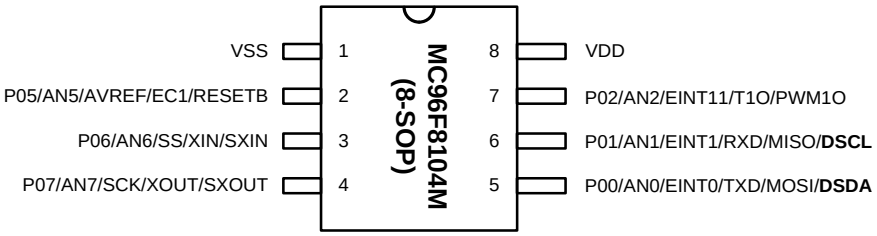
Figure 3.2 MC96F8204M 16SOPN Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P0[1:0] pin as DSCL, DSDA.
2. The P10-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 10-pin package is used.

Figure 3.3 MC96F8104S 10SSOP Pin Assignment



NOTE)

1. On On-Chip Debugging, ISP uses P0[1:0] pin as DSCL, DSDA.
2. The P03-P04, P10-P17 and P20-P21 pins should be selected as a push-pull output or an input with pull-up resistor by software control when the 8-pin package is used.

Figure 3.4 MC96F8104M 8SOP Pin Assignment

4 Package Diagram

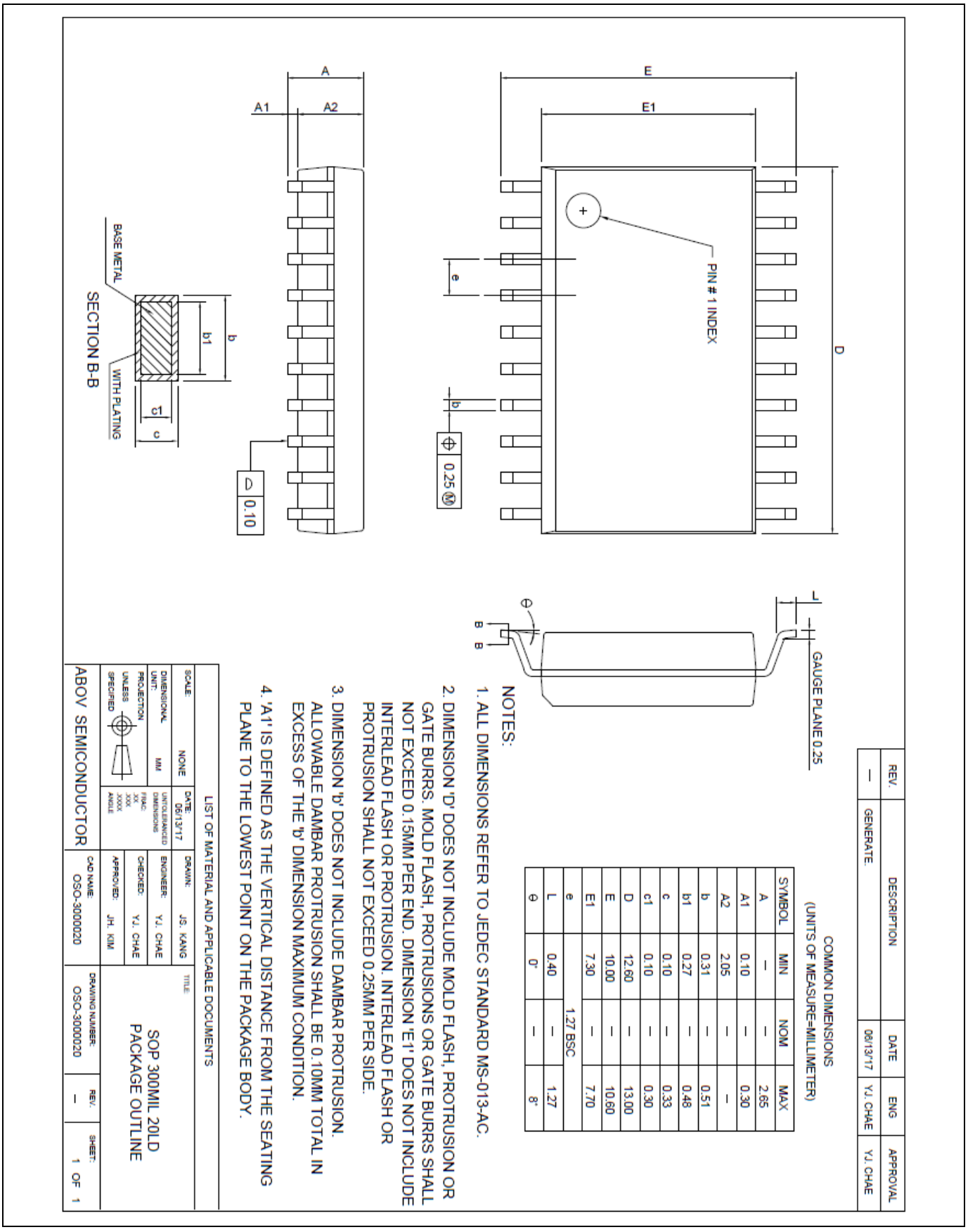


Figure 4.1 20-Pin SOP Package

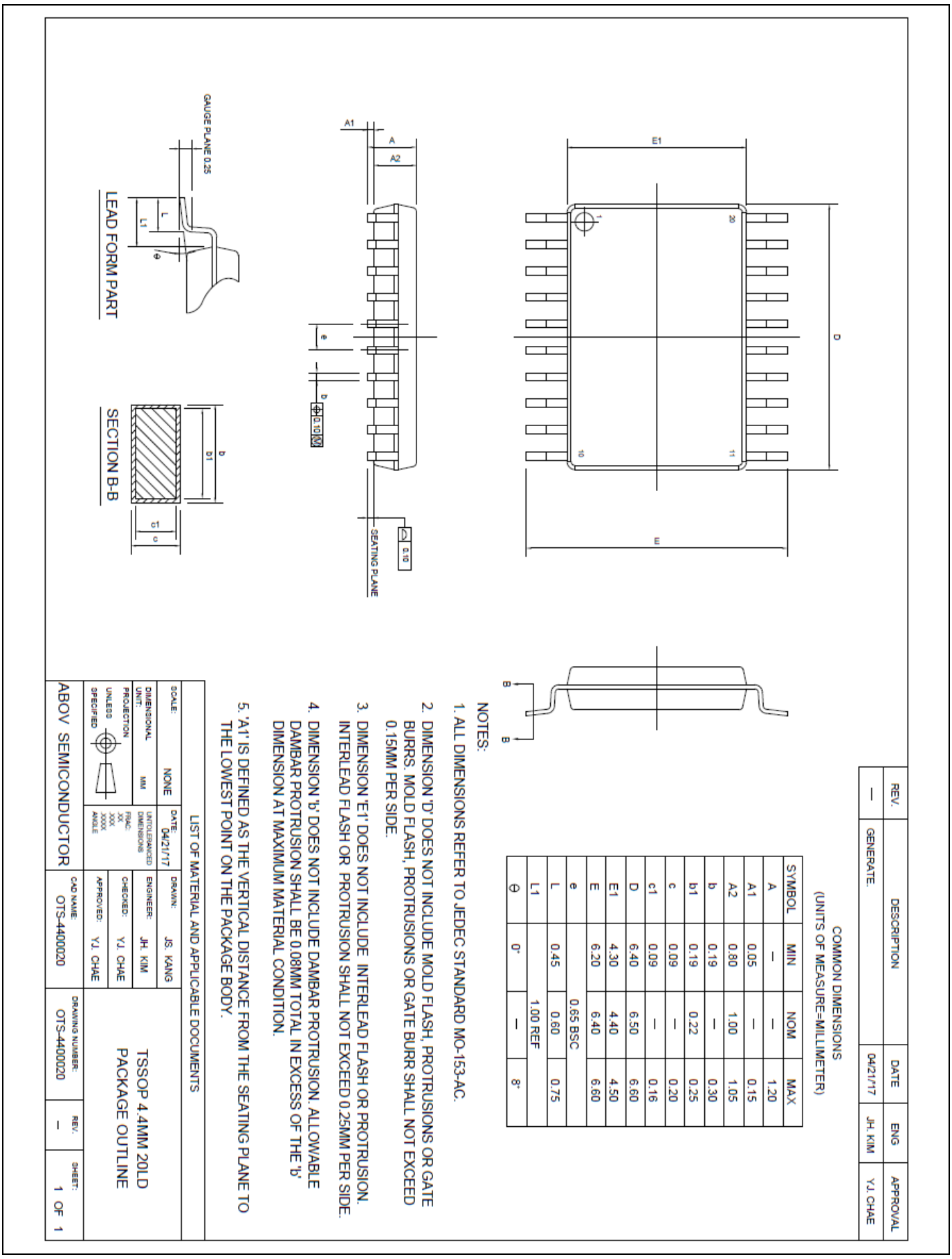


Figure 4.2 20-Pin TSSOP Package

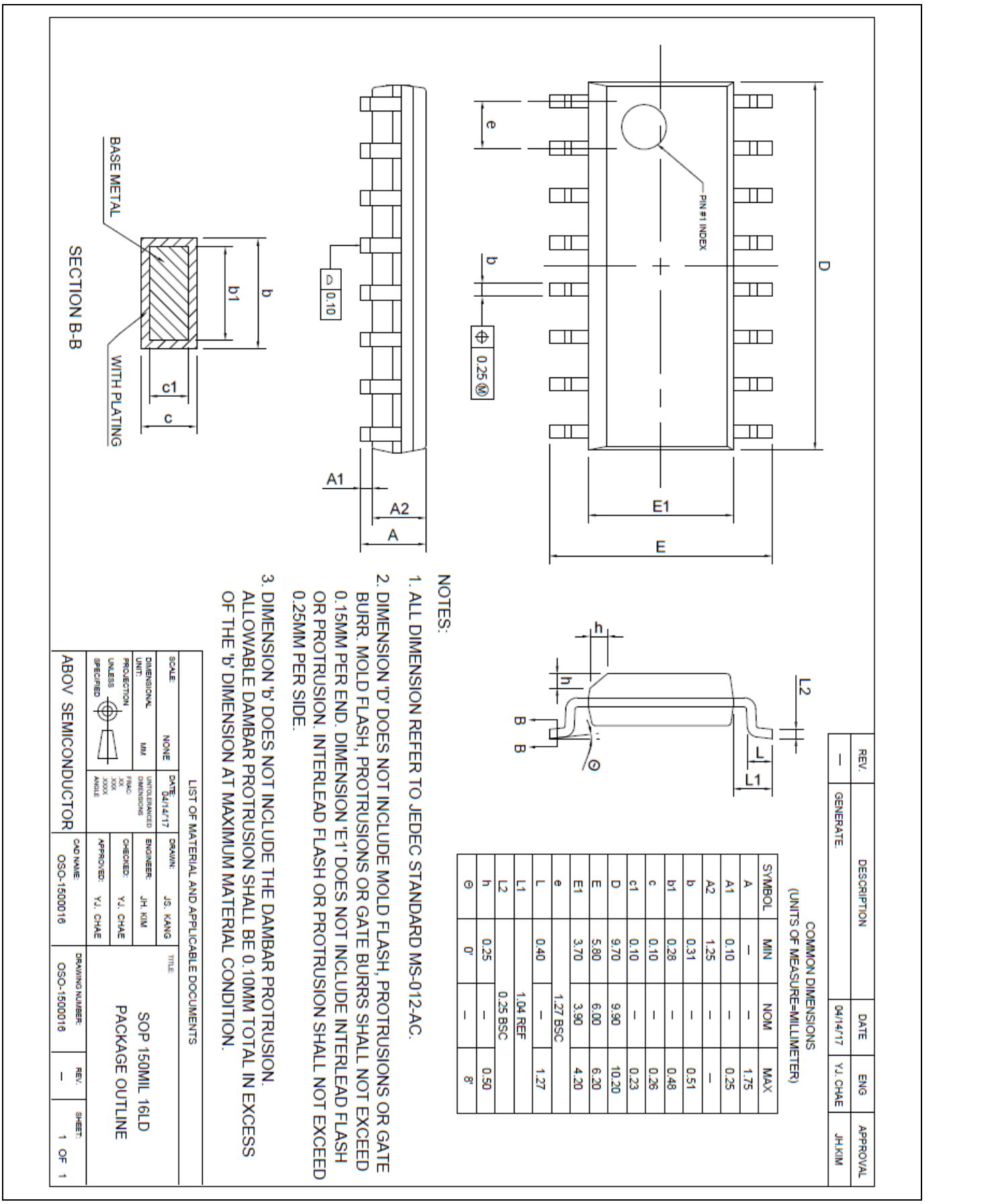


Figure 4.3 16-Pin SOPN Package

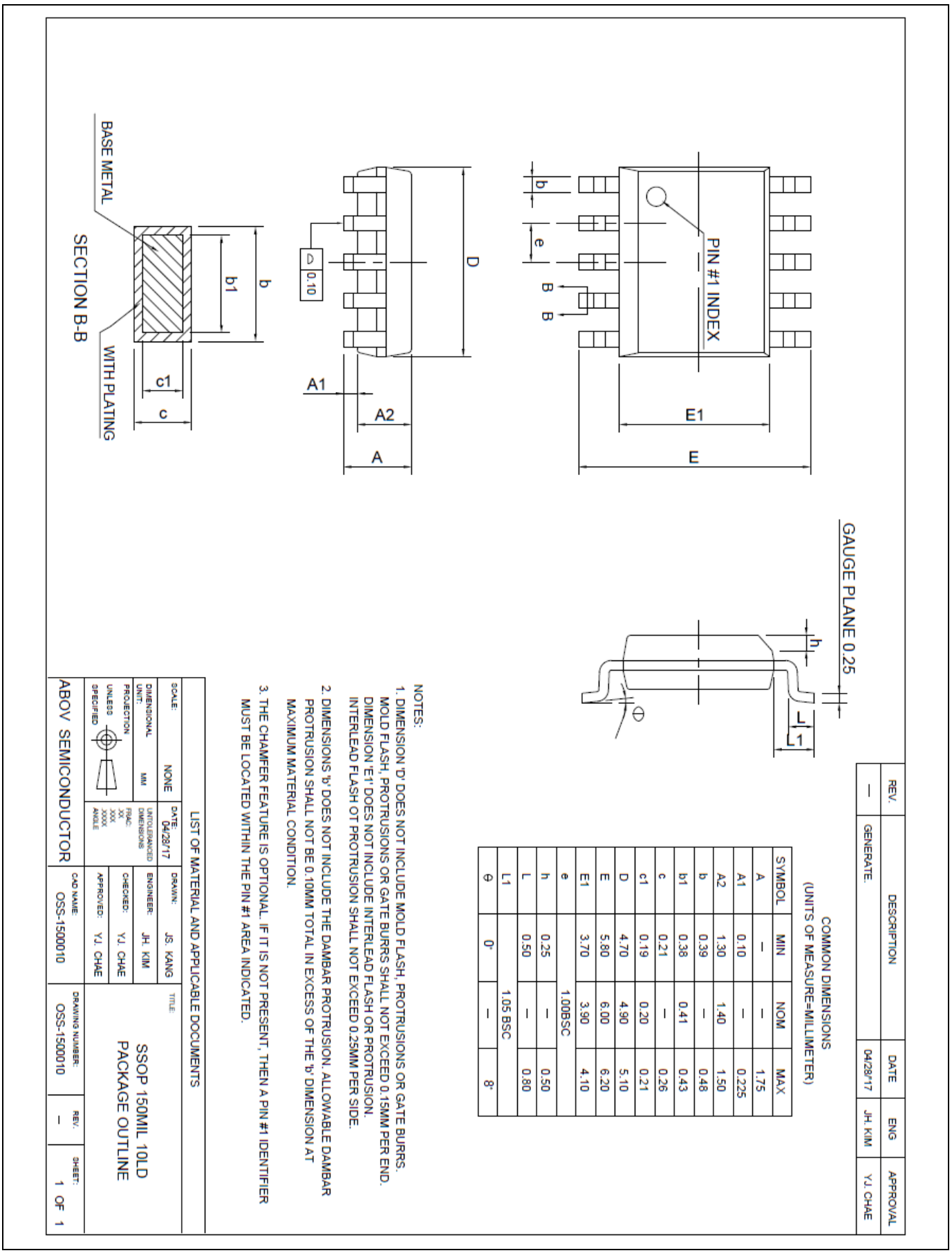
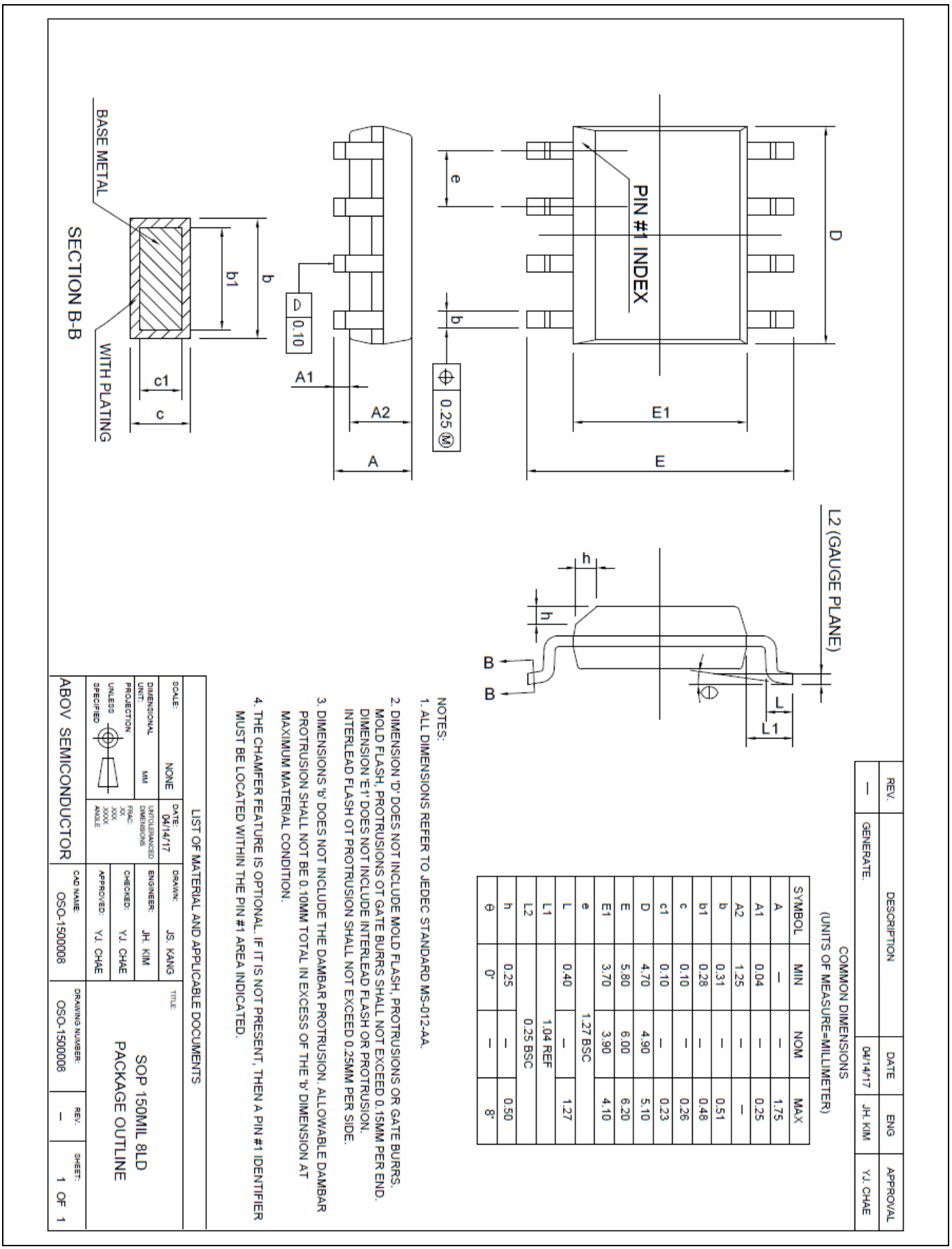


Figure 4.4 10-Pin SSOP Package



REV.	DESCRIPTION	DATE	ENG	APPROVAL
—	GENERATE.	04/14/17	JH. KIM	YJ. CHAE

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.75
A1	0.04	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
b1	0.28	—	0.48
c	0.10	—	0.26
c1	0.10	—	0.23
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e		1.27 BSC	
L	0.40	—	1.27
L1		1.04 REF	
L2		0.25 BSC	
h	0.25	—	0.50
θ	0°	—	8°

NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012-AA.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OT GATE BURRS SHALL NOT EXCEED 0.15MM PER END. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OT PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
3. DIMENSIONS 'b' DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT BE 0.10MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. THE CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN #1 IDENTIFIER MUST BE LOCATED WITHIN THE PIN #1 AREA INDICATED.

LIST OF MATERIAL AND APPLICABLE DOCUMENTS

SCALE: NONE	DATE: 04/14/17	DRAWN: JS. KANG	TITLE: SOP 150MIL 8LD PACKAGE OUTLINE
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS FRAC: XX XXX XXXX ANGLE	ENGINEER: JH. KIM	
PROJECTION		CHECKED: YJ. CHAE	
UNLESS SPECIFIED		APPROVED: YJ. CHAE	
ABOV SEMICONDUCTOR		CAD NAME: OSO-1500008	DRAWING NUMBER: OSO-1500008
			REV: —
			SHEET: 1 OF 1

Figure 4.5 8-Pin SOP Package

5 Pin Description

PIN Name	I/O	Function	@RESET	Shared with
P00	I/O	Port 0 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P03-P04 are not in the 8-Pin package.	Input	AN0/EINT0/TXD/MOSI/DSDA
P01				AN1/EINT1/RXD/MISO/DSCL
P02				AN2/EINT11/T1O/PWM1O
P03				AN3/EINT12/T2O/PWM2O/SCL
P04				AN4/EINT10/EC2/SDA
P05				AN5/AVREF/EC1/RESETB
P06				AN6/SS/XIN/SXIN
P07				AN7/SCK/XOUT/SXOUT
P10	I/O	Port 1 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P10-P17 are not in the 10-Pin/8-Pin package. The P16-P17 are not in the 16-Pin package.	Input	(SDA)
P11				(SCL)
P12				(TXD/MOSI)
P13				(RXD/MISO)
P14				(SCK)
P15				–
P16				–
P17				–
P20	I/O	Port 2 is a bit-programmable I/O port which can be configured as a schmitt-trigger input, a push-pull output, or an open-drain output. A pull-up resistor can be specified in 1-bit unit. The P20-P21 are not in the 16-Pin/10-Pin/8-Pin package.	Input	–
P21				–
EINT0	I/O	External interrupt input	Input	P00/AN0/TXD/MOSI/DSDA
EINT1	I/O	External interrupt input	Input	P01/AN1/RXD/MISO/DSCL
EINT10	I/O	External interrupt and Timer 0 capture input	Input	P04/AN4/EC2/SDA
EINT11	I/O	External interrupt and Timer 1 capture input	Input	P02/AN2/T1O/PWM1O
EINT12	I/O	External interrupt and Timer 2 capture input	Input	P03/AN3/T2O/PWM2O/SCL
T1O	I/O	Timer 1 interval output	Input	P02/AN2/EINT11/PWM1O
T2O	I/O	Timer 2 interval output	Input	P03/AN3/EINT12/PWM2O/SCL
PWM1O	I/O	Timer 1 pulse output	Input	P02/AN2/EINT11/T1O
PWM2O	I/O	Timer 2 pulse output	Input	P03/AN3/EINT12/T2O/SCL
EC1	I/O	Timer 1 event count input	Input	P05/AN5/AVREF/RESETB
EC2	I/O	Timer 2 event count input	Input	P04/AN4/EINT10/SDA
SCK	I/O	Serial 0 clock input/output	Input	P07/AN7/XOUT/SXOUT
MOSI	I/O	SPI 0 master output, slave input	Input	P00/AN0/EINT0/TXD/DSDA (P12)
MISO	I/O	SPI 0 master input, slave output	Input	P01/AN1/EINT1/RXD/DSCL (P13)
SS	I/O	SPI 0 slave select input	Input	P06/AN6/XIN/SXIN
TXD	I/O	UART 0 data output	Input	P00/AN0/EINT0/MOSI/DSDA (P12)
RXD	I/O	UART 0 data input	Input	P01/AN1/EINT1/MISO/DSCL (P13)
SCL	I/O	I2C clock input/output	Input	P03/AN3/EINT12/T2O/PWM2O (P11)
SDA	I/O	I2C data input/output	Input	P04/AN4/EINT10/EC2 (P10)

Table 5.1 Normal Pin Description

PIN Name	I/O	Function	@RESET	Shared with
AVREF	I/O	A/D converter reference voltage	Input	P05/AN5/EC1/RESETB
AN0	I/O	A/D converter analog input channels	Input	P00/EINT0/TXD/MOSI/DSDA
AN1				P01/EINT1/RXD/MISO/DSCL
AN2				P02/EINT11/T1O/PWM1O
AN3				P03/EINT12/T2O/PWM2O/SCL
AN4				P04/EINT10/EC2/SDA
AN5				P05/AVREF/EC1/RESETB
AN6				P06/SS/XIN/SXIN
AN7				P07/SCK/XOUT/SXOUT
RESETB	I/O	System reset pin with a pull-up resistor when it is selected as the RESETB by CONFIGURE OPTION	Input	P05/AN5/AVREF/EC1
DSDA	I/O	On chip debugger data input/output	Input	P00/AN0/EINT0/TXD/MOSI
DSCL	I/O	On chip debugger clock input	Input	P01/AN1/EINT1/RXD/MISO
XIN	I/O	Main oscillator pins	Input	P06/AN6/SS/SXIN
XOUT				P07/AN7/SCK/SXOUT
SXIN	I/O	Sub oscillator pins	Input	P06/AN6/SS/XIN
SXOUT				P07/AN7/SCK/XOUT
VDD, VSS	–	Power input pins	–	–

Table 5.1 Normal Pin Description (Concluded)

NOTE)

1. The P16-P17 and P20-P21 are not in the 16-Pin package.
2. The P10-P17 and P20-P21 are not in the 10-Pin package.
3. The P03-P04, P10-P17 and P20-P21 are not in the 8-Pin package.
4. The P05/RESETB pin is configured as one of the P05 and the RESETB pin by the “CONFIGURE OPTION”.
5. If the P00/AN0/EINT0/TXD/MOSI/DSDA and P01/AN1/EINT1/RXD/MISO/DSCL pins are connected to an emulator during power-on reset, the pins are automatically configured as the debugger pins.
6. The P00/AN0/EINT0/TXD/MOSI/DSDA and P01/AN1/EINT1/RXD/MISO/DSCL pins are configured as inputs with an internal pull-up resistor only during the reset or power-on reset.
7. The P06/XIN/SXIN and P07/XOUT/SXOUT pins are configured as a function pin by software control.

6 Port Structures

6.1 General Purpose I/O Port

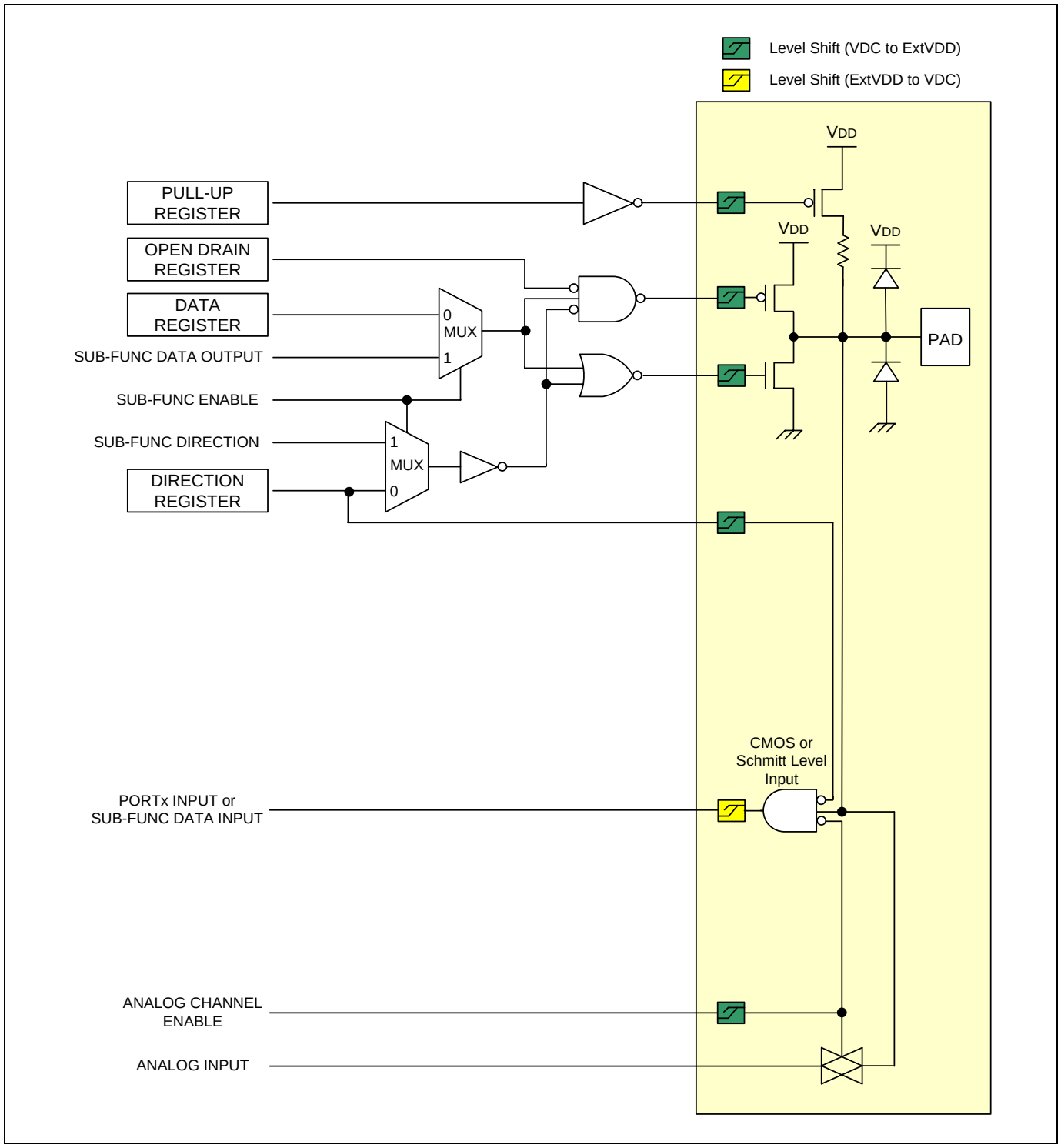


Figure 6.1 General Purpose I/O Port

6.2 External Interrupt I/O Port

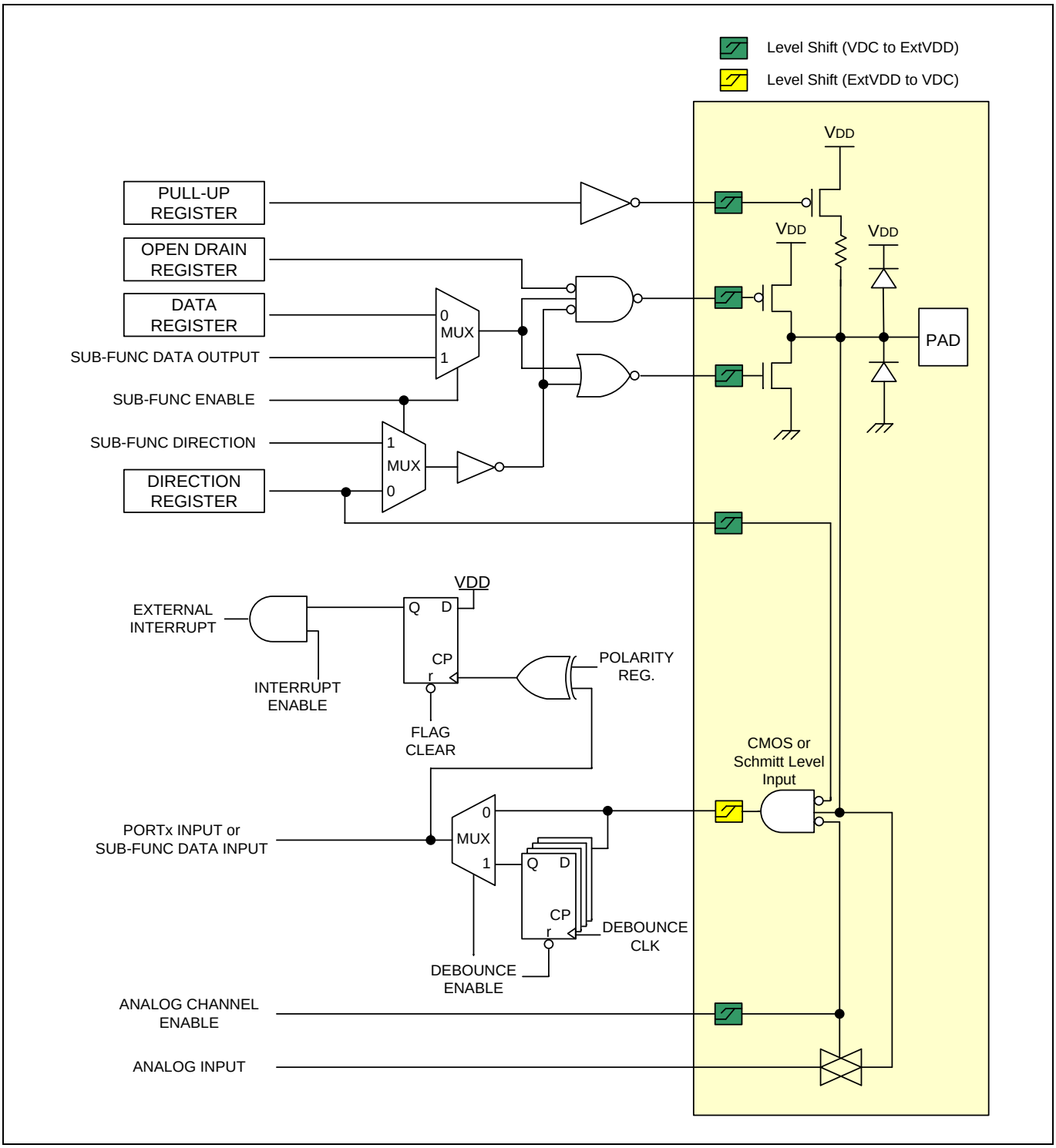


Figure 6.2 External Interrupt I/O Port

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply Voltage	VDD	-0.3 ~ +6.5	V	–
Normal Voltage Pin	V_I	-0.3 ~ VDD+0.3	V	Voltage on any pin with respect to VSS
	V_O	-0.3 ~ VDD+0.3	V	
	I_{IK}	-20 ~ +20	mA	V_I = -0.3V ~ 0V or V_I = VDD ~ VDD+0.3V
	I_{OH}	-10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	$\sum I_{OH}$	-80	mA	Maximum current ($\sum I_{OH}$)
	I_{OL}	60	mA	Maximum current sunk by (I_{OL} per I/O pin)
	$\sum I_{OL}$	120	mA	Maximum current ($\sum I_{OL}$)
Total Power Dissipation	P_T	600	mW	–
Storage Temperature	T_{STG}	-65 ~ +150	°C	–

Table 7.1 Absolute Maximum Ratings

NOTE)

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

(T_A=-40°C ~ +85°C)

Parameter	Symbol	Conditions			MIN	TYP	MAX	Unit
Operating Voltage	VDD	f_X= 32 ~ 38kHz	SX-TAL		1.8	–	5.5	V
		f_X= 0.4 ~ 4.2MHz	X-TAL	Ceramic	1.8	–	5.5	
				Crystal	2.0	–	5.5	
		f_X= 0.4 ~ 12.0MHz	X-TAL		2.7	–	5.5	
		f_X= 0.2 ~ 8.0MHz	Internal RC		1.8	–	5.5	
Operating Temperature	T_{OPR}	VDD= 1.8 ~ 5.5V			-40	–	85	°C

Table 7.2 Recommended Operating Conditions

7.3 A/D Converter Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Resolution	–	–		–	12	–	bit
Integral Linear Error	ILE	AVREF= 2.7V – 5.5V fx= 8MHz		–	–	±6	LSB
Differential Linearity Error	DLE			–	–	±1	
Top Offset Error	TOE			–	–	±5	
Zero Offset Error	ZOE			–	–	±5	
Conversion Time	t_{CON}	AVREF= 4.0V – 5.5V		20	–	–	us
		AVREF= 3.0V – 5.5V		30	–	–	
		AVREF= 2.7V – 5.5V		60	–	–	
Analog Input Voltage	V_{AN}	–		VSS	–	AVREF	V
Analog Reference Voltage	AVREF	*Note 3		1.8	–	VDD	
Internal VDC Voltage	VDD19	–		1.85	1.95	2.05	V
A/DC Input Leakage Current	IAN	AVREF=5.12V		–	–	2	uA
A/DC Current	I_{ADC}	Enable	VDD= 5.12V	–	1	2	mA
		Disable		–	–	0.1	uA

Table 7.3 A/D Converter Characteristics

NOTE)

1. Zero offset error is the difference between 000000000000 and the converted output for zero input voltage (VSS).
2. Top offset error is the difference between 111111111111 and the converted output for top input voltage (AVREF).
3. If AVREF is less than 2.7V, the resolution degrades by 1-bit whenever AVREF drops 0.1V. (@ADCLK = 0.5MHz, Under 2.7V resolution has no test.)

7.4 Power-On Reset Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESET Release Level	V_{POR}	–	–	1.4	–	V
VDD Voltage Rising Time	t_R	–	0.05	–	30.0	V/ms
POR Current	I_{POR}	–	–	0.2	–	μA

Table 7.4 Power-on Reset Characteristics

7.5 Low Voltage Reset and Low Voltage Indicator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Detection Level	V_{LVR} V_{LVI}	The LVR can select all levels but LVI can select other levels except 1.60V		–	1.60	1.79	V
				1.90	2.05	2.20	
				2.00	2.15	2.30	
				2.10	2.25	2.40	
				2.22	2.37	2.52	
				2.35	2.50	2.65	
				2.45	2.65	2.85	
				2.62	2.82	3.02	
				2.81	3.01	3.21	
				3.02	3.22	3.42	
				3.27	3.47	3.67	
				3.46	3.76	4.06	
				3.80	4.10	4.40	
				4.21	4.51	4.81	
LVR Hysteresis	△V	–		–	50	150	mV
LVI Hysteresis	△V	–		–	10	50	
Minimum Pulse Width	t_{LW}	–		100	–	–	us
LVR and LVI Current	I_{BL}	Enable (Both)	VDD= 3V, RUN Mode	–	14.0	24.0	uA
		Enable (One of two)		–	10.0	18.0	
		Disable (Both)	VDD= 3V	–	–	0.1	

Table 7.5 LVR and LVI Characteristics

7.6 High Frequency Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{HFIRC}	–		–	8	–	MHz
Tolerance	–	T_A = 0°C to +50°C		–	–	±2.0	%
		T_A = -20°C to +85°C				±3.0	
		T_A = -40°C to +85°C				±4.0	
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	T_{hfs}	–		–	–	100	us
IRC Current	I_{HFIRC}	Enable	VDD=5V	–	0.2	–	mA
		Disable		–	–	0.1	uA

Table 7.6 High Internal RC Oscillator Characteristics

7.7 Low Frequency Internal RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Frequency	f_{LFIRC}	–		–	200	–	kHz
Tolerance	–	V_{DD} = 2.2 – 5.5V, T_A = -20°C to +85°C		–	–	±3.0	%
Clock Duty Ratio	T_{OD}	–		40	50	60	%
Stabilization Time	t_{LFS}	–		–	–	100	us
IRC Current	I_{LFIRC}	Enable	VDD=5V	–	40	–	uA
		Disable		–	–	0.1	

Table 7.7 Low Internal RC Oscillator Characteristics

7.8 Internal Watch-Dog Timer RC Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Frequency	f_{WDTRC}	–	2	5	10	kHz
Stabilization Time	t_{WDTS}	–	–	–	1	ms
WDTRC Current	I_{WDTRC}	Enable	–	1	–	uA
		Disable	–	–	0.1	

Table 7.8 Internal WDTRC Oscillator Characteristics

7.9 DC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V, VSS= 0V, f_{XIN}= 12MHz)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input High Voltage	V_{IH}	P0, P1, P2, RESETB		0.8VDD	–	VDD	V
Input Low Voltage	V_{IL}	P0, P1, P2, RESETB		–	–	0.2VDD	V
Output High Voltage	V_{OH}	VDD=4.5V, IOH = – 2mA; All output ports		VDD-1.0	–	–	V
Output Low Voltage	V_{OL1}	VDD=4.5V, IOL=10mA; All output ports except VOL2		–	–	1.0	V
	V_{OL2}	VDD=4.5V, IOL=15mA; P00 –P05		–	–	1.0	
Input High Leakage Current	I_{IH}	All Input ports		–	–	1.0	μA
Input Low Leakage Current	I_{IL}	All Input ports		- 1.0	–	–	μA
Pull-Up Resistor	R_{PU1}	VI=0V, TA=25°C, All Input ports	VDD=5.0V	25	50	100	kΩ
			VDD=3.0V	50	100	200	
	R_{PU2}	VI=0V, TA=25°C, RESETB	VDD=5.0V	150	250	400	kΩ
			VDD=3.0V	300	500	700	
OSC feedback resistor	R_{X1}	XIN= VDD, XOUT= VSS T_A= 25°C, VDD= 5V		600	1200	2000	kΩ
	R_{X2}	SXIN= VDD, SXOUT= VSS T_A= 25°C, VDD= 5V		2500	5000	10000	kΩ
Supply Current	I_{DD1} (RUN)	f_{XIN} =12MHz	VDD=5V±10%	–	3.0	6.0	mA
		f_{HFIRC} =8MHz		–	2.0	4.0	
		f_{XIN} =10MHz	VDD=3V±10%	–	2.2	4.4	
		f_{LFIRC} =200kHz		–	120	240	uA
	I_{DD2} (IDLE)	f_{XIN} =12MHz	VDD=5V±10%	–	2.0	4.0	mA
		f_{HFIRC} =8MHz		–	1.0	2.0	
		f_{XIN} =10MHz	VDD=3V±10%	–	1.0	2.0	
		f_{LFIRC} =200kHz		–	65	130	uA
	I_{DD3}	f_{SUB}=32.768kHz, VDD=3V±10%, TA=25°C	Sub RUN	–	90.0	180.0	uA
	I_{DD4}		Sub IDLE	–	8.0	16.0	
	I_{DD5}	STOP, VDD= 5V±10%, T_A= 25°C		–	0.5	3.0	

Table 7.9 DC Characteristics

NOTE)

1. Where the f_{XIN} is an external main oscillator, the f_{HFIRC} and f_{LFIRC} are an internal RC oscillator, and the fx is the selected system clock, the f_{SUB} is an external sub oscillator.
2. All supply current items don't include the current of an internal Watch-dog timer RC (WDTRC) oscillator and a peripheral block.
3. All supply current items include the current of the power-on reset (POR) block.

7.10 AC Characteristics

(T_A= -40°C ~ +85°C, VDD= 1.8V ~ 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
RESETB input low width	t_{RST}	VDD= 5V	10	–	–	us
Interrupt input high, low width	t_{IWH}, t_{IWL}	All interrupt, VDD= 5V	200	–	–	ns
External Counter Input High, Low Pulse Width	t_{ECWH}, t_{ECWL}	EC1/EC2, VDD = 5V	200	–	–	
External Counter Transition Time	t_{REC}, t_{FEC}	EC1/EC2, VDD = 5V	20	–	–	

Table 7.10 AC Characteristics

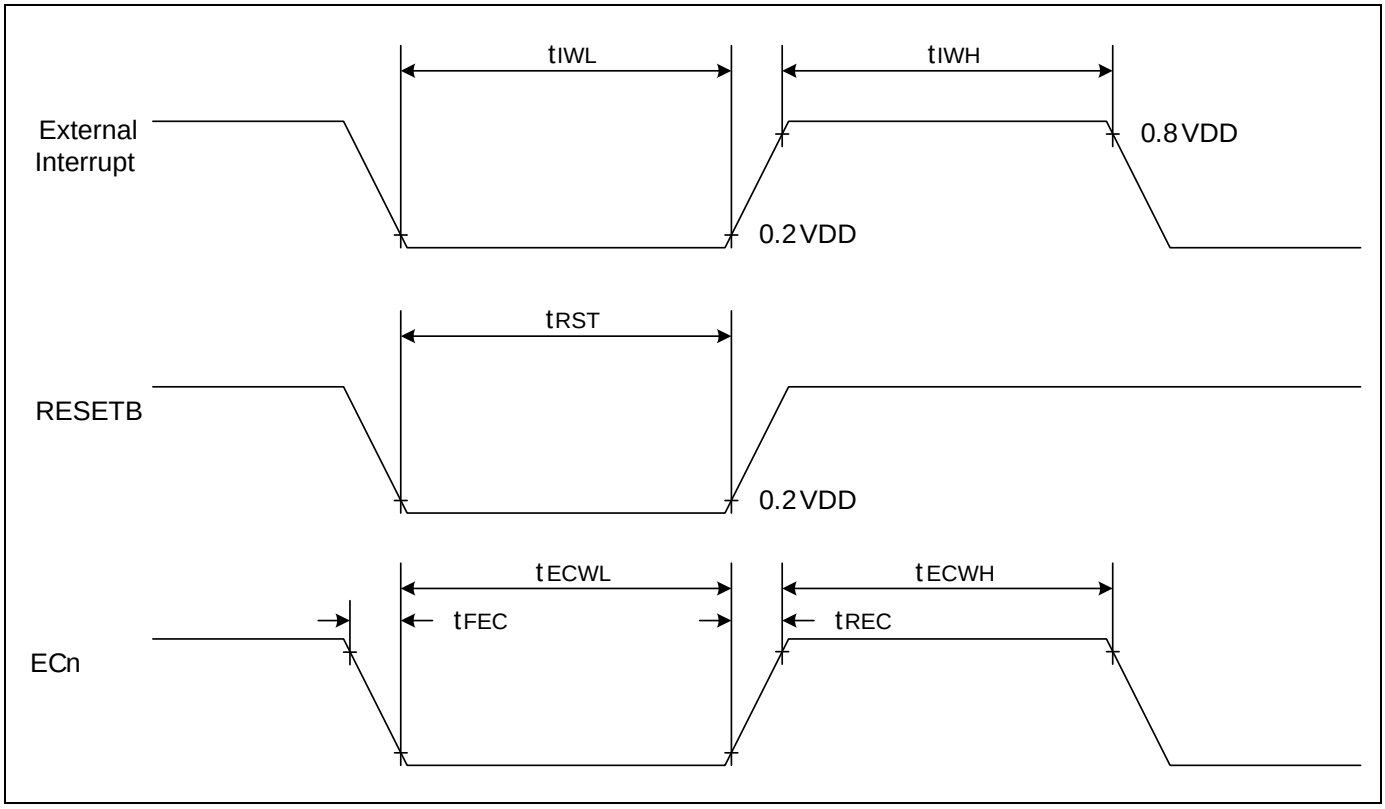


Figure 7.1 AC Timing

7.11 SPI Characteristics

(T_A=-40°C– +85°C, VDD=1.8V – 5.5V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Pulse Period	t_{SCK}	Internal SCK source	400	–	–	ns
Input Clock Pulse Period		External SCK source	400	–	–	
Output Clock High, Low Pulse Width	t_{SCKH}, t_{SCKL}	Internal SCK source	140	–	–	
Input Clock High, Low Pulse Width		External SCK source	140	–	–	
First Output Clock Delay Time	t_{FOD}	Internal/External SCK source	200	–	–	
Output Clock Delay Time	t_{DS}	–	–	–	50	
Input Setup Time	t_{DIS}	–	200	–	–	
Input Hold Time	t_{DIH}	–	200	–	–	

Table 7.11 SPI Characteristics

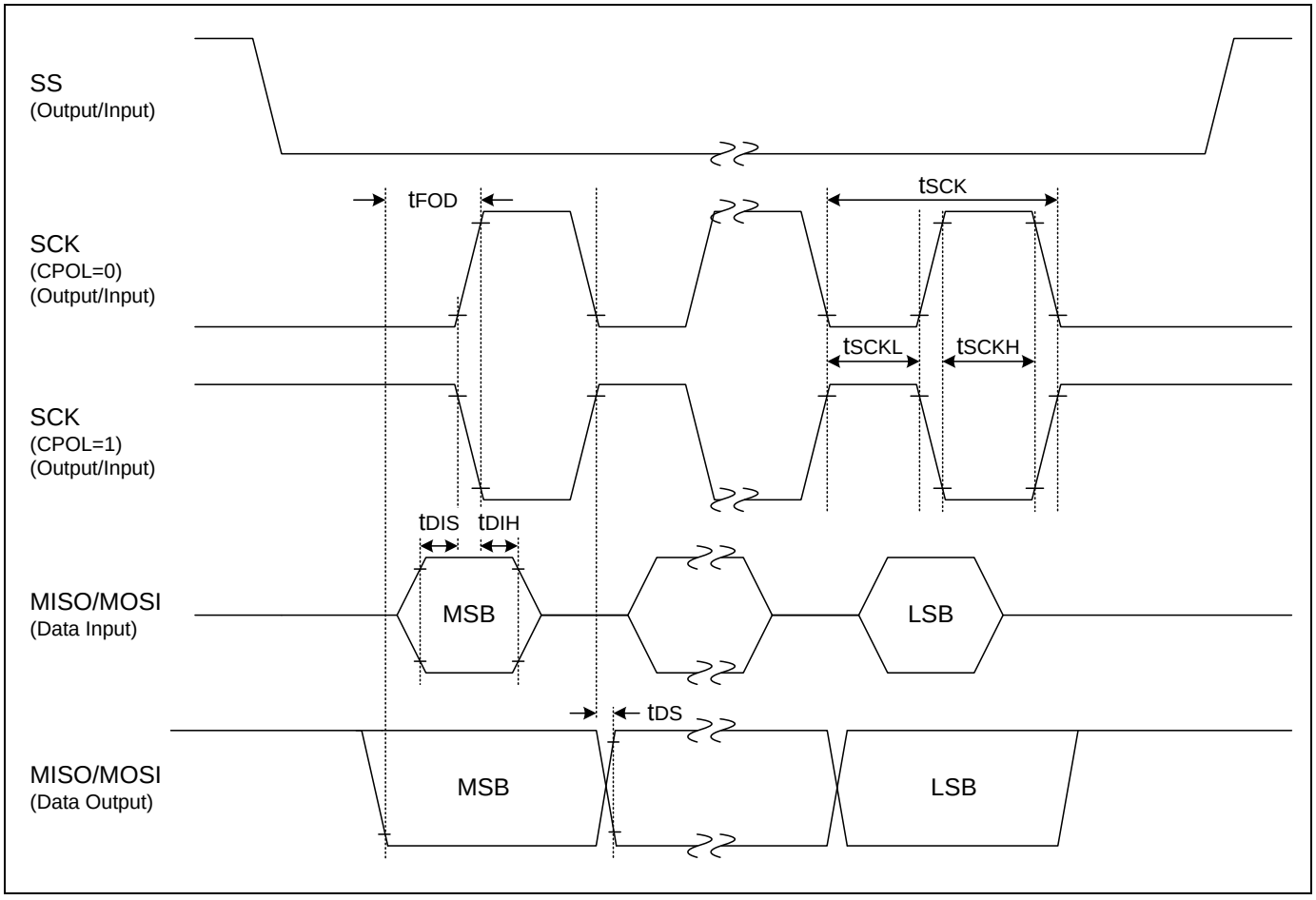


Figure 7.2 SPI Timing

7.12 UART Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, f_{XIN}=11.1MHz)

Parameter	Symbol	MIN	TYP	MAX	Unit
Serial port clock cycle time	t_{SCK}	1250	t_{CPU} x 16	1650	ns
Output data setup to clock rising edge	t_{S1}	590	t_{CPU} x 13	–	
Clock rising edge to input data valid	t_{S2}	–	–	590	
Output data hold after clock rising edge	t_{H1}	t_{CPU}- 50	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	470	t_{CPU} x 8	970	

Table 7.12 UART Characteristics

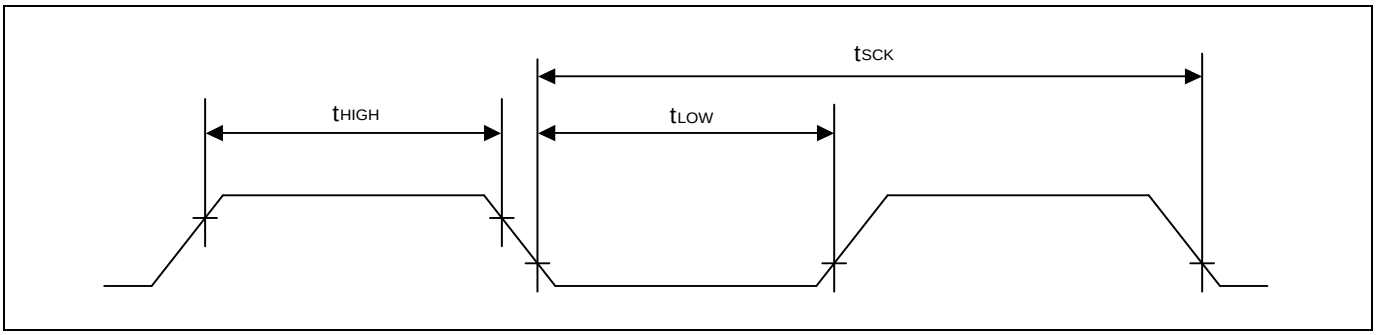


Figure 7.3 Waveform for UART Timing Characteristics

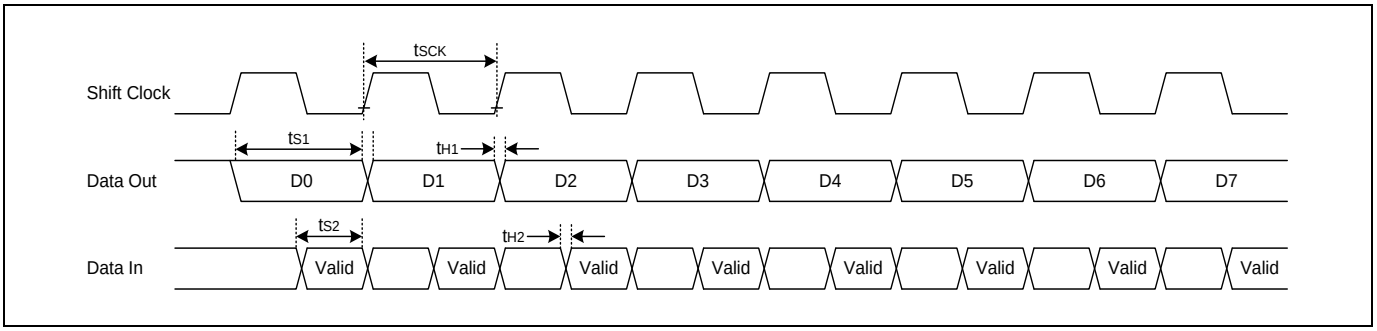


Figure 7.4 Timing Waveform for the UART Module

7.13 I2C Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Parameter	Symbol	Standard Mode		High-Speed Mode		Unit
		MIN	MAX	MIN	MAX	
Clock frequency	t_{SCL}	0	100	0	400	kHz
Clock High Pulse Width	t_{SCLH}	4.0	–	0.6	–	us
Clock Low Pulse Width	t_{SCLL}	4.7	–	1.3	–	
Bus Free Time	t_{BF}	4.7	–	1.3	–	
Start Condition Setup Time	t_{STSU}	4.7	–	0.6	–	
Start Condition Hold Time	t_{STHD}	4.0	–	0.6	–	
Stop Condition Setup Time	t_{SPSU}	4.0	–	0.6	–	
Stop Condition Hold Time	t_{SPHD}	4.0	–	0.6	–	
Output Valid from Clock	t_{VD}	0	–	0	–	
Data Input Hold Time	t_{DIH}	0	–	0	1.0	
Data Input Setup Time	t_{DIS}	250	–	100	–	ns

Table 7.13 I2C Characteristics

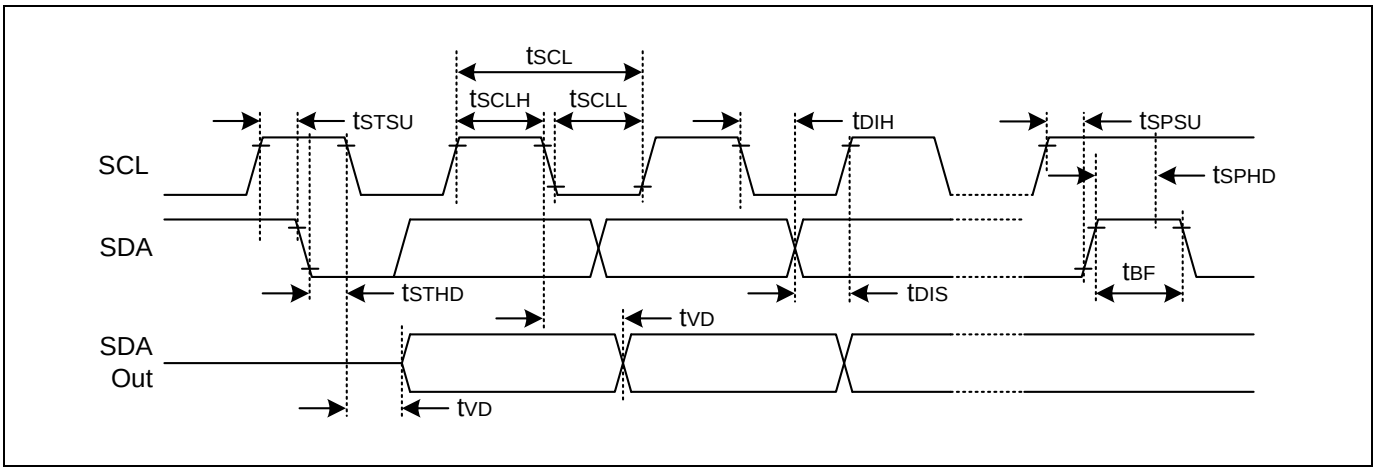


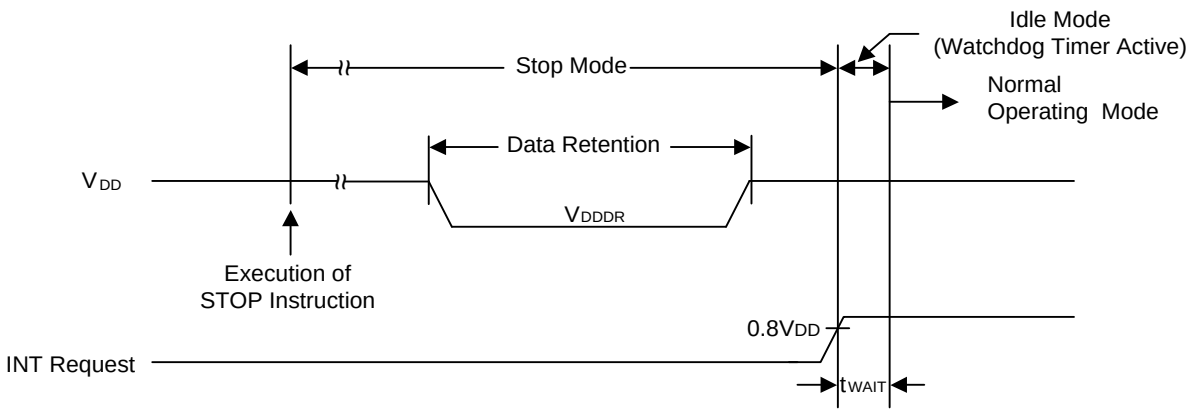
Figure 7.5 I2C Timing

7.14 Data Retention Voltage in Stop Mode

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

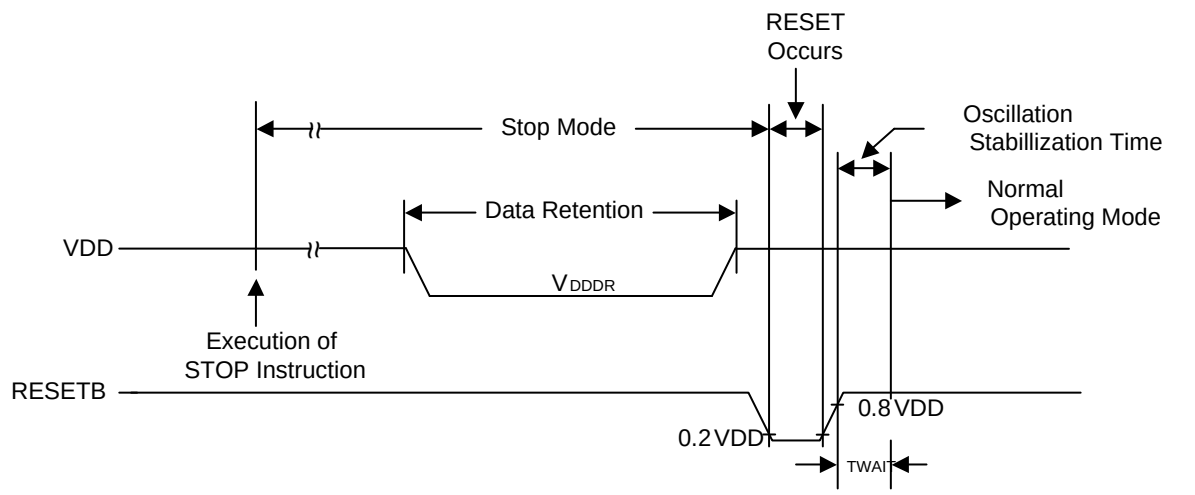
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	VDDR= 1.8V, (T_A= 25°C), Stop mode	–	–	1	uA

Table 7.14 Data Retention Voltage in Stop Mode



NOTE: tWAIT is the same as (the selected bit overflow of BIT) X 1/(BIT Clock)

Figure 7.6 Stop Mode Release Timing when Initiated by an Interrupt



NOTE : tWAIT is the same as (4096 X 4 X 1/fx) (16.4ms @ 1MHz)

Figure 7.7 Stop Mode Release Timing when Initiated by RESETB

7.15 Internal Flash Rom Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V, VSS= 0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Sector Write Time	t_{FSW}	–	–	2.5	2.7	ms
Sector Erase Time	t_{FSE}	–	–	2.5	2.7	
Code Write Protection Time	t_{FHL}	–	–	2.5	2.7	
Page Buffer Reset Time	t_{FBR}	–	–	–	5	us
Flash Programming Frequency	f_{PGM}	–	0.4	–	–	MHz
Endurance of Write/Erase	NF_{WE}	–	–	–	10,000	times
Flash Data Retention Time	t_{RT}	–	10	–	–	years

Table 7.15 Internal Flash Rom Characteristics

NOTE)

1. During a flash operation, SCLK[1:0] of SCCR must be set to “00” or “01” (INT-RC OSC or Main X-TAL for system clock).

7.16 Input/Output Capacitance

(T_A=-40°C ~ +85°C, VDD=0V)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Capacitance	C_{IN}	fx= 1MHz Unmeasured pins are connected to VSS	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 7.16 Input/Output Capacitance

7.17 Main Clock Oscillator Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Main oscillation frequency	2.0V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
Ceramic Oscillator	Main oscillation frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	
External Clock	XIN input frequency	1.8V – 5.5V	0.4	–	4.2	MHz
		2.7V – 5.5V	0.4	–	12.0	

Table 7.17 Main Clock Oscillator Characteristics

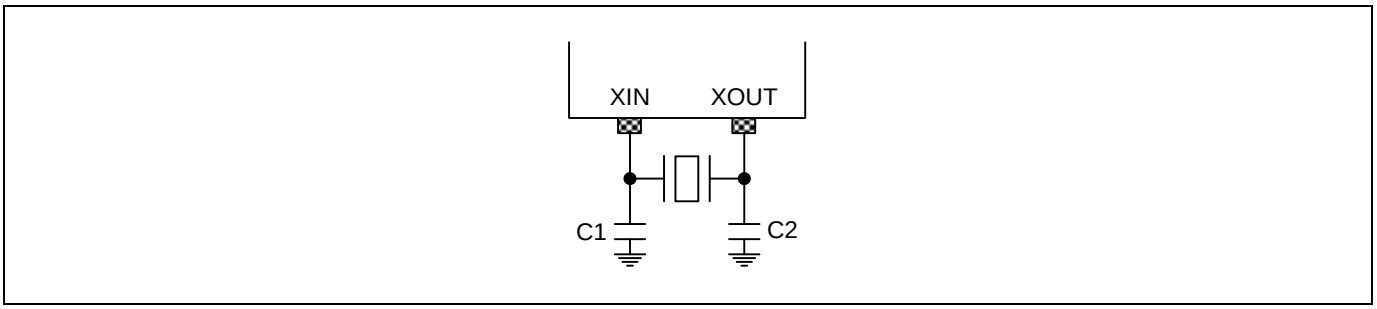


Figure 7.8 Crystal/Ceramic Oscillator

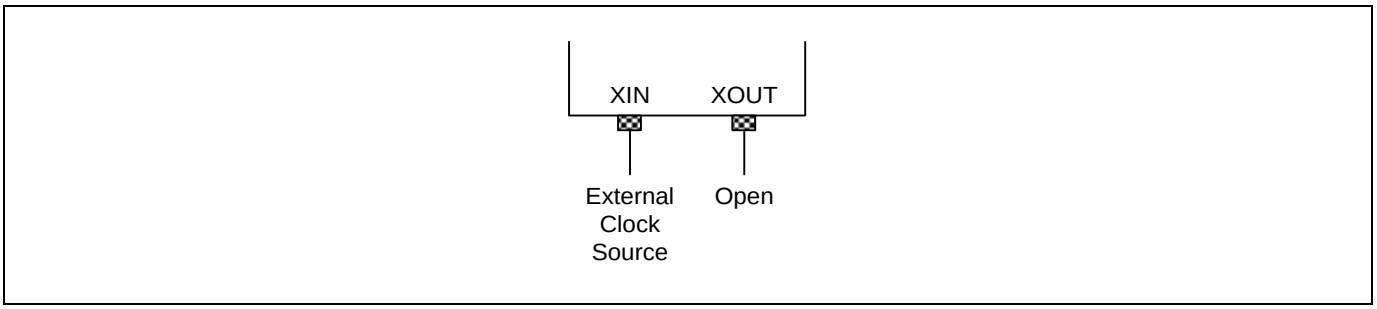


Figure 7.9 External Clock

7.18 Sub Clock Oscillator Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	Condition	MIN	TYP	MAX	Unit
Crystal	Sub oscillation frequency	1.8V – 5.5V	32	32.768	38	kHz
External Clock	SXIN input frequency		32	–	100	kHz

Table 7.18 Sub Clock Oscillator Characteristics

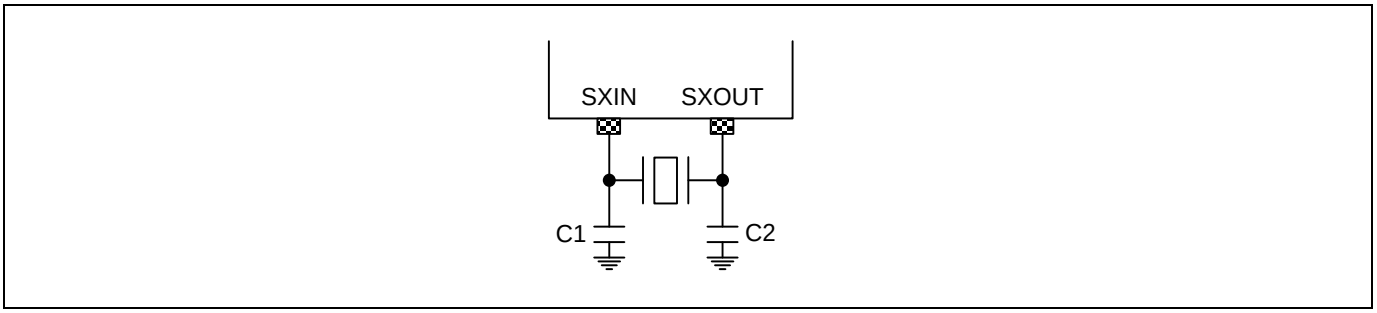


Figure 7.10 Crystal Oscillator

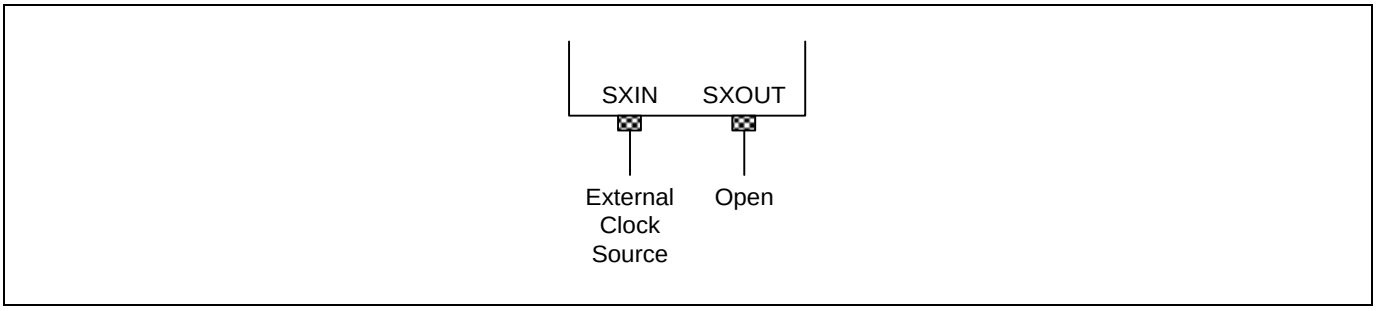


Figure 7.11 External Clock

7.19 Main Oscillation Stabilization Characteristics

(T_A=-40°C ~ +85°C, VDD=1.8V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	fx > 1MHz, VDD = 2.0V~5.5V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	60	ms
Ceramic	fx > 1MHz, VDD = 1.8V~5.5V Oscillation stabilization occurs when VDD is equal to the minimum oscillator voltage range.	–	–	10	ms
External Clock	f_{XIN} = 0.4 to 12MHz XIN input high and low width (t_{XH}, t_{XL})	41.7	–	1250	ns

Table 7.19 Main Oscillation Stabilization Characteristics

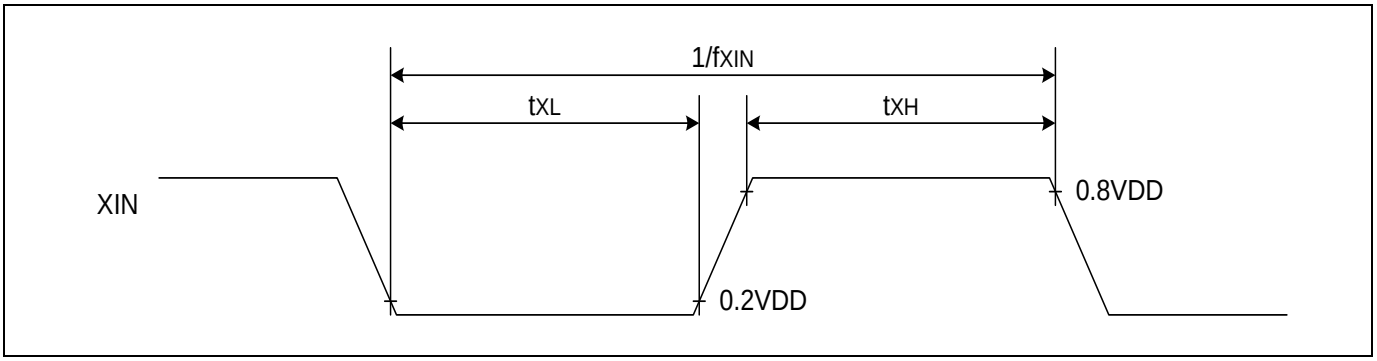


Figure 7.12 Clock Timing Measurement at XIN

7.20 Sub Oscillation Characteristics

(T_A = -40°C ~ +85°C, VDD = 2.2V ~ 5.5V)

Oscillator	Parameter	MIN	TYP	MAX	Unit
Crystal	–	–	–	10	s
External Clock	SXIN input high and low width (t_{XH}, t_{XL})	5	–	15	us

Table 7.20 Sub Oscillation Stabilization Characteristics

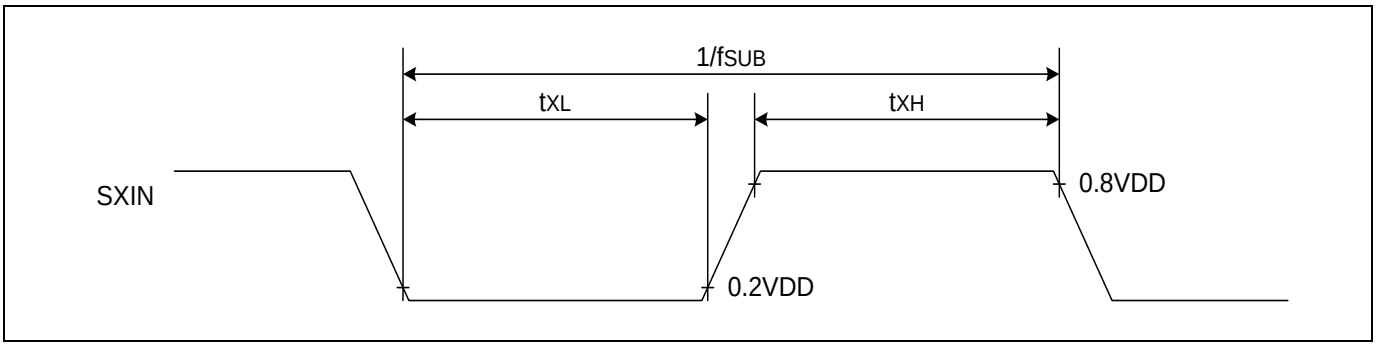


Figure 7.13 Clock Timing Measurement at SXIN

7.21 Operating Voltage Range

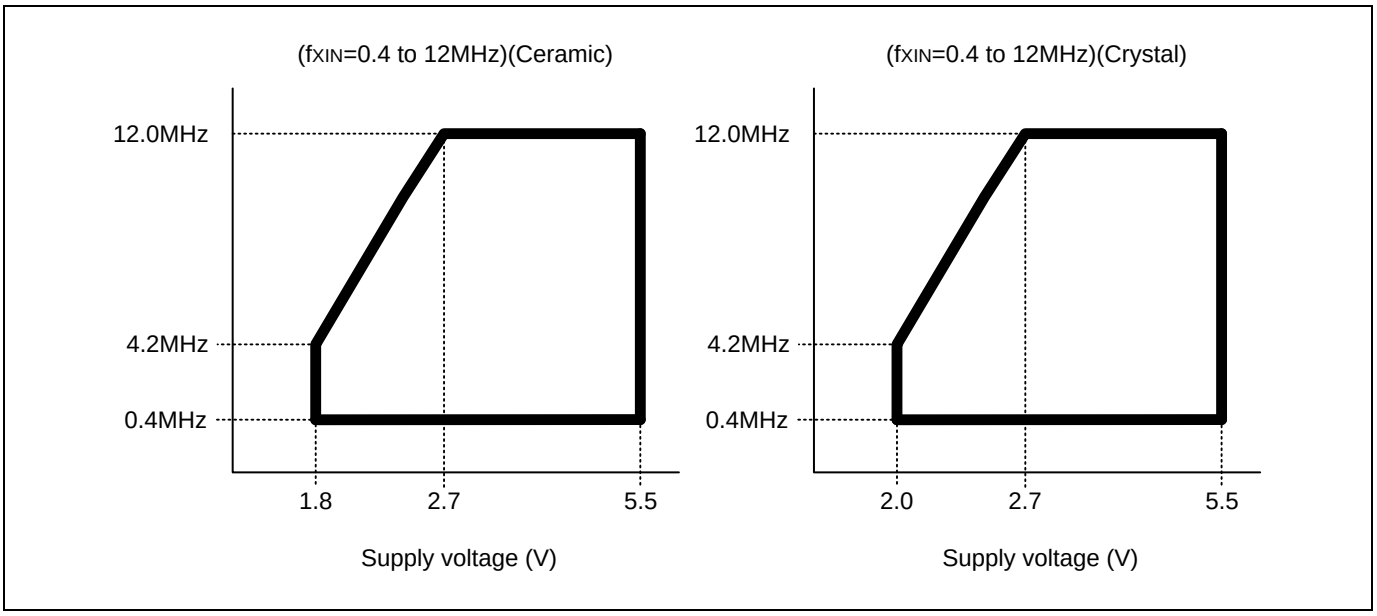


Figure 7.14 Operating Voltage Range (Main OSC)

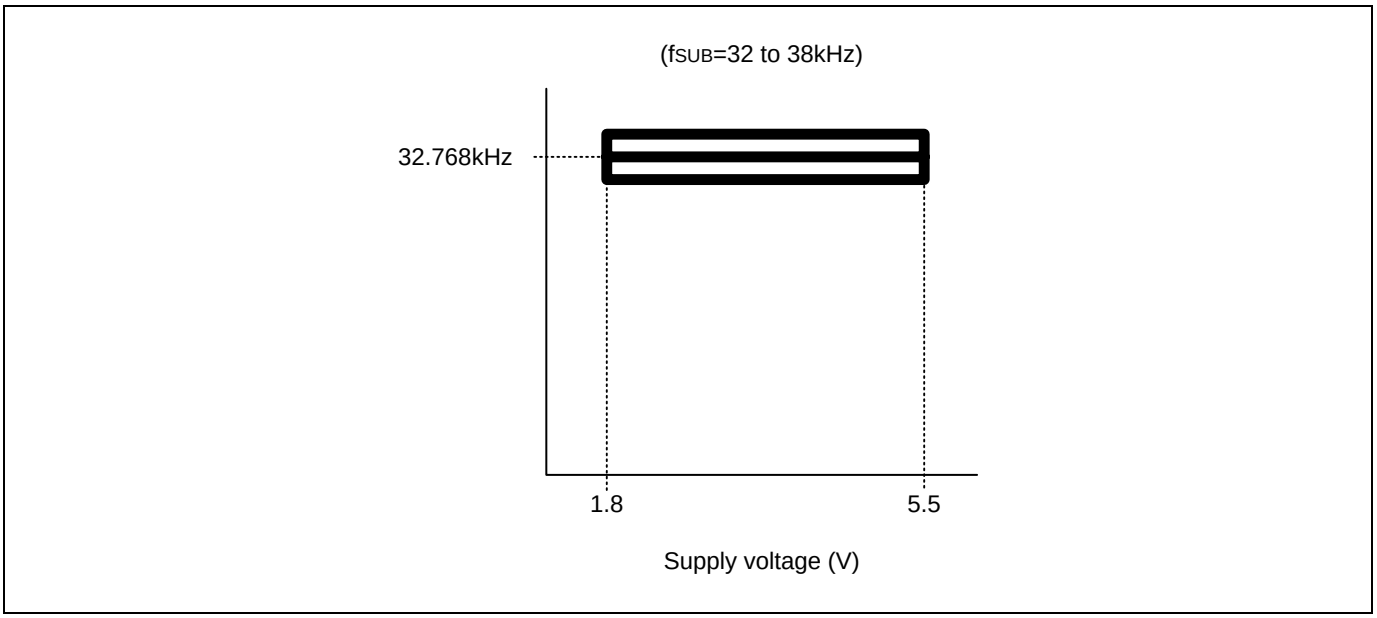


Figure 7.15 Operating Voltage Range (Sub OSC)

7.22 Recommended Circuit and Layout

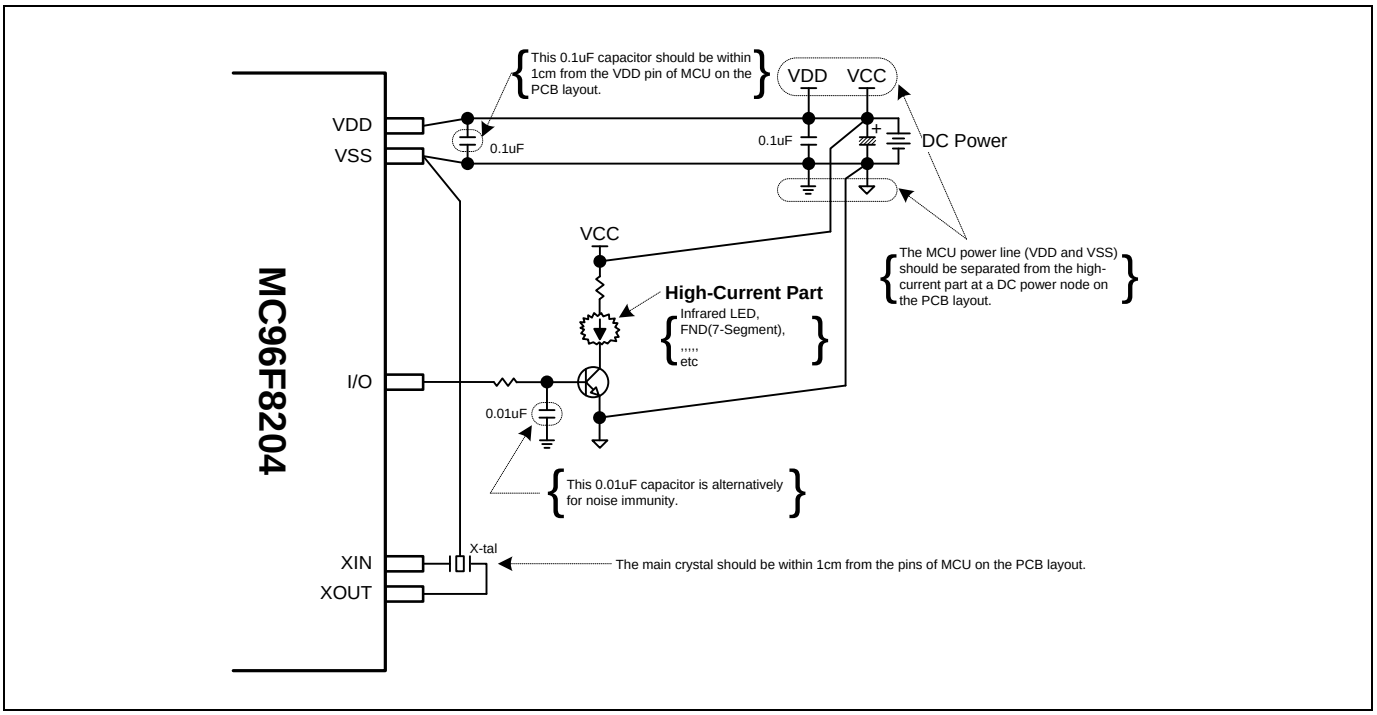


Figure 7.16 Recommended Circuit and Layout for Main X-TAL OSC

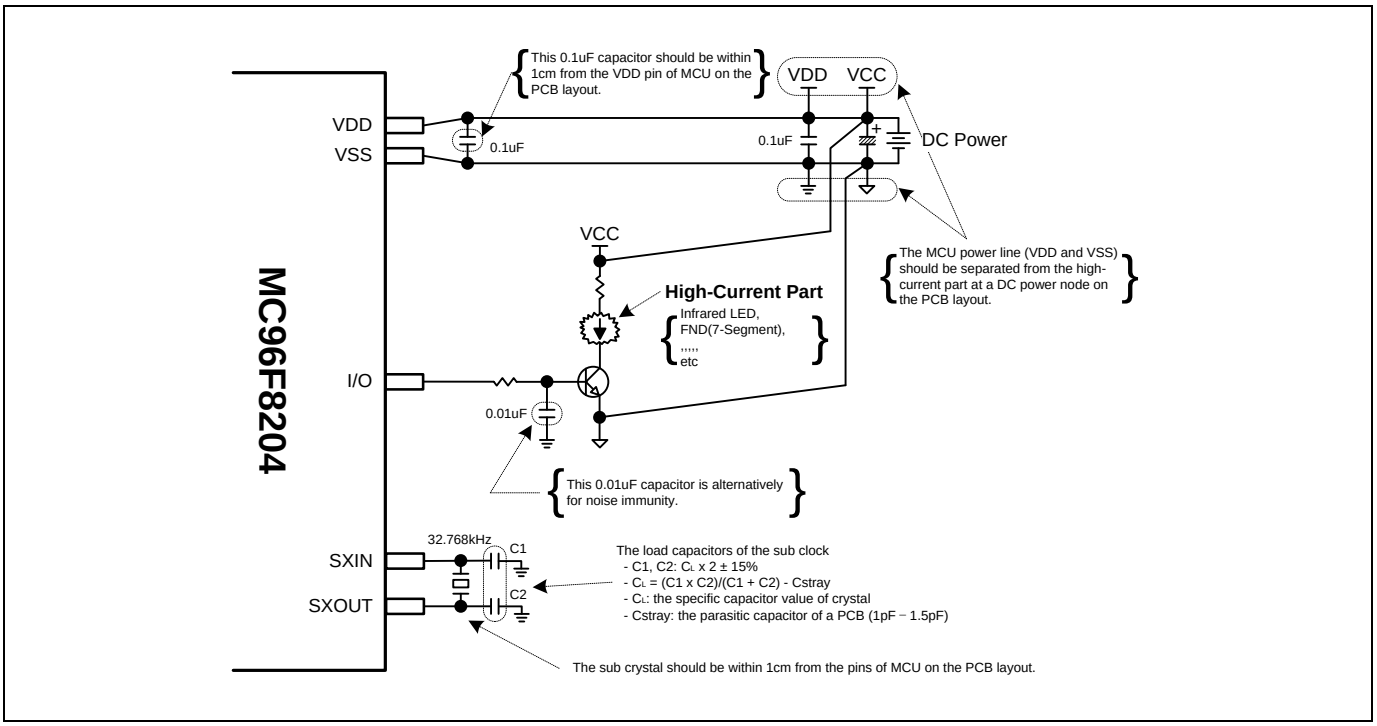
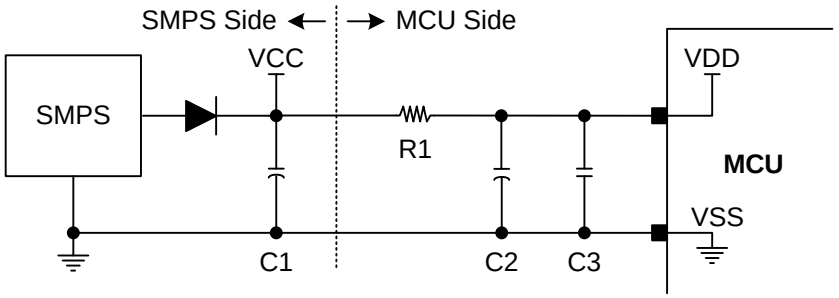


Figure 7.17 Recommended Circuit and Layout for Sub X-TAL OSC

7.23 Recommended Circuit and Layout with SMPS Power



1. The C1 capacitor is to flatten out the voltage of the SMPS power, VCC.
   √ Recommended C1: 470uF/25V more.
2. The R1 and C2 are the RC filter for VDD and suppress the ripple of VCC.
   √ Recommended R1: 10Ω - 20Ω
   √ Recommended C2: 47uF/25V more
   √ The R1 and C2 should be as close by the C3 as possible.
3. The C3 capacitor is used for temperature compensation because an electrolytic capacitor becomes worse characteristics at low temperature.
   √ Recommended C3: ceramic capacitor 2.2uF more
   √ The C3 should be within 1cm from VDD pin of MCU on the PCB layout.
4. The above circuit is recommended to improve noise immunity (EFT, Surge, ESD, etc) when the SMPS supplies the VDD of MCU.

Figure 7.18 Recommended Circuit and with SMPS Power

7.24 Typical Characteristics

These graphs and tables provided in this section are only for design guidance and are not tested or guaranteed. In graphs or tables some data are out of specified operating range (e.g. out of specified VDD range). This is only for information and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

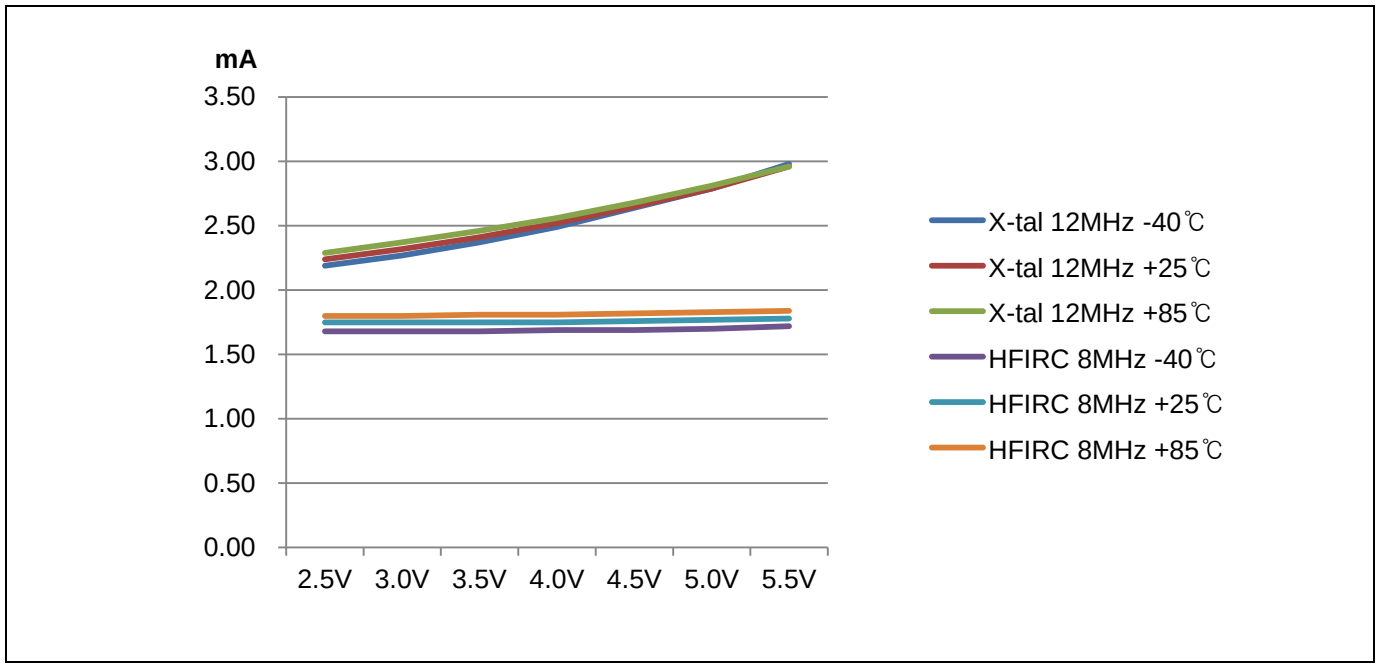


Figure 7.19 X-TAL, HFIRC RUN (IDD1) Current

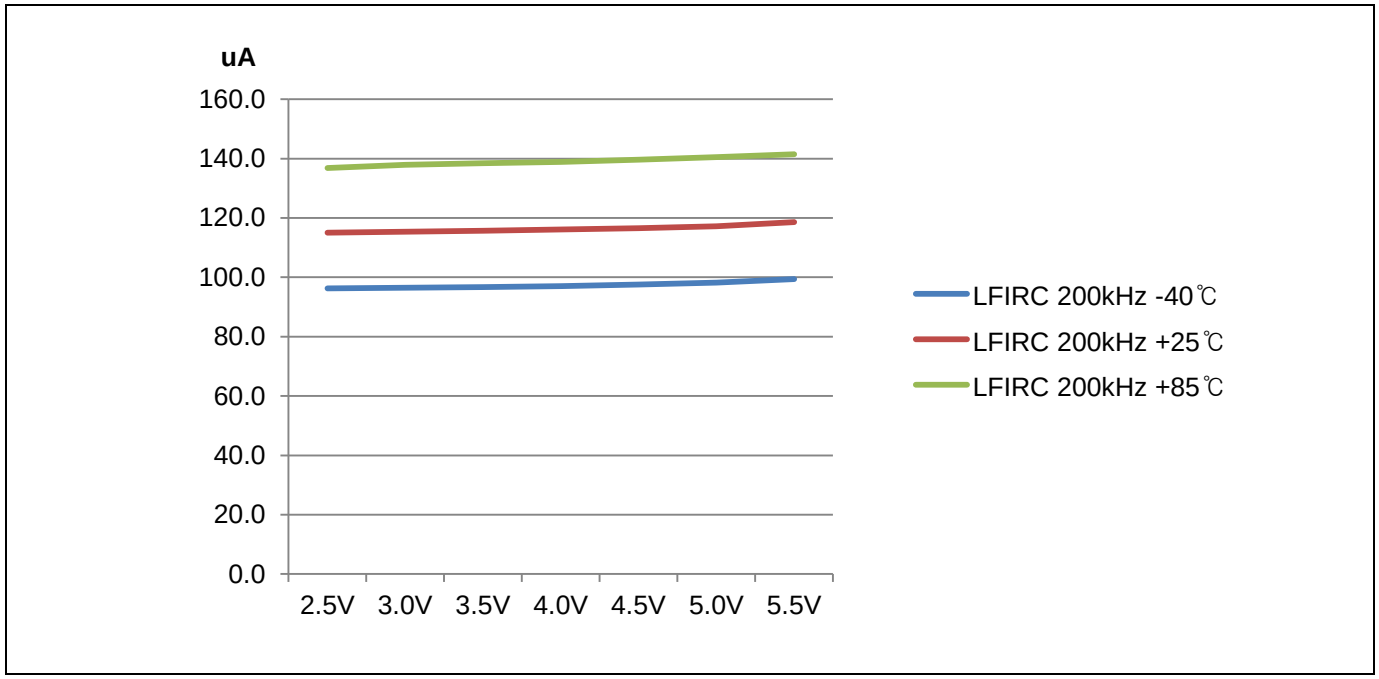


Figure 7.20 LFIRC RUN (IDD1) Current

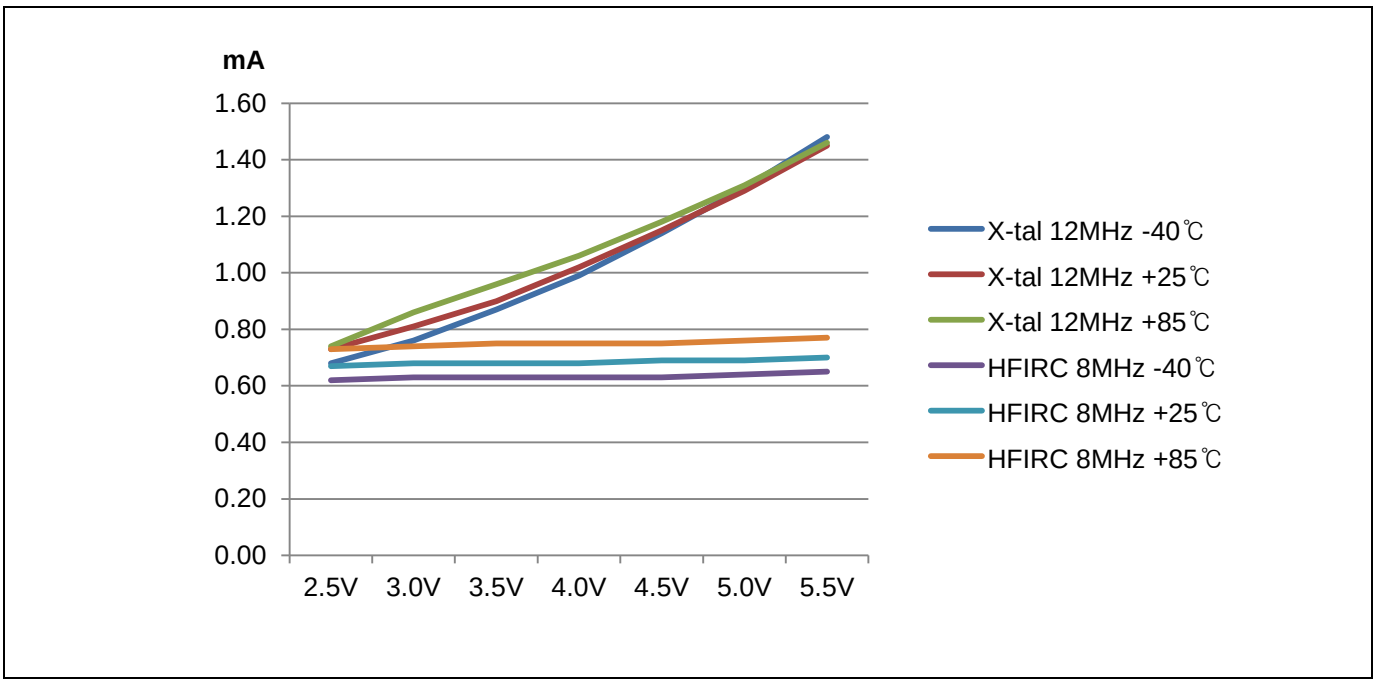


Figure 7.21 X-TAL, HFIRC IDLE (IDD2) Current

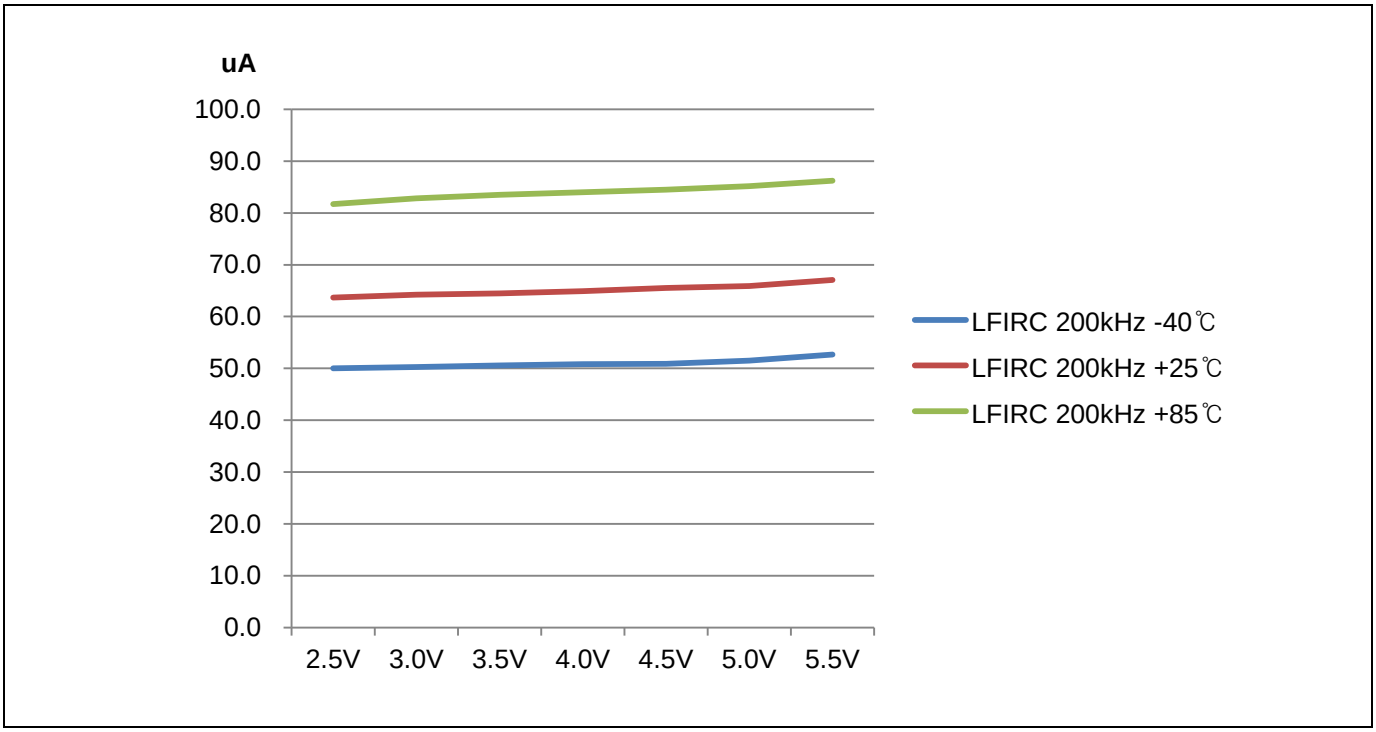


Figure 7.22 LFIRC IDLE (IDD2) Current

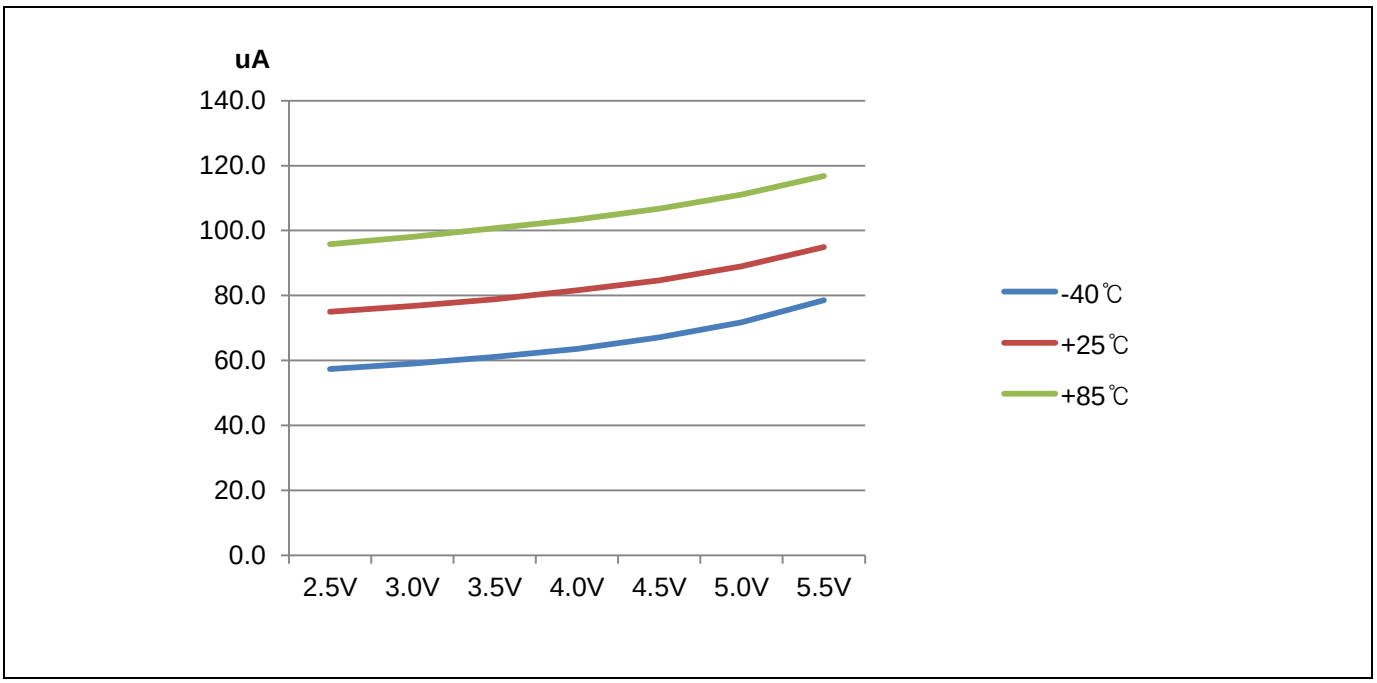


Figure 7.23 SUB RUN (IDD3) Current

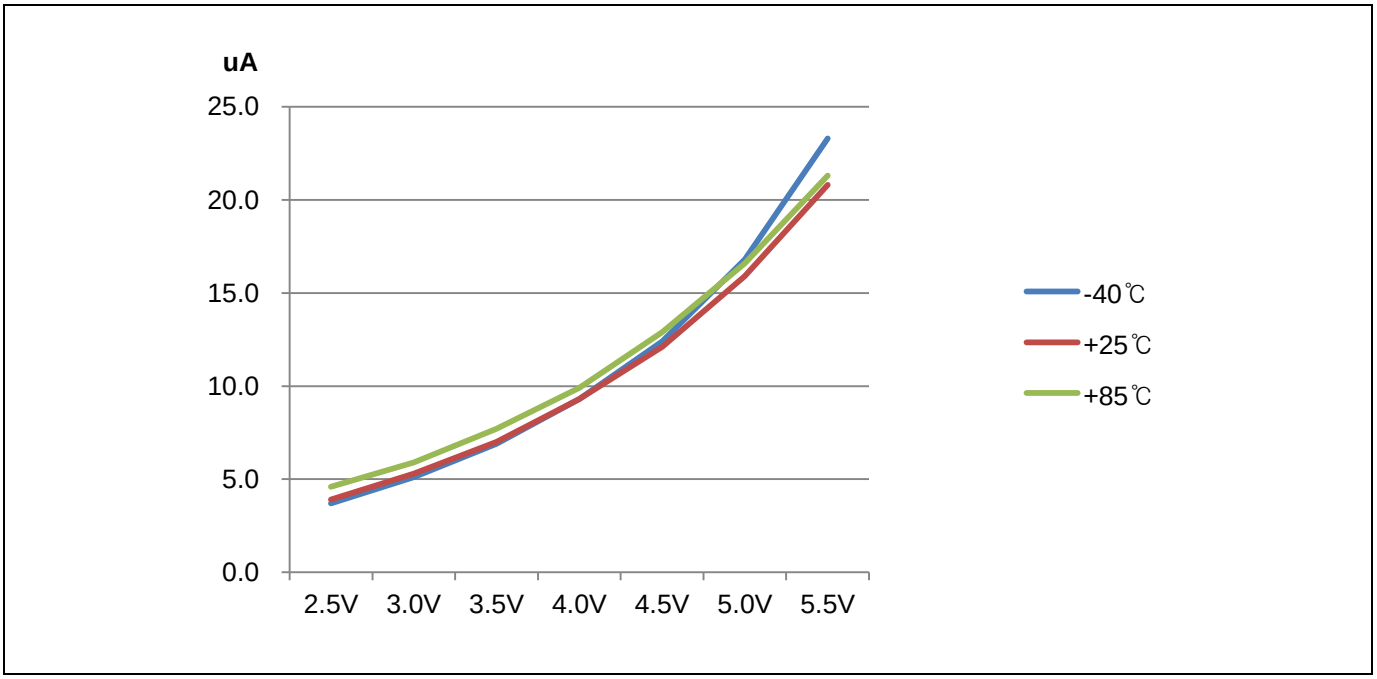


Figure 7.24 SUB IDLE (IDD4) Current

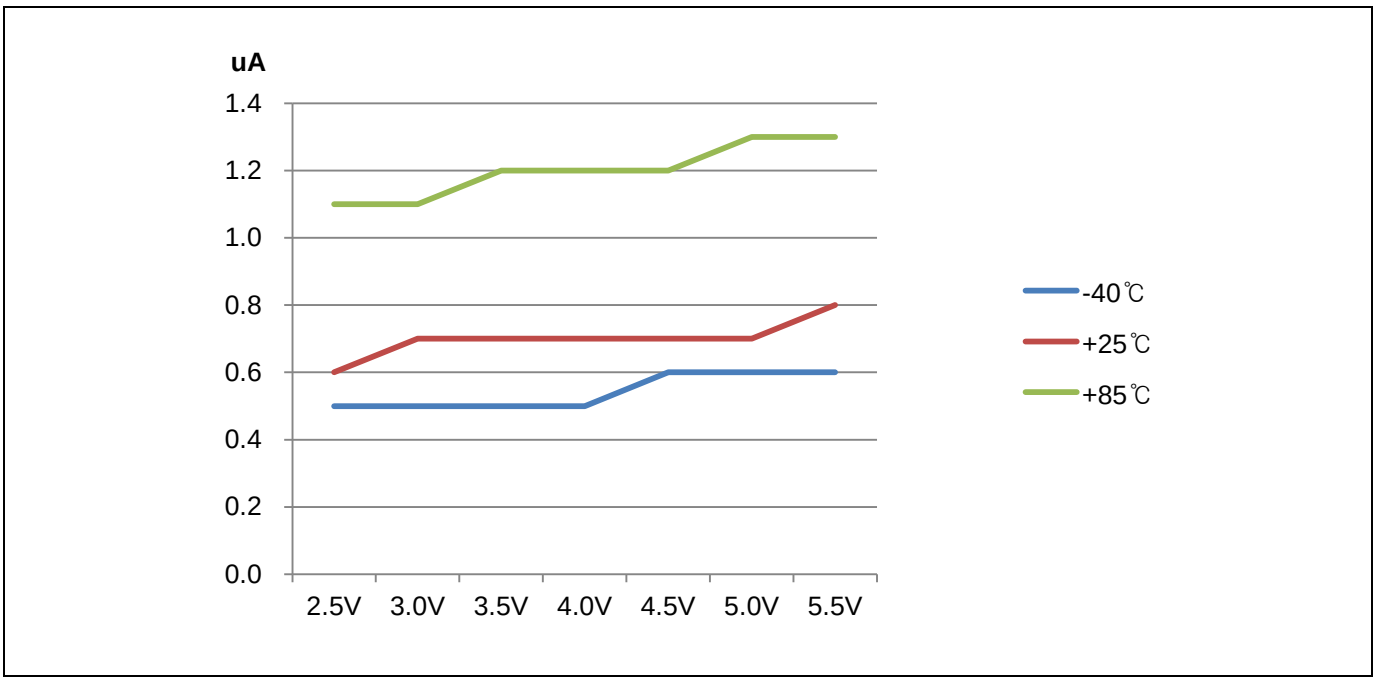


Figure 7.25 STOP (IDD5) Current

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