NSi8210

High Reliability Single-Channel Digital Isolators

Datasheet (EN) 1.2

Product Overview

NSi8210 is a high reliability single channel digital isolator. The NSi8210 device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of NSi8210 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. NSi8210 provides default output level configuration when the input power is lost. Wide supply voltage of NSi8210 supports to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

Key Features

- Up to 5000V_{rms} Insulation voltage
- Date rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- All devices are AEC-Q100 qualified
- High CMTI: 200kV/us
- Chip level ESD: HBM: ±8kV
- Interlock function
- High system level EMC performance:
  - Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation surge voltage: >10kV
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40℃~125℃
- RoHS-compliant packages:
  - SOP8 narrow body
  - SOW8 wide body
  - SOW16 wide body

Safety Regulatory Approvals

- UL recognition: up to 5000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor Control

Device Information

Part Number	*Package*	*Body Size*
NSi8210Nx-XSPR	SOP8	4.90mm × 3.90mm
NSi8210Wx-XSWVR	SOW8	5.85mm × 7.50mm
NSi8210Wx-XSWR	SOW16	10.30mm × 7.50mm

Functional Block Diagrams

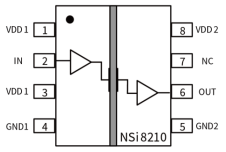

Figure 1. NSi8210Nx-XSPR Block Diagram

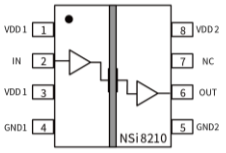

Figure 2. NSi8210Wx-XSWVR Block Diagram

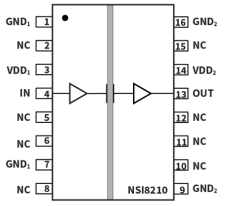

Figure 3. NSi8210Wx-XSWR Block Diagram

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1. Pin Configuration and Functions

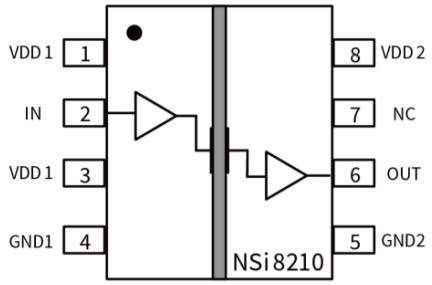


Figure 1.1 NSi8210N Package

Table 1.1 NSi8210N Pin Configuration and Description

NSi8210N PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power Supply for Isolator Side 1
2	IN	Logic Input
3	VDD1	Power Supply for Isolator Side 1
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUT	Logic Output
7	NC	Not connect pin; it has no internal connection
8	VDD2	Power Supply for Isolator Side 2

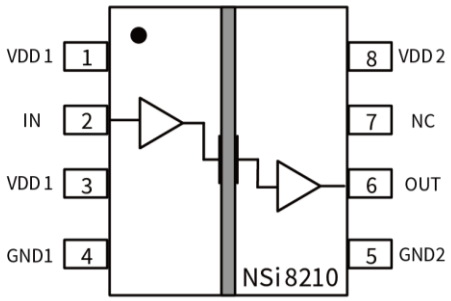


Figure 1.2NSi8210W SOW8 Package

Table 1.2 NSi8210W SOW8 Pin Configuration and Description

NSi8210W PIN NO.	SYMBOL	FUNCTION
1	VDD1	Power Supply for Isolator Side 1
2	IN	Logic Input
3	VDD1	Power Supply for Isolator Side 1
4	GND1	Ground 1, the ground reference for Isolator Side 1
5	GND2	Ground 2, the ground reference for Isolator Side 2
6	OUT	Logic Output
7	NC	Not connect pin; it has no internal connection
8	VDD2	Power Supply for Isolator Side 2

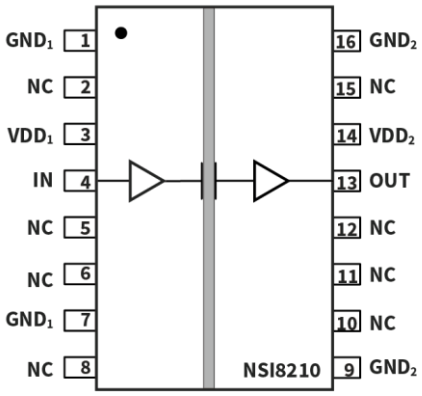


Figure 1.3 NSi8210W SOW16 Package

Table 1.3NSi8210W SOW16 Pin Configuration and Description

NSi8210W PIN NO.	SYMBOL	FUNCTION
1	GND1	Ground 1, the ground reference for Isolator Side 1
2	NC	Not connect pin; it has no internal connection
3	VDD1	Power Supply for Isolator Side 1
4	IN	Logic Input
5	NC	Not connect pin; it has no internal connection
6	NC	Not connect pin; it has no internal connection
7	GND1	Ground 1, the ground reference for Isolator Side 1

8	NC	Not connect pin; it has no internal connection
9	GND2	Ground 2, the ground reference for Isolator Side 2
10	NC	Not connect pin; it has no internal connection
11	NC	Not connect pin; it has no internal connection
12	NC	Not connect pin; it has no internal connection
13	OUT	Logic Output
14	VDD2	Power Supply for Isolator Side 2
15	NC	Not connect pin; it has no internal connection
16	GND2	Ground 2, the ground reference for Isolator Side 2

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	IN	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Output Voltage	OUT	-0.4		VDD+0.4	V	The maximum voltage must not exceed 6.5V
Maximum Input/Output Pulse Voltage	IN, OUT	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Output current	Io	-15		15	mA	
Maximum Surge Isolation Voltage	V_{IOSM}			6.25	kV	$V_{TEST}=V_{IOSM}\times1.6$
Operating Temperature	Topr	-40		125	℃	
Junction Temperature	Tj	-40		150	℃	
Storage Temperature	Tstg	-65		150	℃	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VDD1, VDD2	2.5		5.5	V	
High-level Input Voltage	VIH	2			V	
Low-level Input Voltage	VIL			0.8	V	
Data Rate	DR	0		150	Mbps	
Ambient Temperature	Ta	-40		125	℃	

4. Thermal Information

Parameters	*Symbol*	*SOW16*	*SOW8*	*SOP8*	*Unit*
IC Junction-to-Air Thermal Resistance	θ_{JA}	94.4	84.3	146.1	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	57.3	36.3	63.1	°C/W
Junction-to-board thermal resistance	θ_{JB}	57.1	47.0	80.0	°C/W

5. Specifications

5.1. Electrical Characteristics

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power on Reset	VDD_{POR}		2.2		V	POR threshold as during power-up
	VDD_{HYS}		0.1		V	POR threshold Hysteresis
Input Threshold	V_{IT}		1.6		V	Input Threshold at rising edge
	V_{IT_HYS}		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V_{IH}	2			V	
Low Level Input Voltage	V_{IL}			0.8	V	
High Level Output Voltage	V_{OH}	VDD-0.4			V	I_{OH} =- 4mA
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 4mA
Output Impedance	R_{out}		50		ohm	
Input Pull high or low Current	I_{pull}		8	15	uA	
Start Up Time after POR	trbs		10		usec	
Common Mode Transient Immunity	CMTI	±200	±250		kV/us	See Figure 5.6 , C_L = 15pF

5.2. Supply Current Characteristics – 5V

(VDD1=VDD2=5V ± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1=VDD2=5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	IDD1(Q0)		0.64	0.96	mA	All Input 0V for NSi8210N0 or All Input at supply for NSi8210N1
	IDD2(Q0)		1.27	1.91	mA	
	IDD1(Q1)		1.66	2.49	mA	All Input at supply for NSi8210N0 or All Input 0V for NSi8210N1
	IDD2(Q1)		1.28	1.92	mA	
	IDD1(1M)		1.16	1.74	mA	All Input with 1Mbps, CL=15pF
	IDD2(1M)		1.33	2.00	mA	
	IDD1(10M)		1.17	1.76	mA	All Input with 10Mbps, CL=15pF
	IDD2(10M)		1.78	2.67	mA	
	IDD1(100M)		1.34	2.01	mA	All Input with 100Mbps, CL=15pF
	IDD2(100M)		6.16	9.24	mA	

5.3. Supply Current Characteristics – 3.3V

(VDD1=VDD2=3.3V ± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1=VDD2=3.3V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	IDD1(Q0)		0.6	0.9	mA	All Input 0V for NSi8210N0 or All Input at supply for NSi8210N1
	IDD2(Q0)		1.22	1.83	mA	
	IDD1(Q1)		1.62	2.43	mA	All Input at supply for NSi8210N0 or All Input 0V for NSi8210N1
	IDD2(Q1)		1.23	1.85	mA	
	IDD1(1M)		1.11	1.67	mA	All Input with 1Mbps, CL=15pF
	IDD2(1M)		1.26	1.89	mA	
	IDD1(10M)		1.12	1.68	mA	All Input with 10Mbps, CL=15pF
	IDD2(10M)		1.56	2.34	mA	
	IDD1(100M)		1.17	1.76	mA	All Input with 100Mbps, CL=15pF
	IDD2(100M)		4.48	6.72	mA	

5.4. Supply Current Characteristics – 2.5V

(VDD1=VDD2=2.5V ± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1=VDD2=2.5V,** Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Supply current	IDD1(Q0)		0.58	0.87	mA	All Input 0V for NSi8210N0 or All Input at supply for NSi8210N1
	IDD2(Q0)		1.2	1.8	mA	
	IDD1(Q1)		1.6	2.4	mA	All Input at supply for NSi8210N0 or All Input 0V for NSi8210N1
	IDD2(Q1)		1.2	1.8	mA	
	IDD1(1M)		1.09	1.64	mA	All Input with 1Mbps, CL=15pF
	IDD2(1M)		1.23	1.85	mA	
	IDD1(10M)		1.10	1.65	mA	All Input with 10Mbps, CL=15pF
	IDD2(10M)		1.46	2.19	mA	
	IDD1(100M)		1.07	1.61	mA	All Input with 100Mbps, CL=15pF
	IDD2(100M)		3.72	5.58	mA	

5.5. Switching Characteristics – 5V

(VDD1=5V± 10%, VDD2=5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 5V, VDD2 = 5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	6.54	15	ns	See Figure 5.5 , C_L = 15pF
	t_{PHL}	2.5	8.30	15	ns	See Figure 5.5 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.5 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.6. Switching Characteristics – 3.3V

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 3.3V, VDD2 = 3.3V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	8.0	15	ns	See Figure 5.5 , C_L = 15pF
	t_{PHL}	2.5	8.7	15	ns	See Figure 5.5 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.5 , C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.5 , C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.7. Switching Characteristics – 2.5V

(VDD1=2.5V± 10%, VDD2=2.5V± 10%, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at **VDD1 = 2.5V, VDD2 = 2.5V,** Ta = 25℃)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t_{PLH}	2.5	9.0	15	ns	See Figure 5.5 , C_L = 15pF
	t_{PHL}	2.5	9.3	15	ns	See Figure 5.5 , C_L = 15pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	PWD			5.0	ns	See Figure 5.5 , C_L = 15pF
Rising Time	t_r			5.0	ns	See Figure 5.5, C_L = 15pF
Falling Time	t_f			5.0	ns	See Figure 5.5, C_L = 15pF
Peak Eye Diagram Jitter	t_{JIT}(PK)		350		ps	
Channel-to-Channel Delay Skew	t_{SK}(c2c)			2.5	ns	
Part-to-Part Delay Skew	t_{SK}(p2p)			5.0	ns	

5.8. Typical Performance Characteristics

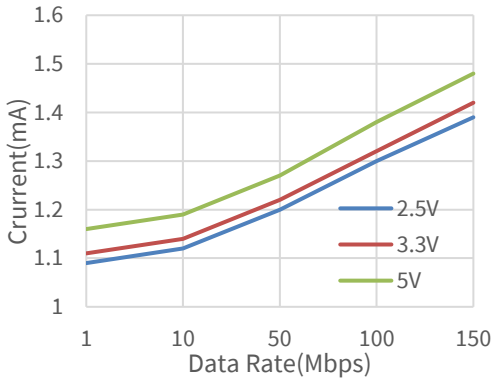


Figure 5.1 NSi8210 VDD1 Supply Current vs Data Rate

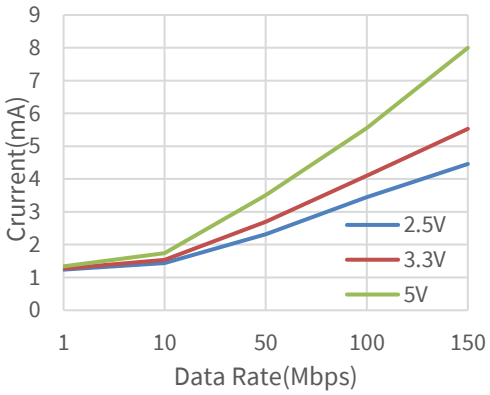


Figure 5.2 NSi8210 VDD2 Supply Current vs Data Rate

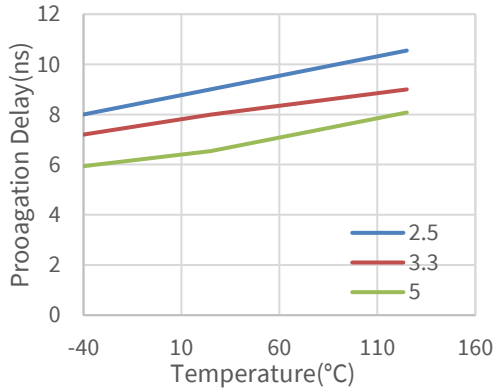


Figure 5.3 Rising Edge Propagation Delay Vs Temp

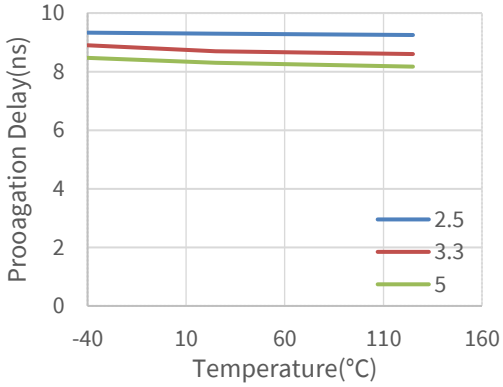


Figure 5.4 Falling Edge Propagation Delay Vs Temp

5.9. Parameter Measurement Information

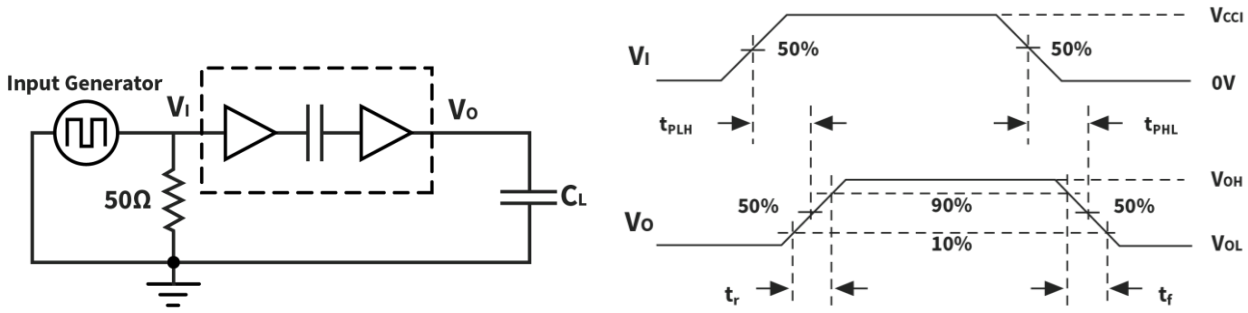


Figure 5.5 Switching Characteristics Test Circuit and Waveform

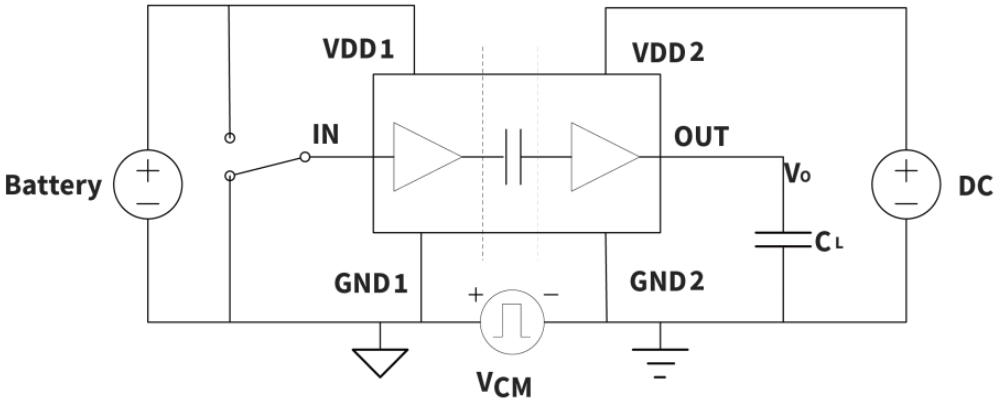


Figure 5.6 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Description	*Test Condition*	*Symbol*	*Value*			*Unit*
			SOP8	SOW8	SOW16	
Minimum External Air Gap (Clearance)		L(I01)	4.0	8.0	8.0	mm
Minimum External Tracking (Creepage)		L(I02)	4.0	8.0	8.0	mm
Minimum internal gap		DTI	28			um
Tracking Resistance(Comparative Tracking Index)	DIN EN 60112 (VDE 0303-11)	CTI	>400	>600	>600	**V**
Material Group	IEC 60112		Ⅱ	Ⅰ	Ⅰ	
Installation Classification per DIN VDE 0110						
For Rated Mains Voltage ≤ 150V_{rms}			Ⅰ to Ⅳ	Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 400V_{rms}			Ⅰ to Ⅲ	Ⅰ to Ⅳ	Ⅰ to Ⅳ	
Climatic Classification			10/105/21	10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	2	
Maximum repetitive isolation voltage		V_{IORM}	565	2121	2121	Vpeak
Input to Output Test Voltage, Method B1	V_{IORM} × 1.5 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, q_{pd} < 5 pC	$V_{pd(m)}$	847	/	/	Vpeak
	V_{IORM} × 1.875 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 sec, q_{pd} < 5 pC		/	3977	3977	
Input to Output Test Voltage, Method A						
After Environmental Tests Subgroup 1	V_{IORM} × 1.2=$V_{pd(m)}$, t_{ini} = 60 sec, t_m=10 sec, q_{pd} < 5 pC	$V_{pd(m)}$	678	/	/	Vpeak
	V_{IORM} × 1.6=$V_{pd(m)}$, t_{ini} = 60 sec, t_m=10 sec, q_{pd} < 5 pC		/	3394	3394	
After Input and /or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2= $V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	678	2545	2545	Vpeak

Description	Test Condition	Symbol	Value			Unit
Maximum transient isolation voltage	t = 60 sec	VIOTM	5300	8000	8000	Vpeak
Maximum withstanding isolation voltage	V_{TEST}= V_{ISO}, t = 60 s (qualification); VTEST= 1.2 × VISO, t = 1 s (100%production)	VISO	3750	5000	5000	V_{RMS}
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.3	VIOSM	5384			Vpeak
	Test method per IEC60065,1.2/50us waveform, VTEST=VIOSM×1.6			6250	6250	Vpeak
Isolation resistance	V_{IO}=500V at T_{amb}=T_S	RIO	>10^9	>10^9	>10^9	Ω
	V_{IO}=500V at 100℃≤T_{amb}≤125℃		>10^{11}	>10^{11}	>10^{11}	Ω
Isolation capacitance	f = 1MHz	CIO	0.6	0.6	0.6	pF
Input capacitance		CI	2	2	2	pF
Total Power Dissipation at 25℃		Ps	856	1483	1324	mW
Safety input, output, or supply current	θJA = 146.1 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	156			mA
	θJA = 84.3 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C			269.6		
	θJA = 94.4 °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C				240.8	mA
Case Temperature		Ts	150	150	150	℃

6.2. Safety-Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi8210N-DSPR SOP8(150mil)

Description	Test Condition	Value	Unit
Safety Supply Power	$R_{θJA}$ = 146.1 ℃/W, T J = 150 ℃, T A = 25 ℃	856	mW
Safety Supply Current	$R_{θJA}$ = 146.1 ℃/W, V I = 5.5 V, T J = 150 ℃, T A = 25 ℃	156	mA
Safety Temperature[2)]		150	°C

1) Calculate with the junction-to-air thermal resistance, $R_{θJA}$, of SOP8(150mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

2) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

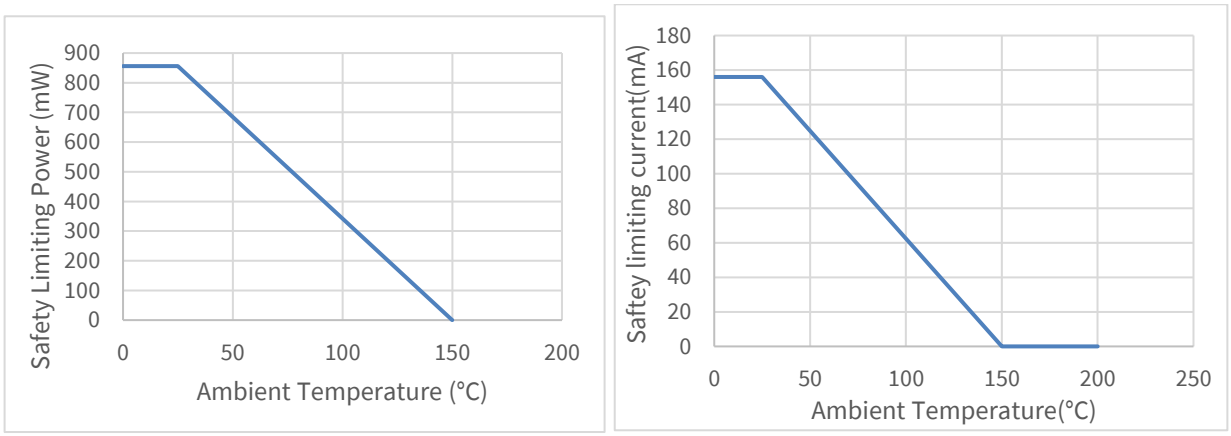


Figure 6.1 NSi8210N-DSPR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi8210W-DSWVR SOW8(300mil)

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 84.3℃/W, T J = 150 ℃, T A = 25 ℃	1483	mW
Safety Supply Current	$R_{\theta JA}$ = 84.3℃/W, V I = 5.5 V, T J = 150 ℃, T A = 25 ℃	270	mA
Safety Temperature[2)]		150	℃

3) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW8(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

4) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

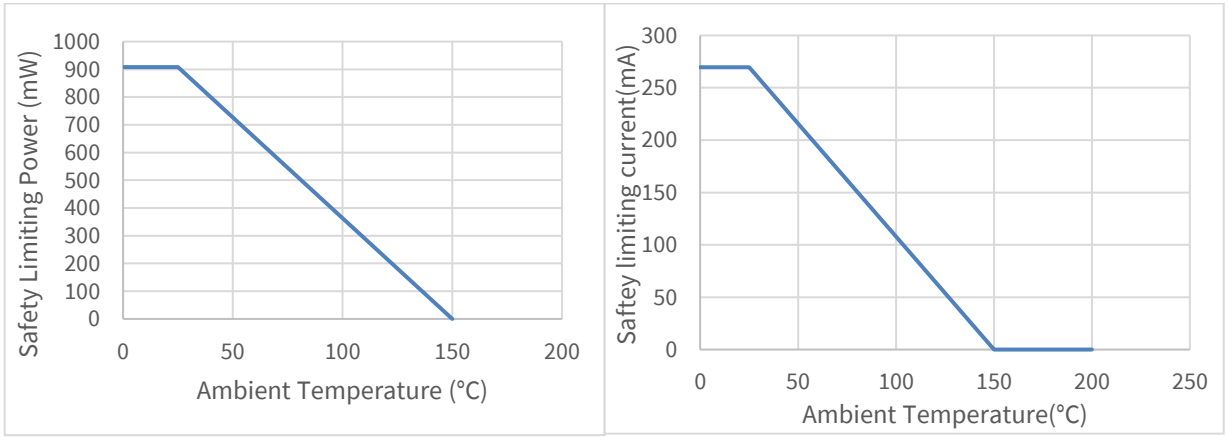


Figure 6.2 NSi8210W-DSWVR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

Reinforced isolation safety-limiting values as outlined in VDE-0884-11 of NSi8210W-DSWR SOW16(300mil)

Description	*Test Condition*	*Value*	*Unit*
Safety Supply Power	$R_{\theta JA}$ = 94.4℃/W, T J = 150 ℃, T A = 25 ℃	1324	mW
Safety Supply Current	$R_{\theta JA}$ = 94.4℃/W, V I = 5.5 V, T J = 150 ℃, T A = 25 ℃	241	mA
Safety Temperature[2)]		150	℃

5) Calculate with the junction-to-air thermal resistance, $R_{\theta JA}$, of SOW16(300mil) package (***Thermal Information Table***) which is that of a device installed on a low effective thermal conductivity test board (1s) according to JESD51-3.

6) The maximum safety temperature has the same value as the maximum junction temperature (T_J) specified for the device.

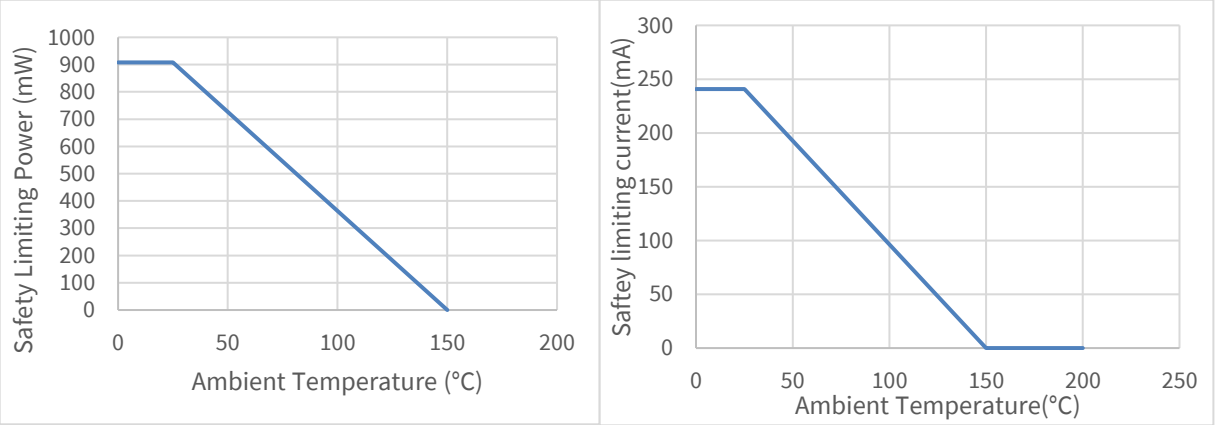


Figure 6.3 NSi8210W-DSWR Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi8210N are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11:2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750V_{rms} Isolation voltage	Single Protection, 3750V_{rms} Isolation voltage	Basic Insulation 565Vpeak, V_{IOSM}=5384Vpeak	Basic insulation at 400V_{rms} (565Vpeak)
File (E500602)	File (E500602)	File (pending)	File (CQC20001264940)

The NSi8210W-DSWVR are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation at 1500V_{rms} (2121Vpeak)
File (pending)	File (pending)	File (5024579-4880-0002 / 276211)	File (CQC20001264938)

The NSi8210W-DSWR are approved by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforced Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation at 1500V_{rms} (2121Vpeak)
File (pending)	File (pending)	File (5024579-4880-0002 / 276211)	File (CQC20001264939)

7. Function Description

7.1. Overview

The NSi8210 is a single-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

NSi8210 is a high reliability single channel digital isolator with AEC-Q100(Grade 1) qualified, it's certified by UL1577 and support 3.75kVrms insulation withstand voltage, while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of NSi8210 is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 200kV/us. NSi8210 provides default output level configuration when the input power is lost. Wide supply voltage of NSi8210 supports to connect with most digital interface directly, easy to do the level shift.

NSi8210 has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 7.1, which helps for diagnosis when power is missing at the transmitter side. The other outputs follow the same status with the input A within 1us after powering up respectively.

Table 7.1 Output status vs. power status with interlock function

Input	*VDD1 status*	*VDD2 status*	*Output*	*Comment*
H[1]	Ready	Ready	H	Normal operation.
L[2]	Ready	Ready	L	
X[3]	Unready	Ready	L(NSi8210x0) H(NSi8210x1)	The output follows the same status with the input within 20us after input side VDD1 is powered on.
X	Ready	Unready	X	The output follows the same status with the input within 20us after output side VDD2 is powered on.
Note: [1]H=Logic high; [2]L=Logic low; [3]X=Logic low or logic high				

7.2. OOK Modulation

NSi8210 is based on a capacitive isolation barrier technique and the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, as shown in Figure 7.1 & Figure 7.2, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side. The modulation uses OOK modulation technique with key benefits of high noise immunity and low radiation EMI.

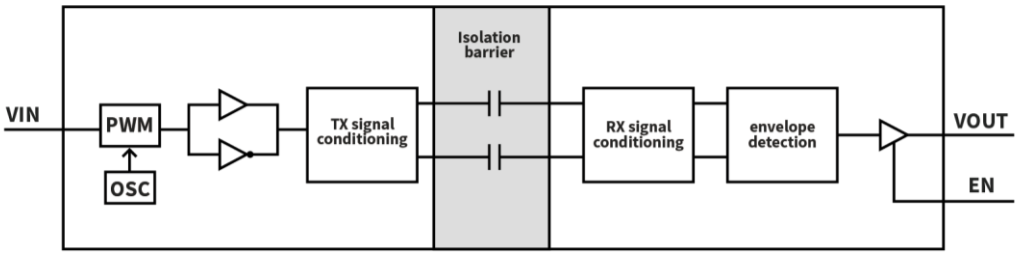


Figure 7.1 Single Channel Function Block Diagram

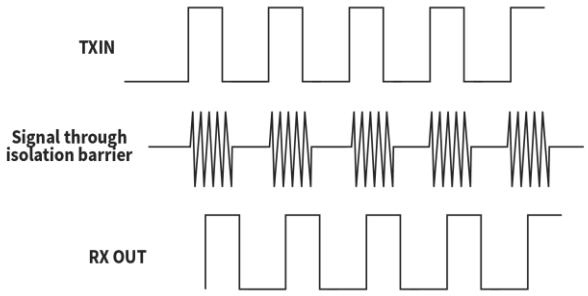


Figure 7.2 OOK Modulation

8. Application Note

8.1. Typical Application Circuit

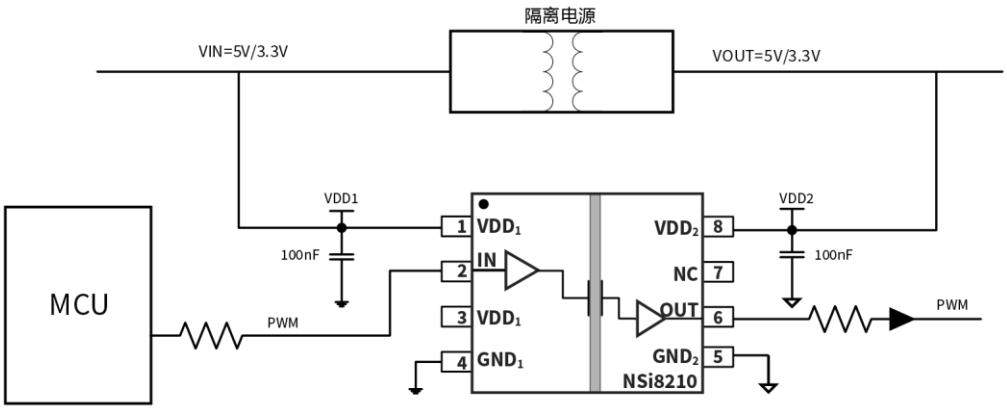


Figure 8.1 Typical PWM isolation circuit

8.2. PCB Layout

NSi8210 requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 8.2 to Figure 8.3 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

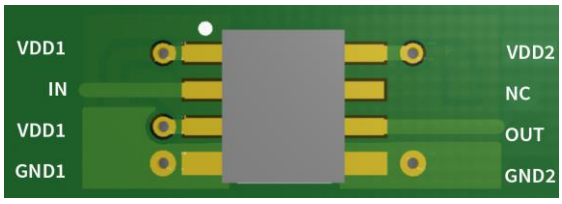


Figure8.2 Recommended PCB Layout — Top Layer

Figure8.3 Recommended PCB Layout — Bottom Layer

8.3. High Speed Performance

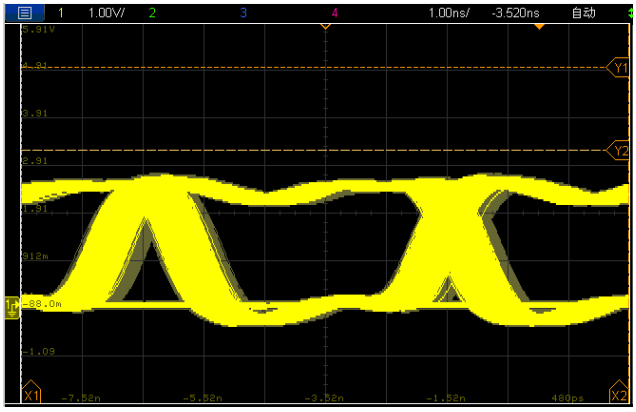


Figure 8.4 NSi8210N Eye diagram of output signal at 200Mbps

8.4. Typical Supply Current Equations

The typical supply current of NSi8210 can be calculated using below equations. I_{DD1} and I_{DD2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF

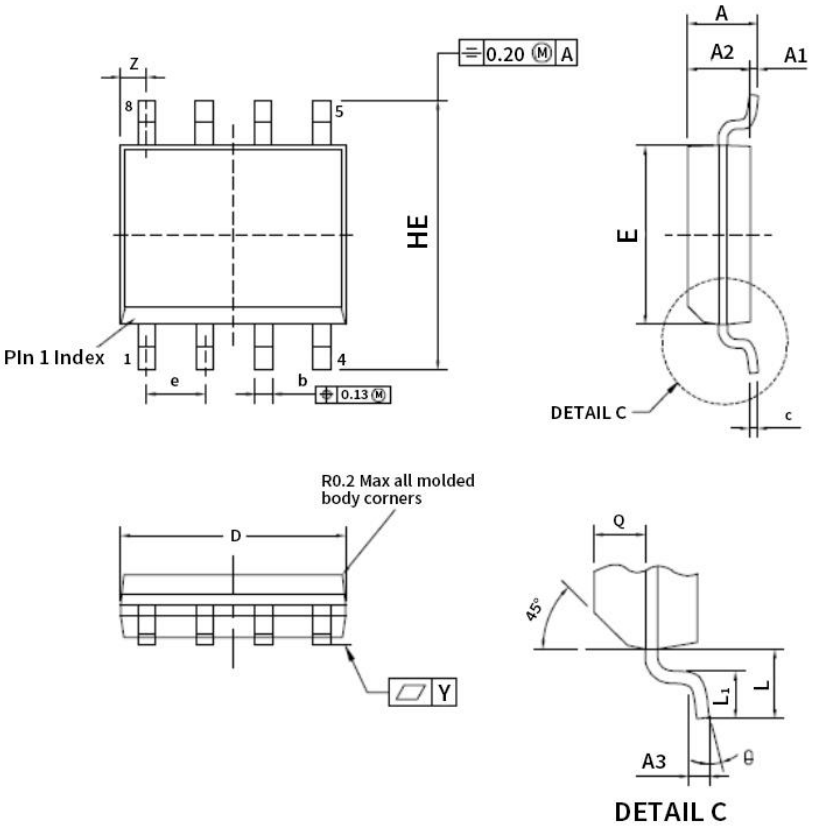
NSi8210:

I_{DD1} = 0.6 *a1+1.25*b1+1.1*c1.

I_{DD2} = 0.9 *a1+1.85*b1+VDD1*f* C_L *c1*10^{-9}

Where a1 is the channel number of low inputs at side 1, b1 is the channel number of high inputs at side 1, c1 is the channel number of switch signal inputs at side 1.

9. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 9.1 SOP8 Package Shape and Dimension in millimeters and (inches)

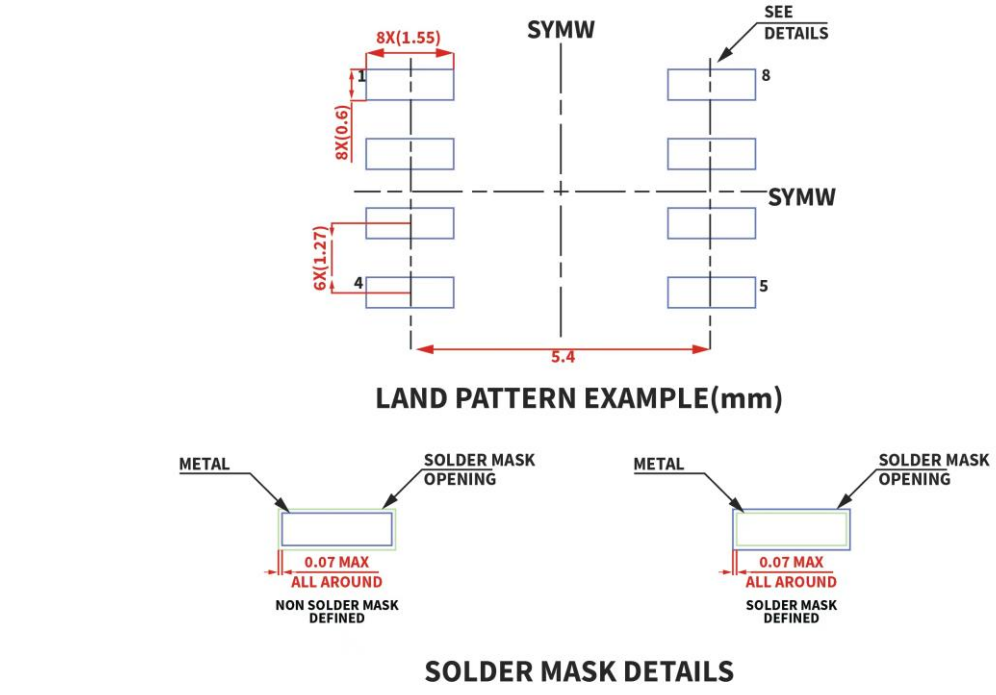
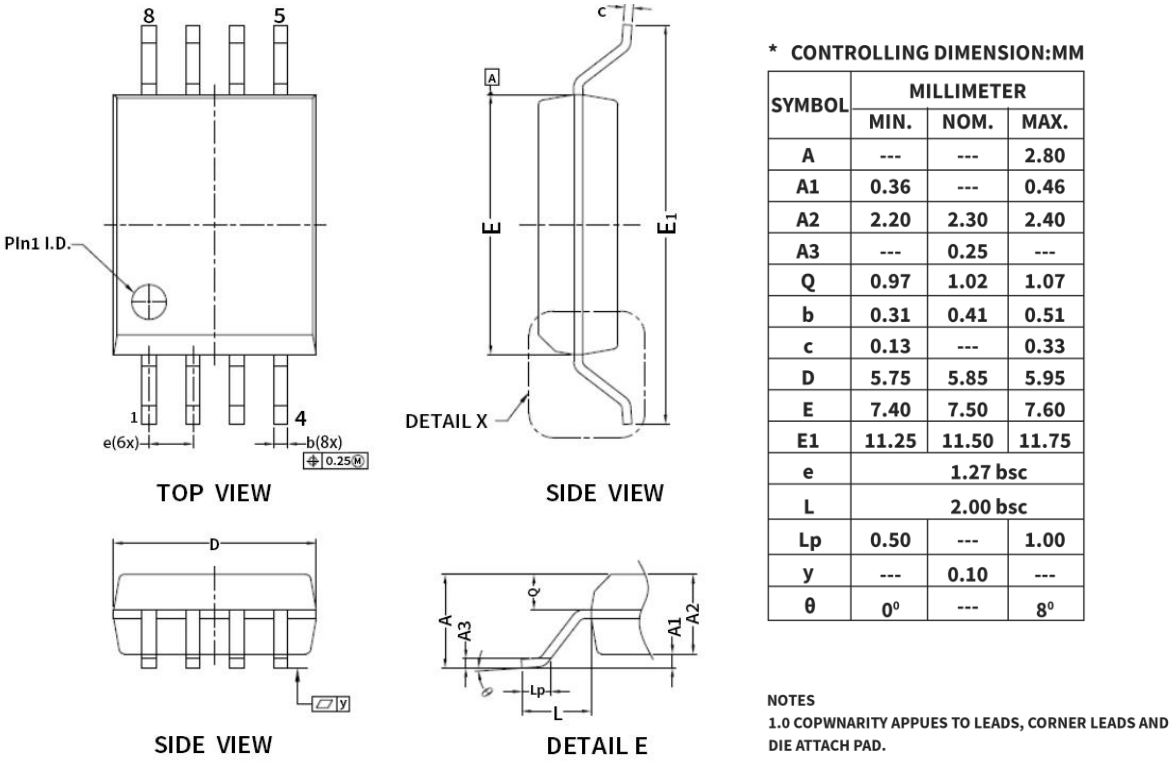


Figure 9.2 SOP8 Package Board Layout Example



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.80
A1	0.36	---	0.46
A2	2.20	2.30	2.40
A3	---	0.25	---
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	---	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	---	1.00
y	---	0.10	---
θ	0°	---	8°

NOTES
1.0 COPWNARITY APPUES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.3 SOW8 Package Shape and Dimension in millimeters and (inches)

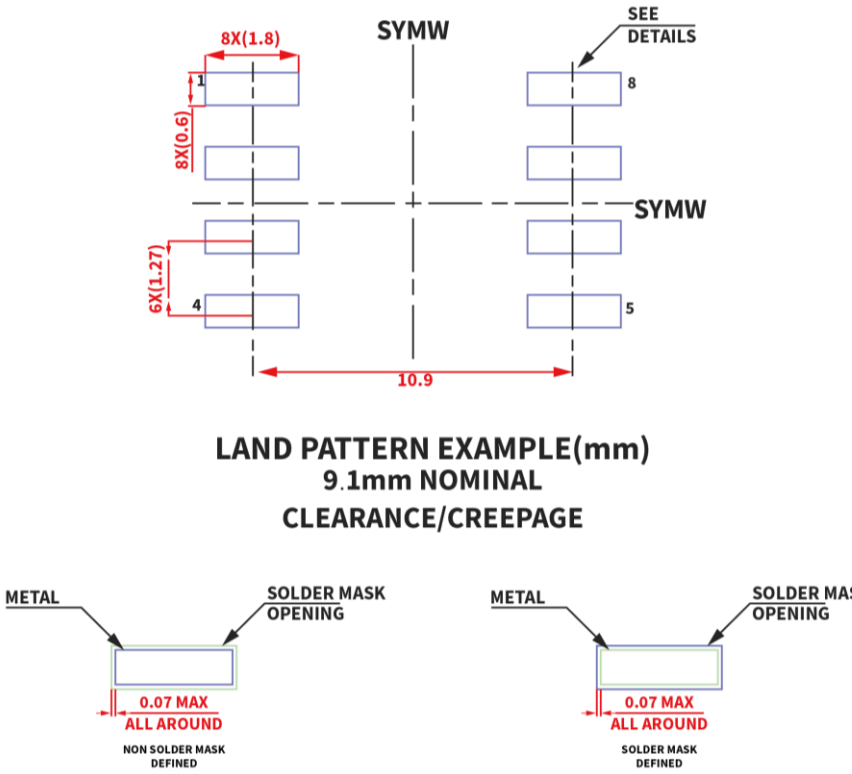
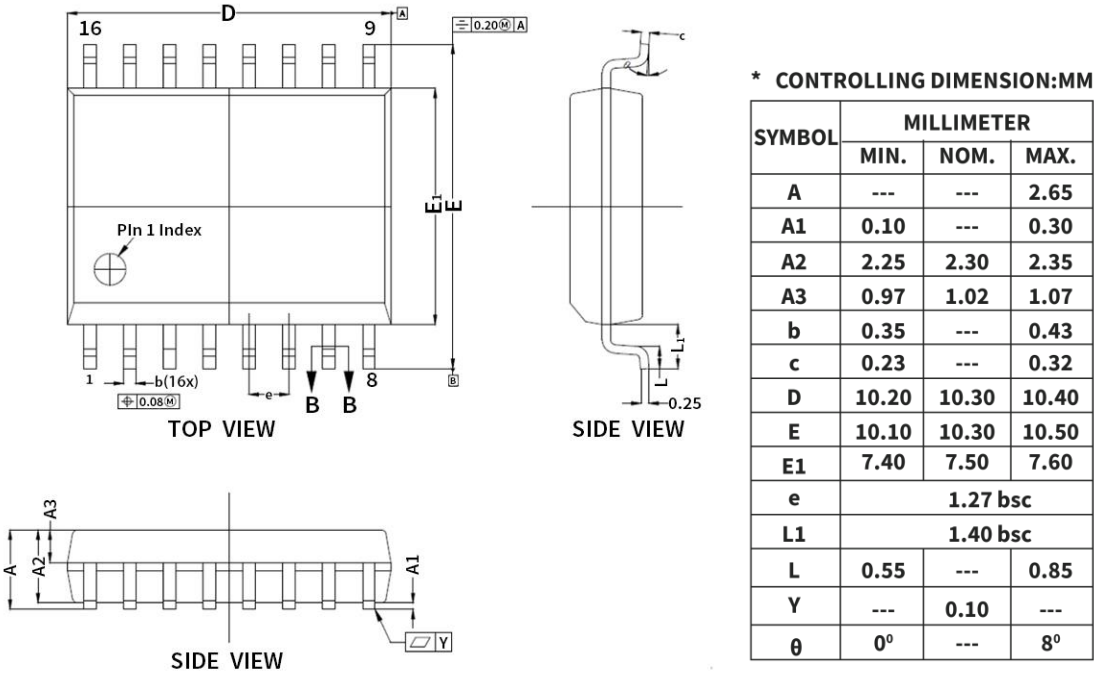


Figure 9.4 SOW8 Package Board Layout Example



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
c	0.23	---	0.32
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

Figure 9.5 SOW16 Package Shape and Dimension in millimeters and (inches)

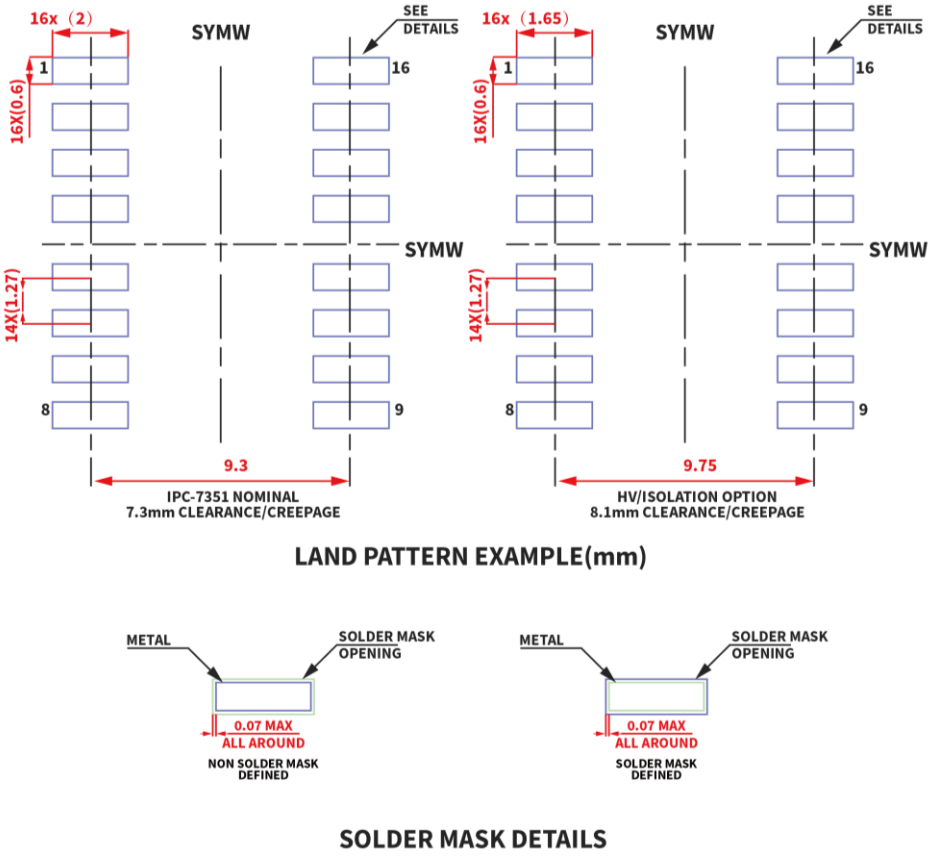


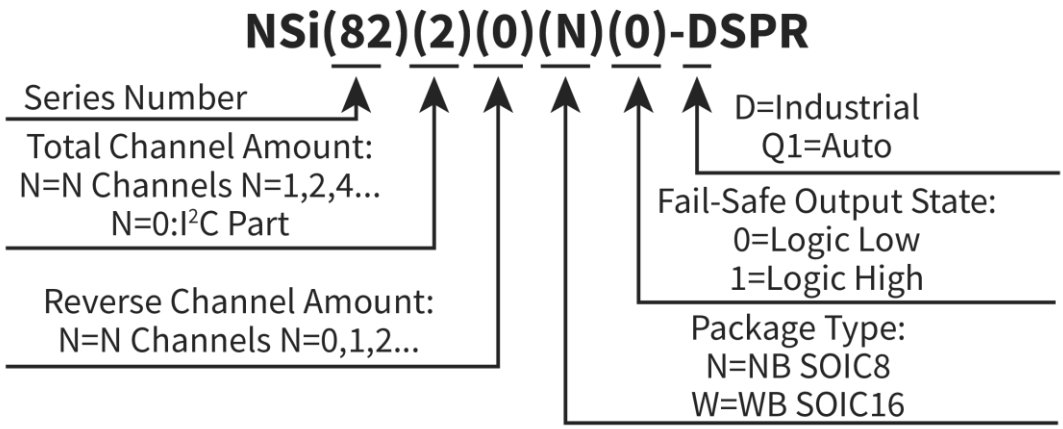
Figure 9.6 SOP16(300mil) Package Board Layout Example

10. Ordering Information

Part Number	*Isolation Rating (kV)*	*Number of side 1 inputs*	*Number of side 2 inputs*	*Max Data Rate (Mbps)*	*Default Output State*	*Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NSi8210N0-DSPR	3.75	1	0	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8210N1-DSPR	3.75	1	0	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8210N0-Q1SPR	3.75	1	0	150	Low	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8210N1-Q1SPR	3.75	1	0	150	High	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NSi8210W0-DSWVR	5	1	0	150	Low	-40 to 125℃	3	SOP8 (300mil)	SOW8	1000
NSi8210W1-DSWVR	5	1	0	150	High	-40 to 125℃	3	SOP8 (300mil)	SOW8	1000
NSi8210W0-Q1SWVR	5	1	0	150	Low	-40 to 125℃	3	SOP8 (300mil)	SOW8	1000
NSi8210W1-Q1SWVR	5	1	0	150	High	-40 to 125℃	3	SOP8 (300mil)	SOW8	1000
NSi8210W0-DSWR	5	1	0	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000

NSi8210W1 -DSWR	5	1	0	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8210W0 -Q1SWR	5	1	0	150	Low	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NSi8210W1 -Q1SWR	5	1	0	150	High	-40 to 125℃	2	SOW16 (300mil)	SOW16	1000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures. Automotive devices are AEC-Q100 qualified.										

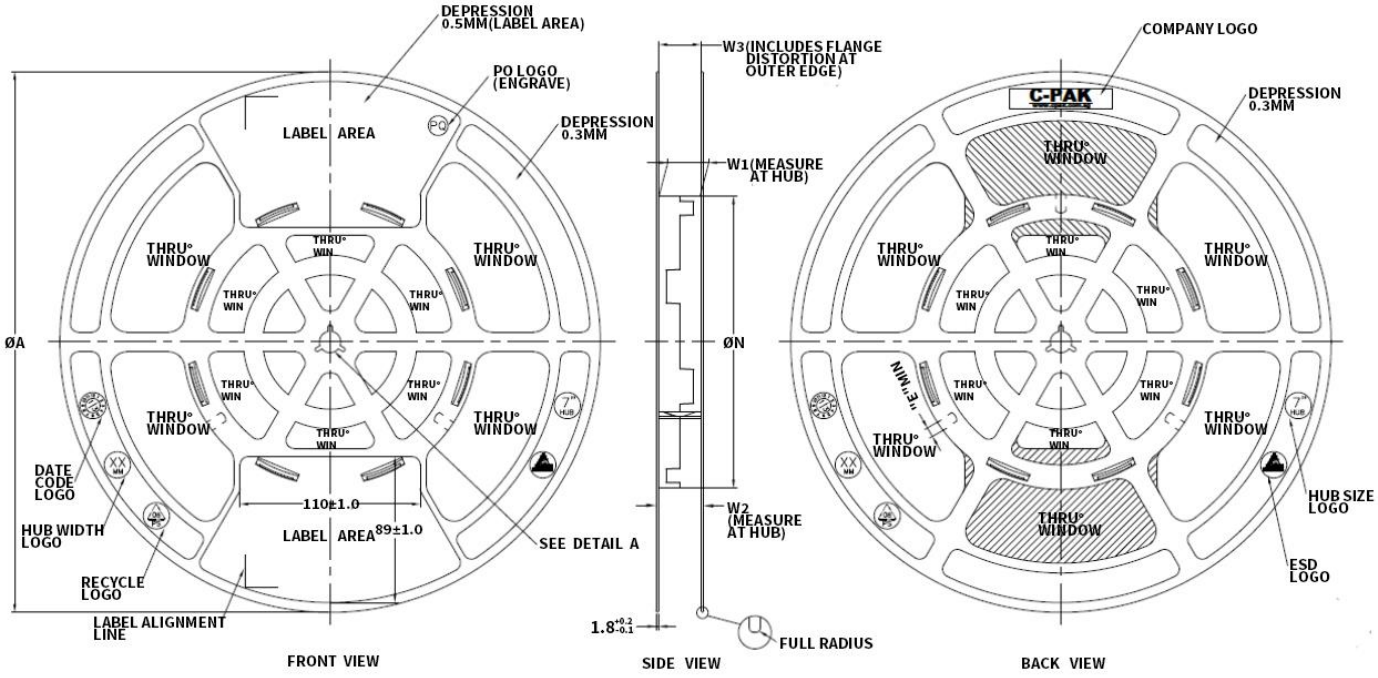
Part Number Rule:

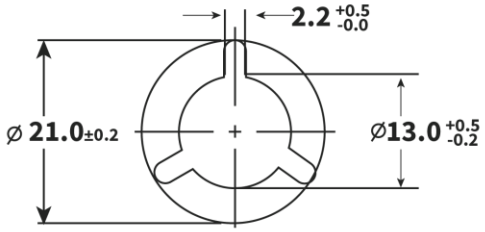


11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSiI8210	tbd	tbd	tbd	tbd

12. Tape and Reel Information



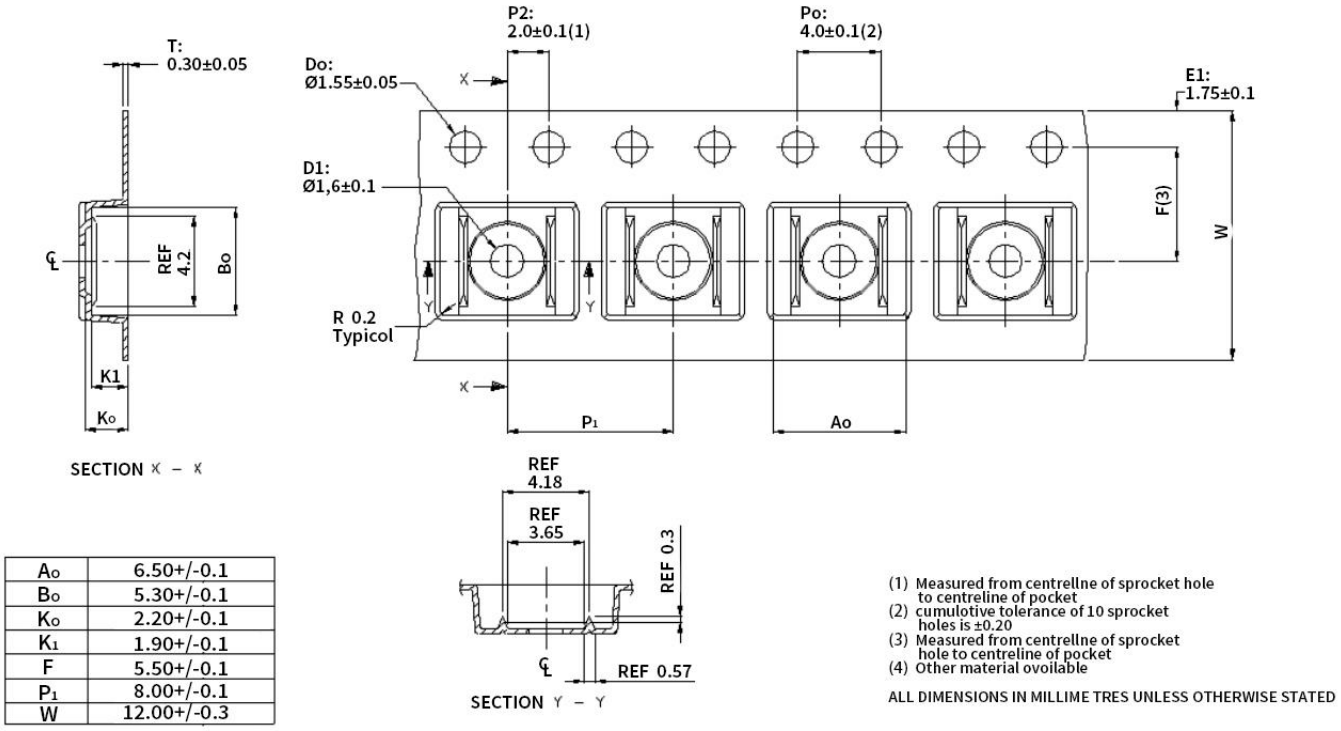


ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

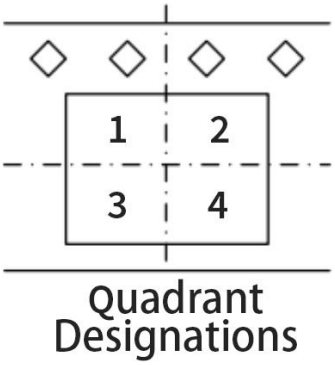
Figure 12.1 Reel Information (for all packages)



A_o	6.50+/-0.1
B_o	5.30+/-0.1
K_o	2.20+/-0.1
K_1	1.90+/-0.1
F	5.50+/-0.1
P_1	8.00+/-0.1
W	12.00+/-0.3

(1) Measured from centrellne of sprocket hole to centreline of pocket
(2) cumulotive tolerance of 10 sprocket holes is ±0.20
(3) Measured from centrellne of sprocket hole to centreline of pocket
(4) Other material ovoilable

ALL DIMENSIONS IN MILLIME TRES UNLESS OTHERWISE STATED



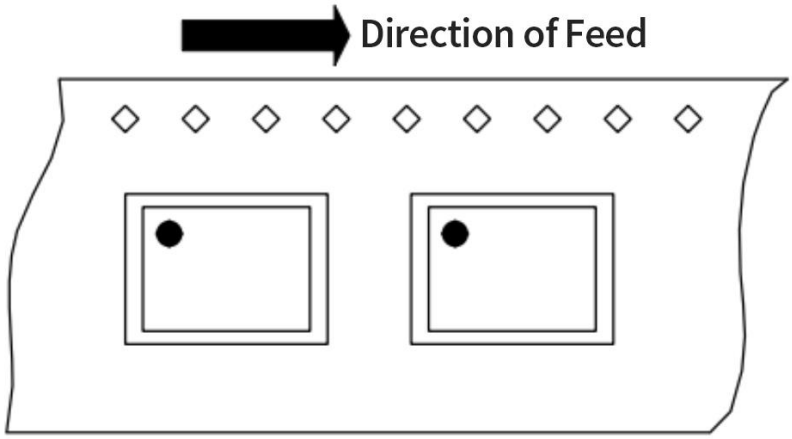


Figure 12.2 Tape Information of SOP8

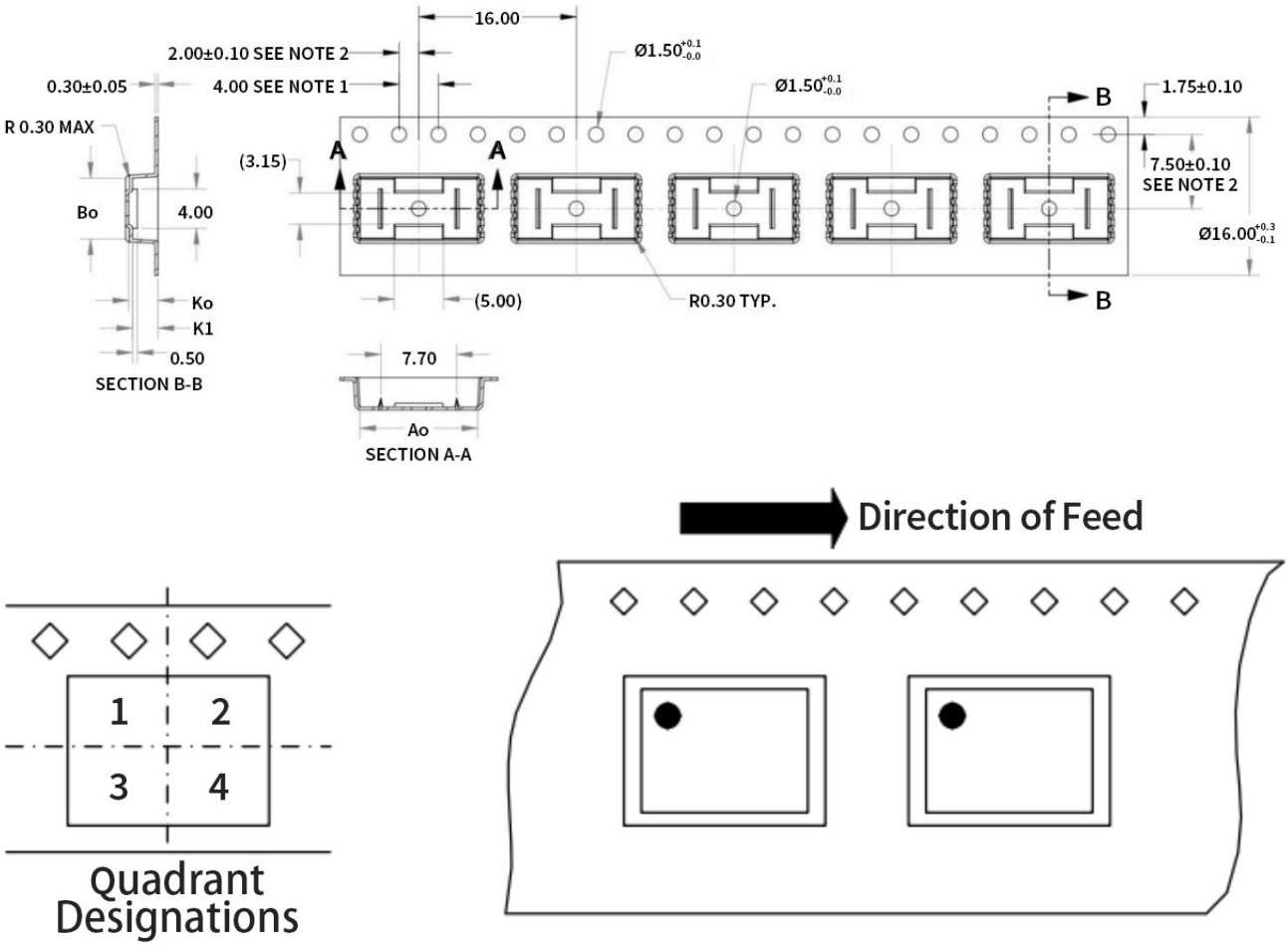
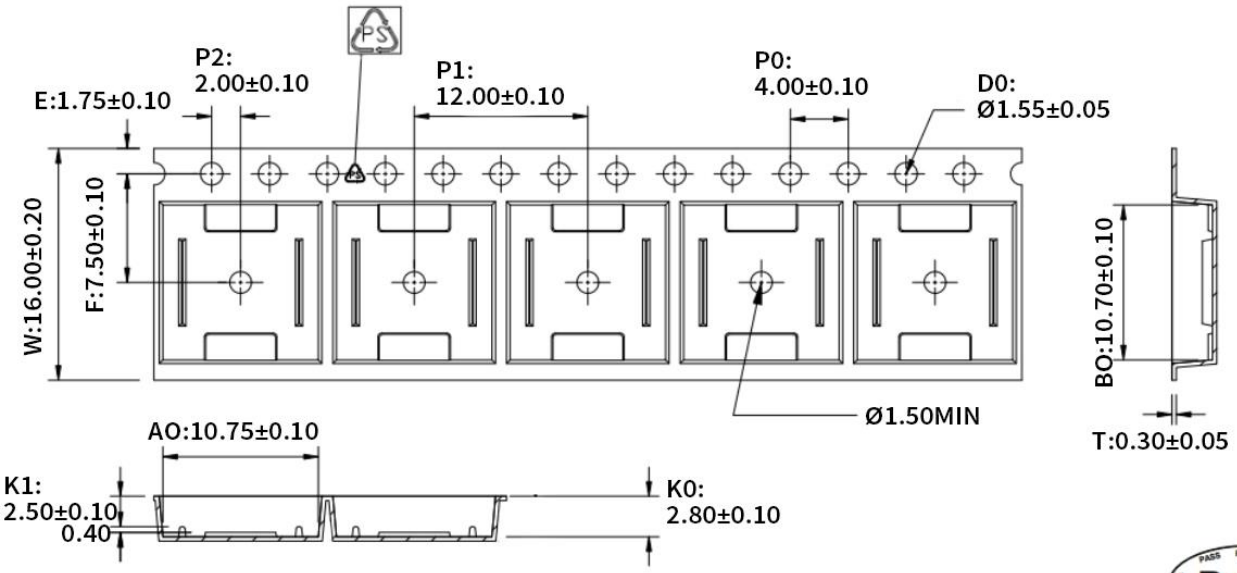
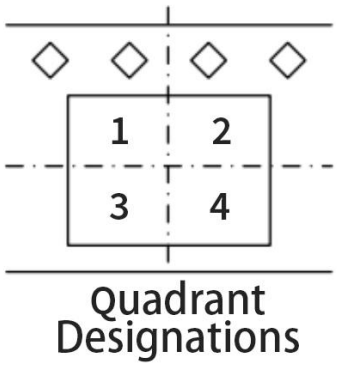


Figure 12.3 Tape Information of SOW8



1.10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481 requirements.
5. Thickness: 0.30±0.05mm.
6. Packing length per 22" reel: 378 Meters.(Rewind N=122)
7. Component load per 13" reel: 1000 pcs.
8. Surface resistivity:10^{5}~ $10^{10}\Omega/\square$

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10



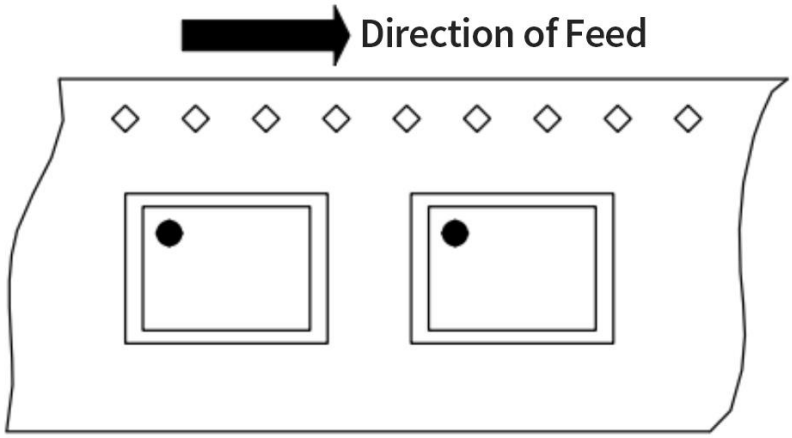


Figure 12.4 Tape Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Initial Version.	2020/12/7
1.1	Update Pin Configuration and Functions	2022/3/1
1.2	Update Insulation and Safety Related Specifications, add Thermal Derating Curve, add Junction Temperature， Change Tstg to -65, Update SOW16 Package information	2022/9/14

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