# NSD1025E

# High Speed, 5A Dual-Channel, Low-Side Gate Driver with Enable Pins

Datasheet (EN) 1.0

## Product Overview

NSD1025E is a wide supply, non-inverting, dual-channel, high speed, low side gate driver for both MOSFET, and IGBT. It has capability to deliver 5A sink and source current to the capacitive load along with rail-to-rail output to reduce the Miller effect during MOSFET's switching transition. Fast rise and fall times as well as matched propagation delay of both output channels enable the NSD1025E suitable for high frequency power converter application.

Both the input and enable pins of NSD1025E has ability to handle -10V which enhance the noise immunity and robustness of the device. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers.

The internal circuitry provides an under-voltage lockout (UVLO) function by holding the output low until the supply voltage is under the UVLO threshold values. Wide band of VDD hysteresis between high and low thresholds offers excellent noise immunity. The NSD1025E device is available in SOP8, and EP-MSOP8 package with operating temperature range from -40°C to 150°C.

## Key Features

- Wide supply voltage range: 4.5 to 24V
- Source/Sink drive current: ±5A (Peak)
- Two independent enable pins to control channel output
- Industry-standard Pin out
- Ability to handle negative swing of (-10V) at each input pin
- Offer High drive current by parallel connection of outputs
- CMOS/TTL compatible logic inputs
- 5A reverse current feature eliminates the need of output protection circuitry
- Operating temperature range: -40°C to 150°C
- Low supply current
- Short propagation delays: 50ns (typical)

## Applications

- Typical SMPS (Solar, Server, Telecom, Industrial)
- Motor Controllers
- Pulse Transformer Driver
- DC-DC Converters
- Class-D switching amplifier
- Line-drivers

## Topologies

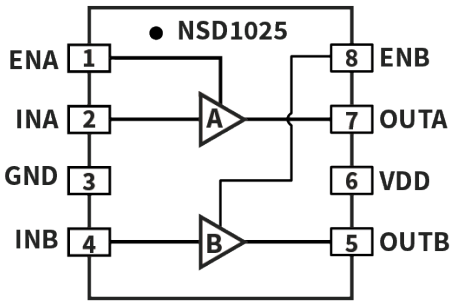
- Synchronous rectifiers
- Single and interleaved PFC
- LLC
- ZVS with pulsed transformer

## Device Information (1)

| *Part Number* | *Package* | *Body Size* |
|---|---|---|
| NSD1025E-DSPR | SOP8(150mil) | 4.9mm × 3.9mm |
| NSD1025E-DHMSR | EP-MSOP8(150mil) | 3.0mm × 3.0mm |
| NSD1025E-DDAER | DFN3X3-8L | 3.0mm × 3.0mm |

1) For all available packages, and order information refer to the end of datasheet.

## Block Diagram




NSD1025E Block Diagram

# INDEX

# 1. Pin Configuration and Functions

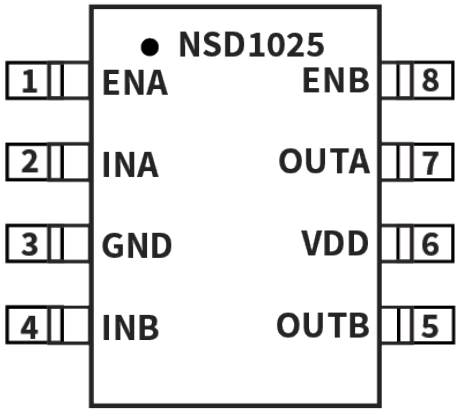



Figure. 1.1 NSD1025E Pin Configuration

Table 1.1 NSD1025E Pin Description

| *PIN NO.* | *SYMBOL* | *FUNCTION* |
|---|---|---|
| 1 | ENA | Channel A Enable Input: ENA is pulled up through a 180k resistor. if ENA is HIGH or left open OUTA depends on INA; to disable the Channel A the ENA pin drive LOW regardless of the INA state |
| 2 | INA | Channel A Logic Input: INA is pulled down through a 180k resistor. OUTA is held LOW if INA is unbiased or floating. This pin should be connected to HIGH state or GND (Not be left unconnected). |
| 3 | GND | Ground - Common ground reference for the device |
| 4 | INB | Channel B Logic Input: INB is pulled down through a 180k resistor. OUTB is held LOW if INB is unbiased or floating. This pin should be connected to HIGH state or GND (Not be left unconnected). |
| 5 | OUTB | Channel B Output – Low impedance output with Source or sink current ability |
| 6 | VDD | Supply Voltage - Provides power to the device |
| 7 | OUTA | Channel A Output – Low impedance output with Source or sink current ability |
| 8 | ENB | Channel B Enable Input: ENB is pulled up to VDD through a 180k resistor. if ENB is HIGH or left open OUTB depends on INB; to disable the Channel B the ENB pin drive LOW regardless of the INB state |

## 2. Absolute Maximum Ratings

| *Parameters* | *Symbol* | *Min* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|
| Supply Voltage | VDD | -0.3 | 24 | V | |
| Input and Enable pins Voltage | $V_{INA}$, $V_{INB}$, $V_{ENA}$, $V_{ENB}$ | -10 | 24 | V | |
| Output Voltage | $V_{OUTA}$, $V_{OUTB}$ | -0.3 | VDD+0.3 | V | |
| | | -2 | VDD+0.3 | V | Pulse<200ns |
| Output Source/Sink pulse current | $I_{SRC}$ , $I_{SNK}$ | | ±5 | A | Pulse<500ns |
| Operating Junction Temperature | $T_J$ | -40 | 150 | °C | |
| Storage Temperature | $T_{STG}$ | -60 | 150 | °C | |
| ESD | Human-body model (HBM),per JESD22-C101 | -4000 | +4000 | V | |
| | Charged-device model (CDM), JESD22-A114 | -1000 | +1000 | V | |

## 3. Recommended Operating Conditions

| *Parameters* | *Symbol* | *Min* | *Max* | *Unit* |
|---|---|---|---|---|
| Supply Voltage | VDD | 4.5 | 20 | V |
| Input Pin Voltage | $V_{INA,B}$ | -5 | 14 | V |
| Enable Pin Voltage | $V_{ENA,B}$ | -3 | 20 | V |
| Operating Ambient Temperature | $T_A$ | -40 | 125 | ℃ |

## 4. Thermal Information

| **Parameters** | **Symbol** | **EP-SOP8** | **SOP8** | **EP-MSOP8** | **DFN3X3-8L** | **Unit** |
|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance(1) | $R_{\theta JA}$ | 80 | 110 | 70 | 90 | °C /W |
| Junction-to-top Characterization parameters(2) | $\Psi_{JT}$ | 10 | 18 | 8 | 8 | °C /W |

1) Tested by High Effective Thermal Conductivity Test Board (2s2p) described in JESD51-7.

2) Obtained by Simulating in an environment described in JESD51-2a

# 5. Specifications

## 5.1 Electrical Characteristics

Use VDD=12V, and 10uF capacitor from VDD to GND. Positive and negative symbols represents the current into and out of the specified terminal, TJ =-40°C to 140°C (unless otherwise noted).

| *Parameters* | *Symbol* | *Min* | *Typ* | *Max* | *Unit* | *Comments* |
|---|---|---|---|---|---|---|
| **VDD Current** | | | | | | |
| Startup current | $IDD_{(OFF)}$ | | 363 | | uA | VDD=3.4V, INA=INB=VDD |
| | | | 350 | | uA | VDD=3.4V, INA=INB=GND |
| Quiescent current | $IDD_Q$ | 750 | 950 | 1150 | uA | VDD=12V, ENA=ENB=VDD, INA=INB=VDD |
| | | 600 | 810 | 1000 | uA | VDD=12V, ENA=ENB=VDD, INA=INB=GND |
| Operating current | $IDD_{(op)}$ | | 25 | | mA | f=500kHz Square wave, VDD=12V, $C_{OUTA}$ =1.8nF & $C_{OUTB}$=1.8nF |
| **Under Voltage Lockout (UVLO)** | | | | | | |
| VDD turn-on threshold | $VDD_{ON}$ | 3.9 | 4.2 | 4.5 | V | |
| VDD turn-off threshold | $VDD_{OFF}$ | 3.6 | 3.9 | 4.2 | V | |
| VDD hysteresis | $VDD_{HYS}$ | | 0.3 | | V | |
| **Input Characteristics** | | | | | | |
| Input signal for LH transition | $V_{INH}$ | 1.4 | 2.1 | 2.7 | V | Output Turns to High, If EN pin is high or left open |
| Input signal for HL transition | $V_{INL}$ | 0.8 | 1.25 | 1.7 | V | Output Turns to low, If EN pin is high or left open |
| Input signal hysteresis | $V_{INHYS}$ | | 0.85 | | V | |
| Enable signal for LH transition | $V_{ENH}$ | 1.7 | 2.1 | 2.6 | V | Output Turns to High, If IN pin is high |
| Enable signal for HL transition | $V_{ENL}$ | 1.0 | 1.25 | 1.6 | V | Output Turns to low, If IN pin is high |
| Enable signal hysteresis | $V_{ENHYS}$ | | 0.85 | | V | |
| Input pull-up resistance | $R_{EN}$ | | 180 | | kΩ | |
| Input pull-down resistance | $R_{IN}$ | | 180 | | kΩ | |
| **Output Characteristics** | | | | | | |
| Peak Source Current | $I_{SRC}$ | | 5 | | A | $t_{pulse}$=200ns |
| Peak Sink Current | $I_{SNK}$ | | -7 | | | $t_{pulse}$=200ns |
| Output pull-up resistance | $R_{OH}$ | 0.2 | 1.0 | 2.0 | Ω | $I_{OUT}$=-100mA |
| Output pulldown resistance | $R_{OL}$ | 0.1 | 0.6 | 1.5 | Ω | $I_{OUT}$=100mA |

## 5.2 Switching Characteristics

| Parameters | Symbol | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|---|
| Input/Enable to output propagation delay(1) | $T_{PDLH}$ | 30 | 50 | 70 | ns | $C_{LOAD}$=1.8Nf, low to high transition |
| | $T_{PDHL}$ | 30 | 50 | 70 | ns | $C_{LOAD}$=1.8Nf, high to low transition |
| Rise time(1) | $T_R$ | | 9 | | ns | $C_{LOAD}$=1.8nF, VDD=12V |
| Fall time(1) | $T_F$ | | 8 | | ns | $C_{LOAD}$=1.8nF, VDD=12V |
| Delay matching between two channels | $T_{DM}$ | | 1 | 4 | ns | INA=INB, OUTA and OUTB at 50% transition point |
| Minimum input pulse width that changes the output state(2) | $T_{PW}$ | 15 | 25 | 35 | ns | $C_{LOAD}$=1.8nF, VDD=12V |

1) See the timing diagrams in Figure 5.1
2) See the timing diagrams in Figure 5.2

## 5.3 Parameters Measurement Information

Figure 5.1 shows the definition of propagation delay, rise and fall time, while the minimum input pulse width that changes the output state in depicted in Figure 5.2. Associated test circuit diagram for specification measurements is shown in Figure 5.3.

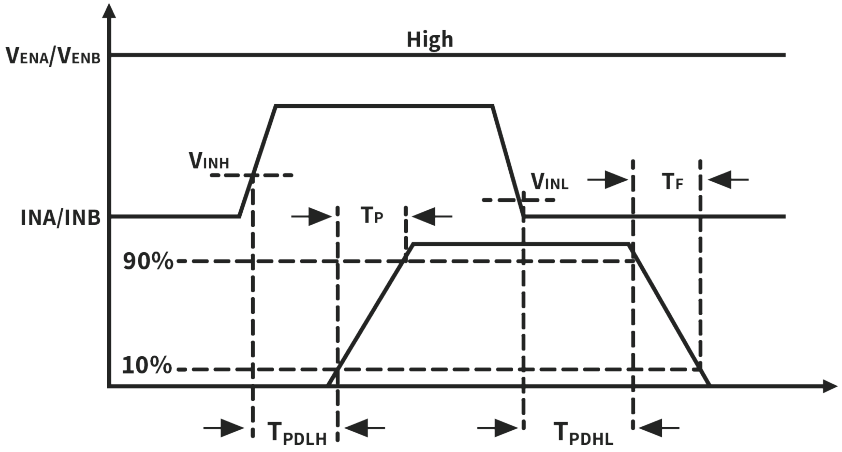



Figure 5.1 Propagation Delay, rise and fall time

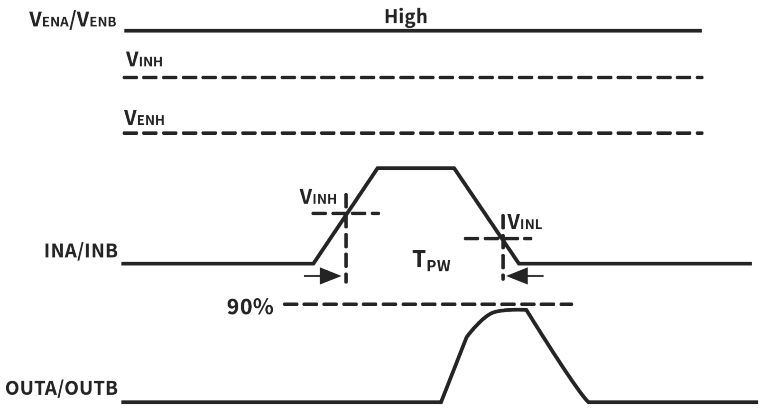



Figure 5.2 Minimum input pulse width that changes the output state

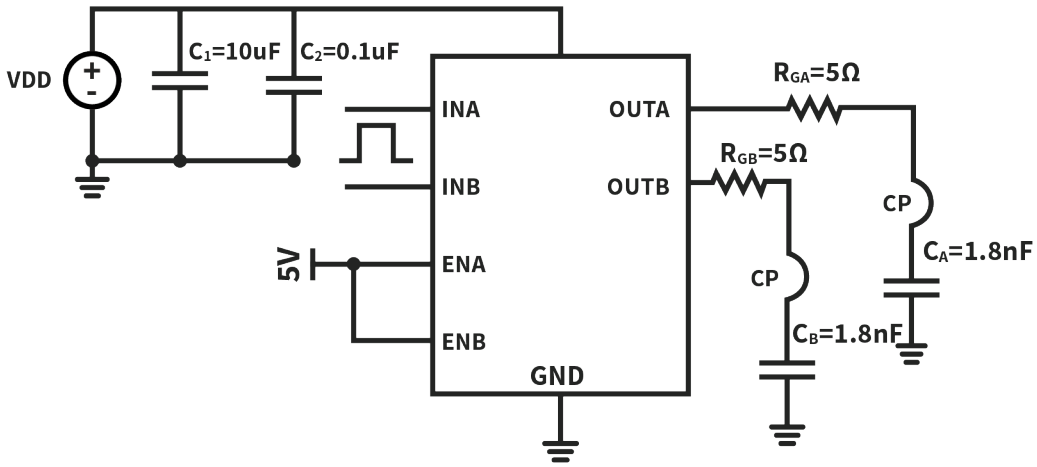



Figure 5.3 Test circuit diagram

## 5.4 Typical Characteristics

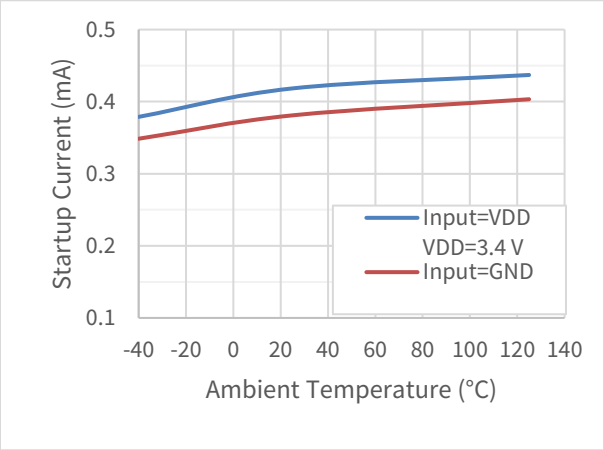



Figure 5.4 Start-up current $IDD_{(off)}$ Vs Temperature

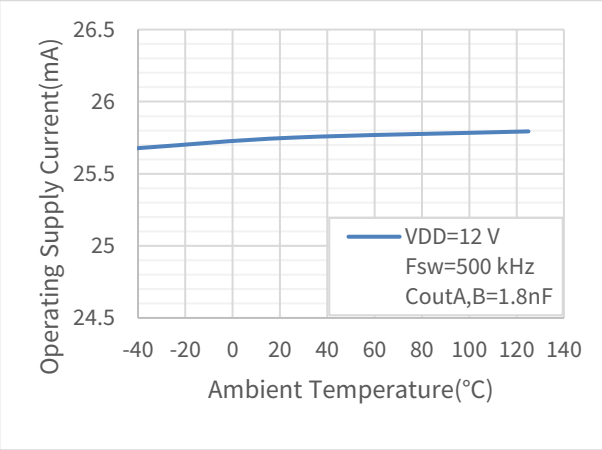



Figure 5.5 Operating supply current $IDD_{(OP)}$ Vs Temperature

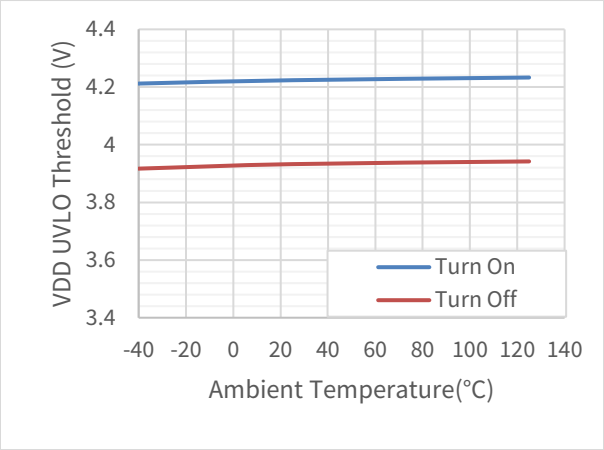



Figure 5.6 VDD UVLO Threshold Vs Temperature

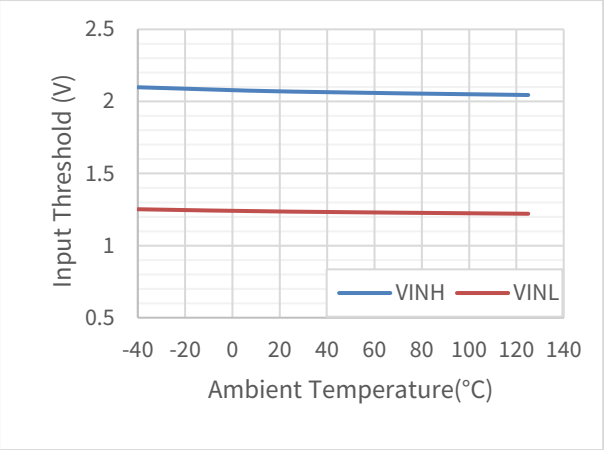



Figure 5.7 Input Threshold Vs Temperature

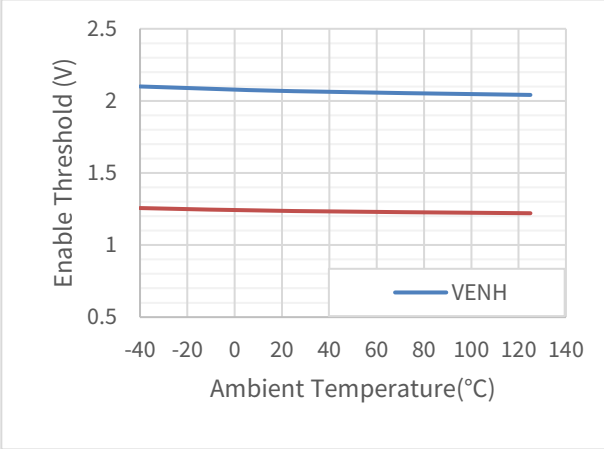



Figure 5.8 Enable threshold Vs Temperature

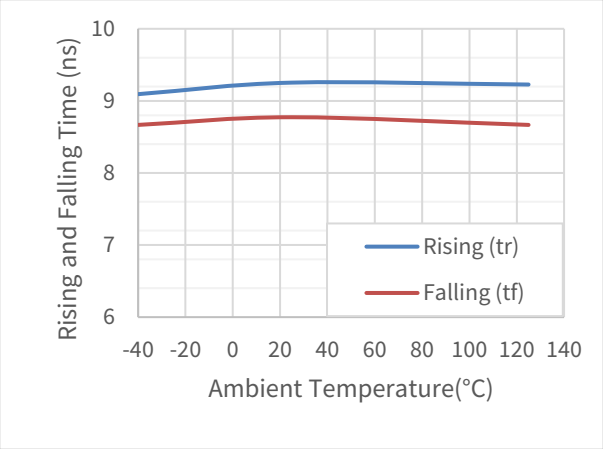



Figure 5.9 Rise and Fall time Vs Temperature

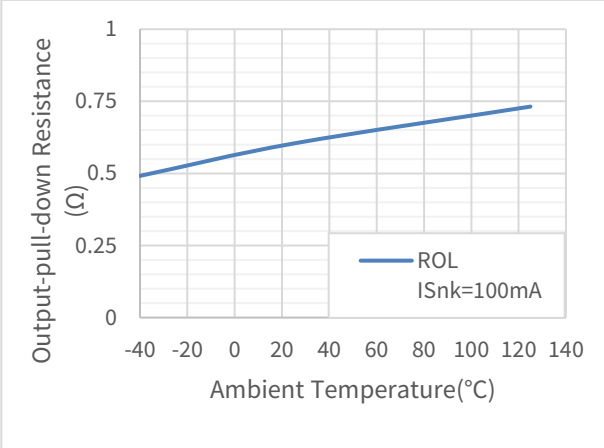



Figure 5.10 Output pull-down Resistance Vs Temperature

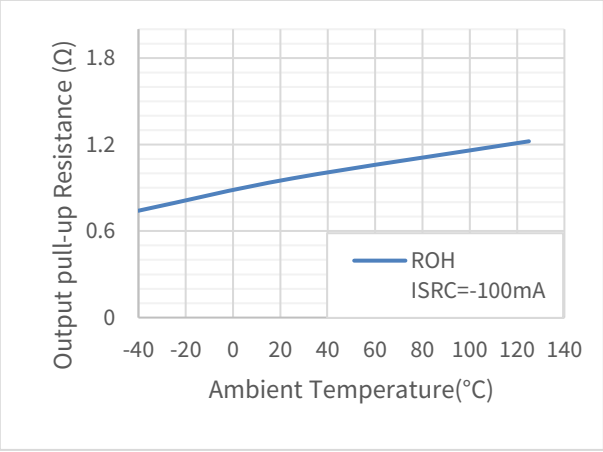



Figure 5.11 Output pull-up Resistance Vs Temperature

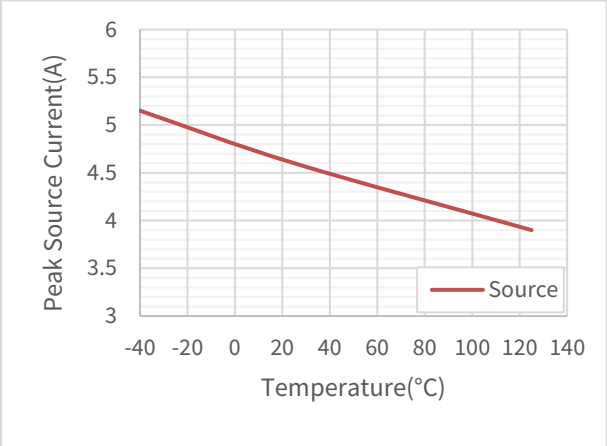



Figure 5.12 Peak Source Current Vs Temperature

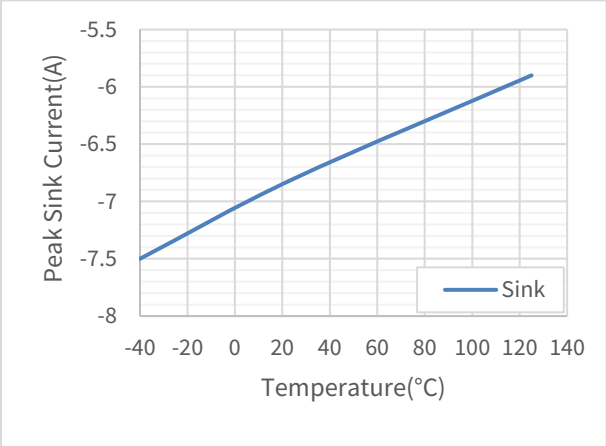



Figure 5.13 Peak Sink Current Vs Temperature

# 6. Detailed Description

## 6.1 Overview

The NSD1025E is a non-inverting high-speed dual-channel low side gate driver device featuring 5-A source and sink current capability. It has capability to deliver 5A sink and source current to the capacitive load. Fast rise and fall times as well as matched propagation delay of both output channels enable the NSD1025E suitable for high frequency power converter application.

Both the input and enable pins of NSD1025E has ability to handle -10V which enhance the noise immunity of the device. Driver inputs are compatible with CMOS and TTL logic hence it provides easy interface with analog and digital controllers.

The following table 2 ensures the efficient, robust and reliable operation in high frequency switching applications.

Table 6.1 NSD1025E Features and Advantages

| *FEATURE* | *ADVANTAGE* |
|---|---|
| 1-ns (typ) delay matching between channels | Enables dual channel outputs be stackable when the driven power device required higher driving capability |
| Wide range of supply voltage (VDD 4.5 to 24 V) | Improves the output stage robustness during switching load transition |
| Wide range of operating temperature -40 to 150°C | Flexibility in system design |
| VDD UVLO Protection | Protects power MOSFETs from running into linear mode, lockout function ensures predictable, glitch-free operation at power-up and power-down |
| Outputs held low when input pins (INx) in floating condition | Safety feature useful in safety certification while passing abnormal condition tests |
| Outputs enable when enable pins (ENx) in floating condition | Independent enable pins for external control of each channel operation, PIN 1 and PIN 8 are in floating condition |
| CMOS/TTL compatible input and enable threshold with wide hysteresis | Increased the noise immunity, compatible with input-logic levels from 3.3 V and 5 V microcontroller |
| Ability to handle -10 V (max) at input and enable pins | Enhanced the robustness in noisy conditions |

## 6.2 Functional Block Diagram

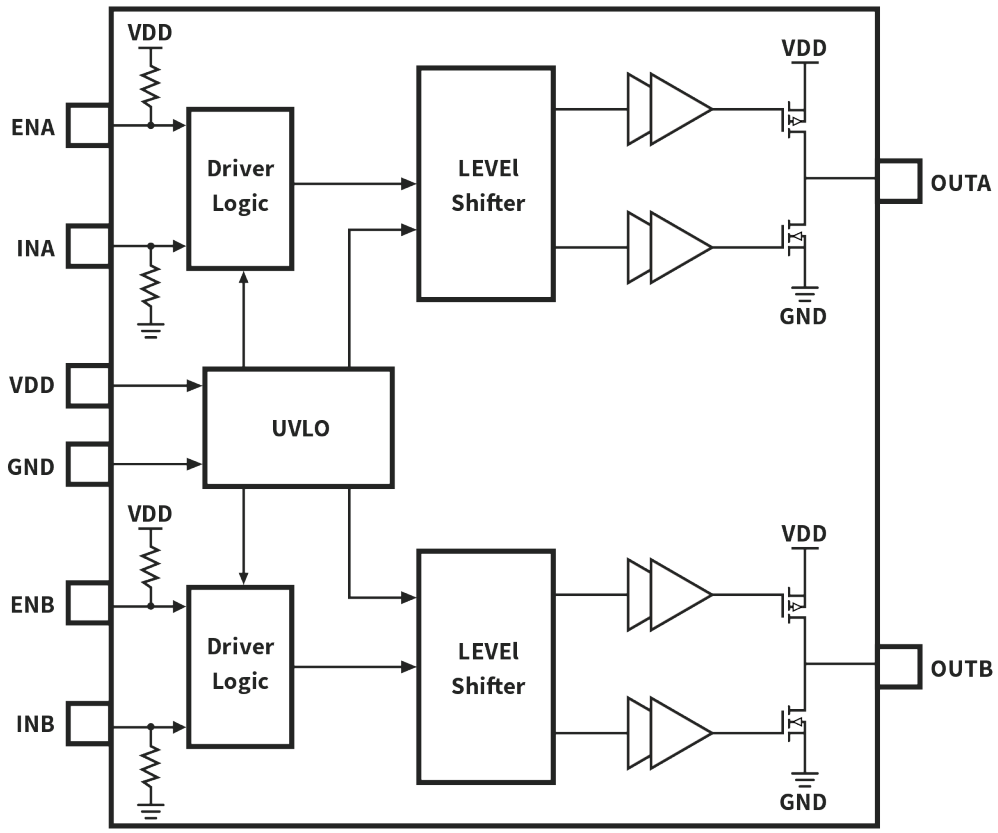



Figure 6.1 Function Block Diagram

## 6.3 Feature Description

### 6.3.1 Supply Voltage

NSD1025E operates under a supply voltage of 4.5V to 24V. The high voltage range of VDD can be useful to achieve the full current capability while driving very large MOSFETs. Two bypass capacitors from VDD to GND are recommended to get better performance and to prevent supply noise at high switching frequency. A 0.1-uF surface mount ceramic capacitor must be placed as close as possible to the VDD-GND pins. Moreover, in order to prevent the unwanted glitch in the VDD supply a large capacitor of 10uf with a low ESR must be connected in parallel and close to the small value bypass capacitor.

### 6.3.2 Under Voltage Lockout (UVLO)

NSD1025E under voltage-lockout rising threshold is typically 4.2V with 0.3V typical hysteresis. This hysteresis prevents output bouncing when low VDD supply voltage have noise from power supply. It also prevents sags in the VDD cause by sudden increase in IDD current while system commences switching. When VDD is below the UVLO threshold the circuit holds the outputs low regardless of the status of the inputs. The capability to operate at low voltage less than 5 V, is especially suited for driving emerging GaN power semiconductor devices.

At power-up, the NSD1025E output remains low until the VDD reaches the turn-on threshold. The magnitude of output signal rises with VDD until it reached to steady-state value. Figure 14, shows that the output remains low until the UVLO threshold is reached, then the output becomes in phase with the input waveform if the EN pin is active or floating.

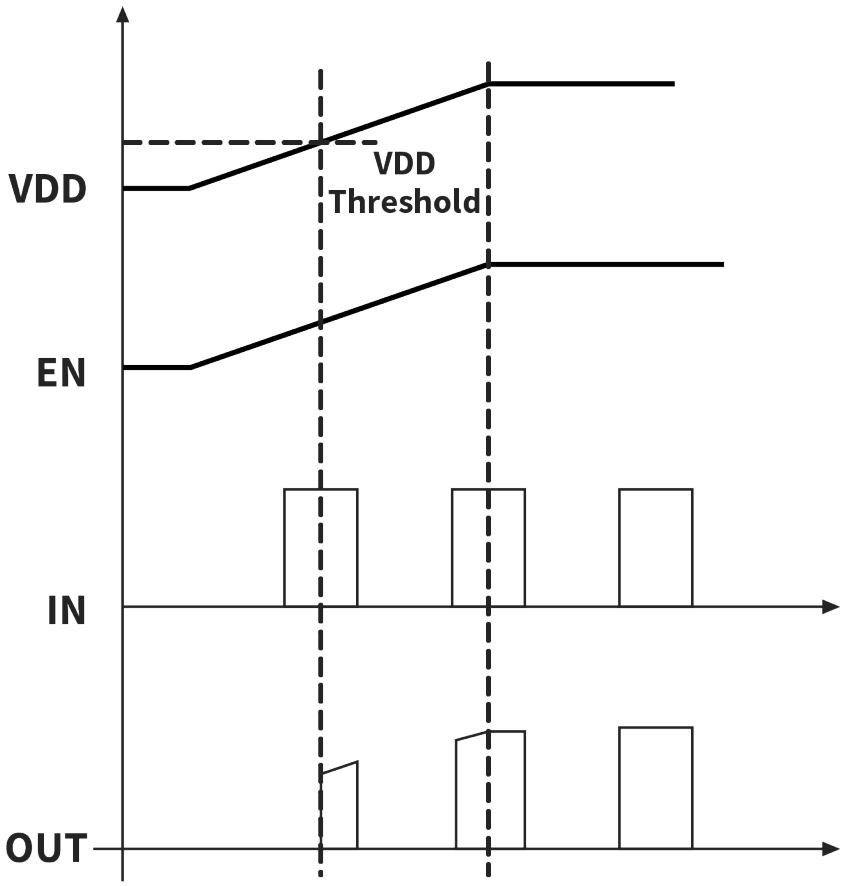



Figure 6.2 Function Block Diagram

### 6.3.3 Input Stage

The input of NSD1025E is compatible to both TTL and CMOS logic threshold that is independent of the supply voltage. The typical value of high input threshold ($V_{INH}$ =2.1V) whereas the low threshold ($V_{INL}$ =1.25V). The logic level thresholds are conveniently driven with PWM control signals derived from 3.3 V and 5 V digital power controller device. Wider hysteresis (typ. 0.85 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis less than 0.5 V. NSD1025E also feature tight control of the input pin threshold voltage levels which ease system design consideration and ensure stable operation across temperature as shown in Figure 8.

### 6.3.4 Enable Function

NSD1025E provides independent enable function for external control of each channel operation. Like the input pins, the enable pins are also based on TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3 V and 5 V microcontroller. When the enable pin voltage reaches to higher threshold ($V_{ENH}$ =2.1V) the driver enables all functions and starts gate driver operation. Whereas, the driver operation is disabled when the enable voltage falls below its lower threshold ($V_{ENL}$ =1.25V). The enable pins are internally pulled up to VDD with 180k pull-up resistors. Therefore, the ENA & ENB pins are left floating or not connecting (NC) for standard operation, where the enable feature is not required. This driver also features tight control of the enable-function threshold-voltage levels which ease system design consideration and ensure stable operation with temperature as depicted in Figure 9.

All input pins have ability to handle negative voltage up to -10 V. This feature enhanced the robustness in noisy environments, and also prevent cross current over single wires during GND shift between signal source and driver input.

### 6.3.5 Device Functional Modes

Table 6.3 NSD1025E Device Logic

| *ENA* | *ENB* | *INA* | *INB* | *OUTA* | *OUTB* |
|---|---|---|---|---|---|
| H | H | L | L | L | L |
| H | H | L | H | L | H |
| H | H | H | L | H | L |
| H | H | H | H | H | H |
| L | L | Any | Any | L | L |
| Any | Any | Floating | Floating | L | L |
| Floating | Floating | L | L | L | L |
| Floating | Floating | L | H | L | H |
| Floating | Floating | H | L | H | L |
| Floating | Floating | H | H | H | H |

# 7. Applications and Implementation

## 7.1 Typical Applications

Typical synchronous rectifier and interleaved PFC power converter configuration by using the driver NSD1025E are shown in Figure 7.1 and 7.2 respectively.

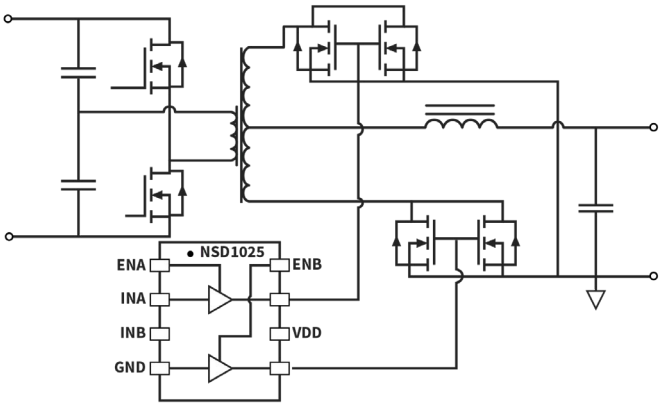



Figure 7.1 Synchronous Rectifier

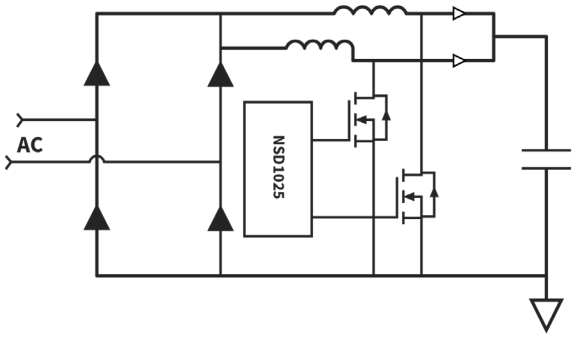



Figure 7.2 Interleaved PFC Converter

## 7.2 Driver Current and Power Dissipation

Power dissipation in the gate driver device for fully charged capacitive load depends on the following factors:

- Switching frequency ($F_{SW}$)
- Supply Voltage ($V_{DD}$)
- Load Capacitor ($C_{LOAD}$)
- External gate resistors ($R_G$)

$$P_G = C_{Load} * V_{DD}^2 * F_{SW} \quad (1)$$

Assuming $C_{LOAD}$=30nF, $V_{DD}$=12V, and $F_{SW}$=100kHz the power loss is calculated using Equation 2.

$$P_G = 30nF * 12V * 12V * 100kHz = 0.432W \quad (2)$$

For the switching load presented by a power MOSFET, the power loss of each channel is can be calculated by the Equation (4), where the gate charge is determined by Equation 3.

$$Q_G = C_{LOAD} * V_{DD} \quad (3)$$

So, the gate charge (QG) includes the effect of input capacitance and the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Generally, manufacturer provides the information of gate charge, in nC, to switch the device under specified conditions. Using gate charge QG, and the power that must be dissipated during charging can be determined by the Equation 4.

$$P_G = Q_G * V_{DD} * F_{SW} \quad (4)$$

This power PG dissipates in the gate resistor of the circuit during the MOSFET switching transitions. Half of the power dissipates when the load capacitor is charge and the other half dissipates during discharging period of the capacitor. With the use of external gate drive resistor, the power dissipation shares between internal and gate resistance of the gate driver.

By using external gate resistor $R_G$, the power dissipation is calculated as:

$$P_G = 0.5 * Q_G * V_{DD} * F_{SW} * \left(\frac{R_{OL}}{R_{OL} + R_G} + \frac{R_{OH}}{R_{OH} + R_G}\right) \quad (5)$$

Where

- $R_{OL}$ is the effective pull down resistance
- $R_{OH}$ is the pull up resistance
- $R_G$ is the gate resistance between driver output and gate of power MOSFET

## 7.3 PCB Layout

For design robustness and proper operation at fast switching and high current applications an appropriate PCB layout design is very important. NSD1025E has ability to provide higher current (5 A peak at VDD=12 V) with very small rise and fall time at the gate of the power MOSFET to assist vary fast voltage transition. The high di/dt causes unwanted ringing, if the trace length and impedance of the loop in not well controlled. Below are the recommended guidelines to design the PCB layout of conferred high-speed gate driver. An example of capacitor and gate resistance placed is shown in Figure 7.3.

**Guidelines**

- Place the driver as close as possible to the power device to minimize the output side high-current trace length
- Put the bypass capacitor (between VDD and GND) very close to the driver pins to minimize the trace length for better noise filtering. Use of SMD type devices with low ESR capacitor are highly recommended.
- For high current driving applications (in case of paralleling both channel outputs), the driver input loop of both input channels must be symmetrical to ensure the equal input propagation delay.
- In order to lower the di/dt transients all the turn-on and turnoff current loop paths must be minimized
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation
- While designing prefer to keep separate power and signal traces
- The star point grounding is recommended to minimize noise coupling from one current loop to the other. The GND of the driver connects to the other circuit nodes such as source of power MOSFET or ground of PWM controller at single point. The connected paths must be short as possible to reduce parasitic inductance and wide as possible to reduce resistance.
- Use ground plane to provide noise shielding and thermal dissipation.

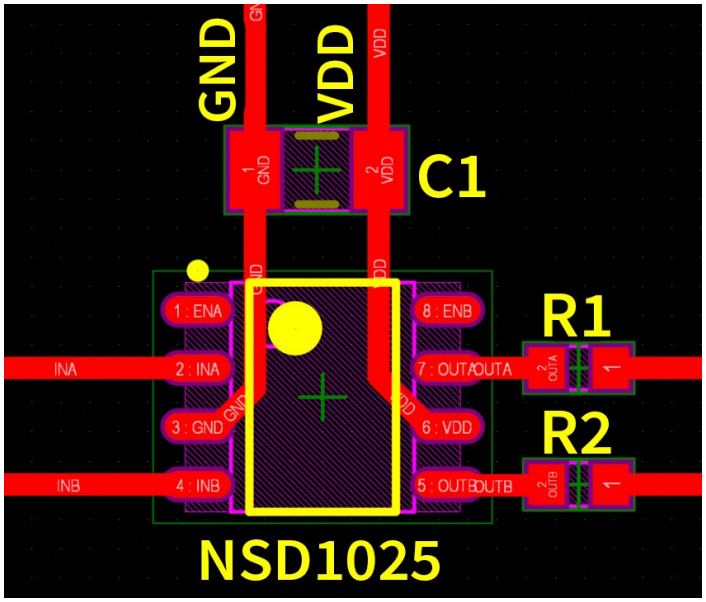
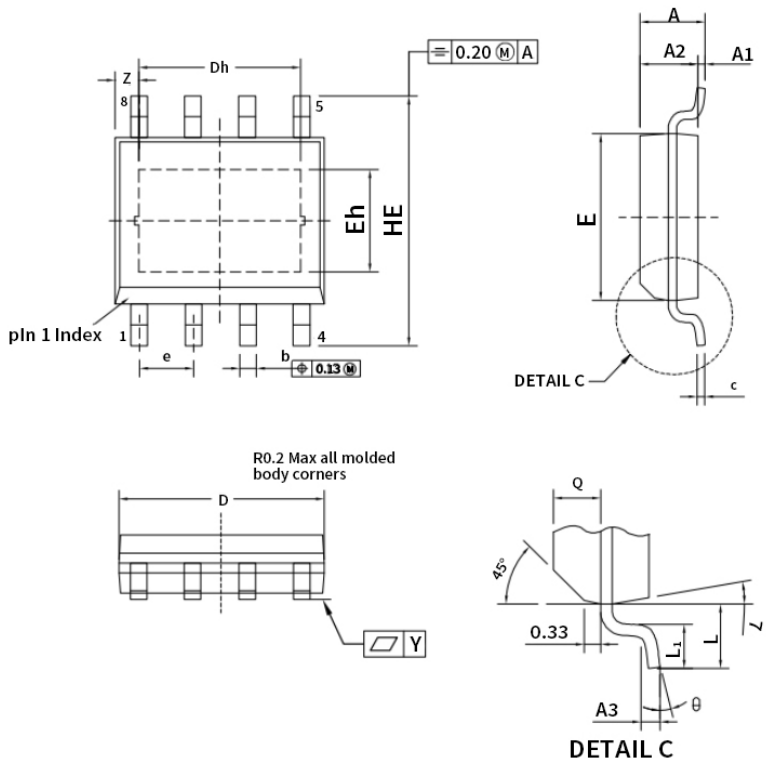



Figure 7.3 PCB layout example

# 8. Package Information

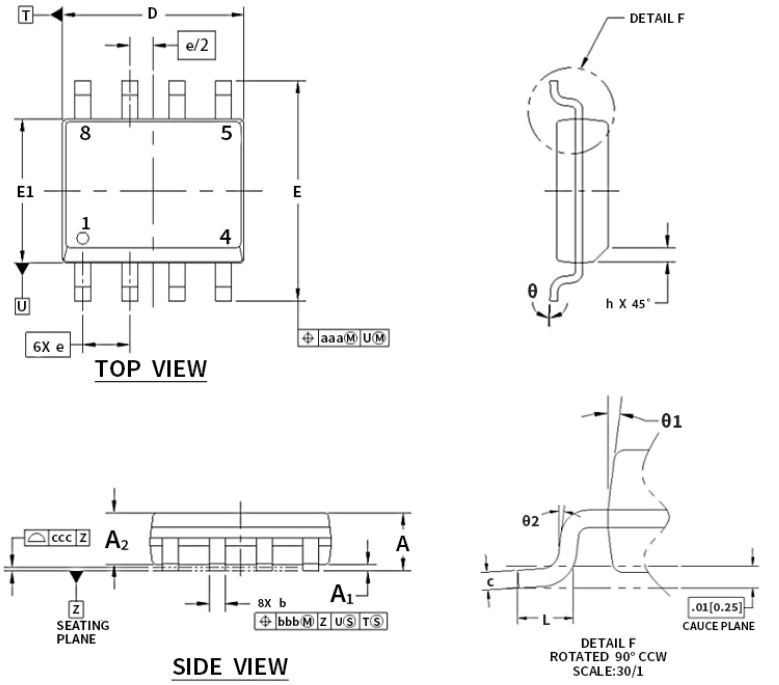



* CONTROLLING DIMENSION:MM

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.43 | 1.55 | 1.68 | 0.056 | 0.061 | 0.066 |
| A1 | --- | 0.05 | 0.10 | --- | --- | 0.004 |
| A2 | 1.43 | 1.50 | 1.58 | 0.056 | 0.059 | 0.062 |
| b | 0.35 | 0.41 | 0.49 | 0.014 | 0..016 | 0.019 |
| c | 0.19 | 0.20 | 0.25 | 0.0075 | 0.0079 | 0.010 |
| D | 4.8 | 4.9 | 5.0 | 0.189 | 0.193 | 0.197 |
| E | 3.8 | 3.9 | 4.0 | 0.150 | 0.154 | 0.157 |
| Q | 0.55 | 0.65 | 0.75 | 0.022 | 0.026 | 0.030 |
| Dh | 2.95 | 3.81 | 3.91 | 0.116 | 0.15 | 0.153 |
| Eh | 1.43 | 2.29 | 2.39 | 0.056 | 0.095 | 0.094 |
| HE | 5.84 | 5.99 | 6.2 | 0.228 | 0.236 | 0.244 |
| e | 1.27 bsc | | | 0.05 bsc | | |
| L | 1.05 bsc | | | 0.041 bsc | | |
| L1 | 0.41 | 0.64 | 0.89 | 0.016 | 0.025 | 0.035 |
| Y | --- | 0.10 | --- | --- | 0.004 | --- |
| Z | 0.3 | 0.5 | 0.7 | 0.012 | 0.020 | 0.028 |
| A3 | --- | 0.25 | --- | --- | 0.010 | --- |
| θ | 0° | 5° | 8° | 0° | 5° | 8° |

Notes:
1. Package body surface finlsh.
   All top surface: Ra 1.2 um to 1.5 um
   All others surface: Ra 1.5 um to 1.8 um
2. LF material: CuFe2P+ESH

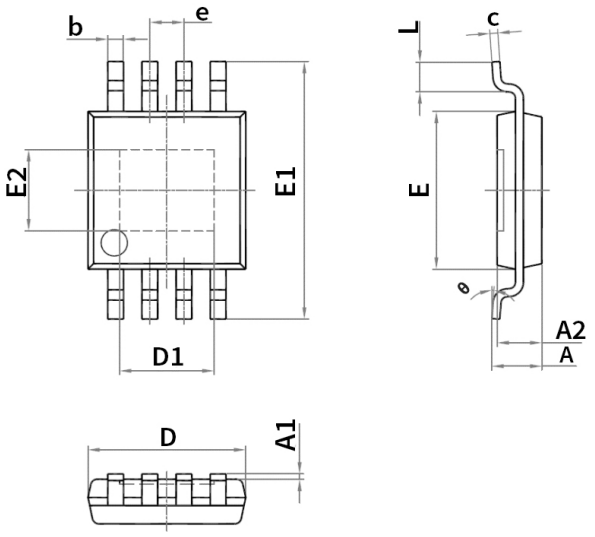
Figure 8.1 EP-SOP8 Package Shape and Dimension




| DESCRIPTION | SYMBOL | INCH | | | MILLIMETER | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| TOTAL THICKNESS | A | .053 | | .069 | 1.35 | | 1.75 |
| STAND OFF | A1 | .004 | | .010 | 0.10 | | 0.25 |
| MOLD THICKNESS | A2 | .049 | | --- | 1.25 | | --- |
| LEAD WIDTH | b | .014 | | .019 | 0.35 | | 0.49 |
| L/F THICKNESS | c | .007 | | .010 | 0.19 | | 0.25 |
| BODY SIZE | D | .189 | | .197 | 4.80 | | 5.00 |
| | E1 | .150 | | .157 | 3.80 | | 4.00 |
| | E | .228 | | .244 | 5.80 | | 6.20 |
| LEAD SIZE | e | .050 BSC | | | 1.27 BSC | | |
| | L | .016 | | .049 | 0.40 | | 1.25 |
| | h | .010 | | .020 | 0.25 | | 0.50 |
| | θ | 0° | | 7° | 0° | | 7° |
| | θ1 | 5° | | 15° | 5° | | 15° |
| | θ2 | 2° | 7° | 12° | 2° | 7° | 12° |
| LEAD EDGE OFFSET | aaa | .010 | | | 0.25 | | |
| LEAD OFFSET | bbb | .010 | | | 0.25 | | |
| COPLANARITY | ccc | .004 | | | 0.10 | | |
| | | | | | | | |

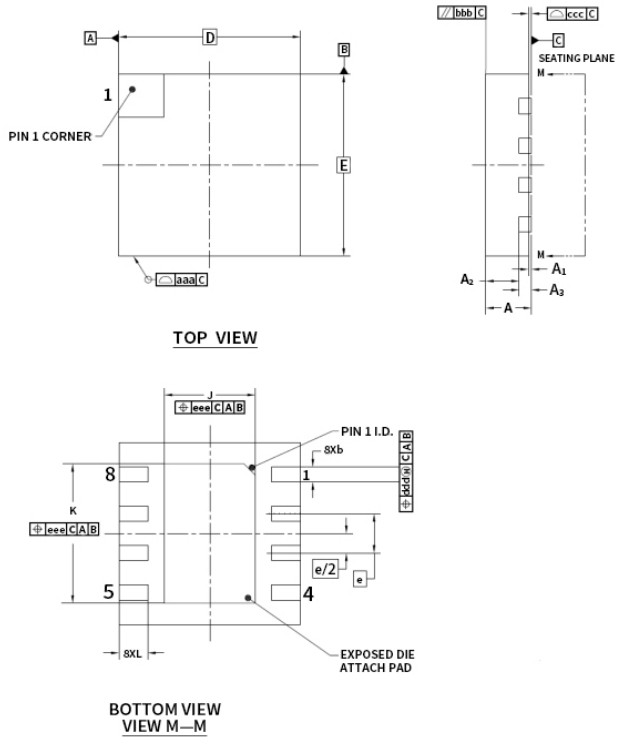
NOTES:
1. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION .006 (0.15) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE .005 (0.127) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

Figure 8.2 SOP8 Package Shape and Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.820 | 1.100 | 0.032 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 1.700 | 1.900 | 0.067 | 0.075 |
| e | 0.65 (BSC) | | 0.026 (BSC) | |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.750 | 5.050 | 0.187 | 0.199 |
| E2 | 1.450 | 1.650 | 0.057 | 0.065 |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 6° | 0° | 6° |

Figure 8.3 EP-MSOP8 Package Shape and Dimension




| DESCRIPTION | | SYMBOL | MILLIMETER | | |
|---|---|---|---|---|---|
| | | | MIN | NOM | MAX |
| TOTAL THICKNESS | | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | | A1 | 0 | --- | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | 0.57 |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.20 | 0.25 | 0.30 |
| BODY SIZE | X | D | 2.95 | 3.00 | 3.05 |
| | Y | E | 2.95 | 3.00 | 3.05 |
| LEAD PITCH | | e | 0.65 BSC | | |
| EP SIZE | X | J | 1.45 | 1.50 | 1.55 |
| | Y | K | 2.25 | 2.30 | 2.35 |
| LEAD LENGTH | | L | 0.425 | 0.475 | 0.525 |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

NOTES:
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 8.4 DFN3X3-8L Package Shape and Dimension

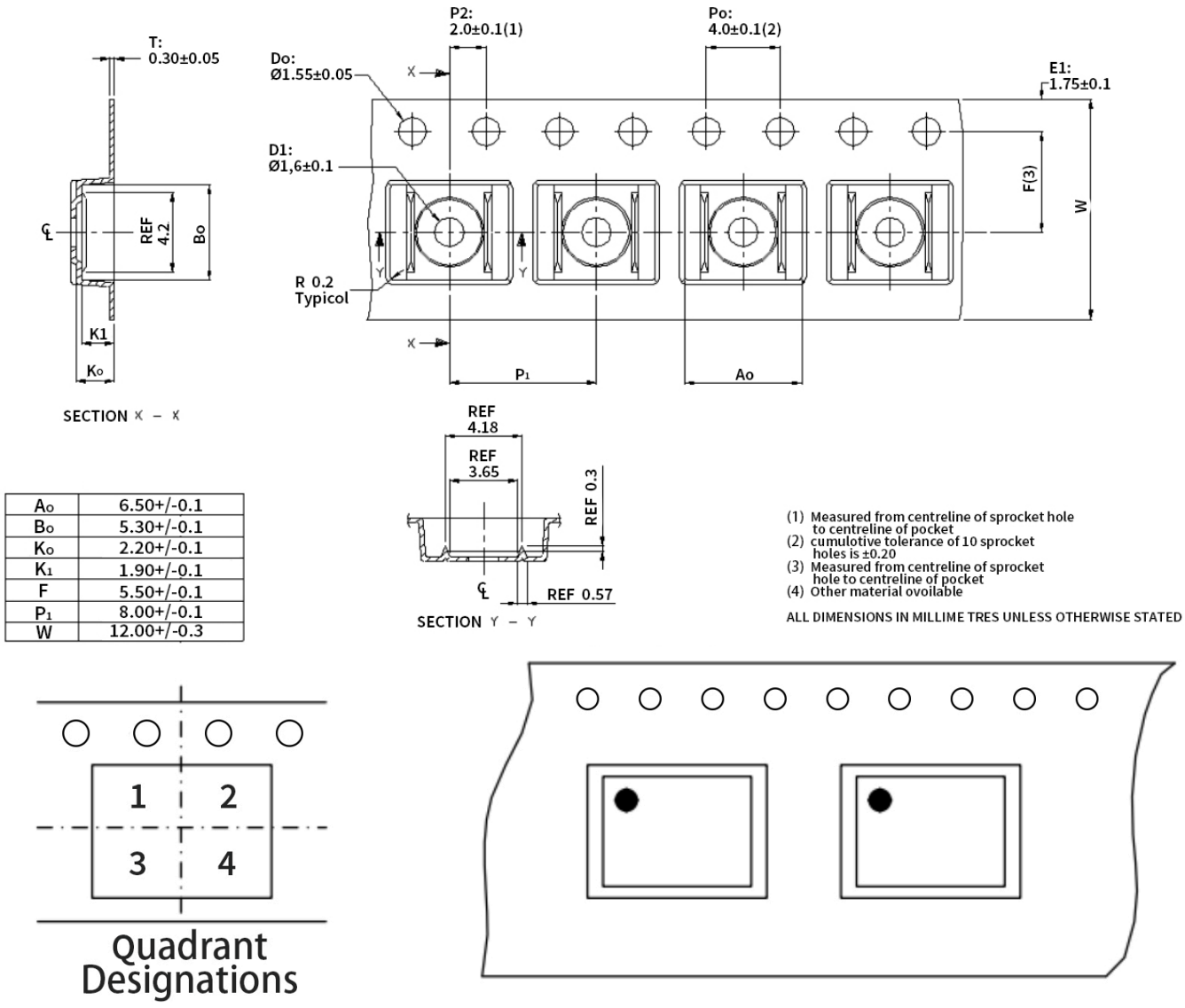
# 9. Ordering Information

| *Part No.* | *Temperature* | *Auto-motive* | *Package Type* | *Package Drawing* | *MSL* | *SPQ* |
|---|---|---|---|---|---|---|
| NSD1025E-DSPR | -40 to 125℃ | NO | SOP8 (150mil) | SOP8 | 3 | 2500 |
| NSD1025E-DHMSR | -40 to 125℃ | NO | EP-MSOP8 (150mil) | EP-MSOP8 | 3 | 3000 |
| NSD1025E-DDAER | -40 to 125℃ | NO | DFN3X3-8L | DFN3X3-8L | 3 | 3000 |

## 10. Documentation Support

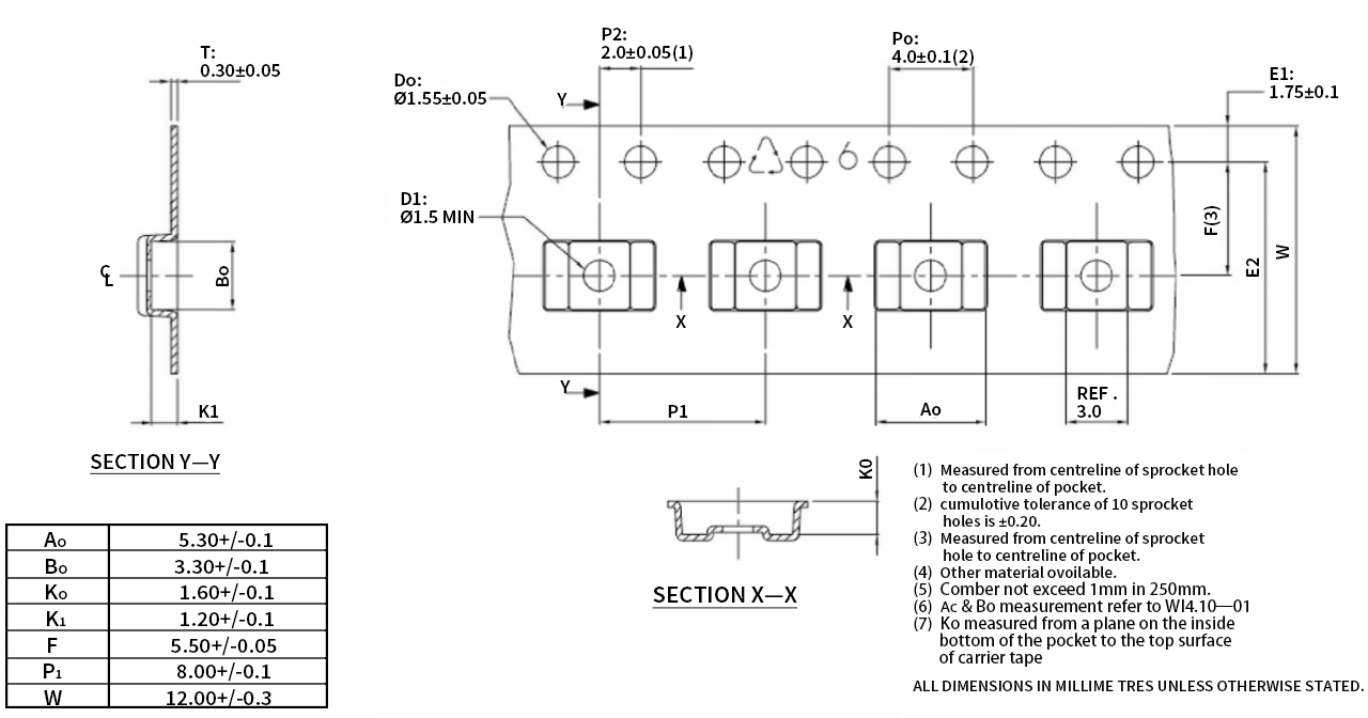
| *Part Number* | *Product Folder* | *Datasheet* | *Technical Documents* | *Isolator selection guide* |
|---|---|---|---|---|
| NSD1025E | Click here | Click here | Click here | Click here |

# 11. Tape and Reel Information



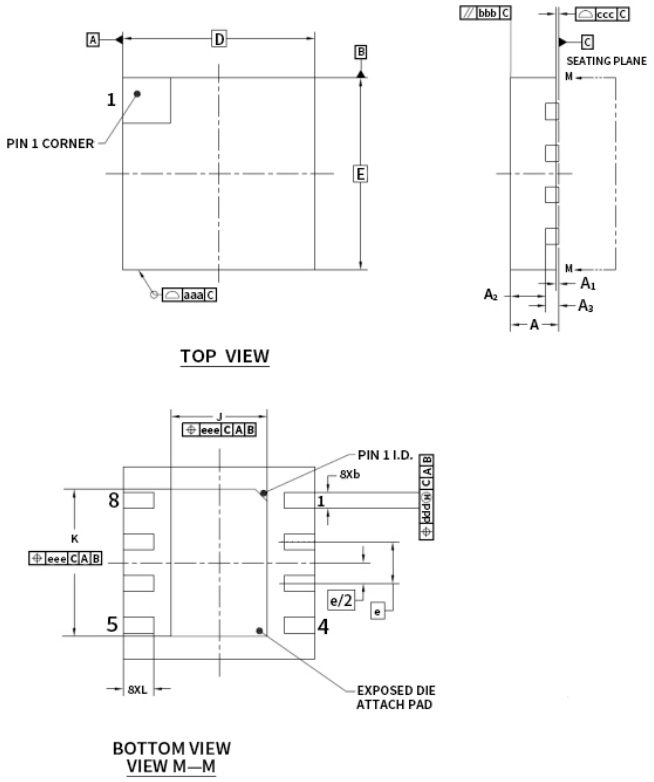

| | |
|---|---|
| $A_o$ | 6.50+/-0.1 |
| $B_o$ | 5.30+/-0.1 |
| $K_o$ | 2.20+/-0.1 |
| $K_1$ | 1.90+/-0.1 |
| F | 5.50+/-0.1 |
| $P_1$ | 8.00+/-0.1 |
| W | 12.00+/-0.3 |

Figure 11.1 SOP8 Package Shape and Dimension




| | |
|---|---|
| $A_o$ | 5.30+/-0.1 |
| $B_o$ | 3.30+/-0.1 |
| $K_o$ | 1.60+/-0.1 |
| $K_1$ | 1.20+/-0.1 |
| F | 5.50+/-0.05 |
| $P_1$ | 8.00+/-0.1 |
| W | 12.00+/-0.3 |

Figure 11.2 Reel information of MSOP8




| DESCRIPTION | | SYMBOL | MILLIMETER | | |
|---|---|---|---|---|---|
| | | | MIN | NOM | MAX |
| TOTAL THICKNESS | | A | 0.70 | 0.75 | 0.80 |
| STAND OFF | | A1 | 0 | --- | 0.05 |
| MOLD THICKNESS | | A2 | --- | 0.55 | 0.57 |
| L/F THICKNESS | | A3 | 0.203 REF | | |
| LEAD WIDTH | | b | 0.20 | 0.25 | 0.30 |
| BODY SIZE | X | D | 2.95 | 3.00 | 3.05 |
| | Y | E | 2.95 | 3.00 | 3.05 |
| LEAD PITCH | | e | 0.65 BSC | | |
| EP SIZE | X | J | 1.45 | 1.50 | 1.55 |
| | Y | K | 2.25 | 2.30 | 2.35 |
| LEAD LENGTH | | L | 0.425 | 0.475 | 0.525 |
| PACKAGE EDGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | bbb | 0.1 | | |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| EXPOSED PAD OFFSET | | eee | 0.1 | | |

NOTES:
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 11.3 DFN3X3-8L Package Shape and Dimension

# 12. Revision History

| *Revision* | *Description* | *Date* |
|---|---|---|
| 1.0 | Initial Version | 2021/07/22 |
| | | |

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