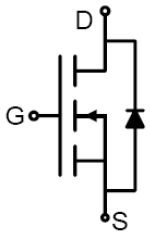
Feature

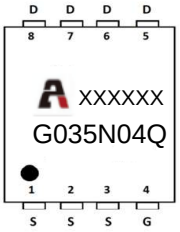
- 40V,100A
  $R_{DS(ON)}$ <3.2mΩ @V_{GS}=10V (TYP:2.8mΩ)
  $R_{DS(ON)}$ <5.2mΩ @V_{GS}=4.5V (TYP:4.3mΩ)
- Split Gate Trench Technology
- Lead free product is acquired
- Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

- PWM applications
- Load Switch
- Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
G035N04	APG035N04Q	PDFN3*3-8L	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_a =25℃)	I_D	100	A
Continuous Drain Current (T_a =100℃)	I_D	56	A
Pulsed Drain Currenr (1)	I_{DM}	376	A
Singel Pulsed Avalanche Energy (2)	E_{AS}	100	mJ
Power Dissipation	P_D	51.6	W
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.42	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	40	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V, V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1.2	1.7	2.2	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =30A	-	2.8	3.5	mΩ
		V_{GS} =4.5V, I_D =20A	-	4.3	5.2	
Gate Resistance	R_g	V_{DS} =V_{GS} =0V, f =1MHz	-	3.2	-	Ω
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =20V, V_{GS} =0V, f =1MHz	-	1280	-	pF
Output Capacitance	C_{oss}		-	462	-	
Reverse Transfer Capacitance	C_{rss}		-	22	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V, I_D=25A, V_{GS}=10V, R_G=4.7Ω	-	4	-	ns
Turn-on rise time	t_r		-	25.5	-	
Turn-off delay time	$t_{d(off)}$		-	20.5	-	
Turn-off fall time	t_f		-	9.2	-	
Total Gate Charge	Qg	VDS=20V, ID=25A, VGS=10V	-	20.3	-	nC
Gate-Source Charge	Qgs		-	4.1	-	
Gate-Drain Charge	Qgd		-	3.5	-	
Reverse Recovery Chrage	Qrr	I_F=50A,di/dt=100A/us		13		nC
Reverse Recovery Time	Trr	I_F=50A,di/dt=100A/us		22.1		ns
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{SD}	V_{GS} =0V, I_S=50A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	100	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=20V,R_G=25Ω,L=0.5Mh,I_{AS}=20A
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board,t≤10 sec

■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

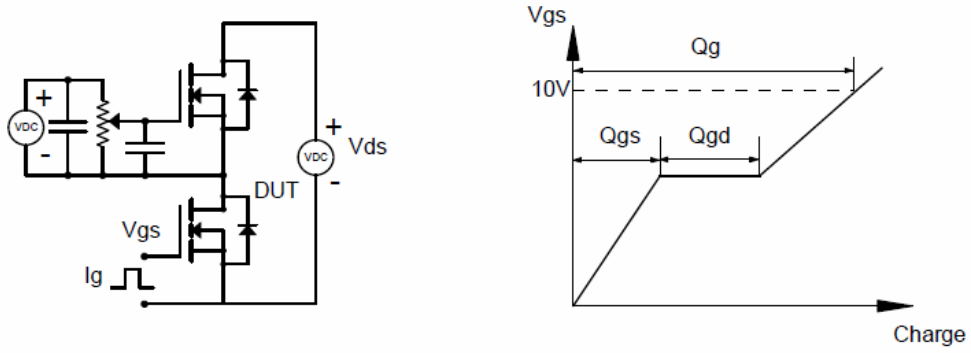


Figure B: Resistive Switching Test Circuit & Waveforms

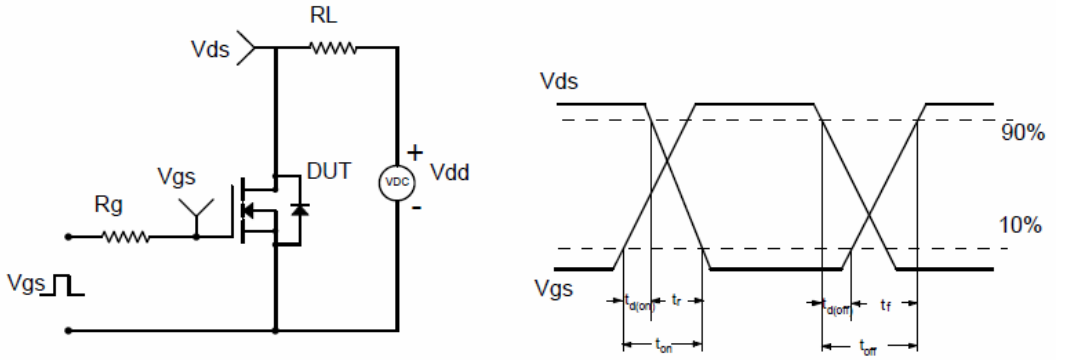


Figure C: Unclamped Inductive Switching (UIS) Test

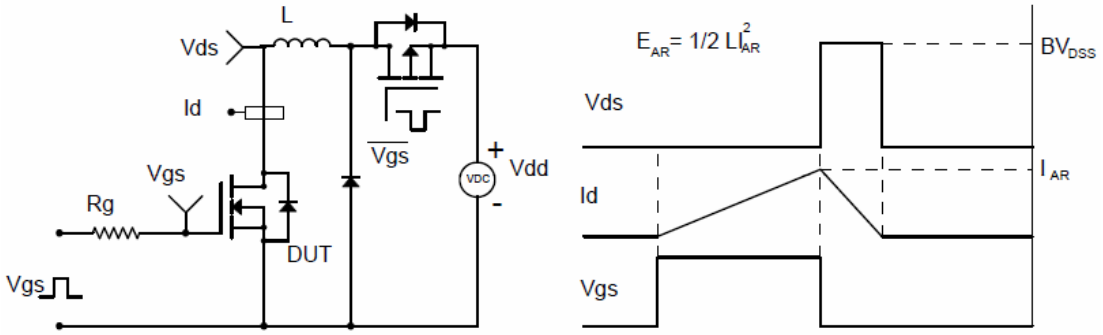
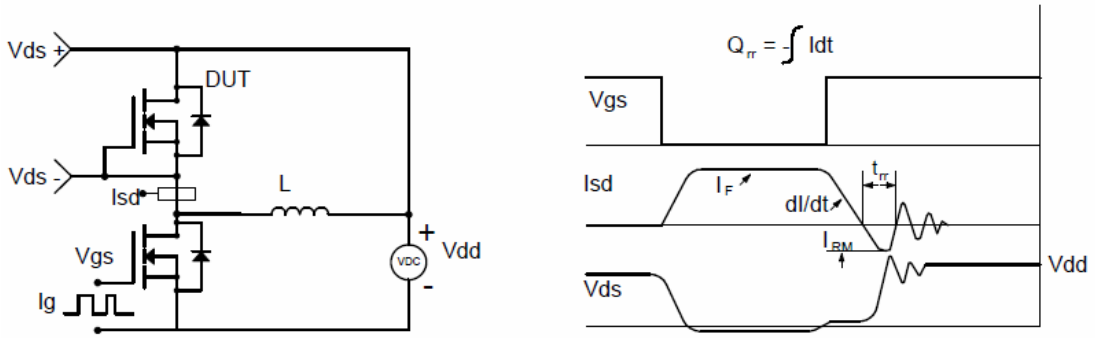
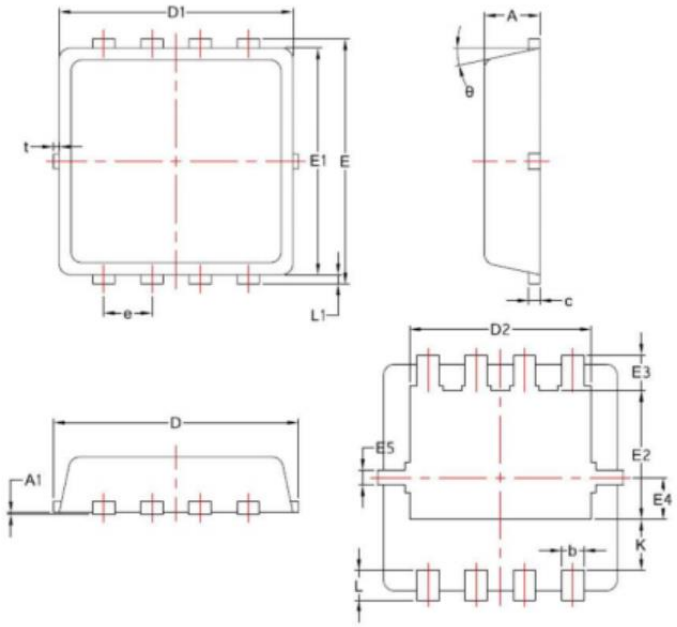


Figure D: Diode Recovery Test Circuit & Waveforms



PDFN3X3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°