10V SINGLE CHANNEL PROGRAMMABLE LOAD SWITCH

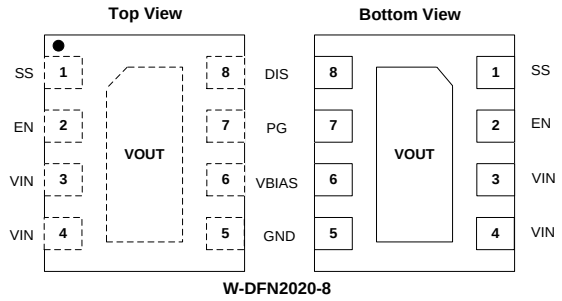
Description

AP22850 is an integrated P-Channel load switch, which features an adjustable ramp-up and discharge rate that can be set via an external capacitor and a resistor, respectively. In addition, it incorporates a "power good" output to flag when the switch is fully enhanced. The P-Channel switch has a typical $R_{DS(ON)}$ of 21mΩ, enabling a current handling capability of up to 8A.

AP22850 is designed to operate from 4.5V to 11V. The near-zero quiescent supply current makes it ideal for use in battery powered distribution systems where power consumption is a concern.

Even as a P-Channel load switch, AP22850 does not require an external gate pull-up resistor, and consequently, stays true to its headlining feature of near-zero quiescent current specification. It also features circuitry to suppress fast input transients (with EN low) from coupling to VOUT.

Pin Assignments



W-DFN2020-8

Feature

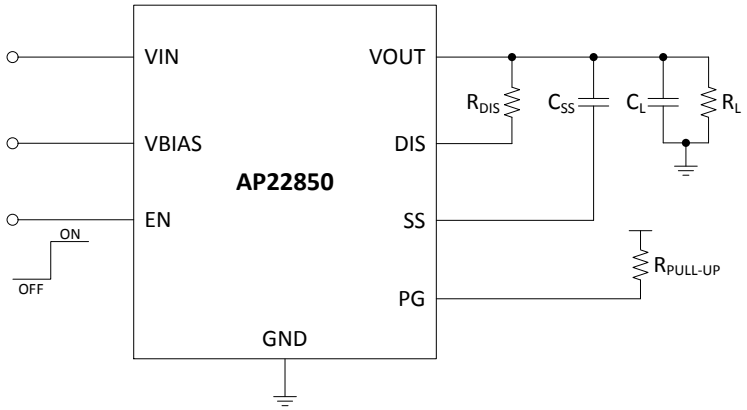
- Near-Zero Quiescent Current
- No External Gate Pull-Up Resistor Required
- Suppresses Fast Transients on VIN
- 4.5V to 11V Input Voltage Range
- Low Typical $R_{DS(ON)}$ of 21mΩ
- Adjustable Start-Up and Discharge Rate
- Small Form Factor Package W-DFN2020-8
  – Footprint of just $4mm^2$
- Thermally Efficient Package with an Exposed Pad
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Lead-Free Plating (NiPdAu Finish over Copper Leadframe). Terminals: Solderable per MIL-STD-202, Method 208 e4
- Weight: TBD grams (Approximate)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Integrated Load Switches in Ultrabook PCs
- Power Up/Down Sequencing in Ultrabook PCs
- Tablets
- Notebooks / Netbooks
- E-Readers
- Consumer Electronics
- Set-Top Boxes
- Industrial Systems
- Telecom Systems

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

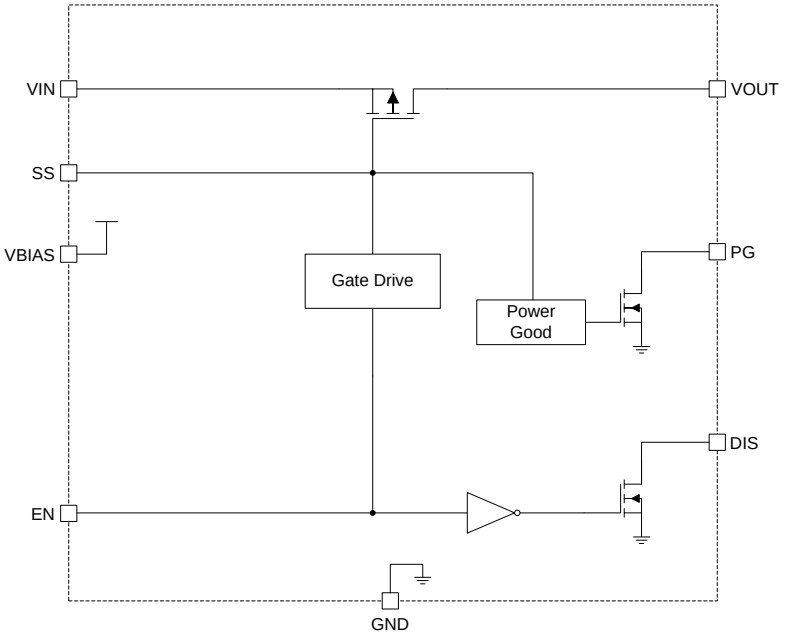
Typical Applications Circuit



Pin Descriptions

Pin Name	Pin Number	Function
SS	1	Soft-Start Adjust An external capacitor connected between this pin and VOUT sets the ramp-up time of VOUT
EN	2	Enable Input Active high
VIN	3, 4	Input Voltage Connects to the Source of the P-channel MOSFET
GND	5	Ground
VBIAS	6	Supply Voltage Recommended range: 2.5V ≤ VBIAS ≤ 5.5V
PG	7	Power Good Open-drain output to indicate when the P-channel pass switch is fully enhanced
DIS	8	Output Discharge An external resistor between DIS and VOUT sets the discharge rate of VOUT
VOUT	PAD	Output Voltage PAD connects to the Drain of the P-channel MOSFET

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter		Ratings	Units
V_{IN}	Input Voltage		12.0	V
V_{OUT}	Output Voltage		12.0	V
V_{EN}	Enable Voltage		6.0	V
V_{BIAS}	Bias Voltage		6.0	V
I_L	Load Current		8.0	A
$T_{J(max)}$	Maximum Junction Temperature		125	°C
T_{ST}	Storage Temperature		−55 to +150	°C
P_D	Power Dissipation	(Note 5)	0.35	W
		(Note 6)	1.8	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 5)	300	°C/W
		(Note 6)	60	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	-	5	°C/W

Notes:
4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. For a device surface mounted on minimum recommended pad layout, in still air conditions; the device is measured when operating in a steady state condition.
6. For a device surface mounted on 25mm by 25mm by 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady state condition.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
V_{IN}	Input Voltage	4.5	11.0	V
V_{BIAS}	Bias Voltage	2.5	5.5	V
V_{EN}	Enable Voltage	0	5.5	V
V_{PG}	Power Good Voltage Range	0	11.0	V
T_A	Operating Ambient Temperature	−40	+85	°C

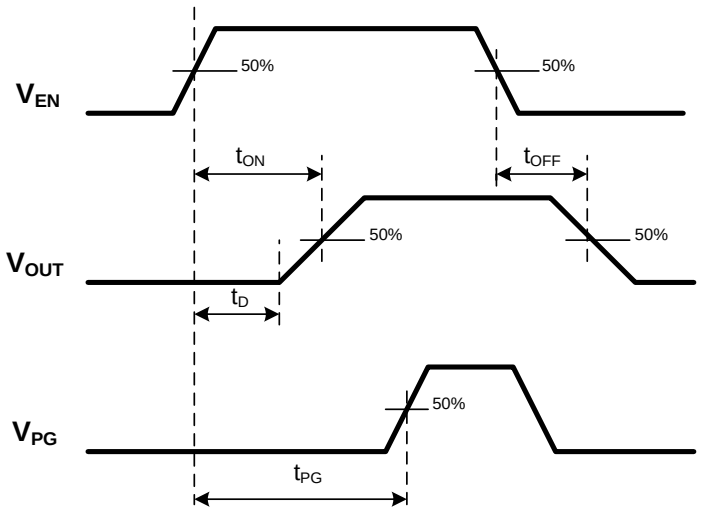
Electrical Characteristics (@T_A = +25°C, V_{BIAS} = 2.5V – 5.5V, C_{IN} = 1µF, C_L = 100nF, unless otherwise specified.)

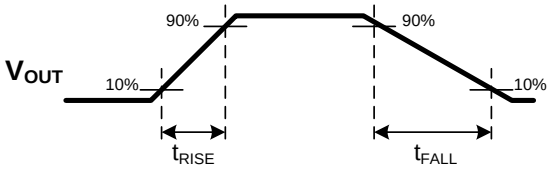
Symbol	Parameters	Conditions		Min	Typ	Max	Unit
I_{VIN_Q}	V_{IN} Quiescent Current	I_{OUT} = 0A	V_{IN} = 10.0V	-	5.0	200	nA
			V_{IN} = 8.4V	-	3.0	200	
			V_{IN} = 5.0V	-	1.0	200	
I_{VBIAS_Q}	V_{BIAS} Quiescent Current	V_{IN} = 12.0V, I_{OUT} = 0A		-	1.0	200	nA
I_{VIN_SD}	V_{IN} Shutdown Current	V_{IN} = 12.0V, V_{EN} = 0V		-	2.0	200	nA
I_{VBIAS_SD}	V_{BIAS} Shutdown Current	V_{IN} = 12.0V, V_{EN} = 0V		-	2.0	200	nA
$R_{DS(ON)}$	Load Switch On-Resistance	I_{OUT} = −1A	V_{IN} = 10.0V	-	21	31	mΩ
			V_{IN} = 8.4V	-	21	31	
			V_{IN} = 5.0V	-	23	33	
V_{IH_EN}	EN Input Logic High Voltage	-		1.0	-	-	V
V_{IL_EN}	EN Input Logic Low Voltage	-		-	-	0.5	V
I_{LEAK_EN}	EN Input Leakage	V_{EN} = V_{BIAS}		-	-	100	nA
R_{DS_DIS}	Discharge FET On-Resistance	V_{EN} = 0V, I_{DIS} = 10mA	V_{BIAS} = 5.0V	-	8	11	Ω
			V_{BIAS} = 2.5V	-	11	16	Ω
V_{OL_PG}	Power Good Output Low Level	I_{OL_PG} = 100µA, V_{EN} = 0V		-	-	0.2	V
I_{OZ_PG}	Power Good High-Impedance Current	V_{PG} = V_{BIAS}, V_{EN} = V_{BIAS}		-	-	0.05	µA

Switching Characteristics (@T_A = +25°C, V_{BIAS} = 2.5V – 5.5V, C_{IN} = 1µF, C_L = 100nF, unless otherwise specified)

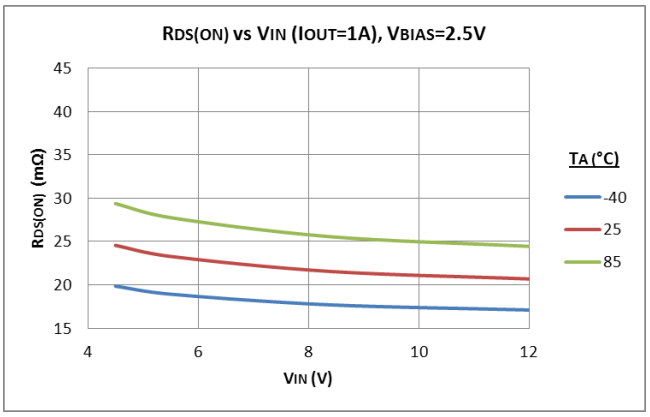
Symbol	Parameters	Conditions		Min	Typ	Max	Unit
t_{RISE}	Output Rise Time	R_L = 10Ω, C_{SS} = 10nF	V_{IN} = 10.0V	-	100	-	µs
			V_{IN} = 8.4V		102		
			V_{IN} = 5.0V		104		
t_{ON}	Output Turn-ON Delay Time	R_L = 10Ω, C_{SS} = 10nF	V_{IN} = 10.0V	-	70	-	µs
			V_{IN} = 8.4V		75		
			V_{IN} = 5.0V		82		
t_{FALL}	Output Fall Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	V_{IN} = 10.0V	-	70	-	µs
			V_{IN} = 8.4V		71		
			V_{IN} = 5.0V		75		
t_{OFF}	Output Turn-OFF Delay Time	R_L = Open, R_{DIS} = 240Ω, C_{SS} = 10nF	V_{IN} = 10.0V	-	41	-	µs
			V_{IN} = 8.4V		45		
			V_{IN} = 5.0V		60		
t_D	Output Start Delay Time	R_L = 10Ω, C_{SS} = 10nF	V_{IN} = 10.0V	-	12	-	µs
			V_{IN} = 8.4V		16		
			V_{IN} = 5.0V		22		
t_{PG}	Power Good Delay Time	R_L = 10Ω, C_{SS} = 10nF	V_{IN} = 10.0V	-	250	-	µs
			V_{IN} = 8.4V		230		
			V_{IN} = 5.0V		205		

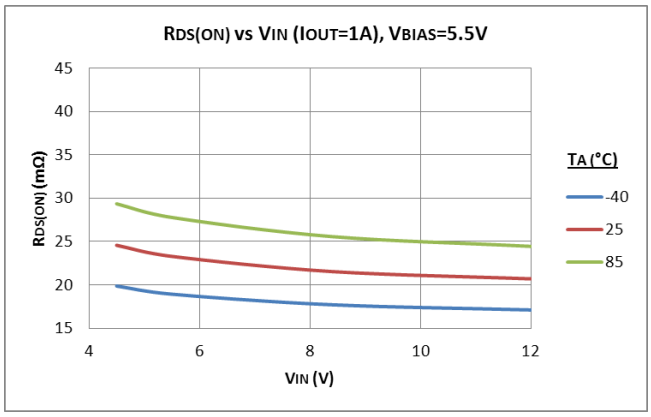
t_{ON}/t_{OFF} Waveforms

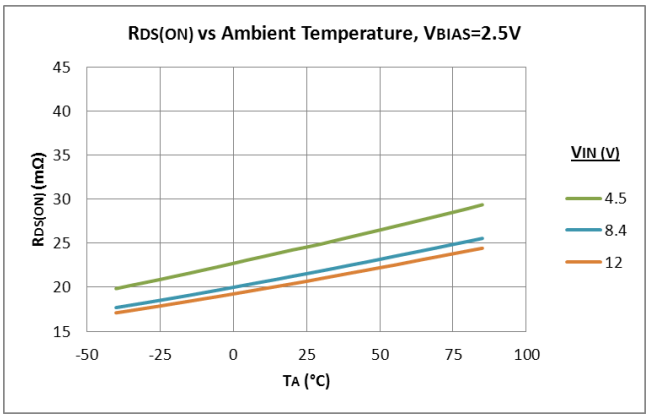


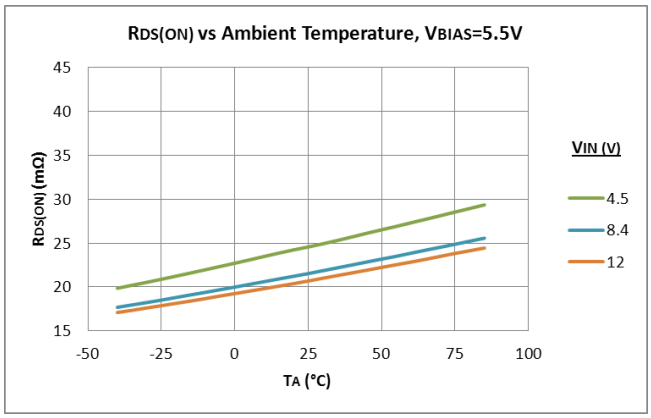


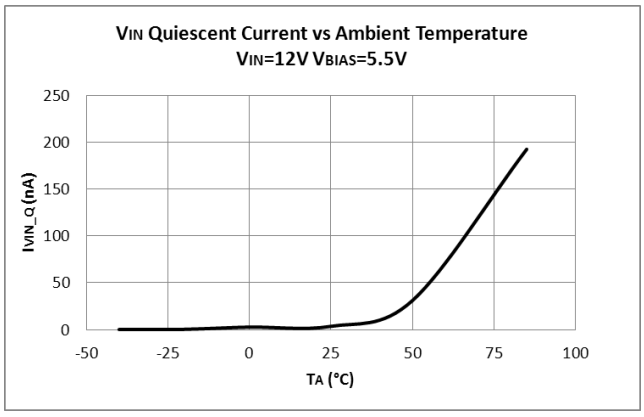
Typical Performance Characteristics (@T_A = +25°C, V_{BIAS} = 5V, unless otherwise specified.)

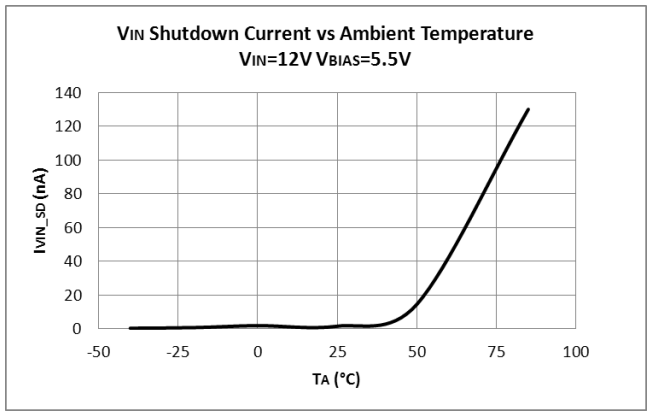


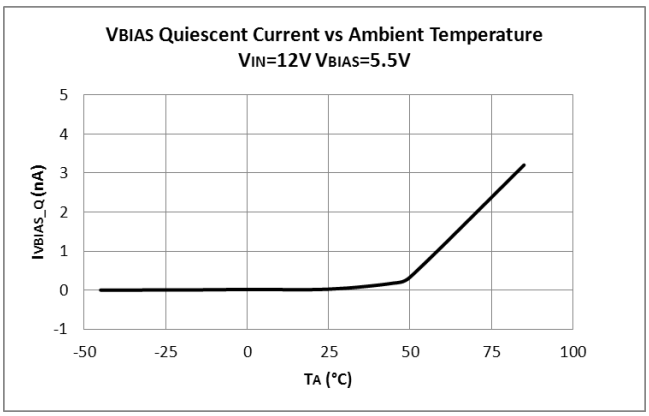


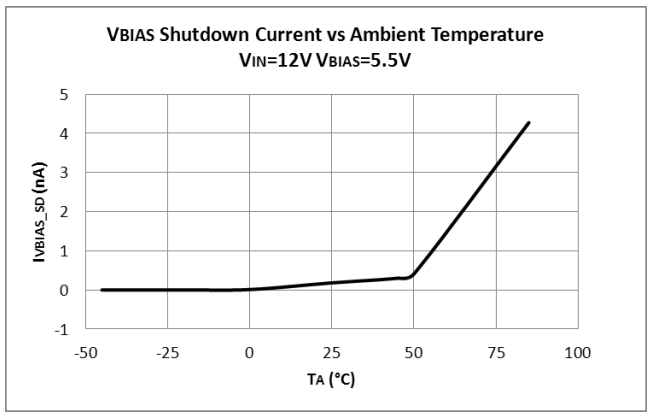




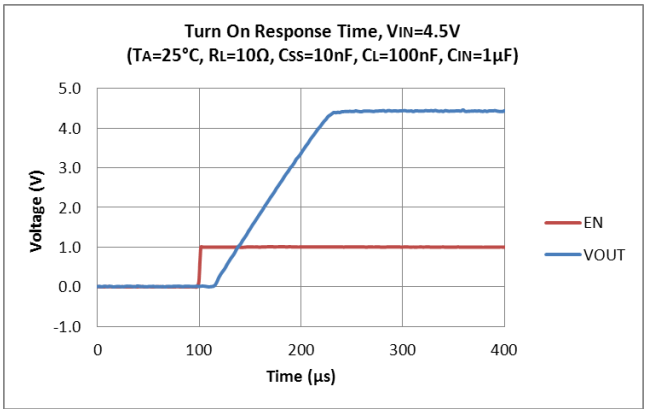


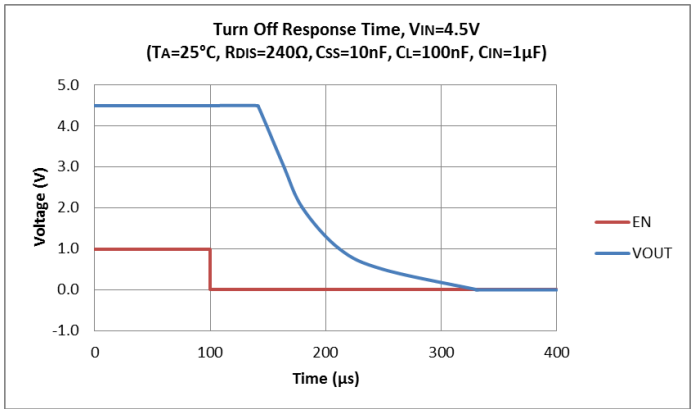


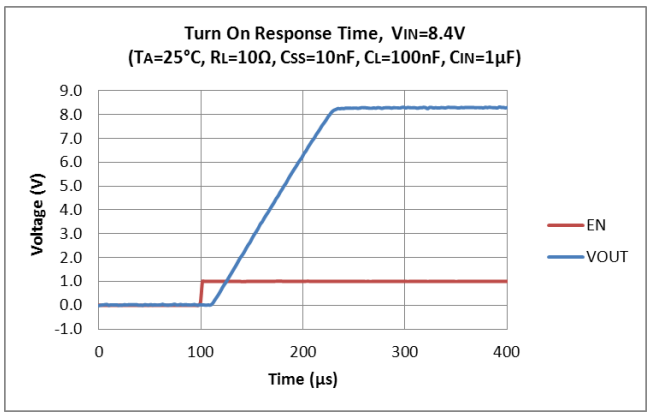


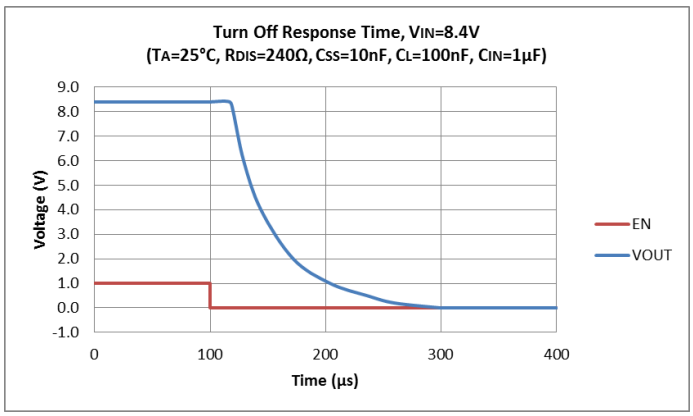


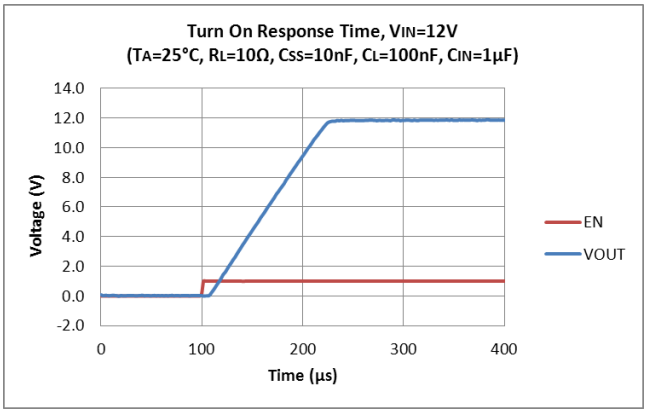
Typical Performance Characteristics (cont.) (@T_A = +25°C, V_{BIAS} = 5V, unless otherwise specified.)

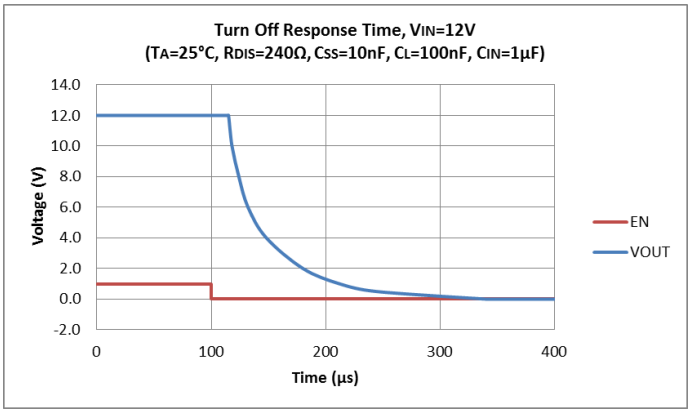












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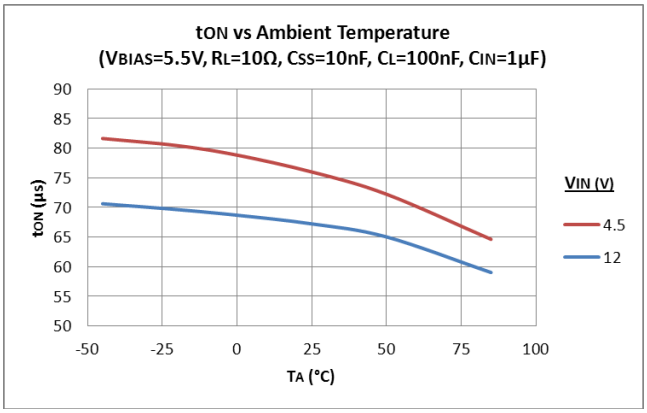
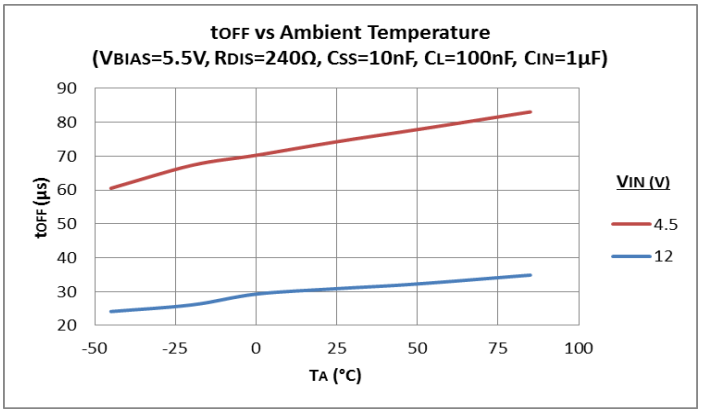
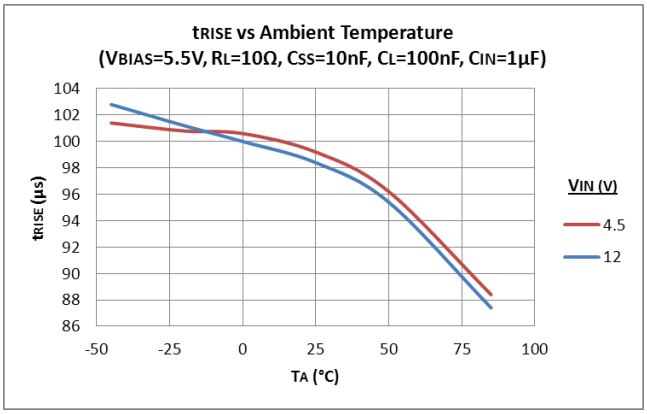
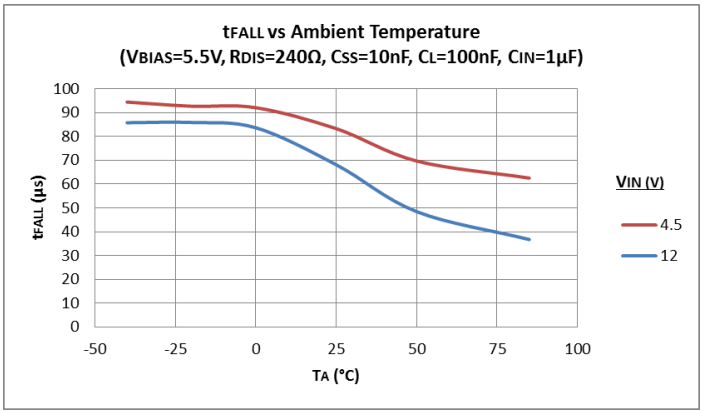
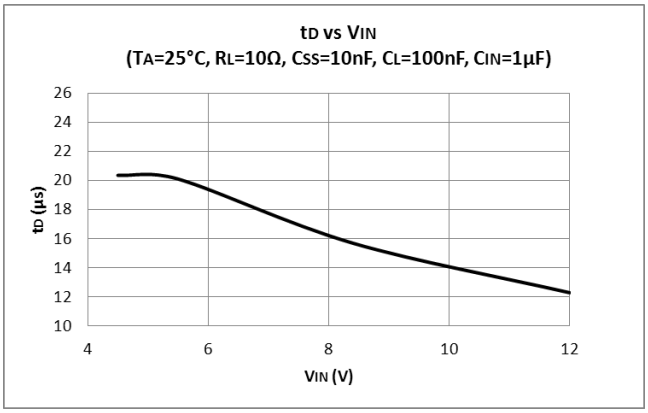










Application Information

Theory of Operation

The AP22850 is a load switch that can be used to isolate or power-down part of a system in order to reduce power consumption, particularly in battery-powered devices. The PMOS pass element in AP22850 is turned on when the EN pin is pulled high. This provides a controlled current source to decrease the voltage on the SS pin to GND, effectively turning on the PMOS pass switch and connecting VOUT to VIN.

During the turn-on phase, once the SS voltage reaches close to GND, the PMOS pass switch is fully enhanced with maximum available overdrive. Power is deemed to be good and the Power Good (PG) output is pulled high via an external pull-up resistor. The rise-time on VOUT is controlled by the value of the external capacitor between the SS and VOUT pin.

When EN is pulled low, the switch turns off and isolates VOUT from VIN. In addition, PG is pulled to indicate that the power is no longer good. The discharge pin keeps VOUT grounded while EN is low. The fall time on VOUT is largely controlled by the value of the discharge resistor and the capacitance on the output.

Input and Output Voltage

The Input Voltage (VIN) should be between 4.5V and 11V. With the switch is activated, the Output Voltage (VOUT) will be the input voltage minus the voltage drop across the device.

Enable

The GPIO compatible EN input allows the output current to be switched on and off. A high signal (switch on) should be at least 1V, and the low signal (switch off) no higher than 0.5V.

This pin should not be left floating. It is advisable to hold EN low when applying or removing power.

VBIAS

The VBIAS input provides a positive power supply to the controller circuitry. It should be set in the range of 2.5V to 5.5V. VBIAS signal is essential for the device to power up and should be set before the switch is enabled.

Power Good

Power Good is an open-drain output that indicates when the pass switch is enhanced enough to deliver current to the load. PG is high (open-drain high impedance) when power is deemed good, and low when the power is deemed to not be good.

PG can be pulled up to any voltage to a maximum of 11V, although it is recommended to pull it up to VOUT with a resistor greater than 20kΩ. The advantage of pulling up PG to VOUT is that when EN is low, VOUT is also grounded. Thus, no power is wasted in the pull-up resistor.

If this feature is not required, then PG pin can be left floating

Input and Output Capacitors

AP22850 does not require any capacitor on VIN for successful operation. In addition, this device has no input-to-output capacitor ratio stipulation to account for current through the body diode. However, to minimize voltage dip on VIN due to inrush current at start-up, a capacitor can be place on VIN.

For heavier loads, it is recommended that the VIN and VOUT trace lengths be kept to a minimum. In addition, a bulk capacitor (≥ 10μF) may also be placed close to the VOUT pin. If using a bulk capacitor on VOUT, it is important to control the inrush current by choosing an appropriate soft-start time in order to minimize the droop on the input supply.

Application Information (cont.)

Adjustable Slew Rate/Soft-Start

SS pin allows the output ramp time of the switch to be controlled using an external capacitor (C_{SS}). This timing capacitor is connected between the SS and VOUT pin. Rise times (in µs) for different values of C_{SS} and V_{IN} are shown in the table below with V_{BIAS} = 5.5V.

Rise Time (in µs) Measured at +25°C using 0805 X7R 10% 50V capacitors, C_L = 100nF, R_{DIS} = 1K, R_L = 10Ω				
V_{IN} / C_{SS}	**4.5V**	**7.0V**	**9.0V**	**11.0V**
1nF	13.6	12.4	12.0	11.4
10nF	97.2	99.2	98.8	97.9
100nF	955	1,075	1,154	1253

Table 1 Timing Capacitors and Rise Times

Adjustable Discharge

When EN goes low, VOUT is discharged to ground through the discharge resistor (R_{DIS}) on the DIS pin. A value greater than 240Ω is recommended for R_{DIS}.

While the discharge/fall-time on VOUT can be controlled using R_{DIS}, capacitors on VOUT and SS also contribute to the timing. Higher discharge resistance increases the RC time constant and hence, the discharge time. Fall times (in µs) for different values of R_{DIS} and V_{IN} are shown in the table below with V_{BIAS} = 5.5V.

1,206 250mW 1% Discharge resistor (Ω)	Fall Time (in µs) Measured at +25°C, C_L = 100nF, C_{SS} = 1nF, R_L = open	
	5V	**11V**
240	71.8	69.5
1,000	264.2	276.7
3,900	1,029	1,078

Table 2 Discharge Resistors and Output Voltage Fall Time

Board Layout and Thermal Considerations

Due to the high current capacity of the load switch, PCB layout needs to ensure good thermal distribution during operation. The top and bottom of AP22850EV1, (the evaluation board for AP22850), can be seen below.

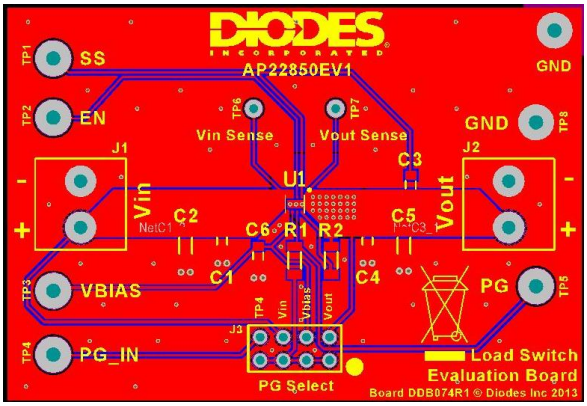


Figure 3 PCB Copper Layout & Silk Screen – Top

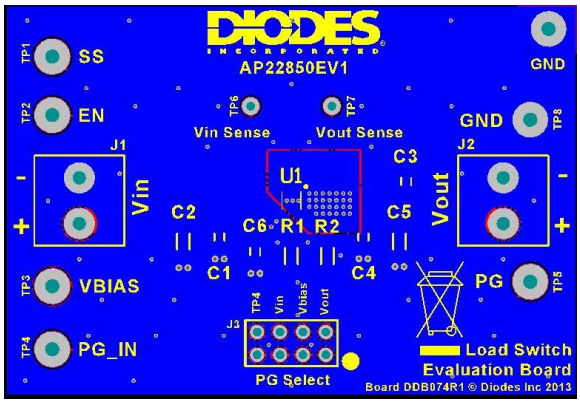


Figure 4 PCB Copper Layout & Silk Screen – Bottom

Thermal vias are used directly underneath the chip to help distribute the heat from the device. The ground plane on the underside of the board effectively acts as a large heatsink. The widths of the tracks carrying VIN and VOUT are kept wide. Vias are also distributed around the board to aid thermal conduction and to ensure a consistent potential, particularly around the ground connections of the capacitors. All capacitors used are located as close as possible to the AP22850 to minimize any parasitic effects.

The maximum junction temperature of the AP22850 is +125°C. To ensure that this is not exceeded, the following equation can be used to give an approximation of junction temperature. Temperature readings taken with a thermal camera can also give a good approximation of power dissipation with the use of this equation. The board layout has a major influence on the parameter θ_{JA}.

$$T_J = T_A + (\theta_{JA} \times P_D)$$

Where, T_J = Junction Temperature (°C)
T_A = Ambient Temperature (°C)
θ_{JA} = Junction to Ambient Thermal Impedance (°C/W)
P_D = Power Dissipation (voltage drop across device × output current) (W)

Ordering Information

AP22850 XYZ-7

Package	Packing
SH8 : W-DFN2020-8	-7 : Tape and Reel

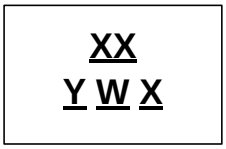
Part Number	Package Code	Packaging (Note 7)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP22850SH8-7	SH8	W-DFN2020-8	3,000/Tape & Reel	-7

Note: 7. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

Marking Information

W-DFN2020-8

(Top View)

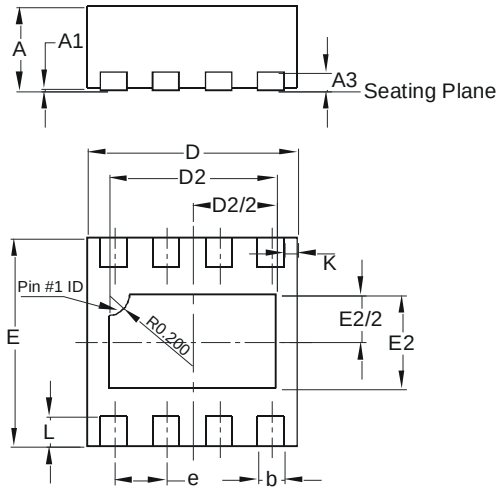


XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents 52 and 53 week
X : A~Z : Internal Code

Device	Package	Identification Code
AP22850SH8-7	W-DFN2020-8	WC

Package Outline Dimensions (All dimensions in mm)

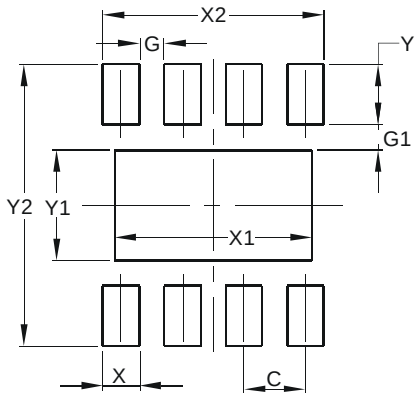
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



W-DFN2020-8 Type C			
Dim	**Min**	**Max**	**Typ**
A	0.770	0.830	0.800
A1	0	0.05	0.02
A3	-	-	0.152
b	0.20	0.30	0.25
D	1.950	2.075	2.000
D2	1.50	1.70	1.60
E	1.950	2.075	2.000
E2	0.80	1.00	0.90
e	-	-	0.50
K	-	-	0.125
L	0.240	0.340	0.290
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.500
G	0.200
G1	0.210
X	0.300
X1	1.600
X2	1.750
Y	0.490
Y1	0.900
Y2	2.300