MOSFET Silicon N-Channel MOS

1. Applications

Synchronous rectification in SMPS,
Hard switching and High speed circuit
DC/DC in telecoms and industrial

2. Features

Low drain-source on-resistance: RDS(on) = 2.9mΩ (typ.)
High speed power switching
Enhanced body diode dv/dt capability
Enhanced avalanche ruggedness

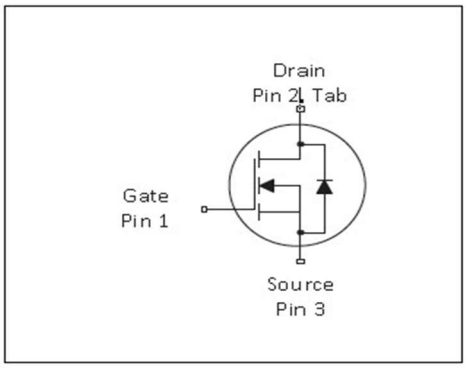
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	100	V
$R_{DS(on),max}$	3.4	mΩ
$Q_{g,typ}$	138	nC
$I_{D,pulse}$	856	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
AUP034N10	TO220	AUP034N10
AUB034N10	TO263	AUB034N10

TO263	TO220
	



1 Maximum ratings

At T_j= 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current at sikicon[1)]	I_D		-	214	A	T_C=25°C
Continuous drain current at package[1)]	I_D		-	195	A	T_C=25°C
Continuous drain current at silicon[1)]	I_D			151	A	T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-		856	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	512	mJ	Tc=25°C,VDD=40V,Vgs=10V, L=1mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	32	A	Tc=25°C, VDD=40V, L=1mH, RG=25Ω
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Power dissipation	P_{tot}	-	-	330	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	170	°C	
Operating junction temperature	T_j	-55	-	170	°C	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			300	°C	

[1)] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table Thermal characteristics(TO263&TO252)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.46	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	63	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	2		4	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=100V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	2.9	3.4	mΩ	V_{GS}=10V, I_D=80A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	2.6	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	10000	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Output capacitance	C_{oss}	-	2900	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	280	-	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	38	-	ns	V_{DD}=50V, V_{GS}=10V, I_D=80A, R_G=2.5Ω
Rise time	t_r	-	50	-	ns	V_{DD}=50V, V_{GS}=10V, I_D=80A, R_G=2.5Ω
Turn-off delay time	$t_{d(off)}$	-	69	-	ns	V_{DD}=50V, V_{GS}=10V, I_D=80A, R_G=2.5Ω
Fall time	t_f	-	33	-	ns	V_{DD}=50V, V_{GS}=10V, I_D=80A, R_G=2.5Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	58	-	nC	V_{DD}=50V, I_D=80A, V_{GS}=10V
Gate to drain charge	Q_{gd}	-	44	-	nC	V_{DD}=50V, I_D=80A, V_{GS}=10V
Gate charge total	Q_g	-	138	-	nC	V_{DD}=50V, I_D=80A, V_{GS}=10V

Table 7 Reverse diode characteristics(by caculating)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous Source Current at silicon	I_{SD}	-	214	-	A	*Maximum Ratings*
Diode forward voltage	V_{SD}	-	1.2	-	V	V_{GS}=0V, I_s=80A, T_j=25°C
Reverse recovery time	t_{rr}	-	95	-	ns	*Vgs=0V*, I_F=80A, di_F/dt=100A/μs
Reverse recovery charge	Q_{rr}	-	143	-	nC	*Vgs=0V*, I_F=80A, di_F/dt=100A/μs

4 Electrical characteristics diagram

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

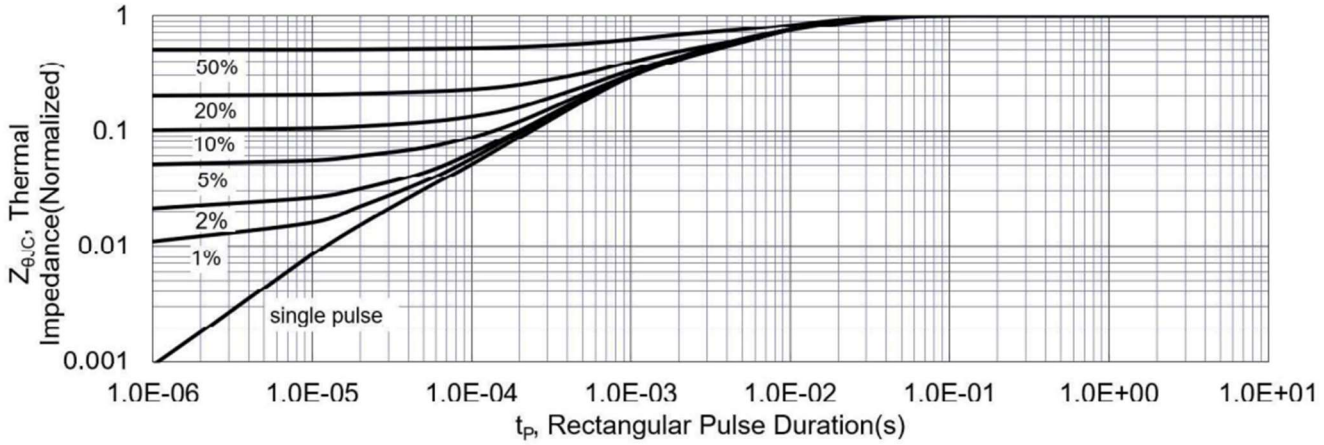


Figure 2. Maximum Power Dissipation vs. Case Temperature

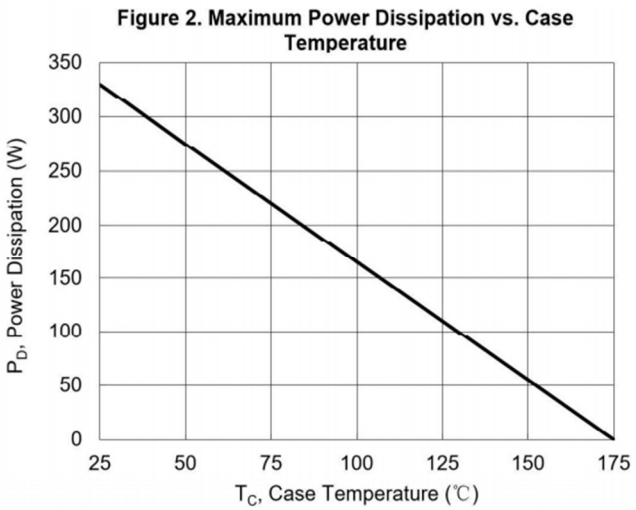


Figure 3. Maximum Continuous Drain Current vs Case Temperature

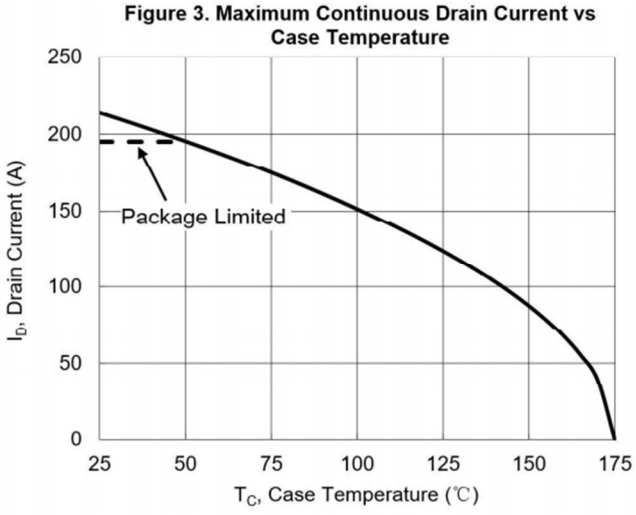


Figure 4. Typical Output Characteristics

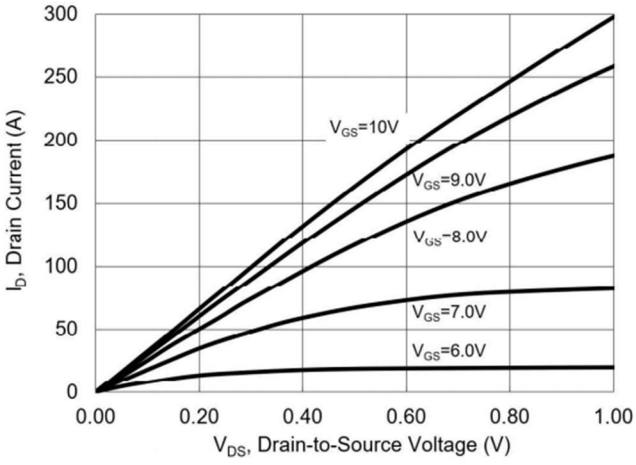


Figure 5. Unclamped Inductive Switching Capability

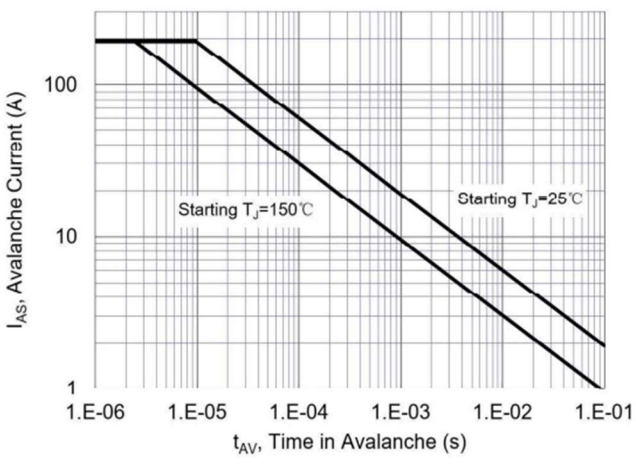


Figure 6. Maximum Peak Current Capability

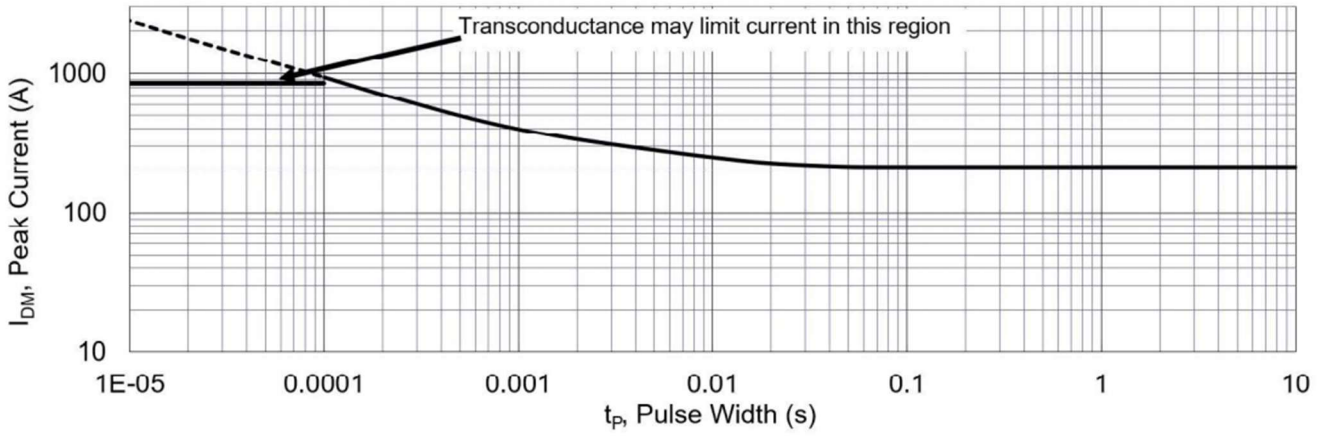


Figure 7. Maximum Forward Safe Operation Area

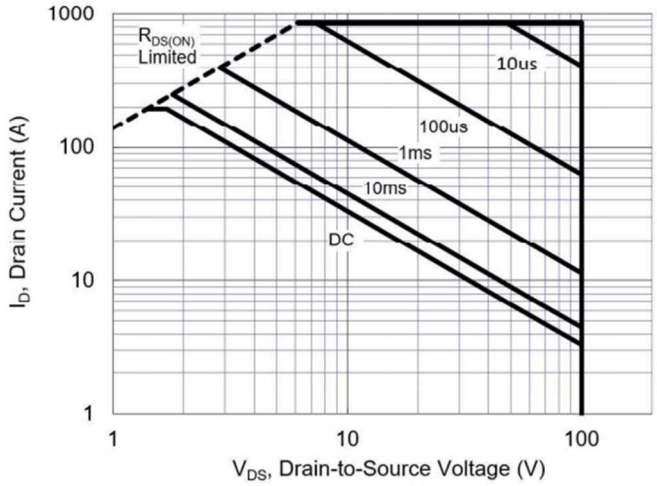


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

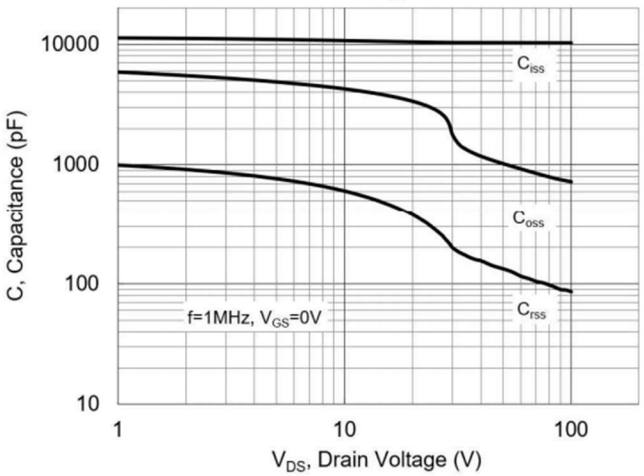
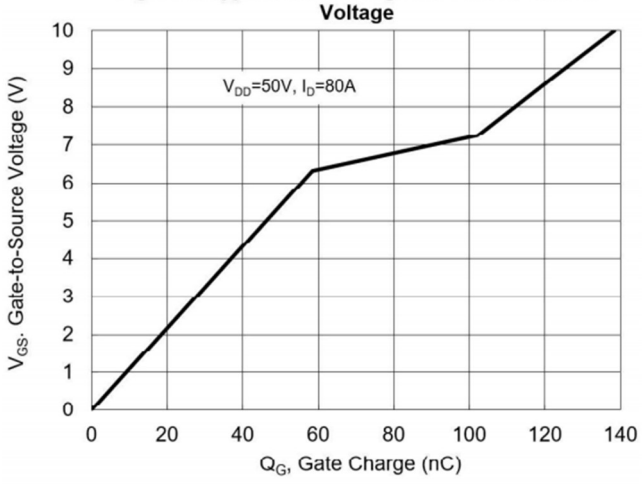
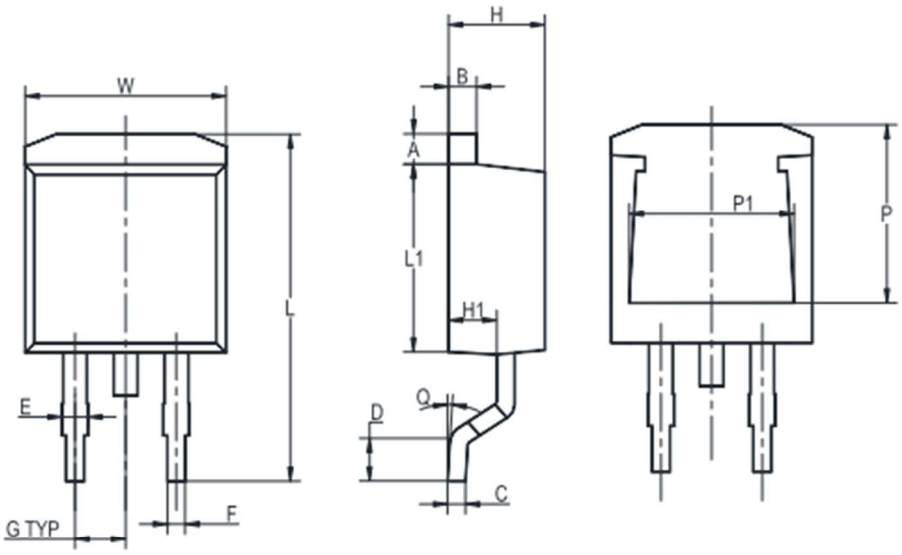


Figure 9. Typical Gate Charge vs. Gate-to-Source Voltage

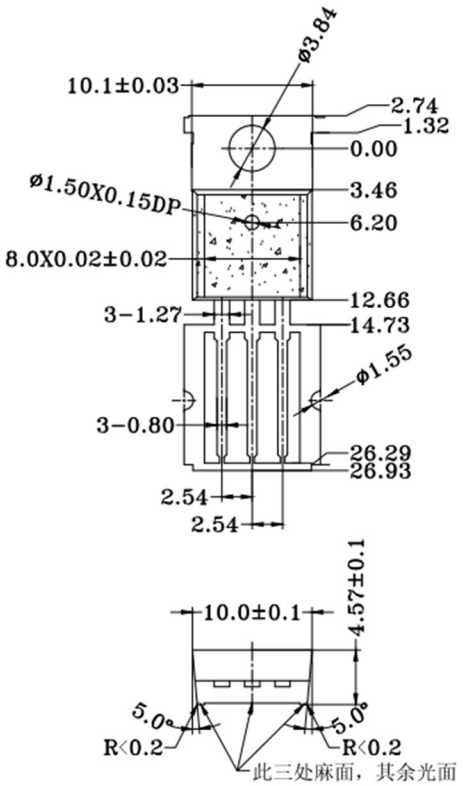


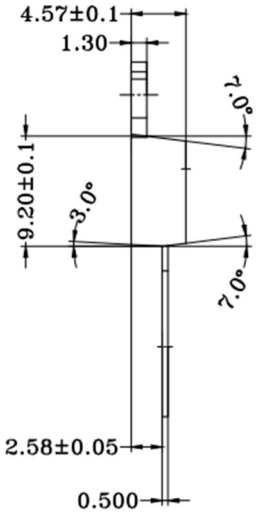
5. Package Outlines



UNIT	A	B	C	D	E	F	G	W	H	H1	L	L1	Q	P	P1
mm	1.5	1.5	0.5	2.60	1.6	0.94	2.54	10.5	4.8	2.9	16.5	8.7	8°	7.6	8.2
	1.1	1.1	0.3	2.15	1.1	0.68	TYP	9.6	4.4	2.5	14.5	8.2	MAX	7.1	7.4

Figure1：Outline PG-TO263(HC)





注：如图麻面Ra0.8~1.0

Figure2：Outline PG-TO220(HT)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2022-04-15	Preliminary version