MOSFET Silicon N-Channel MOS

1. Applications

Boost PFC switch, Half bridge or Asymmetric half bridge or Series resonance half bridge and full bridge topologies.
Server power,Telecom power,EV charging, Solar inverter,UPS Application.

2. Features

Low drain-source on-resistance: RDS(ON) = 0.095Ω (typ.)
Easy to control Gate switching
Enhancement mode: Vth = 2.8 to 4.2 V

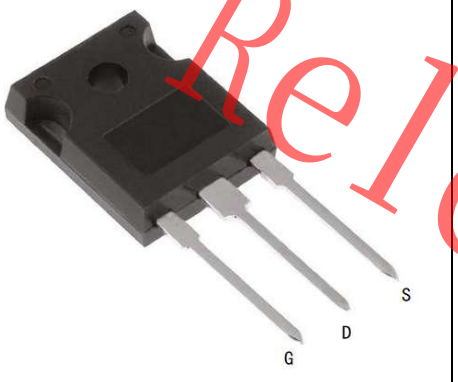
Table 1 Key Performance Parameters

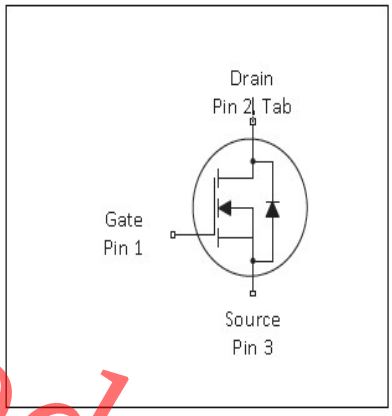
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	700	V
$R_{DS(on),max}$	110	mΩ
$Q_{g,typ}$	52	nC
$I_{D,pulse}$	90	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R110E	TO247	ASW65R110E

TO247





1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D		-	30	A	T_C=25°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	90	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	2528	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	36	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	277.8	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	100	°C	
Operating junction temperature	T_j	-55	-	100	°C	
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=48A, T_j=25°C see table 8

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.45	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	V_{GS}=0V, I_D=10mA
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=30V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.095	0.110	Ω	V_{GS}=10V, I_D=14A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	13.4	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2497	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Output capacitance	C_{oss}	-	239	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Reverse transfer capacitance	C_{rss}	-	6.75	-	pF	V_{GS}=0V, V_{DS}=50V, f=10kHz
Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2Ω; see table 9
Rise time	t_r	-	28	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	108.4	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2Ω; see table 9
Fall time	t_f	-	24	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2Ω; see table 9

Table 6 Gate charge characteristics

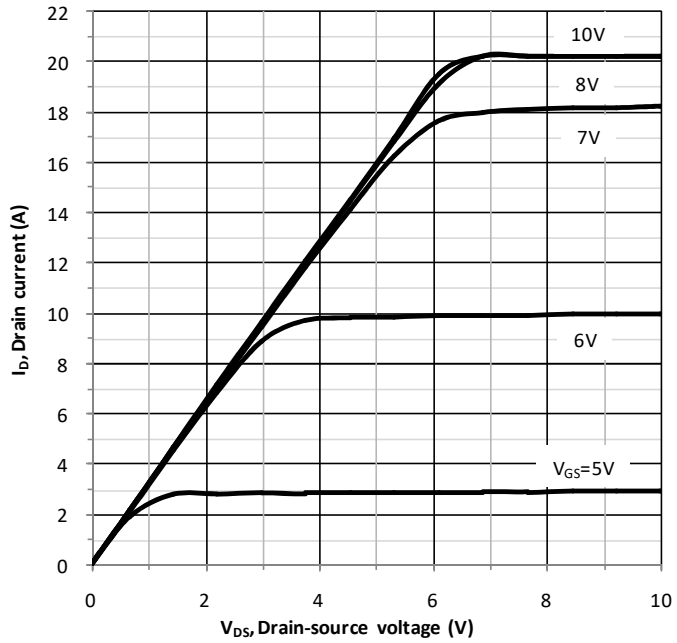
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		7.1	-	nC	V_{DD}=400V, I_D=25A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	20	-	nC	V_{DD}=400V, I_D=25A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	52	-	nC	V_{DD}=400V, I_D=25A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	9	-	V	V_{DD}=400V, I_D=25A, V_{GS}=0 to 10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.69	-	V	V_{GS}=0V, I_F=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	380.8	-	ns	V_R=400V, I_F=25A,di_F/dt=100A/μs; see table 8
Reverse recovery charge	Q_{rr}	-	8.8	-	uC	V_R=400V, I_F=25A,di_F/dt=100A/μs; see table 8
Peak reverse recovery current	I_{rrm}	-	45.2	-	A	V_R=400V, I_F=25A,di_F/dt=100A/μs; see table 8

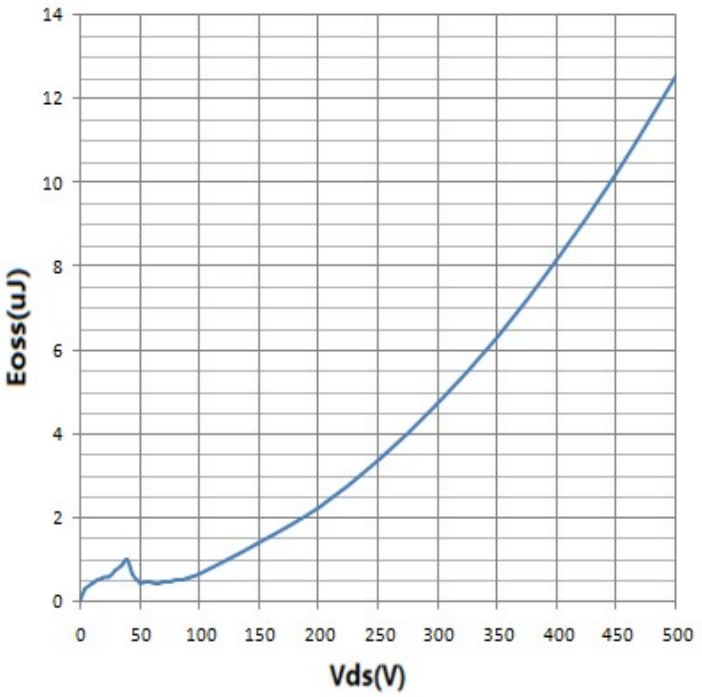
4 Electrical characteristics diagram

Diagram 1: Typ. output characteristics



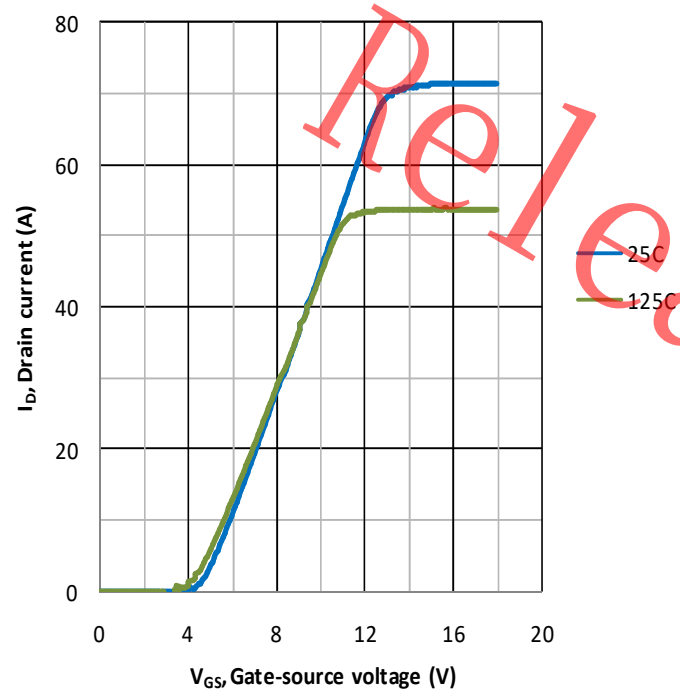
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 2: Typ. Coss stored energy



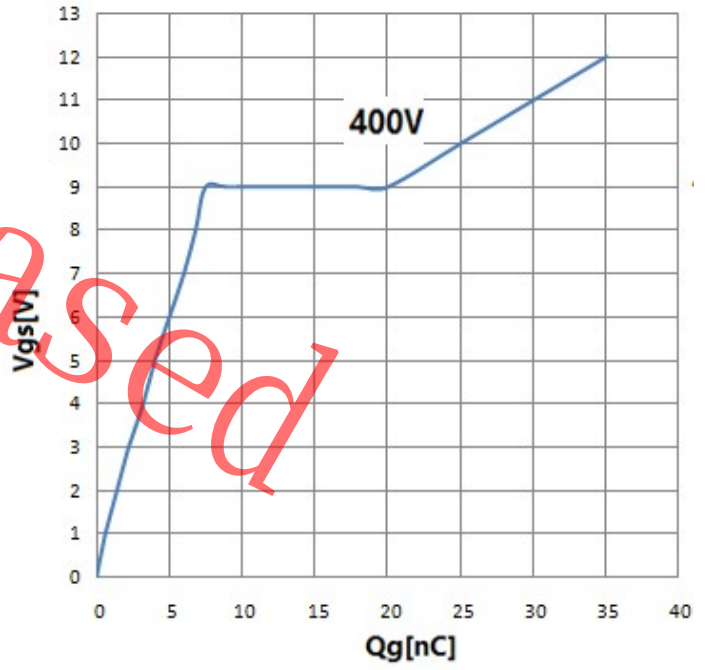
Eoss=f(VDS)

Diagram 3: Typ. transfer characteristics

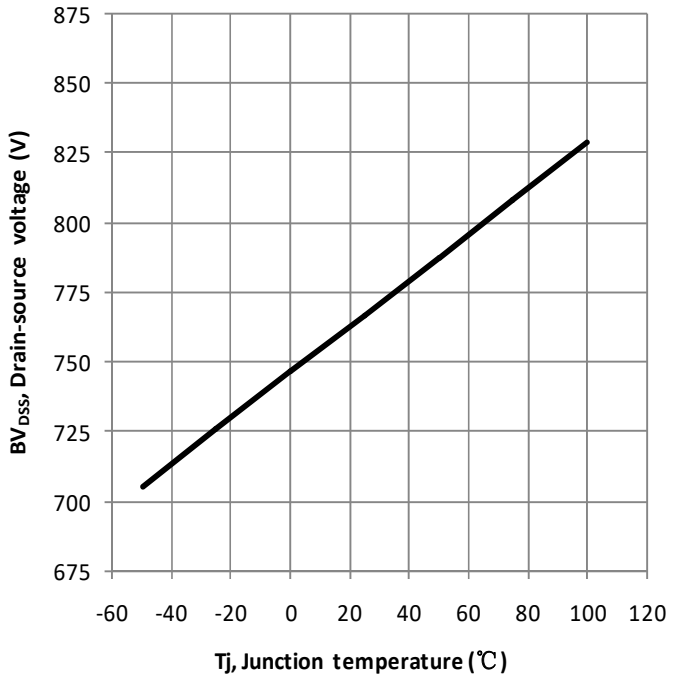
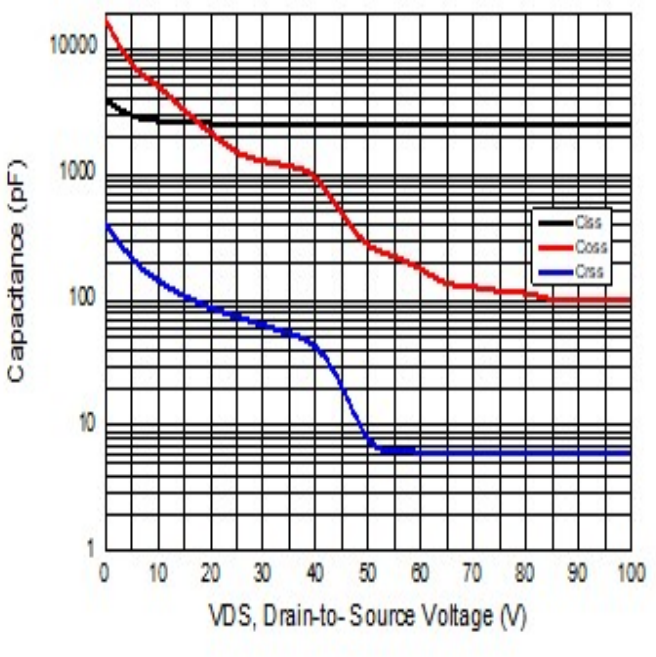


I_D=f(V_{GS}); parameter: T_j

Diagram 4: Typ. gate charge



V_{GS}=f(Q_{gate}); I_D=25 A pulsed; parameter: V_{DD}

Diagram 5: Drain-source breakdown voltage	Diagram 6: Typ. capacitances
	
$V_{BR(DSS)}$=f(T_j); I_D=10 mA	C=f(V_{DS}); V_{GS}=0 V; f=10 kHz

5 Test Circuits

Table 8 Diode characteristics

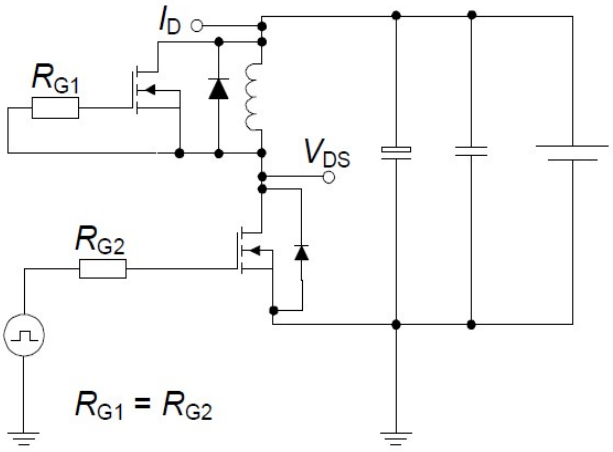
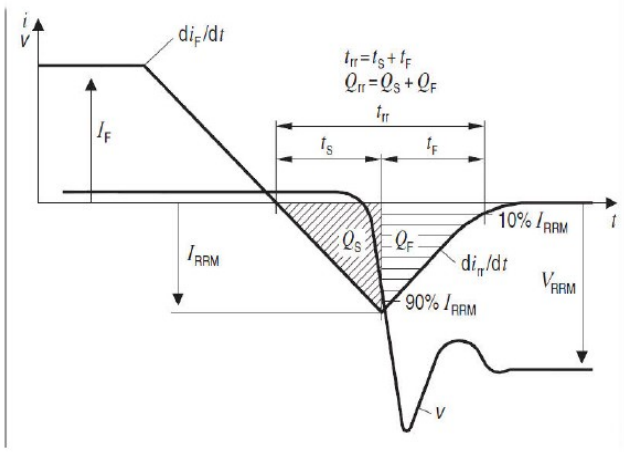
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

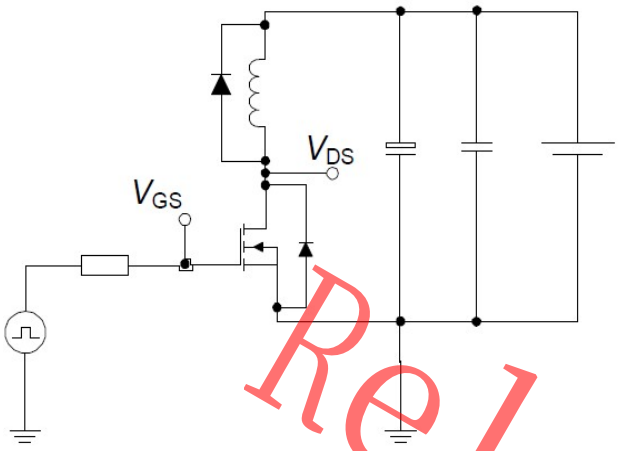
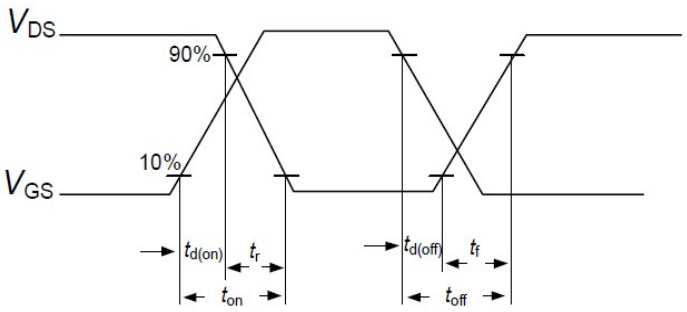
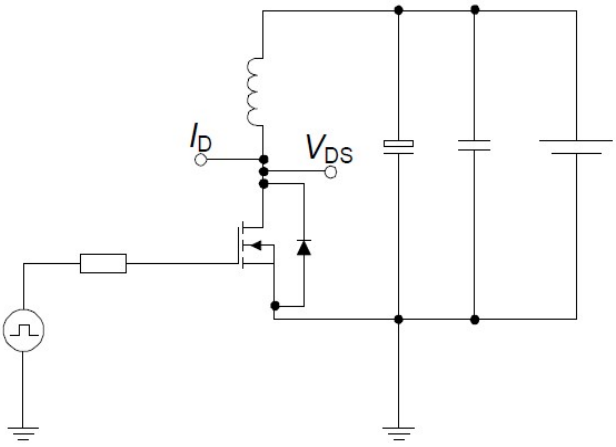
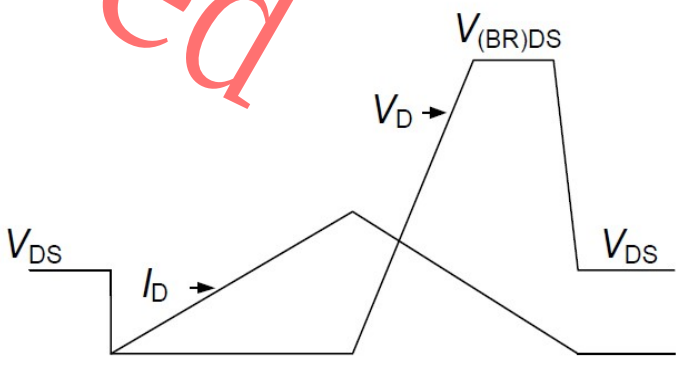
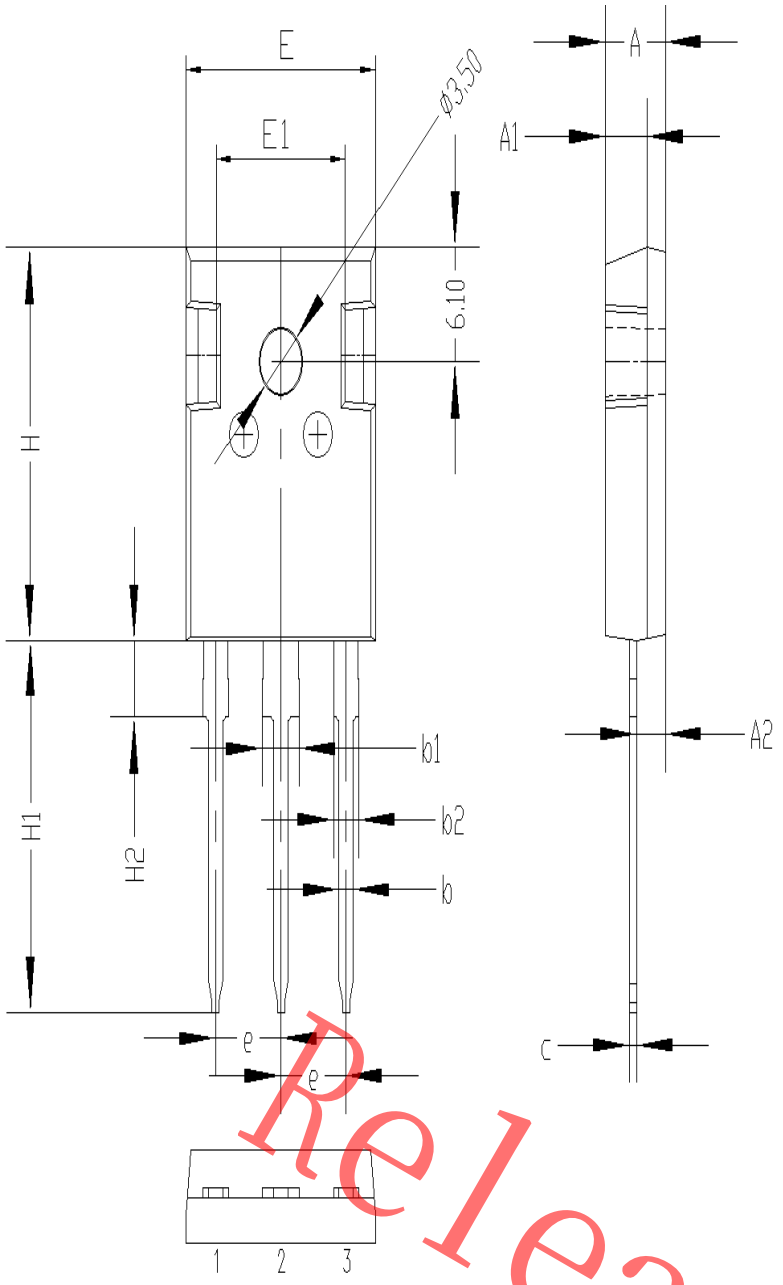
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



	单位: mm		
	MIN	NOM	MAX
A	4.8	5	5.2
A1	3.3	3.5	3.7
A2	2.1	2.3	2.5
b	1	1.2	1.4
b1	2.9	3.1	3.3
b2	1.9	2.1	2.3
c	0.4	0.6	0.8
e	5.25	5.45	5.65
E	15.6	15.8	16
E1	10.6	10.8	11
H	20.8	21	21.2
H1	19.4	19.9	20.4
H2	3.9	4.1	4.3
G	5.9	6.1	6.3
ØP	3.3	3.5	3.7

Figure1：Outline PG-TO247

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2020-03-05	Release version
2.0	2020-03-19	Add Electrical characteristics Curve